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1 Scope

The present document describes the I3C interface for the communication of an SSP, as defined in ETSI TS 103 666-1 [1] using the SCL protocol. The present document details the implementation of MIPI I3C Basic specification [4] for an SSP. Specifically, I3C electrical characteristics, Target state diagram, data link layer for I3C are defined.

2 References

2.1 Normative references

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

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The following referenced documents are necessary for the application of the present document.

[1] ETSI TS 103 666-1: "Smart Secure Platform (SSP); Part 1: General characteristics".

[2] ETSI TS 102 613: "Smart Cards; UICC - Contactless Front-end (CLF) Interface; Physical and data link layer characteristics".

[3] ISO/IEC 13239: "Information Technology -- Telecommunications and information exchange between systems -- High-level Data Link Control (HDLC) procedures".

[4] MIPI Alliance: "Specification for I3C Basic^{SM} - Improved Inter Integrated Circuit" Version 1.1.1".

2.2 Informative references

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The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

[i.1] ETSI TR 102 216: "Smart cards; Vocabulary for Smart Card Platform specifications".

3 Definition of terms, symbols and abbreviations

3.1 Terms

For the purposes of the present document, the terms given in ETSI TR 102 216 [i.1] and the following apply:

data transfer: information exchange during an I3C Basic Access between the Controller and the Target

NOTE: As defined in I3C Basic [4].

flow control: mechanism of the Data Link Layer that consists of methods applied by the transmitter in order to send at any time a number of logical data units that can be accepted by the receiver

I3C Basic Access: private read/write defined in MIPI I3C used for an uninterrupted data transfer of link layer frame between the Controller and a Target

I3C Basic Frame: I3C communication that begins with START followed by one or more transfers and a STOP

NOTE: As defined in clause 4.1 of MIPI I3C Basic Specification [4].

Link Layer Frame: link layer data structure consisting of a prologue or frame header, payload and epilogue or trailer usually containing the CRC bytes

MAC access request: request from the Target to the Controller for a data transfer, i.e. a MAC phase initiated by the Target by using the IBI

MAC phase: initiation of a data transfer by the Controller and/or request for a data transfer by the Target

window size: maximum number of logical data units that can be sent from the transmitter to the receiver without any link layer acknowledgements for any of these data units

window size slot: fixed space used by the Target in the receive buffer for the logical data units

NOTE: The length of a window size slot equals the Data Link Layer MTU.

3.2 Symbols

Void.

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AC	Alternating Current
ACK	ACKnowledged
ACT	ACTivation protocol
CCC	Common Command Code
CLF	ContactLess Frontend
CLT	ContactLess Tunnelling
CMD	CoMmanD
CRC	Cyclic Redundancy Check
HDR	High Data Rate
High-Z	High Impedance
I3C	Improved Inter Integrated Circuit
IBI	In-Band Interrupt
LLC	Logical Link Control
LPDU	Link Protocol Data Unit
MAC	Medium Access Control
MCT	MAC aCTivation
MDB	Mandatory Data Byte

MRL	Maximum Read Length
MSb	Most Significant bit
MSB	Most Significant Byte
MTU	Maximum Transmission Unit
MWL	Maximum Write Length
NACK	Not ACKnowledge
OSI	Open Systems Interconnection
POT	Power-ON Time
PSM	Power Saving Mode
RFU	Reserved for Future Use
SCL	Serial Clock
SDA	Serial DAta
SDR	Single Data Rate
SHDLC	Simplified High Level Data Link Control
SSP	Smart Secure Platform
SWP	Single Wire Protocol
UICC	Universal Integrated Circuit Card
VDD	Supply Voltage

4 Introduction

The Improved Inter Integrated Circuit (I3C) is a serial synchronous half-duplex communication interface between a one or more Controllers and one or more Targets present on the same I3C bus. This clause defines the physical, MAC and data link layers for the I3C interface.

Since the terms Master and Salve have been deprecated, in order to be aligned with the MIPI I3C Basic specification [4], they are replaced respectively with the terms Controller and Target without any change in the technical definition and role. Definition of the Controller and the Target are provided in clause 3.1 of the present document, and definitions are the same as present in the MIPI I3C Basic specification [4].

5 SCL Under-Layers Protocol Stack

Figure 5-1 illustrates the protocol stack below the SCL supporting the I3C interface.

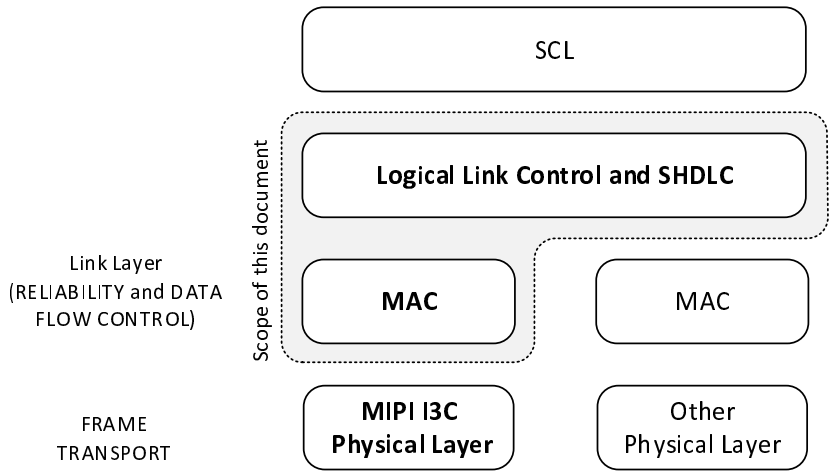


Figure 5-1: Protocol stack for I3C Interface

6 Electrical interfaces

6.1 Introduction

In the following clauses, an implementation of I3C interface is defined. This implementation, based on MIPI I3C Basic specification [4], allows bi-directional communication and the possibility for the Target device to initiate communication with the Controller when it has data available thus avoiding the necessity for continuous polling to be performed by the Controller. The Target may initiate a communication when data will be available for transfer.

6.2 Physical interface

Figure 6.2-1 illustrates the I3C interface using 2 signals.

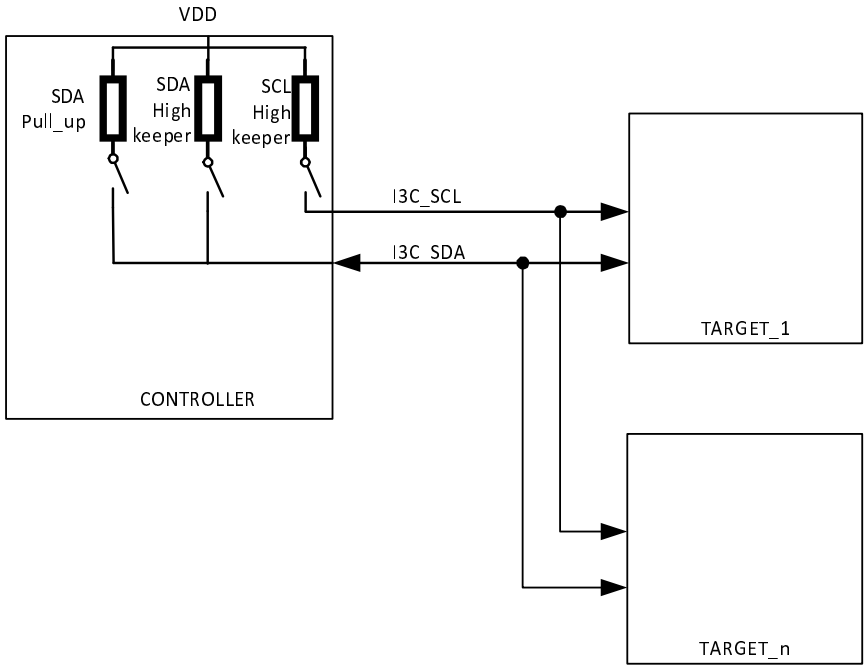


Figure 6.2-1: I3C electrical interface

The I3C interface with 2 signals describes two signals:

- SDA: Serial Data line
- SCL: Serial Clock line

The IBI request may be used by the I3C Target as per MIPI I3C Basic specification [4] in cases where the Target has this capability and it is enabled by the Controller, and thus an additional signal line is not required for the Target to generate an interrupt to the Controller.

6.3 Electrical characteristics

The provisions of MIPI I3C Basic specification [4], clause 6.1 and clause 6.2 shall apply. Electrical I/O stage characteristics defined in table 82 shall apply.

Support of multiple voltage classes may affect timing parameters specified in clause 6.2 of MIPI I3C Basic specification [4]. In this case the Controller and the Target devices shall follow the guidelines provided in clause 5.1.9.3.18 of MIPI I3C Basic specification [4] specification and electrical characteristics specified in table 82 of MIPI I3C Basic specification [4].

6.4 Target state

6.4.1 Target state definitions

The Target device shall be in one of the following states:

- **Powered Not Initialized State:**

  The Target device enters this state as soon as it is powered on and VDD is valid or after a reset. In this state, the Target is not initialized and the I3C module is not ready to send or receive any data. The Controller shall not perform any I3C communication while the Target device is in this state.

  After the T5, following VDD valid or a reset, the Target shall transition to the "Initial State".

- **Initial State:**

  At T5, after power-on and a valid VDD, the Target is ready to be assigned a Dynamic Address. This shall be done according to the MIPI I3C Basic specification [4], clause 5.1.4 and its subclauses. Once assigned a Dynamic Address the Target shall transit into the Idle state.

- **Idle State:**

  The Target device in this state has to process all SDA and SCL signals and process the data on the bus according to the I3C protocol and the MCT phase may be initiated by the Controller. The target enters this state at POT from the VDD valid, as reported in the MCT_DATA.

- **Pro-active state:**

  This is the state where the Target device sends an In-Band Interrupt to the Controller. The Target generates the MAC access request by using the IBI as defined in MIPI I3C Basic specification [4]. In case the I3C Target device sends the Mandatory Data Byte, it shall be used to identify the interrupt. Once the IBI has been sent, the Controller can initiate a read request and read the MAC data.

- **Busy state:**

  The Target devices can NACK the Read/Write requests to notify the Controller that the Target device is busy. This can help the Controller to do another communication with other Target devices until the Target device is ready or wait for the Target device to have the data ready.

- **Power saving mode state:**

  In the Power Saving Mode (PSM) the Target device should preserve the configured Dynamic Address. The exit shall be triggered by the wake up condition described in clause 7.8.3. After detecting the exit condition, the Device will switch to Busy State for the duration of the Target resume time from Power Saving Mode. After the Target resume time from Power Saving Mode the Device will go to Idle State.

- **Active State:**

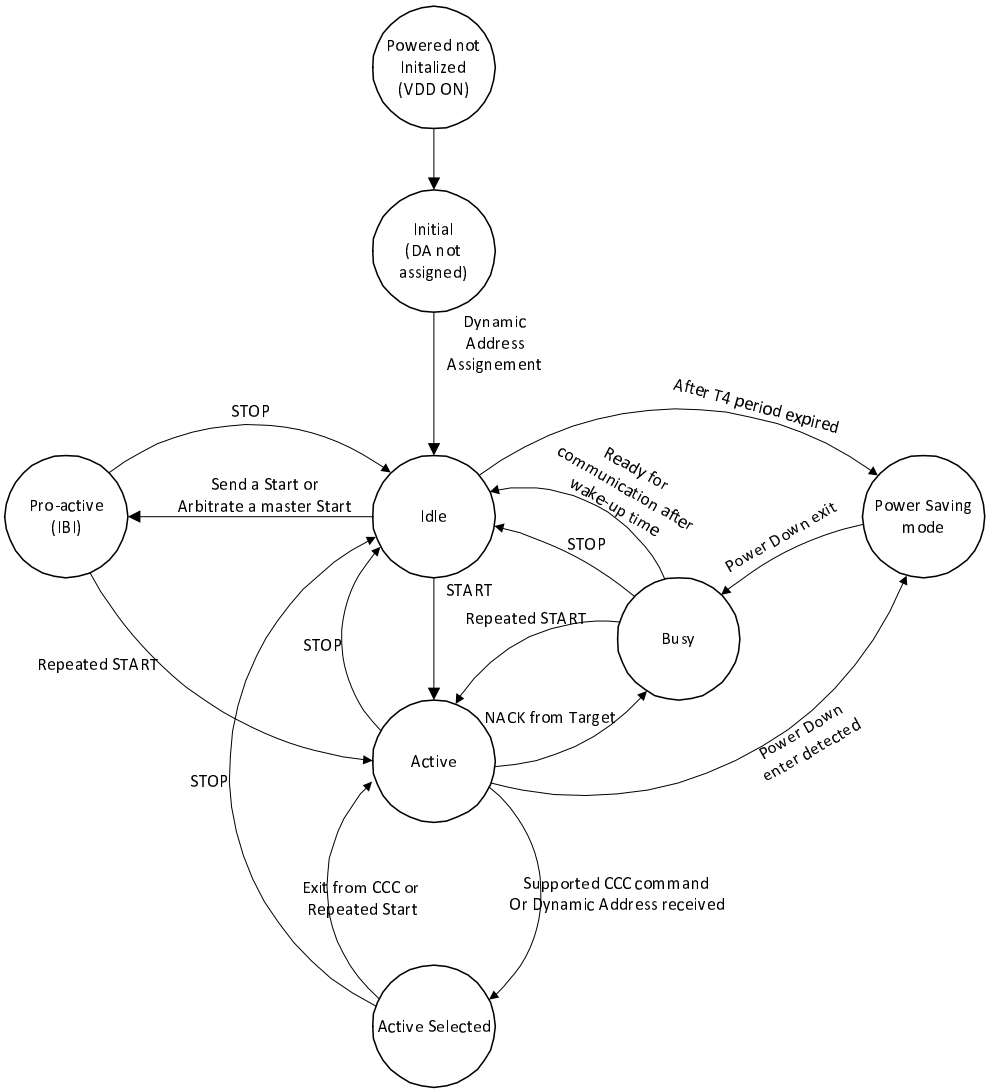
  In this state, communication is ongoing on the bus and the Target device is sampling SDA and SCL lines checking if it is addressed by the Controller. In this state the CCC commands and the Addresses after Repeated START and START are processed. If the CCC command is supported or the Address matches the Dynamic Address, the data will be processed in Active Selected State.

- **Active Selected State:**

  In this state, the Target device is selected for communication and performs transaction requests by the Master.

6.4.2 Target state diagram

Figure 6.4.2-1 shows the diagram of the Target states.



NOTE: For the sake of readability, the transitions to the Powered not Initialized state if a reset occurs are not shown.

Figure 6.4.2-1: Diagram of the Target states

7 Data Link Layer

7.1 Overview

Clause 9.1 in ETSI TS 102 613 [2] shall apply.

7.2 MAC Layer

7.2.1 Overview

The MAC phase is the initial handshake phase between the I3C Controller and the I3C Target followed by the I3C data transfer phase.

7.2.2 Timing

7.2.2.1 Timing definitions

Table 7.2.2.1-1 describes the timing parameters of the MAC layer. In addition to these MAC timings, the timing requirements listed in AC electrical characteristics shall apply for all MAC diagrams in the following clauses.

Table 7.2.2.1-1: MAC timing parameters

Symbol	Definition	Value (min)/ Reference	Description
T3	Target Resume Time from Power Saving Mode	Reported in MCT_READY	The duration of the Target Resume Time from Power Saving Mode.

7.2.2.2 T3 = Target Resume Time from Power Saving Mode

T3 is the Target Resume Time from the Power Saving Mode. It is Target implementation dependant. The Target reports at initialization in MCT_READY the minimum value of T3 required for the Target to become ready for the I3C Basic Access. Whenever the Controller needs to resume the Target from Power Saving Mode it should use during the MAC phase at least the time T3.

7.2.3 MAC layer

7.2.3.1 Introduction

As a Target I3C module is normally always ready for an access from the Controller, the Target remains in Idle state. The Controller initiates a MAC phase by issuing an I3C Private Write. The Target will move into (Active-Selected) state when the address sent by the Controller in the address header (MIPI I3C Basic specification [4], clause 5.1.2.2) matches the Target Dynamic Address. The Target can request MAC access to the Controller by sending an IBI. Requesting a MAC access request by sending an IBI the I3C module can be achieved in two ways:

- Checking if the bus is in Bus Available condition, (a Stop is generated on the bus and both SDA and SCL line remain high for at least 1 µs), and pull down the SDA line, generating a START and sending its Dynamic Address when the Controller provides a clock. The Dynamic Address is sent in open-drain mode to allow arbitration.
- Waiting for a START (but not Repeated START) from the Controller and send its Dynamic Address in open-drain mode to allow arbitration.

The arbitration is used as a way to allow multiple devices to initiate sending data simultaneously and the device that loses the arbitration will backoff and wait for the next opportunity to send an IBI, or wait for the Controller to address it for a communication.

The START could be generated simultaneously by the Controller and the Target module or multiple Target modules and in this case the arbitration will determine which device wins and then continues to send data.

7.2.3.2 Initiation of the data transfer from the Controller

The Controller initiates communication as described in MIPI I3C Basic specification [4], clauses 5.1.2.2 and A.2.

7.2.3.3 Initiation of the data transfer from the Target

In I3C data transfers are always initiated by the Controller. The Target can request a transfer to the Controller through an In Band Interrupt (IBI). Upon reception of the IBI the Controller initiates the data transfer as described in clause 5.1.6.2.2 of MIPI I3C Basic specification [4]. IBI is described in MIPI I3C Basic specification [4], clause 5.1.6.

7.2.3.4 Simultaneous initiation of the data transfer from both Controller and Target

The data transfer could be initiated simultaneously by the Controller and the Target module or multiple Target modules and in this case the arbitration will determine which device wins and then continues to send data, as described in MIPI I3C Basic specification [4], clauses 5.1.6 and 5.1.2.2.1.

7.2.3.5 MAC activation

The MAC activation procedure shall be the following:

- The Controller shall drive the VDD power line ON.
- I3C Dynamic address assignment shall follow the VDD power line on to complete the MAC activation.

7.2.3.6 MAC deactivation

The MAC deactivation procedure shall be the following:

- The Controller shall put the bus in Idle state. In the present document, MAC deactivation implies the Controller driving the VDD power line off.

7.3 Link Layer Frame

7.3.1 Overview

The Controller and the Target exchange Frames. The format of the Frames generated by the Controller and the Target is determined by the link layer and it is shown in figure 7.3.1-1.

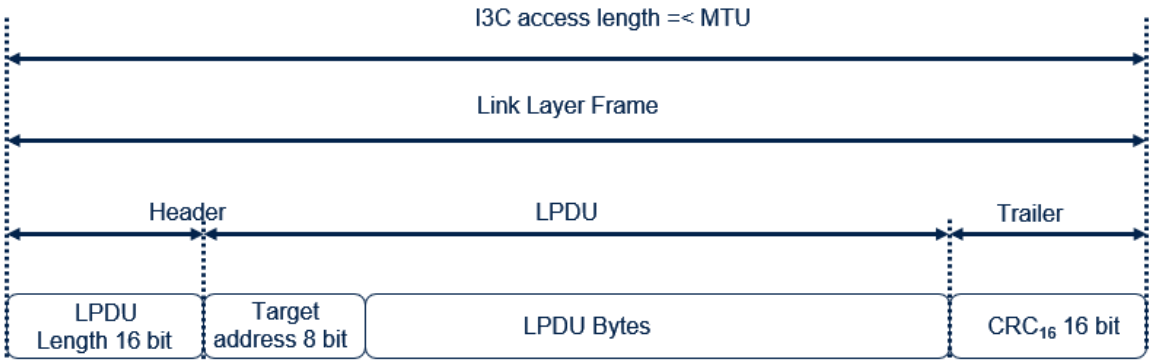


Figure 7.3.1-1: Link Layer Frame structure

MWL (Maximum Write Length) or MRL (Maximum Read Length) are negotiated based on the buffer size of the devices according to the I3C Basic protocol [4], clause 5.1.9.3.5 and clause 5.1.9.3.6. The maximum value of MTU is set to the minimum of the negotiated MWL and MRL values. MWL and MRL values are the sum of Header, LPDU and Trailer bytes. Data flow from the Target is controlled using the T-bit as described in [4], clause 5.1.2.3.4.

A Controller shall use a single I3C Basic Frame when reading Link Layer Frame from the Target devices. This means each Link Layer Frame shall be sent and received in a single I3C Basic Access without interruptions.

In the case where upper layer message/packet may be transferred over multiple subsequent Link Layer Frames, then each Frame will follow the Link Layer Frame requirement.

All bytes shall be transmitted with MSB first (most significant bit first). All Frames are transferred with the bytes in the order shown in figure 7.3.1-1, starting with the LPDU Length. The LPDU field is transferred starting with the LLC Control byte followed by the data generated by the upper OSI layer.

The Link Layer Frame shall contain the following fields:

- LPDU length: length of the LPDU, 2 bytes.

NOTE: The length is specified on 2 bytes, however the maximum Link Layer Frame size is '0FF9' due to CRC properties LPDU (Link Protocol Data Unit):

- Target Address: 1 bit fixed to 0 (MSb) plus 7 bit Target Dynamic Address, 1 byte total;
- LPDU includes the LLC control byte as defined in clause 7.4.

- CRC informs about the integrity of the whole Frame, i.e. Length and LPDU. Detection of errors in a Frame shall be based on the 16-bit Frame checking sequence as given in ISO/IEC 13239 [3]. The CRC polynomial is: $X^{16} + X^{12} + X^5 + 1$. Its initial value is 'FFFF'.

Link Layer Frames are exchanged between the Controller and the Target during I3C MAC accesses. The Controller determines the number of bytes exchanged in an I3C Basic Access and the Target controls the number of bytes during a read operation using the T-bit according to MIPI I3C Basic specification [4], clause 5.1.2.3.4. The maximum length of an access is MTU. Link Layer Frames (including Header, LPDU and Trailer) shall always be prepared with length less than or equal to MTU.

The Controller should compare the Target address included in the LPDU first byte with the Target address used to initiate a Private read and verify if the data is from the intended Target device. If there is a mismatch then the Frame will be discarded.

The Target device shall compare the Target address included in the LPDU first byte with its own Target Dynamic Address and verify if the data sent from the Controller is addressed to it. If there is a mismatch then the Frame will be discarded.

MWL and MRL values are negotiated at I3C Basic interface initialization as described in clause 5.1.9.3.5 and clause 5.1.9.3.6 of MIPI I3C Basic specification [4]:

- MWL can be used to negotiate maximum write lengths.
- MRL can be used to negotiate maximum read lengths.
- The maximum value of MTU is set to the minimum of the negotiated MWL and MRL values.

I3C protocol allows the Controller to limit the maximum size of data transferred in a single communication. These limitations are configured using SETMWL/GETMWL or SETMRL/GETMRL CCC commands. I3C also allows a separate maximum data transfer limit for Read and Write communications. From this the minimum value that can be set to MRL and MWL is the maximum MTU expected.

The maximum values for Writing to a Target are configured as follows:

- The Controller sends a GETMWL command to the Target device to read the maximum value configured on the device.
- The Controller can optionally send a SETMWL command to set this maximum limit. The value set by the Controller shall be less than or equal to the value reported in the first GETMWL command.
- The Controller then sends a GETMWL command to verify if the maximum value is set.
- SETMWL shall be negotiated after Dynamic Address assignment and prior to MAC transfers.
- MWL shall not be renegotiated.

The maximum values for Reading from a Target are configured as follows:

- The Controller sends a GETMRL command to the Target device to read the maximum value configured on the device.
- The Controller can optionally send a SETMRL command to set this maximum limit. The value set by the Controller shall be less than or equal to the value reported in the first GETMRL command and based on the input buffer limitation of the Controller.
- The Controller then sends a GETMRL command to verify if the maximum value is set.
- SETMRL shall be negotiated after Dynamic Address assignment and prior to MAC transfers.

- MRL shall not be renegotiated.

I3C communications are also characterized by their use of the 9th bit as a transition bit (T-bit). This means that the bit value from the Target devices notifies the Controller that the Target device has finished sending the data. This use of the T-bit during a read operation is used along with the LPDU length to identify the end of transmission. The Controller should perform an access of length determined by the T-bit or LPDU length (T-bit may be corrupted) but no longer than the MTU.

The MWL and MRL values determine the MTU i.e. the maximum value of the sum of the header, LPDU and trailer data expressed in Bytes. An LPDU Link Layer Frame may be shorter than the configured MWL and MRL level but it can never exceed these limits. The Controller can terminate a write operation by using a Repeated START or STOP as mentioned in clause 5.1.2.3.3 of MIPI I3C Basic Specification [4]. When the Target is sending Data that is shorter than the configured MRL value the Target shall follow the guidelines of clause 5.1.2.3.4 of MIPI I3C Basic Specification [4] and use the T-bit to indicate the end of transmission.

The MWL/MRL values configured do not include the address bytes from the I3C address header (MIPI I3C Basic specification [4], clause 5.1.2.2) used for indexing a write or read operation.

7.3.2 Frames generation and transfer rules

The Controller initiates an I3C Basic Access either to send a Frame, or retrieve a Frame from the Target after a MAC access request.

If the Controller has a Frame to send or receive, the Controller shall send/receive that Frame in a single I3C Basic Access. Maximum Read and Write lengths are determined by MTU as explained in clause 7.3.1.

To retrieve a Target Frame the Controller may proceed with the following steps:

- When the Controller does not have a Frame to send and the Target initiates a MAC access request asking for data transfer as explained in clause 7.2.3.3:
  - The Controller SHALL initiate an I3C Read access. When the Target has finished transferring all the Link Layer Frame data then it indicates it using the T-bit as per MIPI I3C Basic Specification [4], clause 5.1.2.3.4.
- When the Controller has a frame to send:
  - The Controller generates an I3C private write access with the Frame length less than the configured MWL following the Link Layer Frame structure.
  - When both, the Target and the Controller, have data to transfer and initiate a communication then the IBI arbitration shall be handled as defined in MIPI I3C Basic [4], clause 5.1.2.2. After the Arbitration the Controller has two possible options after the IBI:
    - Proceed to retrieve the data IBI from the Target by issuing a Private Read.
    - Continue to send the Frame by issuing a Private Write.

7.3.3 Data transfer cases

Some of the most representative data transfer cases, based on the Frames generation and transfer rules in clause 7.3.2, are described below. Any Frame sent by the Controller or the Target shall be preceded by a MAC phase issued respectively by the Controller or the Target.

Case 1: the Controller initiates the MAC phase and then sends a frame (Private Write access). I3C Basic Access length is determined by the Controller Frame length according to the MTU configuration of the Target.

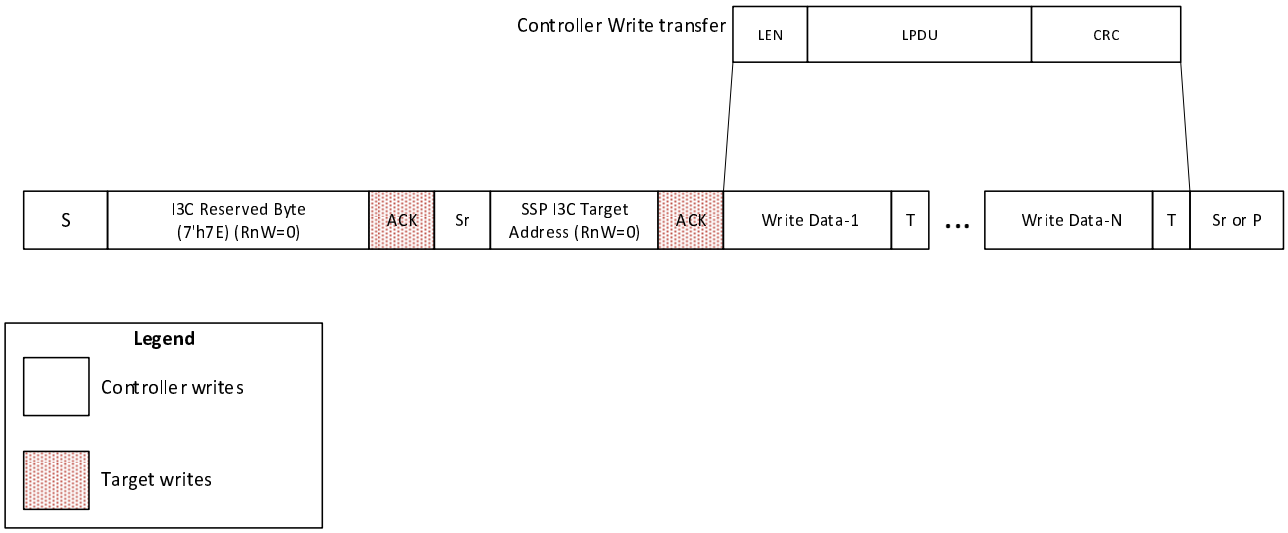


Figure 7.3.3-1: Controller sends a frame

Case 2: the Controller initiates the MAC phase and then reads a Frame (Private Read access). I3C maximum access length is determined by the Target Frame length according to the MTU configuration of the Target and the actual access length is determined by the Target control of T-bit.

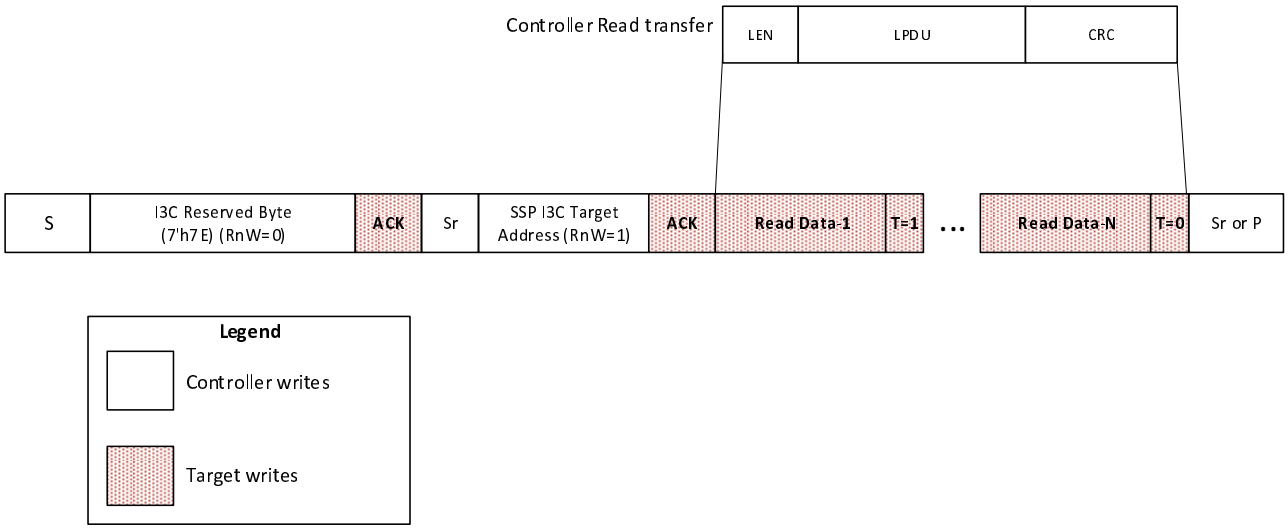


Figure 7.3.3-2: Controller reads a Frame

Case 3a: the Target initiates a Target MAC access request to transfer a Frame by issuing an IBI. The Target has a dedicated pending read MDB byte that allows the Controller to receive IBI request with special code that follows the type of IBI request. The Controller shall proceed with the appropriate step after receiving the MDB byte.

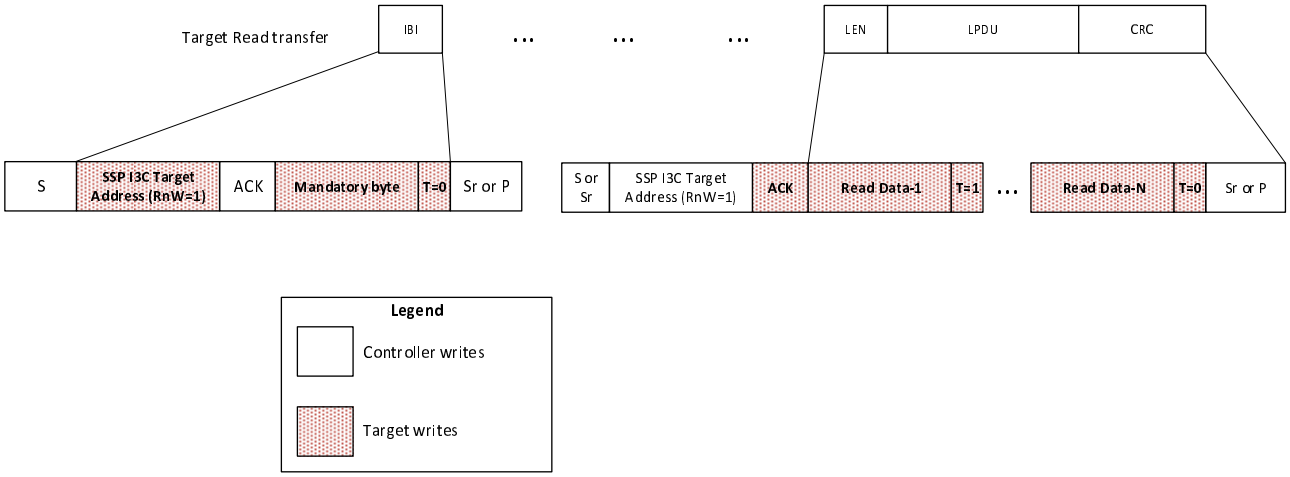


Figure 7.3.3-3: Target transfer a Frame by issuing an IBI with a dedicated pending read MDB byte

Case 3b: the Target initiates a Target MAC access request to transfer a Frame by issuing an IBI. The Target has no MDB byte and the Controller shall proceed with the appropriate measures it decides.

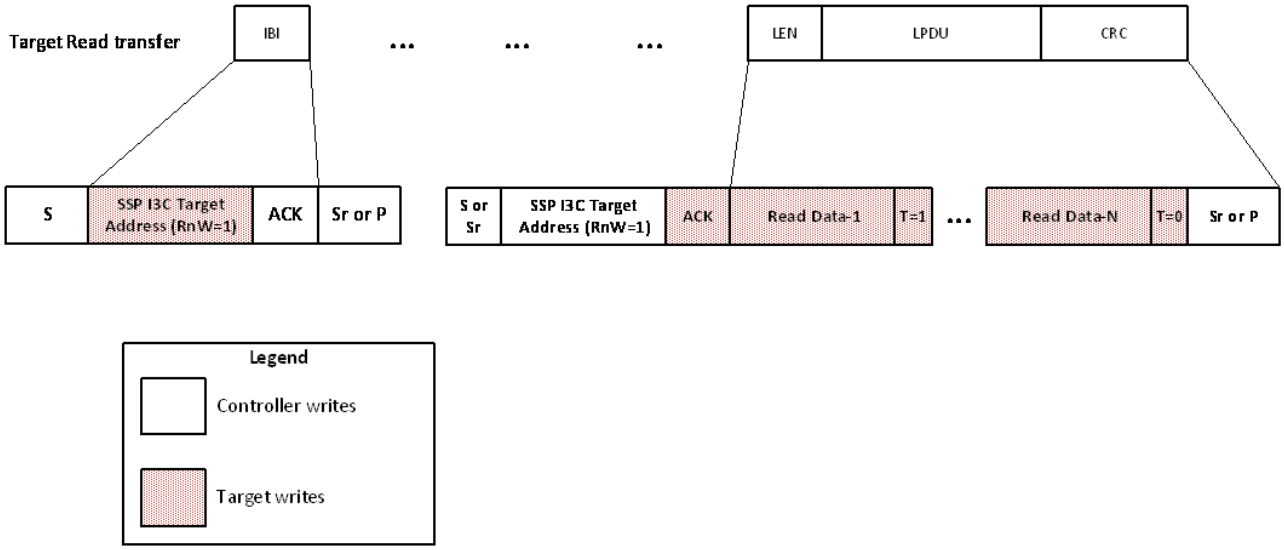


Figure 7.3.3-4: Target transfer a Frame by issuing an IBI with no MDB

Case 4: error case, when there is an early termination by the Controller. In such cases the Target and the Controller should assume the Frame is lost.

7.4 LLC layers

Three Logical Link Control (LLC) layers are defined in the present document:

- SHDLC: this is the generic LLC. SHDLC is defined in ETSI TS 102 613 [2], clause 10. Support of this LLC is mandatory for the Controller and the Target.
- CLT: this LLC is used for some proprietary protocol handling. CLT mode is defined in ETSI TS 102 613 [2], clause 11. Support of this LLC is optional for the Controller and the Target.
- MCT: this LLC consist of frames used during interface activation. Support of this LLC is mandatory for the Controller and the Target.

The control field is the first byte of the LPDU. Definition for the different LLC layers can be found in table 7.4-1.

Table 7.4-1: LLC control field coding

Frame types	Bit field							
	8	7	6	5	4	3	2	1
RFU	0	0	0	All settings				
MCT	0	0	1	MCT type				
ACT (not used)	0	1	1					
CLT	0	1	0	CLT CMD				
SHDLC	1	All settings						

The LPDUs shall be structured according to figures 7.4-1, 7.4-2 or 7.4-3, depending on the frame type.

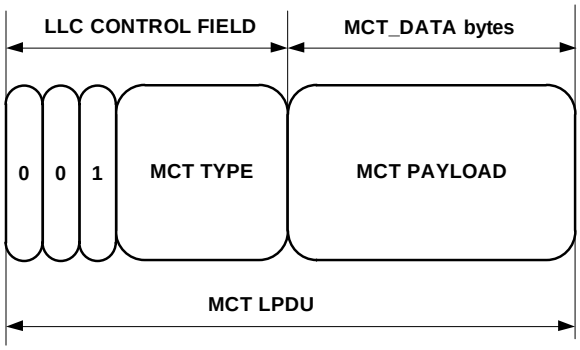


Figure 7.4-1: LPDU structure of the LLC layer of type MCT

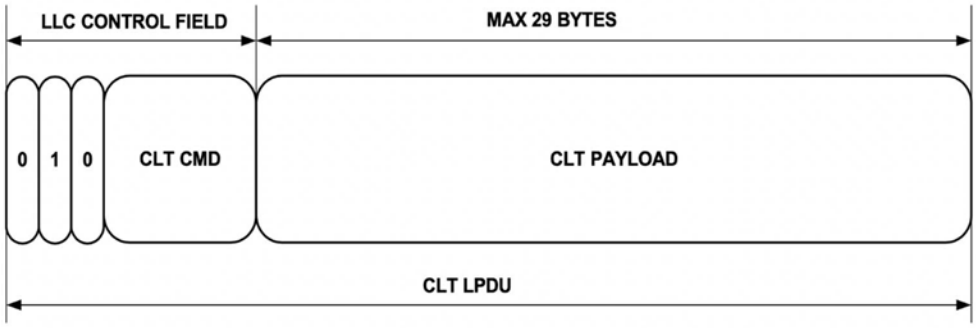


Figure 7.4-2: LPDU structure of the LLC layer of type CLT

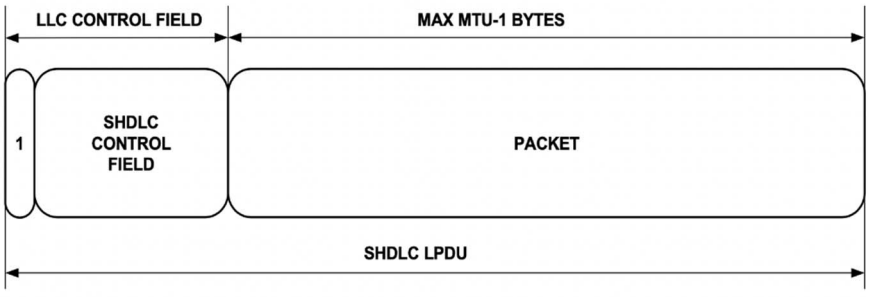


Figure 7.4-3: LPDU structure of the LLC layer of type SHDLC

7.5 Interworking of the LLC layers

After the MAC activation, the SHDLC link shall not be established and no CLT session shall be open. Only the MCT LLC shall be used by the Controller and by the Target for the I3C Link Layer initialization.

The Controller shall take the following action after a successful MCT LLC phase:

- If the Controller has data to be sent to the Target (e.g. due to a contactless transaction) that requires the use of the CLT LLC, it shall initiate a CLT LLC session.
- Otherwise it shall start the establishment of an SHDLC link as soon as possible.

After the Target and the Controller have established the SHDLC link or opened the CLT session, the Target and the Controller shall not send MCT LLC frames; received MCT LLC frames shall be ignored.

To enter the SHDLC LLC for the first time after MCT LLC, the link establishment procedure as described in clause 7.7.1 shall apply.

Once the SHDLC link is established, a CLT session shall not invalidate the SHDLC context and the endpoint capabilities negotiated during the SHDLC link establishment.

To enter the CLT LLC from MCT LLC or SHDLC LLC, the CLT session shall be opened as described in clause 11.6 of ETSI TS 102 613 [2]. The Controller shall open a CLT session only when all SHDLC I-Frames are acknowledged. SHDLC LLC frames received by the Target or by the Controller during a CLT session close the CLT session.

In case the Target or the Controller receives a corrupted frame, then the receiving entity shall use the error recovery procedure defined for the LLC of the last correctly received frame. Immediately after MAC activation, the error handling of the MCT LLC shall apply.

LPDU may be the SCL packet as defined in ETSI TS 103 666-1 [1], clause 8.3.2.

7.6 MCT LLC definition

7.6.1 MCT LPDU structure

The MCT LPDU shall be structured according to figure 7.6.1-1.

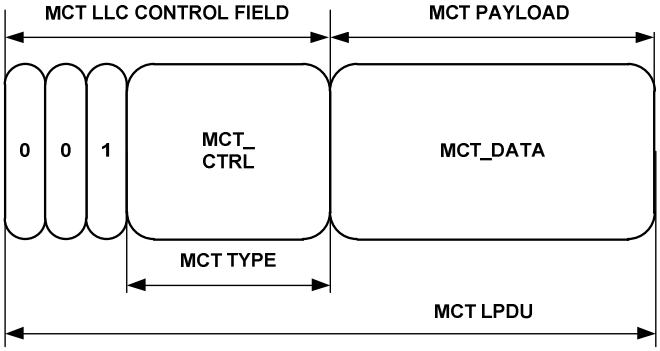


Figure 7.6.1-1: MCT LPDU structure

The meaning of MCT_CTRL and MCT_DATA is given in table 7.6.1-1.

Table 7.6.1-1: Meaning of MCT_CTRL and MCT_DATA

MCT_CTRL	Meaning	MCT_DATA
00000	MCT_READY Sent from the Target to the Controller	See table 7.6.3-1
00010	MCT_CONTROLLER_REQ Sent from the Controller to the Target	See table 7.6.2-1
All other values (see NOTE)	RFU	
NOTE: All other values are reserved for future use. These values shall not be set by the transmitting entity and shall be ignored by the receiving entity.		

7.6.2 MCT_DATA from Controller

Tables 7.6.2-1, 7.6.2-2 and 7.6.2-3 define the capabilities of the Controller.

Table 7.6.2-1: Controller-specific MCT_DATA field

Byte	Info/parameter	Meaning
0	ETSI I3C specification version	Specification version to which the Controller is compliant. Defined in table 7.6.2-2
1	Capabilities	Defined in table 7.6.2-2.
2, 3	T4	Inactivity period for Power Saving Mode (ms) according to clause 7.8.2.1.
NOTE: All additional bytes (4 to 26) are reserved for future extensions of the protocol. They should not be sent by the Controller and shall be ignored by the Target.		

Table 7.6.2-2: I3C Basic Specification version

Bit field	Value	Meaning
8 to 4	00001	Major version of the ETSI I3C interface
3 to 1	000	Minor version of the ETSI I3C interface

Table 7.6.2-3: Controller capabilities indication in MCT_DATA field

Bit field	Value	Meaning
8 to 4	00000	RFU
3, 2	11	Full Power Mode 3 supported
	10	Full Power Mode 2 supported
	01	Full Power Mode 1
	00	Low Power Mode
1	1	RFU
	0	Flow control SHDLC-based (default)

After the I3C Basic activation, as defined in clause 7.2.3.4 or in clause 7.2.3.2, the Controller shall send the MCT_CONTROLLER_REQ frame and the Target shall respond with the MCT_READY frame.

The MCT phase shall be performed with the default I3C_CLK = 1MHz. If the Target supports limiting its maximum current, it should start in Low Power Mode following VDD ON and it may switch to a Full Power Mode, depending on the power mode capabilities received from the Controller in MCT_CONTROLLER_REQ.

MTU size is negotiated during device initialization according to clause 7.3.1 of the present document using Maximum Write Length and Maximum Read Length. The minimum MTU value supported by the Controller and by the Target shall be 32 bytes.

The Controller indicates in MCT_CONTROLLER_REQ its power source availability, (i.e. Low Power, Full Power Mode 1, Full Power Mode 2 or Full Power Mode 3).

7.6.3 MCT_DATA from Target

Tables 7.6.3-1 and 7.6.3-2 define the capabilities of the Target.

Table 7.6.3-1: Target-specific MCT_DATA field (bytes 0…9)

Byte	Info/parameter	Meaning
0	ETSI I3C specification version	Specification version to which the Target is compliant. Defined in table 7.6.2-2.
1	I3C_CLK	Max I3C_CLK value supported by the I3C Target (MHz).
2	Capabilities	Defined in table 7.6.3-2.
3	T3	Target Resume Time from Power Saving Mode (µs).
4, 5	T4	The Target supported Inactivity period for entering Power Saving Mode T4 (ms), according to clause 7.8.2.1.
6	T5	The time (ms) from VDD valid until a Target device is ready to be assigned a dynamic address (ms) (see note 1 and note 2).
7	POT	Power-ON Time: time after Target VDD valid when the Target is initialized, according to I3C Basic protocol, and the Controller can send MCT_CONTROLLER_REQ (ms) (see note 1 and note 2).
NOTE 1: This value should be used by the Controller at next power on. The initial value used by the Controller for the first time Target power on should be 1 s. NOTE 2: POT includes the time from VDD valid until a Target device is initialized and ready to receive the MCT_CONTROLLER_REQ. T5 value shall be less than or equal to POT reported. NOTE 3: All additional bytes (8 to 26) are reserved for future extensions of the protocol. They should not be sent by the Target and shall be ignored by the Controller.		

Table 7.6.3-2: Target capabilities indication in MCT_DATA field byte 0

Bit field	Value	Meaning
8 to 4	00000	RFU.
3, 2	11	Full Power Mode 3 supported.
	10	Full Power Mode 2 supported.
	01	Full Power Mode 1.
	00	Low Power Mode.
1	1	RFU.
	0	Flow control SHDLC based (default).

Low Power, Full Power Mode 1, Full Power Mode 2 and Full Power mode 3 current values are out of scope of the present document. These power modes are described for general reference for the Controller and the Target when applicable and are not mandatory. The Controller and the Target may agree at the system design time on the implementation of specific power requirements, on the power modes to be supported, and specific current levels may be defined for the power modes. In a particular case the Controller includes in its power budget the maximum current required by the Target and in this case the Target may ignore the power modes information sent by the Controller in MCT_DATA.

The interface specification defines only the negotiation mechanism to be used at interface initialization (MCT), while the power levels and other related requirements are defined in other specifications, for specific use-cases, as needed.

7.6.4 MCT activation procedure

Target start up time following power on includes the dynamic addressing state. T5 is defined as a minimum delay for the Target to be able to receive a Dynamic Address. The Controller can assign a Dynamic Address at any time after the T5 reported and the initial value of T5 is 1s for the first power on. The T5 shall always be less than or equal to the POT Target start up time following power on is defined as POT and has an initial value of 1 s for the first power on, when the Target reported MCT_READY parameters are not yet available. After POT (from the time VDD is valid after power-on) if the Dynamic Address is assigned the Target shall be ready to receive the MCT_CONTROLLER_REQ from the Controller. Shorter POT and T5 values may be reported by the Target in MCT_READY. The Controller shall use T5 value reported by the Target or a higher value in subsequent dynamic address procedures after a power up sequence. The Controller shall use the POT value reported by the Target or a higher value in subsequent power up sequences, as the minimum time after VDD valid before sending the MCT_CONTROLLER_REQ.

The Controller shall wait for MCT_READY from the Target after sending MCT_CONTROLLER_REQ. In case the Target did not send MCT_READY response (no MAC access request) within MCT_TARGET_TIMEOUT or if MCT_READY is corrupted, the Controller shall retry the MCT activation by sending another MCT_CONTROLLER_REQ frame. The Controller shall retry at least two times, i.e. shall resend MCT_CONTROLLER_REQ at least twice without power toggle. Further specific recovery procedures, after these retries are implementation specific and out of scope of the present document.

After power up, if the Target gets a corrupted frame or any other frame instead of the MCT_CONTROLLER_REQ, the Target shall discard the data and remain in receive state. If the Target receives three corrupted or invalid frames instead of MCT_CONTROLLER_REQ, the Target should enter Power Saving Mode. If the MCT activation has not been successfully performed or the Controller did not initiate an I3C Basic Access within MCT_CONTROLLER_TIMEOUT following power on or for the subsequent retries in case of errors, the Target should enter Power Saving Mode.

MCT_CONTROLLER_TIMEOUT is the maximum time within which the Controller shall send the MCT_CONTROLLER_REQ after power on or for the retries in case of errors. The value defined is 1 s.

MCT_TARGET_TIMEOUT is the maximum time within which the Target shall send the MCT_READY response to MCT_CONTROLLER_REQ. The default value defined is 200 ms. A Target may send MCT_READY faster according to certain applications requirements.

7.7 SHDLC LLC definition

7.7.1 SHDLC overview

The provisions of ETSI TS 102 613 [2], clause 10.1 shall apply. The SWP SHDLC layer is replaced by the I3C SHDLC layer defined in the present document.

The SHDLC layer shall ensure that data passed up to the next layer has been received exactly as transmitted i.e. error free, without loss and in the correct order. Also, the SHDLC layer manages the flow control, which ensures that data is transmitted only as fast as the receiver may receive it.

The provisions of ETSI TS 102 613 [2] clauses from 10.3 to 10.8 shall apply. Additional SHDLC rules are defined below.

7.7.2 Endpoints

SHDLC communication occurs between two endpoints. Those endpoints may be either the Controller endpoint or the Target endpoint. There is no priority of traffic.

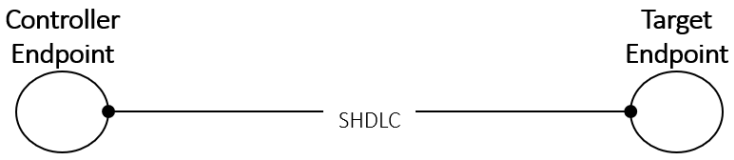


Figure 7.7.2-1: Endpoints

In ETSI TS 102 613 [2], clause 10, the term CLF refers to the Controller endpoint and the term UICC to the Target endpoint.

7.7.3 Flow control

7.7.3.1 Overview

Flow control is performed by a transmitter in order to avoid corruption or loss of data. It consists of methods applied by the transmitter and receiver in order to send a maximum number of SHDLC frames that can be accepted by the receiver, after which it shall stop sending data until the receiver sends at least an acknowledgement (e.g. SHDLC I-frame or SHDLC S-frame) for one of the received SHDLC frames.

7.7.3.2 Flow control based on SHDLC

The method defined in this clause is based on SHDLC flow control, as defined in ETSI TS 102 613 [2].

In addition to the provisions of clause 7.3.2, the total number of bytes transferred on I3C Basic shall be done in a single frame where the maximum frame lengths shall be less than MTU or a window size slot depth.

The maximum number of SHDLC frames that can be sent by a transmitter is determined by the negotiated window size.

7.8 Power management

7.8.1 Power saving mode

In order to optimize the power consumption, both the Controller and the Target may enter into Power Saving Mode. This clause defines the conditions for the Target to enter into Power Saving Mode and the procedures for the Controller for resuming the Target from Power Saving Mode.

The Controller and the Target shall both resume in the same LLC context following the Controller or the Target resumption. The Controller and the Target may then initiate the switch to a different LLC context according to clause 7.5.

7.8.2 Conditions for entering Power Saving Mode

7.8.2.1 Target entering Power Saving Mode

The Target shall not enter into Power Saving Mode, if the Target has issued a MAC access request and is waiting for data transfer from the Controller.

The Target may enter into Power Saving Mode in one of the cases below, assuming there is no pending activity:

1) All frames have been transmitted by the Target, acknowledged successfully by the Controller and the Target detects an inactivity time T4 with no MAC request by the Controller. Entering into Power Saving Mode based on the inactivity period may be disabled by the Controller through the inactivity period value negotiated at interface initialization as described below.

2) The Target informs that it does not require or expect any further activities e.g. through EVT_LINK_END_OF_OPERATION sent from its Link Application Gate to the Link Service Gate of the Network Controller Host, as defined in ETSI TS 103 666-1 [1]. The Target may enter into Power Saving Mode after it receives the SHDLC link layer acknowledgement for EVT_LINK_END_OF_OPERATION.

3) Following the power-up or during MCT activation procedure as described in clause 7.6.4, when the Target does not detect any activity for more than the default inactivity period MCT_CONTROLLER_TIMEOUT.

The inactivity period T4 is negotiated by the Controller and the Target at interface initialization as described in clause 7.6. The Controller shall provide an inactivity period in MCT_CONTROLLER_REQ and the Target shall send back an MCT_READY with the same T4 value for acceptance, or a different value if it cannot support the value received from the Controller. If the Controller sends T4='FFFF' in MCT_CONTROLLER_REQ, the Target shall disable the entering Power Saving Mode on detection of an inactivity period and the Target shall send an MCT_READY with the same T4 value. If the Target sends T4='FFFF' in MCT_READY it indicates to the Controller that the Target will not enter into Power Saving Mode based on the detection of inactivity time, regardless the value sent by the Controller in the MCT_CONTROLLER_REQ and the Controller should not resume the Target on this condition.

In Power Saving Mode the Target shall maintain the high impedance state (High-Z) on SCL and SDA lines.

7.8.2.2 Controller entering Power Saving Mode

The Controller may enter into an implementation-specific Power Saving Mode at any time, without informing the Target. The Target power source status and capabilities indicated by the Controller at interface initialization shall not change when the Controller enters into Power Saving Mode, is in Power Saving Mode, is resuming from Power Saving Mode or after the Controller has resumed. SDA and SCL lines shall be maintained high impedance state (High-Z) by the Controller when the Controller is in Power Saving Mode and when the Controller is resuming. The Controller shall maintain the Pull-up or High keeper to keep the high level at all times the bus is not used for the communication.

The Controller before entering low power mode may send a DISEC CCC. This will disable the Target from sending an IBI. Therefore, the Target may not be able to communicate with the Controller until the Controller leaves the Power Saving Mode and executes the ENEC CCC enabling the IBI.

7.8.3 Resuming from Power Saving Mode

7.8.3.1 Resuming the Target from Power Saving Mode

The Controller may perform one of the following procedures to resume the Target:

- Use an out of band line to signal wake up.
- Use a private communication using the Target dynamic address:
  - This communication shall be sent without the broadcast address:
    - Sending a private communication without the broadcast address may conflict with IBI requests and this should be handled according to MIPI I3C Basic Specification [4], clause 5.1.2.2.3.
  - Since Target devices are in Power Saving Mode (offline) the dynamic address will not be acknowledged.
- If the Target detects an out of band wake up signal or the Target detects an address matching its dynamic address, then it shall resume from Power Saving Mode.
- Optional wakeup procedures based on a private agreement between the Target and the Controller may be implemented in addition to the mandatory wakeup procedures described above. (i.e. Target Rest pattern of I3C Basic Specification).

7.8.3.2 Resuming the Controller from Power Saving Mode

If the Controller has entered into Power Saving Mode without sending DISEC CCC to disable the IBI , then it shall resume when the Target initiates a MAC access request. The Target initiates the MAC access request with the procedures as described in clause 7, regardless the power management status of the Controller. Following a resume by a MAC access request , the Controller shall provide an SCL clock as specified in MIPI I3C Basic Specification [4], clause 5.1.6.

The leading edge of the MAC access request (pull down on SDA line) should trigger the resuming of the Controller.

The Target may use an out of band signal or other proprietary methods to initiate the Controller resume from power-saving mode. These methods are out of scope for the present document.

Annex A (normative): SSP Adoption of MIPI Alliance I3C Basic specification

A.1 Overview

ETSI TS 103 818 refers MIPI I3C Basic specification [4]. For the scope of SSP platform not all the mandatory features and commands present in MIPI I3C Basic specification [4] are mandatory in ETSI TS 103 818.

A.2 SSP I3C features classification

A.2.1 Mandatory features for SSP

The following features defined in MIPI I3C Basic specification [4] are mandatory for each SSP supporting ETSI TS 103 818:

- Dynamic Addressing
- In Band Interrupt
- SDR Mode Target
- Private Read and Write with MWL and MRL support
- CCC commands Broadcast, direct

A.2.2 Optional features for SSP

The following features defined in MIPI I3C Basic specification [4] are optionally supported by each SSP supporting ETSI TS 103 818:

- HDR modes
- Secondary Controller role
- Target Reset pattern
- Multi-Lane Data Transfer
- Timing control
- Events timestamping
- Group Addressing
- Virtual addressing
- Mandatory Data Byte for IBI
- Pending read notification (IBI)

A.2.3 Not Supported features for SSP

Table 83 described in MIPI I3C Basic specification [4] allows voltage ranges not supported by ETSI SSP specifications. To avoid misunderstanding, following voltage is explicitly defined not supported by each SSP supporting ETSI TS 103 818:

- 1.0V electrical.

A.3 SSP I3C CCC commands classification

A.3.1 CCC mandatory commands for SSP

The following Common Command Codes (CCC) defined in MIPI I3C Basic specification [4] are mandatory for each SSP supporting ETSI TS 103 818:

- ENTDAA
- SETDASA
- GETSTATUS
- GETMRL
- SETMRL
- GETMWL
- SETMWL
- ENEC
- DISEC
- RSTDAA
- SETNEWDA
- GETPID
- GETBCR
- GETDCR

A.3.2 CCC optional commands for SSP

The following Common Command Codes (CCC) defined in MIPI I3C Basic specification [4] are optionally supported by each SSP supporting ETSI TS 103 818:

- GETMXDS
- ENTAS0
- ENTAS1
- ENTAS2
- ENTAS3
- ENTTM
- SETBUSCON

- ENDXFER
- ENTHDR0
- ENTHDR1
- ENTHDR2
- ENTHDR3
- ENTHDR4
- ENTHDR5
- ENTHDR6
- ENTHDR7
- SETXTIME
- SETAASA
- RSTACT
- SETGRPA
- RSTGRPA
- MLANE
- GETCAPS

History

Document history		
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