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Technical Specification

Satellite Earth Stations and Systems;
Air Interface for S-band Mobile Interactive Multimedia (S-MIM);
Part 4: Physical Layer Specification,
Return Link Synchronous Access

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Foreword

This Technical Specification (TS) has been produced by ETSI Technical Committee Satellite Earth Stations and Systems (SES).

The present document is part 4 of a multi-part deliverable. Full details of the entire series can be found in part 1 [5].

Introduction

The present document concerns the S-MIM (S-band Mobile Interactive Multimedia) system in which a standardised S-band satellite mobile broadcast system is complemented by the addition of a return channel.

The technology applied has been developed in the framework of the publicly funded project "DENISE" (ESTEC/Contract Number 22439/09/NL/US).

The S-MIM system specified herein is designed to provide:

- interactive mobile broadcast services enhancing DVB-SH services;

- messaging services for handhelds and vehicular terminals, capable of serving millions of terminals due to a novel optimised air-interface in the RTN link;

- real-time emergency services such as voice and file transfer, mainly addressing institutional users on-the-move such as fire brigades, civil protection, etc.

Inside the S-band, the 2 GHz MSS band is of particular interest for interactive multimedia, since it allows two-way transmission. Typically, the DVB-SH standard [i.4] is applied for broadcast transmission; ESDR [i.2] is an alternative. Essential requirements under the R&TTE directive are covered by the harmonized standard EN 302 574 [i.3], [1] and [2].

1   Scope

The present document is part 4 of a multipart deliverable and concerns aspects of the air interface for the S-band Mobile Interactive Multimedia (S-MIM) system, and in particular it specifies the Physical Layer REturn Link for Synchronous Access.

The other parts are listed in the foreword of part 1 [5].

2   References

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

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2.1   Normative references

The following referenced documents are necessary for the application of the present document.

[1]   ETSI EN 302 574-2: "Satellite Earth Stations and Systems (SES); Harmonized standard for satellite earth stations for MSS operating in the 1 980 MHz to 2 010 MHz (earth-to-space) and 2 170 MHz to 2 200 MHz (space-to-earth) frequency bands; Part 2: User Equipment (UE) for wideband systems: Harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive".

[2]   ETSI EN 302 574-3: "Satellite Earth Stations and Systems (SES); Harmonized standard for satellite earth stations for MSS operating in the 1 980 MHz to 2 010 MHz (earth-to-space) and 2 170 MHz to 2 200 MHz (space-to-earth) frequency bands; Part 3: User Equipment (UE) for narrowband systems: Harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive".

[3]   ETSI TS 125 212: "Universal Mobile Telecommunications System (UMTS); Multiplexing and channel coding (FDD) (3GPP TS 25.212)".

[4]   ETSI TS 125 213: "Universal Mobile Telecommunications System (UMTS); Spreading and modulation (FDD) (3GPP TS 25.213)".

[5]   ETSI TS 102 721-1: "Satellite Earth Stations and Systems; Air Interface for S-band Mobile Interactive Multimedia (S-MIM); Part 1: General System Architecture and Configurations".

[6]   ETSI TS 102 721-6: "Satellite Earth Stations and Systems; Air Interface for S-band Mobile Interactive Multimedia (S-MIM); Part 6: Protocol Specifications, System Signalling".

2.2   Informative references

The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

[i.1]   "Bandlimited Quasi-Synchronous CDMA: A Novel Satellite Access Technique for Mobile and Personal Communications Systems". R. De Gaudenzi, C. Elia, R. Viola, 1992. IEEE Journal on Selected Areas in Communications.

[i.2]   ETSI EN 302 550 (all parts): "Satellite Earth Stations and Systems (SES); Satellite Digital Radio (SDR) Systems; Part 1: Physical Layer of the Radio Interface".

[i.3]   ETSI EN 302 574-1: "Satellite Earth Stations and Systems (SES); Harmonized standard for satellite earth stations for MSS operating in the 1 980 MHz to 2 010 MHz (earth-to-space) and 2 170 MHz to 2 200 MHz (space-to-earth) frequency bands; Part 1: Complementary Ground Component (CGC) for wideband systems: Harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive".

[i.4]   ETSI TS 102 585: "Digital Video Broadcasting (DVB); System Specifications for Satellite services to Handheld devices (SH) below 3 GHz".

3   Definitions, symbols and abbreviations

3.1   Definitions

For the purposes of the present document, the following terms and definitions apply:

2 GHz MSS band: 1 980 to 2 010 MHz (earth-to-space) and 2 170 to 2 200 MHz (space-to-earth) frequency bands

   NOTE: These paired bands are assigned to MSS.

architecture: abstract representation of a communications system

   NOTE: Three complementary types of architecture are defined:

   - Functional Architecture: the discrete functional elements of the system and the associated logical interfaces.

   - Network Architecture: the discrete physical (network) elements of the system and the associated physical interfaces.

   - Protocol Architecture: the protocol stacks involved in the operation of the system and the associated peering relationships.

S-band: equivalent to 2 GHz MSS band

user plane: plane that has a layered structure and provides user information transfer, along with associated controls

3.2   Symbols

For the purposes of the present document, the following symbols apply:

E_b Received energy per information (payload) bit
E_s Received energy per (channel) symbol
I_0 Single-sided interference power spectral density
N_0 Single-sided noise power spectral density

3.3   Abbreviations

For the purposes of the present document, the following abbreviations apply:

C   number of Columns
CDMA   Code Division Multiple Access
CGC   Complementary Ground Component
CMF   Control and Monitoring Functions
CW   CodeWord
DCH   Dedicated Channel
DMPCCH   Dedicated Mobile Physical Control Channel
DMPDCH   Dedicated Mobile Physical Data CHannel

DPDCH	Dedicated Physical Data CHannel
DW	DataWord
EIRP	Effective Isotropic Radiated Power
EIRP	Equivalent Isotropically Radiated Power
ESDR	ETSI Satellite Digital Radio
FWD	Forward
LHCP	Left-Hand Circular Polarization
MAC	Medium Access Control
ML	Maximal Length
MSS	Mobile Satellite Services
OVSF	Orthogonal Variable Spreading Factor
PCCC	Parallel Concatenated Convolutional Code
PCRACH	Physical Control Random Access Channel
PDRACH	Physical Data Random Access CHannel
QPSK	Quadrature Phase Shift Keying
QS-CDMA	Quasi-Synchronous CDMA
QSCM	QS-CDMA Configuration Messages
QSCT	QS-CDMA Configuration Table
QSDT	QS-CDMA Dynamic Table
QSPCT	QS-CDMA Power Correction Table
RACH	Random Access CHannel
RF	Radio Frequency
RHCP	Right-Hand Circular Polarization
RL	Return-Link
RMS	Root Mean Square
RTN	Return
Rx	Receive
SAP	Service Access Point
SF	Spreading Factor
S-MIM	S-band Mobile Interactive Multimedia
SNIR	Signal to Noise plus Interference Ratio
SSA	Spread Spectrum Aloha
Tx	Transmit
UE	User Equipment
ULB	Up-Link Burst
ULB	Up-Link Burst
WCDMA	Wideband Code Division Multiple Access

4 General Description

The present document specifies the physical layer for the Synchronous Access option of the Return Link using the Quasi-Synchronous CDMA (QS-CDMA) technique [i.1].

The present document covers the Return-Link (RL) satellite transmission.

S-MIM quasi-synchronous access is intended for real-time emergency services since:

- it maximises the number of simultaneous connections without the need for complex interference cancellation techniques; and

- it provides a good solution to return link band-sharing with S-MIM Asynchronous access (SSA for interactive messaging) due to the spread spectrum characteristic of both transmission schemes.

4.1 Relationship to other layers

4.1.1 General Protocol Architecture

The overall protocol architecture for the return link of S-MIM synchronous access is shown in Figure 4.1.
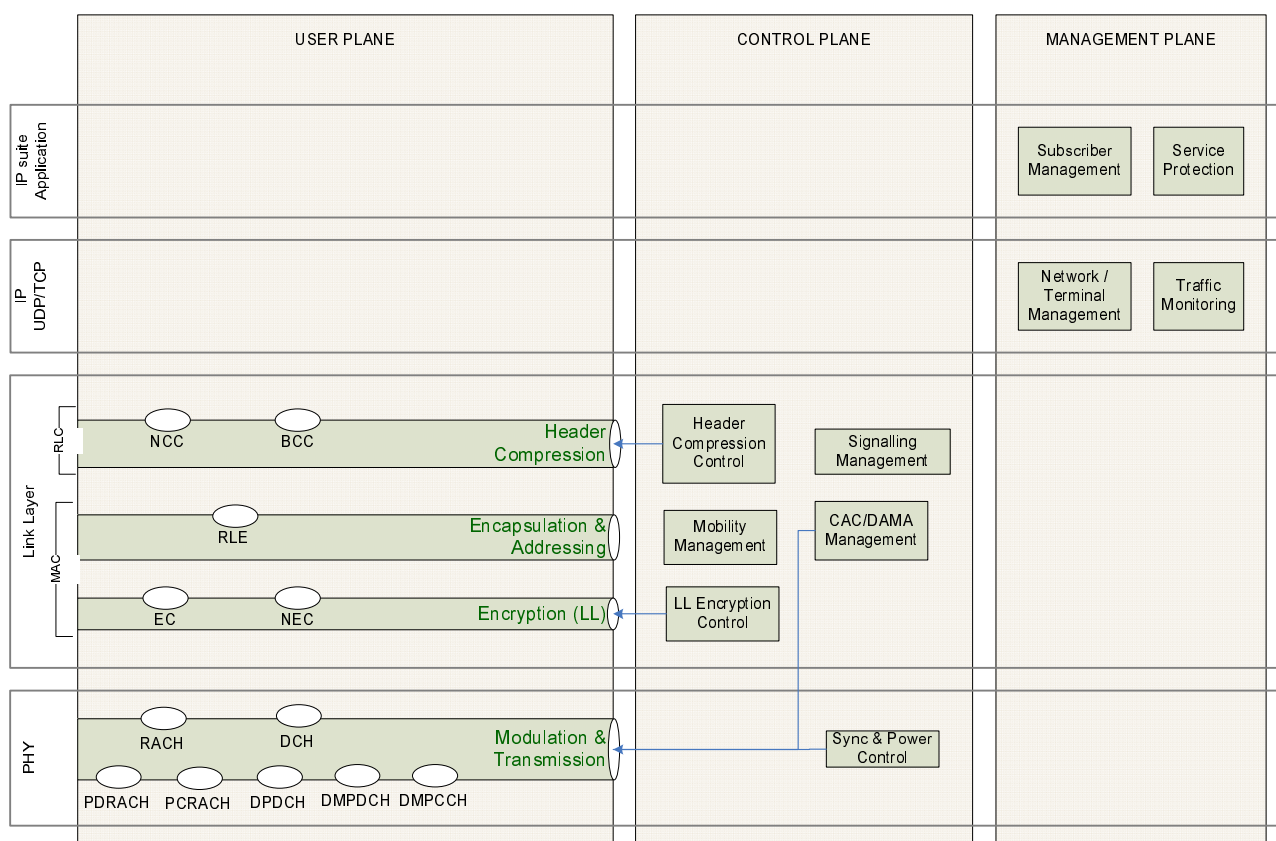
Figure 4.1: Protocol Architecture for the Synchronous Return Link

The circles between different layer/sub-layers indicate Service Access Points (SAPs).

The MAC offers different Logical channels to the higher layer. A logical channel is characterized by the type of information transferred. The physical layer has an interface to, and offers Transport channels to, the Medium Access Control (MAC) sub-layer. A transport channel is characterized by how, and with which characteristics, the information is transferred over the radio interface. Physical channels are defined in the physical layer and are characterized by the physical resources (time, frequency, code, and space) that are used to transport data/control/signalling to/from a single user or a multitude of users.

The present document is concerned with the Physical Layer.

4.1.2 Services provided to higher layers

The physical layer offers data transport services to higher layers. The access to these services is through the use of transport channels via the MAC sub-layer. The physical layer is expected to perform the following functions in order to provide the data transport service:

- Error detection on transport channels and indication to higher layers.

- FEC encoding/decoding of transport channels.

- Multiplexing of transport channels and demultiplexing of coded composite transport channels

- Mapping of coded transport channels on physical data channels.

- Power weighting and combining of physical channels.

- Modulation and spreading/demodulation and de-spreading of physical channels.

- Frequency and time (chip, bit, burst) synchronisation.

- Radio characteristics measurements and indication to higher layers (for further study).

- RF processing.

4.2   Transmitter functional architecture

In the transmission direction Physical Layer functional block diagram is shown in Figure 4.2.
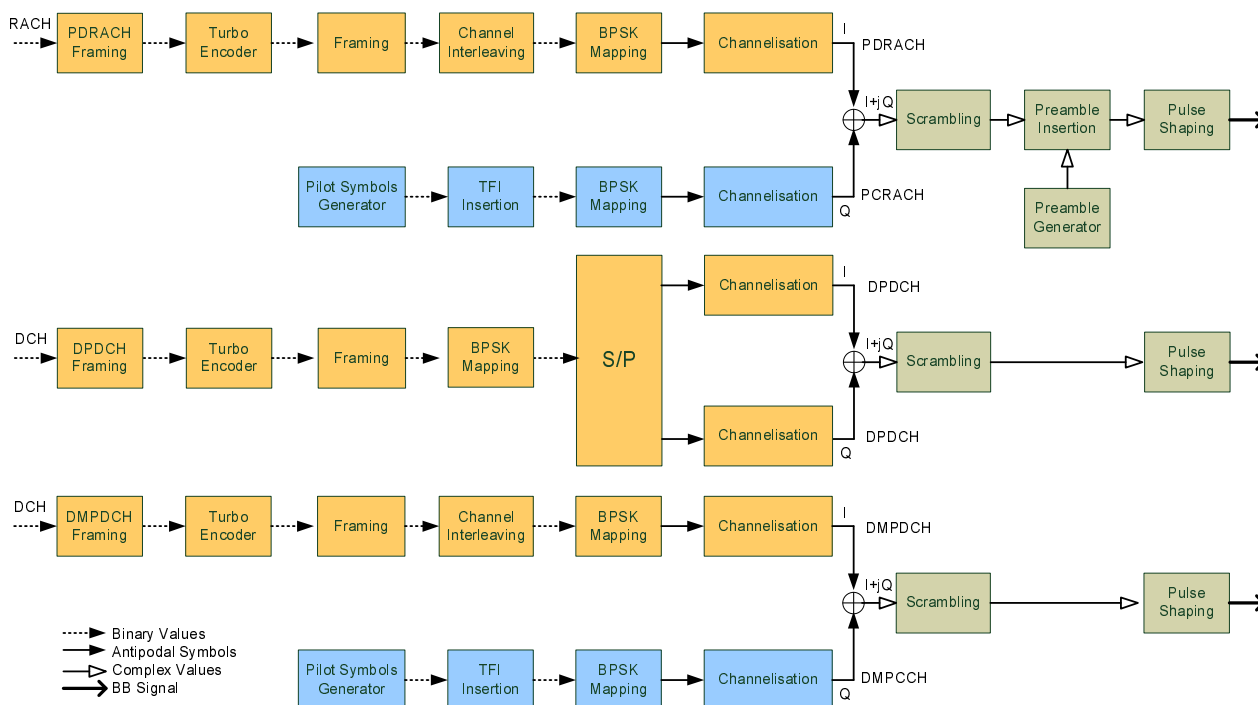
Figure 4.2: Transmitter Functional Block Diagram

4.3   Channel description

4.3.1   Transport channels

Two transport channels are defined, namely:

- A Random Access Channel (RACH), characterized by limited size data field, a collision risk and by the use of open loop power control, used to convey system specific signalling whenever no dedicated channel is available, e.g. at terminal logon. The RACH has a fixed burst length of 416 bits.

- A Dedicated Channel (DCH). DCHs are assigned to the different terminals through a DAMA protocol and are used to convey both data traffic and system specific signalling. The DCH has variable packet length of 952 bits, 1 976 bits or 4 024 bits for fixed terminals and of 968 bits, 1 992 bits, 4 040 bits or 8 128 bits for mobile terminals.

4.3.1.1   Transport-to-Physical Channel Mapping

The RACH is channel is mapped onto the PDRACH (see clause 5.1.1).

The DCH is mapped onto the DPDCH for stationary terminals (see clause 5.2.1) and onto the DMPDCH for mobile terminals (see clause 5.2.2).

4.3.2 Physical channels

Up to five physical channels are defined, namely:

1) a Physical Data Random Access Channel (PDRACH), mapped to the RACH;

2) a Physical Control Random Access Channel (PCRACH), carrying pilot symbols;

3) a Dedicated Physical Data Channel (DPDCH), mapped to DCH for stationary terminals;

4) a Dedicated Mobile Physical Data Channel (DMPDCH), mapped to DCH for mobile terminals;

5) a Dedicated Mobile Physical Control Channel (DMPCCH), carrying pilot symbols.

4.3.2.1 Random Access Channels

The PDRACH and the PCRACH are I/Q code multiplexed to form an Up-Link Burst (ULB), composed of three parts (Figure 4.3):

- a preamble;

- a Physical Data Random Access Channel (PDRACH);

- a Physical Control Random Access Channel (PCRACH)

The preamble is transmitted before the start of the PDRACH and PCRACH.

	PDRACH
Preamble	PCRACH

Figure 4.3: The Up-Link Burst and its constituent parts

4.3.2.2 Dedicated physical channels

Dedicated physical channels (DPDCH, DMPDCH, DMPCCH), assigned to different users and sharing the same radio channels are kept orthogonal to each other by use of orthogonal spreading codes. The DMPDCH and DMPCCH are I/Q code multiplexed together.

4.3.3 Radio channels

The following channelisations shall be supported by all terminals:

- 5 MHz bandwidth channels (baseline);

- 625 kHz bandwidth channels;

- 312,5 kHz bandwidth channels.

5 Physical Channel Structure

5.1 Random Access Channel Structure

The PDRACH and the PCRACH are I/Q code multiplexed to form an Up-Link Burst (ULB), to which is added the preamble (see Figure 4.3).

5.1.1   PDRACH structure

The PDRACH is composed of one or more frames, where each frame of 1 536 bits is composed (as illustrated in Figure 5.1) as follows:

- UW: 36-bits uncoded Unique Word. The word is 0xBDC686ECB (1011-1101-1100-0110-1000-0110-1110-1100-1011). The leftmost bit is transmitted first.

- Coded data: 1 500-bit codeword (CW) built from channel encoding the 496-bit dataword (DW) (as detailed in clause 6.1).
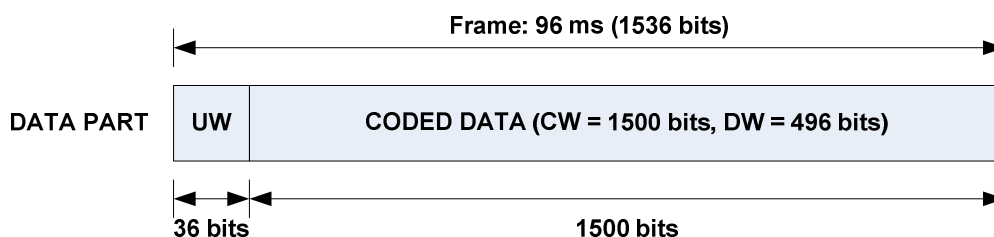
Figure 5.1: PDRACH frame structure

The content of the PDRACH dataword is shown in Figure 5.2.
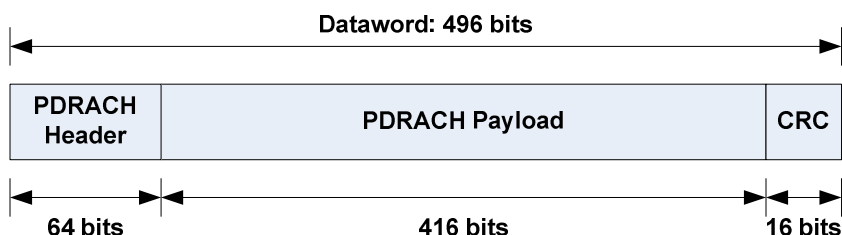
Figure 5.2: PDRACH dataword

The 496-bit dataword consists of three parts:

- PDRACH Header: 64-bit header:

  - *MAC_addr*: 48-bit MAC address.

  - *Frame_counter*: 4-bit frame counter starting from 0.

  - *Total_frames*: 4-bit field indicating the total number of frames. The total number of frames is *Total_frames* + 1.

  - *RFU:* 8-bit field reserved for future use.

- PDRACH Payload: 416-bit field carrying the RACH data.

- CRC: 16-bit CRC computed on the PDRACH Header and PDRACH Payload bits. The following polynomial is used: $g_{CRC}(X) = X^{16} + X^{15} + X^2 + 1$.

The set of allowed parameters of the PDRACH is reported in Table 5.1. The configuration is uniquely determined by the chip rate, i.e. by the RF channel width.

Table 5.1: Allowed PDRACH configurations

PDRACH Configuration ID	Chip rate (kchip/s)	SF	Symbol rate (kbauds)	Coding scheme
$CR_{4\,096}$-PDRACH	4 096	256	16	TC 1/3
CR_{512}- PDRACH	512	32	16	TC 1/3
CR_{256}- PDRACH	256	16	16	TC 1/3

5.1.2   PCRACH structure

The PCRACH is composed of a sequence of pilot symbols, which is a segment of a Maximal Length (ML) sequence. The polynomial for the pseudo-random binary sequence generator is:

$$G(X) = X^{15} + X^{14} + 1$$

The shift register generating the sequence is loaded with a given value PF_{seed}. The shift register shall be reset to PF_{seed} at the start of each PDRACH frame. Thus, the first bit at the output of the generator corresponds to the first pilot symbol in a frame.

The value PF_{seed} shall be broadcast by the Hub within the QSCT table defined in TS 102 721-6 [6].

The pilot symbol generator is shown in Figure 5.3.
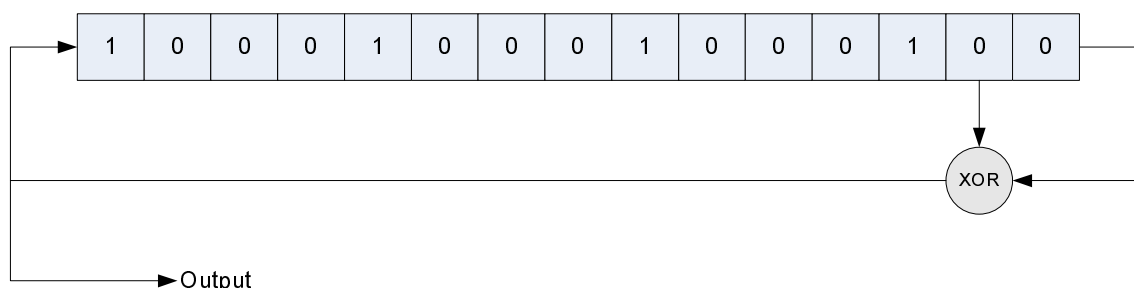
Figure 5.3: Pilot symbols generator

5.1.3   Preamble format

The preamble is composed of a sequence of N_p symbols, which is repeated in both in-phase and quadrature components.

The sequence of symbols is a segment of a Maximal Length (ML) sequence. The polynomial for the pseudo-random binary sequence generator is:

$$G(X) = X^{10} + X^7 + 1$$

The shift register generating the sequence is loaded with an initial value P_{seed}. The first bit at the output of the generator corresponds to the first symbol in the preamble.

The value P_{seed} and the number of symbols N_p of the preamble shall be broadcast by the Hub within the QSCT table in TS 102 721-6 [6].

The preamble generator is shown in Figure 5.4.
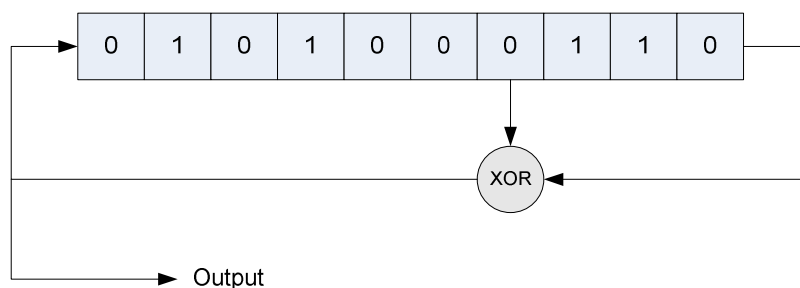
Figure 5.4: Up-Link Burst Preamble generator

5.2 Dedicated Channel Structure

5.2.1 DPDCH structure

The DPDCH is structured in frames as it is illustrated in Figure 5.5.
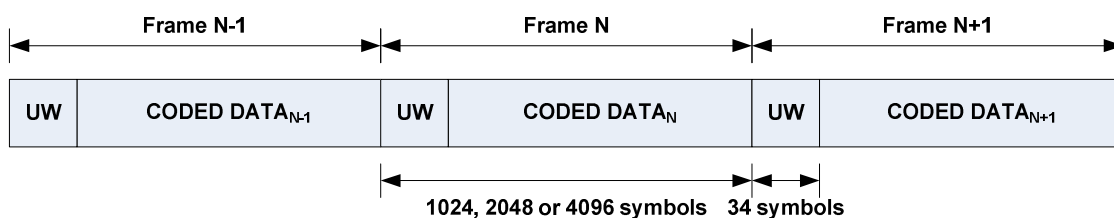
Figure 5.5: DPDCH frame structure

Three different frame lengths (1 024 bits, 2 048 bits and 4 096 bits) are defined. Each frame is composed of two fields:

- UW: 34-bits uncoded Unique Word. The word is 0x3DE8B6230 (11-1101-1110-1000-1011-0110-0010-0011-0000). The leftmost bit is transmitted first.

- Coded data: variable size codeword (CW) built from channel encoding a DPDCH dataword (as detailed in clause 6.1) according to Table 5-2.

The content of the DPDCH dataword is shown in Figure 5.6.
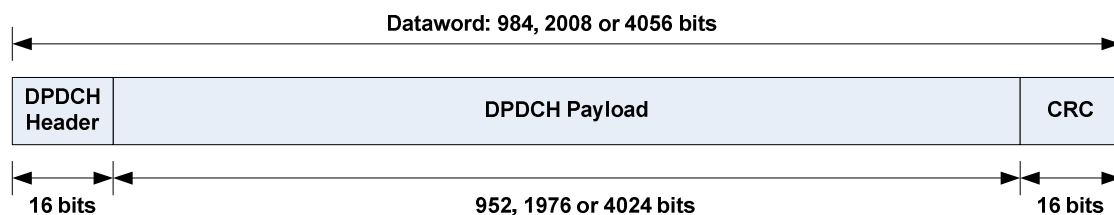
Figure 5.6: DPDCH dataword

The DPDCH dataword consists of three parts:

- DPDCH Header: 16-bit header.

  - *Frame_counter*: 8-bit frame counter.

  - *RFU:* 8-bit field reserved for future use.

- DPDCH Payload: field carrying the DCH data.

- CRC: 16-bit CRC computed on the PHY Header and PHY Payload fields. The following polynomial is used:
$g_{CRC}(X) = X^{16} + X^{15} + X^2 + 1$.

DPDCH frames specification is shown in Table 5.2. The frame configuration is uniquely determined by its symbol rate.

Table 5.2: DPDCH frame specification

Symbol rate (kbauds)	Frame length (symbols)	Frame period (ms)	Codeword (bits)	Dataword (bits)	DPDCH payload (bits)	DPDCH net bit rate (kbit/s)
16	1 024	64	1 980	984	952	14,875
32	1 024	32	1 980	984	952	29,75
64	2 048	32	4 028	2 008	1 976	61,75
128	2 048	16	4 028	2 008	1 976	123,5
256	4 096	16	8 124	4 056	4 024	251,5
512	4 096	8	8 124	4 056	4 024	503

The set of allowed parameters of the DPDCH is reported in Table 5.3. The configuration is uniquely determined by the chip rate, i.e. by the RF channel width, and by the selected spreading factor.

Table 5.3: DPDCH channel definition

| DPDCH Configuration ID	Chip rate (kchip/s)	SF	Symbol rate (kbauds)	Coding scheme
CR_{4096}-SF_{256}-DPDCH	4 096	256	16	TC 1/2
CR_{4096}-SF_{128}-DPDCH	4 096	128	32	TC 1/2
CR_{4096}-SF_{64}-DPDCH	4 096	64	64	TC 1/2
CR_{4096}-SF_{32}-DPDCH	4 096	32	128	TC 1/2
CR_{4096}-SF_{16}-DPDCH	4 096	16	256	TC 1/2
CR_{4096}-SF_{8}-DPDCH	4 096	8	512	TC 1/2
CR_{512}-SF_{32}-DPDCH	512	32	16	TC 1/2
CR_{512}-SF_{16}-DPDCH	512	16	32	TC 1/2
CR_{512}-SF_{8}-DPDCH	512	8	64	TC 1/2
CR_{512}-SF_{4}-DPDCH	512	4	128	TC 1/2
CR_{256}-SF_{16}-DPDCH	256	16	16	TC 1/2
CR_{256}-SF_{8}-DPDCH	256	8	32	TC 1/2
CR_{256}-SF_{4}-DPDCH	256	4	64	TC 1/2

5.2.2   DMPDCH and DMPCCH structure

The DMPDCH and DMPCCH are I/Q code multiplexed to form frames with a fixed period of 128 ms, as illustrated in Figure 5.7.
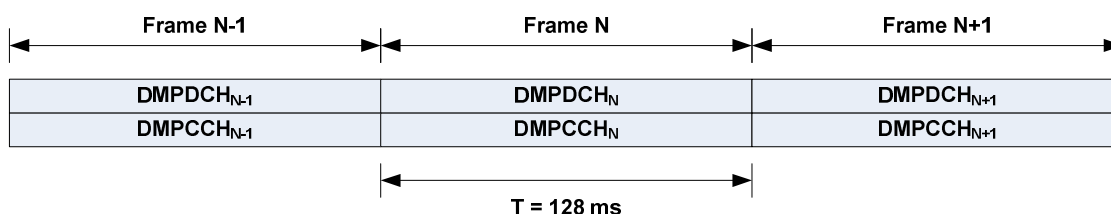
Figure 5.7: DMPDCH and DMPCCH frame structure

Each frame is thus composed of two parts:

- A Dedicated Mobile Physical Data Channel (DMPDCH), uniquely determined by its chip rate and spreading factor as detailed in Table 5.5.

- The Dedicated Mobile Physical Control Channel (DMPCCH), determined by the chip rate of the DMPDCH, carrying pilot symbols generated in the same way described in clause 5.1.2. The spreading factor shall be 256, 32 and 16 for the three channelisations available (5 MHz, 625 kHz and 312,5 kHz).

The DMPDCH frame is composed of two fields as illustrated in Figure 5.8.
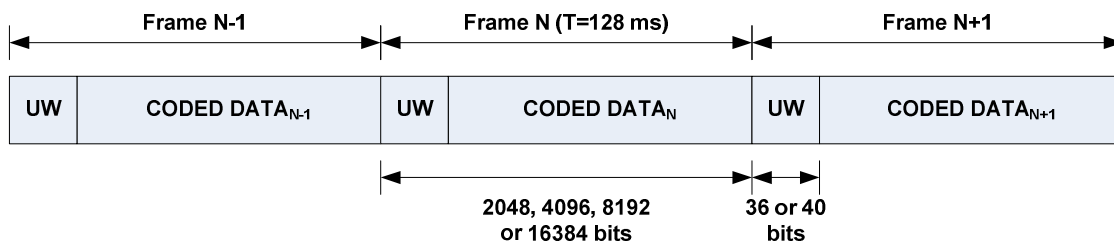
Figure 5.8: DMPDCH frame structure

The DMPDCH frame consists of:

- UW: 36- or 40-bits uncoded Unique Word:

    - The 36-bits word is 0xBDC686ECB (1011-1101-1100-0110-1000-0110-1110-1100-1011). The leftmost bit is transmitted first.

    - The 40-bits word is 0x8FA2ED7BC9 (1000-1111-1010-0010-1110-1101-0111-1011-1100-1001). The leftmost bit is transmitted first.

- Coded data: variable size codeword (CW) built from channel encoding a DMPDCH datawords (as detailed in clause 6.1) according to Table 5.4.

The content of the DMPDCH dataword is shown in Figure 5.9.
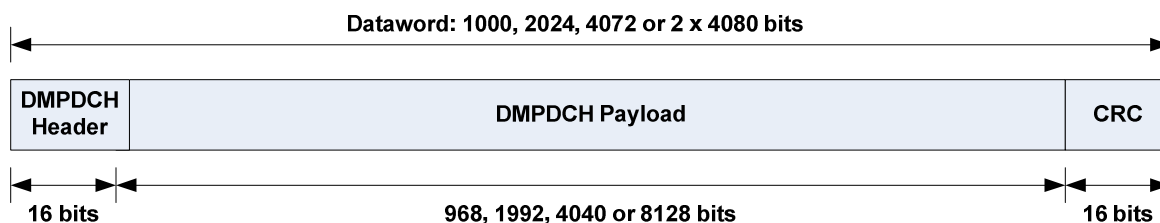
Figure 5.9: DMPDCH dataword

The DMPDCH dataword consists of three parts:

- DMPDCH Header: 16-bit header.

    - *Frame_counter*: 8-bit frame counter.

    - *RFU:* 8-bit field reserved for future use.

- DMPDCH Payload: field carrying the DCH data.

- CRC: 16-bit CRC computed on the DMPDCH Header and DMPDCH Payload fields. The following polynomial is used: $g_{CRC}(X) = X^{16} + X^{15} + X^2 + 1$.

The DMPDCH frame specification is shown in Table 5.4. The frame configuration is uniquely determined by its symbol rate.

Table 5.4: DMPDCH frame specification

Symbol rate (kbauds)	Frame length (symbols)	Frame period (ms)	UW length (symbols)	Codeword (bits)	Dataword (bits)	DMPDCH payload (bits)	DMPDCH net bit rate (kbit/s)
16	2 048	128	36	2 012	1 000	968	7,5625
32	4 096	128	36	4 060	2 024	1 992	15,5625
64	8 192	128	36	8 156	4 072	4 040	31,5625
128	16 384	128	40	2 x 8 172	2 x 4 080	8 128	63,5

The set of allowed parameters of the DPDCH is reported in Table 5.5. The configuration is uniquely determined by the chip rate, i.e. by the RF channel width, and by the selected spreading factor.

Table 5.5: DMPDCH channel definition

DMPDCH Configuration ID	Chip rate (kchip/s)	SF	Symbol rate (kbauds)	Coding scheme
CR_{4096}-SF_{256}-DMPDCH	4 096	256	16	TC 1/2
CR_{4096}-SF_{128}-DMPDCH	4 096	128	32	TC 1/2
CR_{4096}-SF_{64}-DMPDCH	4 096	64	64	TC 1/2
CR_{4096}-SF_{32}-DMPDCH	4 096	32	128	TC 1/2
CR_{512}-SF_{32}-DMPDCH	512	32	16	TC 1/2
CR_{512}-SF_{16}-DMPDCH	512	16	32	TC 1/2
CR_{512}-SF_{8}-DMPDCH	512	8	64	TC ½
CR_{512}-SF_{4}-DMPDCH	512	4	128	TC ½
CR_{256}-SF_{16}-DMPDCH	256	16	16	TC ½
CR_{256}-SF_{8}-DMPDCH	256	8	32	TC ½
CR_{256}-SF_{4}-DMPDCH	256	4	64	TC ½

6 Channel Coding and Interleaving

6.1 Channel Coding

Channel coding is performed differently for:

1) PDRACH.

2) DPDCH and DMPDCH.

6.1.1 PDRACH channel coding

The PDRACH employs the same turbo-coding scheme as the 3GPP WCDMA standard [3], of coding rate 1/3.

As illustrated in Figure 6.1, the Turbo-coder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one Turbo code internal interleaver.
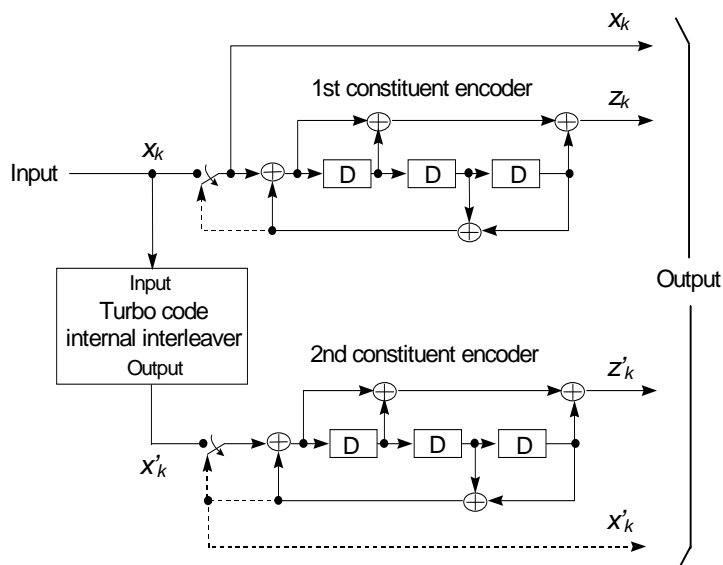
Figure 6.1: Structure of rate 1/3 Turbo-coder (dotted lines apply for trellis termination only)

6.1.2 DPDCH and DMPDCH channel coding

The coding scheme for DPDCH and DMPDCH is based on the coding scheme used by the PDRACH defined above, but a final puncturing stage is added in order to reduce the coding rate from 1/3 to 1/2.

6.1.2.1 Puncturing pattern

The code used is systematic, which means that only parity bits (z_k or z'_k) are punctured, whereas the input bits x_k are kept. The puncturing pattern is defined in Table 6.1, where '1' means that the bit is transmitted and '0' means that it is punctured.

Table 6.1: Puncturing pattern for coding rate 1/2

	k	k+1
Systematic bit x_k	1	1
Parity bit z_k	1	0
Parity bit z'_k	0	1

Puncturing is only applied on information bits, preserving tail bits.

6.2 Channel Interleaving

Coded bits are interleaved before spreading and modulation. The interleaving is only applied to:

- PDRACH (all terminals)

- DMPDCH (mobile terminals only)

The interleaver acts over the coded bits of each individual frame, not including the UW. Thus, the resulting interleaving depths are 93,75 ms for the PDRACH and slightly less than 128 ms for the DMPDCH, depending on the frame and UW lengths specified in Table 5.4.

The following channel interleaver specification is based on the 2nd interleaving stage defined for 3GPP [3].

The channel interleaver is a block interleaver and consists of bits input to a matrix with padding, the inter-column permutation for the matrix and bits output from the matrix with pruning. The bits input to the block interleaver are denoted by $u_1, u_2, u_3, ..., u_U$, where U is the number of bits in one radio frame. The output bit sequence from the block interleaver is derived as follows:

1) Select the number of columns of the matrix C from Table 6.2. The columns of the matrix are numbered 0, 1, 2, …, C - 1 from left to right.

2) Determine the number of rows of the matrix, R, by finding minimum integer R such that:

$$U \leq R \times C.$$

The rows of rectangular matrix are numbered 0, 1, 2, …, R - 1 from top to bottom.

3) Write the input bit sequence $u_1, u_2, u_3, ..., u_U$ into the $R \times C$ matrix row by row starting with bit y_1 in column 0 of row 0:

$$\begin{bmatrix} y_1 & y_2 & y_3 & \cdots & y_C \\ y_{(C+1)} & y_{(C+2)} & y_{(C+3)} & \cdots & y_{2C} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{((R-1)C+1)} & y_{((R-1)C+2)} & y_{((R-1)C+3)} & \cdots & y_{RC} \end{bmatrix}$$

where $y_k = u_k$ for $k = 1, 2, …, U$ and if $R \times C > U$, the dummy bits are padded such that $y_k = 0$ or 1 for $k = U + 1, U + 2, …, R \times C$. These dummy bits are pruned away from the output of the rectangular matrix after the inter-column permutation.

4) Perform the inter-column permutation for the matrix based on the pattern $\left\langle P(j) \right\rangle_{j \in \{0,1,...,C-1\}}$ that is shown in Table 6.2, where $P(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the bits are denoted by y'_k.

$$\begin{bmatrix} y'_1 & y'_{(R+1)} & y'_{(2R+1)} & \cdots & y'_{((C-1)R+1)} \\ y'_2 & y'_{(R+2)} & y'_{(2R+2)} & \cdots & y'_{((C-1)R+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_R & y'_{2R} & y'_{3R} & \cdots & y'_{CR} \end{bmatrix}$$

5) The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted $R \times C$ matrix. The output is pruned by deleting dummy bits that were padded to the input of the matrix before inter-column permutation, i.e. bits y'_k that correspond to bits y_k with $k > U$ are removed from the output. The bits after interleaving are denoted by $v_1, v_2, ..., v_U$, where v_1 corresponds to the bit y'_k with the smallest index k after pruning, v_2 to the bit y'_k with the second smallest index k after pruning, and so on.

Table 6.2: Inter-column permutation patterns for channel interleaving

| Turbo-coder coding rate	Number of columns *C*	Inter-column permutation pattern < *P*(0), *P*(1), …, *P*(C-1) >
1/3	30	<0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29,12, 2, 7, 22, 27, 17>
1/2	16	<0, 8, 4, 12, 2, 10, 6, 14, 1, 9, 5, 13, 3, 11, 7, 15>

7 Spreading and Modulation

7.1 Spreading

The adopted spreading scheme is based on 3GPP [4]; any differences are described.

Spreading is applied to all physical channels. It consists of two operations. The first is the channelisation operation, which transforms every data symbol into a number of chips, thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation, where a scrambling code is applied to the spread signal.

With the channelisation, data symbol on so-called I- and Q-branches are independently multiplied with an OVSF code. With the scrambling operation, the resultant signals on the I and Q-branches are further multiplied by a complex-valued scrambling code.

7.1.1 PDRACH and PCRACH spreading

Figure 7.1 illustrates the principle of the spreading and scrambling of the PDRACH and PCRACH, or data and pilot parts respectively. The binary data and pilot parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value -1. PDRACH and PCRACH are spread to the chip rate by the channelisation codes $C_{ch,i}$ and $C_{ch,q}$, respectively.
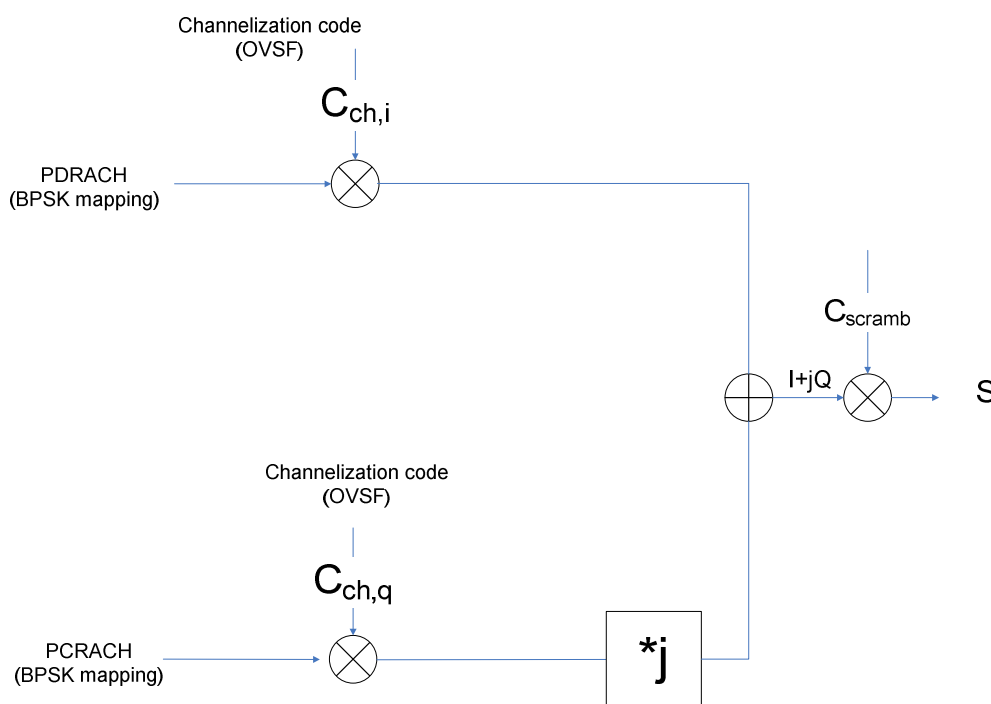
Figure 7.1: PDRACH and PCRACH spreading scheme

After channelisation, the stream of real-valued chips on the I and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code C_{scramb}. The scrambling code is applied aligned with the PDRACH and PCRACH frames.

Channelisation and scrambling codes are broadcast in the QS-CDMA Configuration Table (QSCT), see TS 102 721-6 [6].

7.1.2 DPDCH spreading

Figure 7.2 illustrates the principle of the spreading and scrambling for the DPDCH. The binary data to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value -1.

A serial to parallel multiplexing of the incoming DPDCH frames is performed as shown in Figure 7.2. Note that the UW present in each DPDCH frame according to clause 5.2.1 is not multiplexed, but repeated entirely on both I and Q branches instead. Data is spread to the chip rate by the channelisation codes $C_{ch,i}$ and $C_{ch,,q}$ respectively.

After channelisation, the stream of real-valued chips on the I and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code C_{scramb}. The scrambling code is applied aligned with the DPDCH frames.

Channelisation and scrambling codes are given in the QS-CDMA Terminal Information Message (QSTIM), see TS 102 721-6 [6].

The same channelisation code could be used for the I and Q-branches in order to improve system capacity. All DPDCHs transmitted within the same radio frequency channel use the same scrambling sequence.
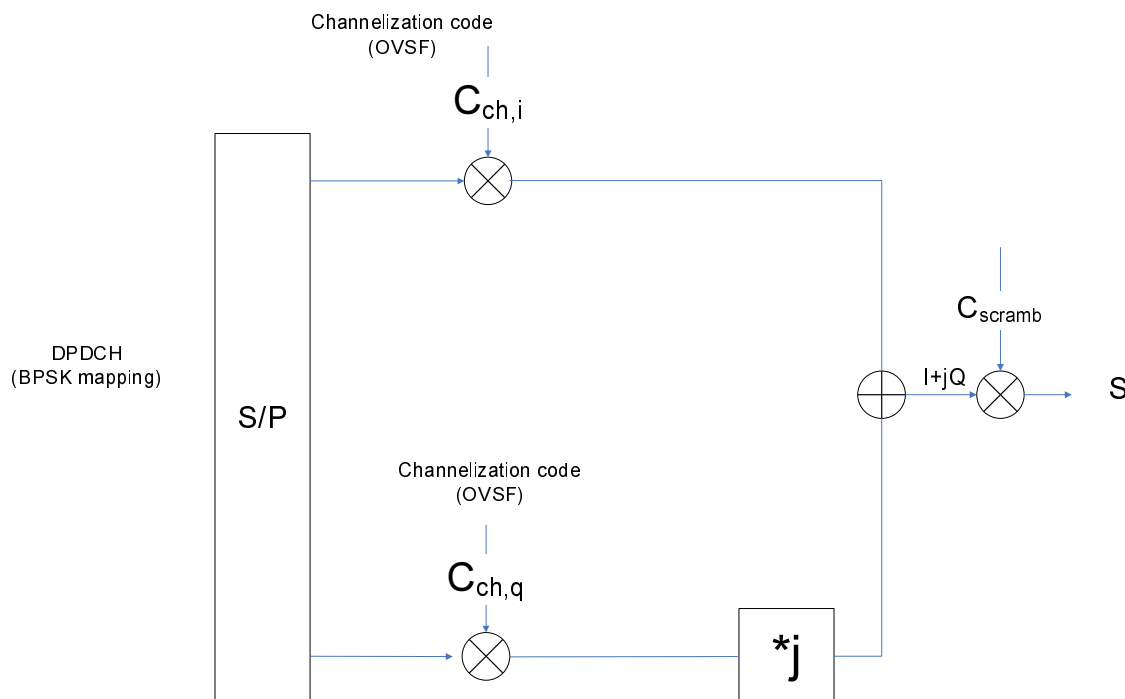
Figure 7.2: DPDCH spreading scheme

7.1.3   DMPDCH and DMPCCH spreading

Figure 7.3 illustrates the principle of the spreading and scrambling for the DMPDCH and DMPCCH. The binary data and pilot parts to be spread are represented by real-valued sequences, i.e. the binary value "0" is mapped to the real value +1, while the binary value "1" is mapped to the real value -1. Data and pilot parts are spread to the chip rate by the channelisation codes $C_{ch,i}$ and $C_{ch,q}$, respectively.

Channelization code
(OVSF)

$C_{ch,i}$

DMPDCH
(BPSK mapping)

C_{scramb}

I+jQ

S

Channelization code
(OVSF)

Control Channel
Gain Factor

$C_{ch,q}$

β

DMPCCH
(BPSK mapping)

*j
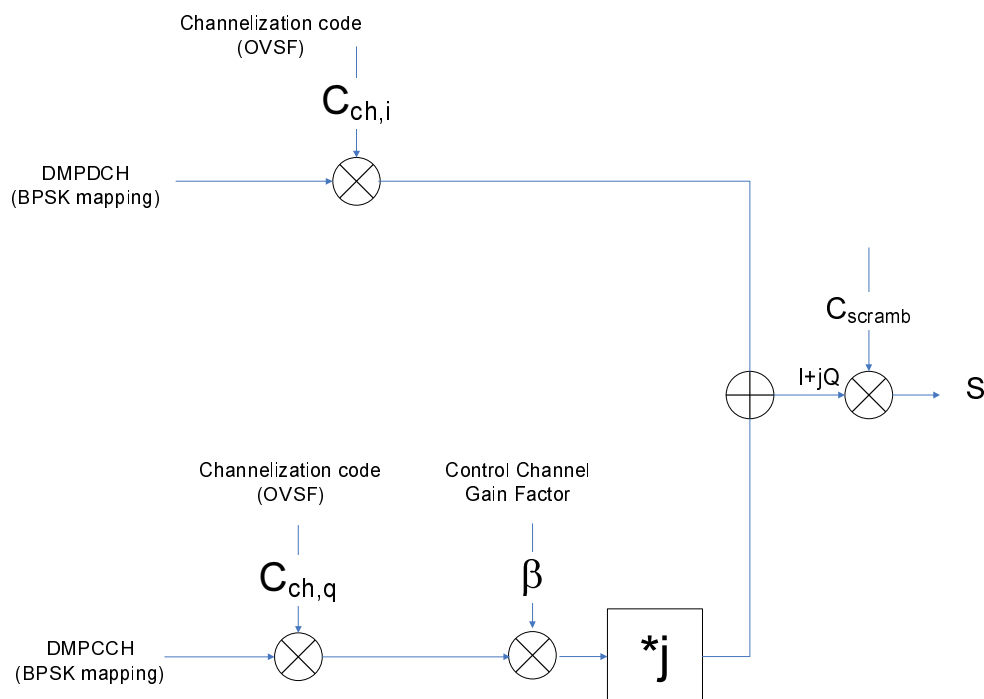
Figure 7.3: DMPDCH and DMPCCH spreading scheme

After channelisation, the DMPCCH symbols are weighted by a gain factor β. The β -values are quantised into 4 bit words. The quantisation steps are given in Table 7.1.

Table 7.1: Quantisation of the gain parameter

Signalling values for β	Quantised amplitude ratios
15	1,0
14	14/15 = 0,9333
13	13/15 = 0,8667
12	12/15 = 0,8000
11	11/15 = 0,7333
10	10/15 = 0,6667
9	9/15 = 0,6000
8	8/15 = 0,5333
7	7/15 = 0,4667
6	6/15 = 0,4000
5	5/15 = 0,3333
4	4/15 = 0,2667
3	3/15 = 0,2000
2	2/15 = 0,1333
1	1/15 = 0,0667
0	Switch off

After the weighting, the stream of real-valued chips on the I and Q-branches are treated as a complex-valued stream of chips. This complex-valued signal is then scrambled by the complex-valued scrambling code C_{scramb}. The scrambling code is applied aligned with the DMPDCH and DMPCCH frames.

All DMPDCHs and DMPCCH transmitted within the same radio frequency channel use the same scrambling sequence.

7.1.3.1 Channelisation code generation

The channelisation codes are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between different physical channels (dedicated physical channels only). The OVSF codes can be defined using the code tree of the Figure 7.4.

$$C_{ch,4,0} = (1,1,1,1)$$
$$C_{ch,2,0} = (1,1)$$
$$C_{ch,4,1} = (1,1,-1,-1)$$
$$C_{ch,1,0} = (1)$$
$$C_{ch,4,2} = (1,-1,1,-1)$$
$$C_{ch,2,1} = (1,-1)$$
$$C_{ch,4,3} = (1,-1,-1,1)$$

SF = 1   SF = 2   SF = 4
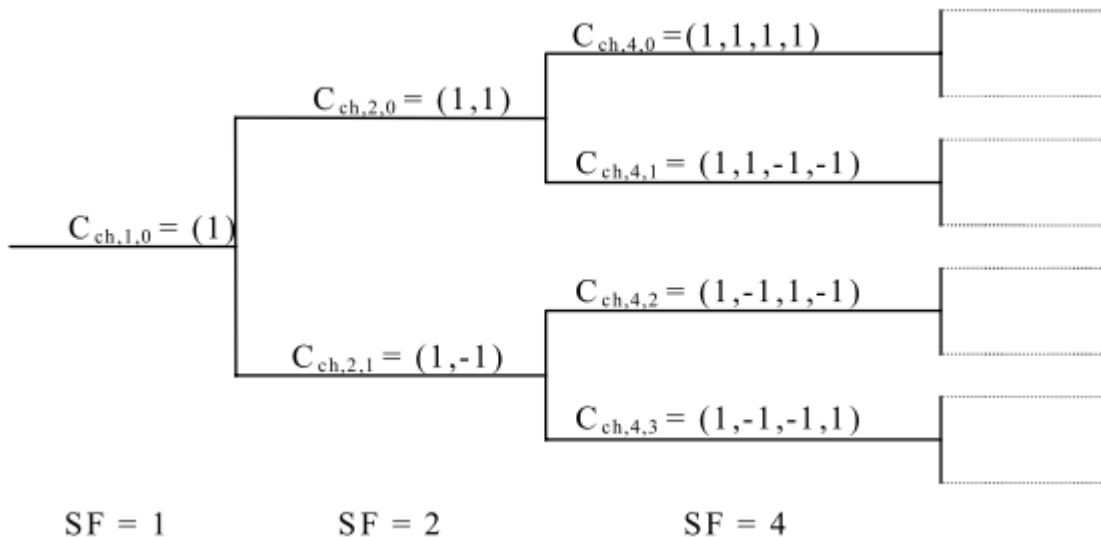
Figure 7.4: Code-tree for generation of Orthogonal Variable Spreading Factor (OVSF) codes

Channelisation codes are uniquely described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and k is the code number, $0 \le k \le SF-1$.

Each level in the code tree defines channelisation codes of the length SF, corresponding to a spreading factor of SF in Figure 7.4.

The generation method for the channelisation code is defined as:

$$C_{ch,1,0} = 1$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2^{(n+1)},0} \\ C_{ch,2^{(n+1)},1} \\ C_{ch,2^{(n+1)},2} \\ C_{ch,2^{(n+1)},3} \\ \vdots \\ C_{ch,2^{(n+1)},2^{(n+1)}-2} \\ C_{ch,2^{(n+1)},2^{(n+1)}-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix}$$

The leftmost value in each channelisation code word corresponds to the chip transmitted first in time.

7.1.3.2   Scrambling codes generation

All physical channels are subjected to scrambling with a complex-valued scrambling code. All physical channels use scrambling codes of length 256 chips. The approach adopted corresponds to one of the solutions foreseen in the 3GPP WCDMA for the uplink (short scrambling).

The scrambling sequences $c_{1,n}(i)$ and $c_{2,n}(i)$ are defined from a sequence from the family of periodically extended S(2) codes.

Let $n_{23}n_{22}...n_0$ be the 24 bit binary representation of the code number n.

The n-th quaternary S(2) sequence $z_n(i)$, $0 \leq n \leq 2^{24}-1$, is obtained by modulo 4 addition of three sequences, a quaternary sequence $a(i)$ and two binary sequences $b(i)$ and $d(i)$, where the initial loading of the three sequences is determined from the code number n. The sequence $z_n(i)$ of length 255 is generated according to the following relation:

$z_n(i) = a(i) + 2b(i) + 2d(i)$ modulo 4, $i = 0, 1, ..., 254;$

where the quaternary sequence $a(i)$ is generated recursively by the polynomial $g_0(x) = x^8 + x^5 + 3x^3 + x^2 + 2x + 1$ as:

$a(0) = 2n_0 + 1$ modulo 4;

$a(i) = 2n_i$ modulo 4, $i = 1, 2, ..., 7;$

$a(i) = 3a(i-3) + a(i-5) + 3a(i-6) + 2a(i-7) + 3a(i-8)$ modulo 4, $i = 8, 9, ..., 254;$

and the binary sequence $b(i)$ is generated recursively by the polynomial $g_1(x) = x^8 + x^7 + x^5 + x + 1$ as:

$b(i) = n_{8+i}$ modulo 2, $i = 0, 1, ..., 7;$

$b(i) = b(i-1) + b(i-3) + b(i-7) + b(i-8)$ modulo 2, $i = 8, 9, ... 254;$

and the binary sequence $d(i)$ is generated recursively by the polynomial $g_2(x) = x^8 + x^7 + x^5 + x^4 + 1$ as:

$d(i) = n_{16+i}$ modulo 2, $i = 0, 1, ..., 7;$

$d(i) = d(i-1) + d(i-3) + d(i-4) + d(i-8)$ modulo 2, $i = 8, 9, ... 254;$

The sequence $z_n(i)$ is extended to length 256 chips by setting $z_n(255) = z_n(0)$.

The mapping from $z_n(i)$ to the real-valued binary sequences $c_{1,n}(i)$ and $c_{2,n}(i)$, $i = 0, 1, …, 255$ is defined in Table 7.2.

Table 7.2: Mapping from $z_n(i)$ to $c_{1,n}(i)$ and $c_{2,n}(i)$, i = 0, 1, …, 255

$z_n(i)$	$c_{1,n}(i)$	$c_{2,n}(i)$
0	+1	+1
1	-1	+1
2	-1	-1
3	+1	-1

Finally, the complex-valued scrambling sequence $c_n(i)$ is defined as:

$$c_n(i) = c_{1,n}(i \bmod 256)\left(1 + j(-1)^i c_{2,n}\left(2\left\lfloor (i \bmod 256)/2 \right\rfloor\right)\right)$$

Where $i = 0, 1, 2, …$ and $\left\lfloor \ \right\rfloor$ denotes rounding to nearest lower integer.

An implementation of the scrambling sequence generator for the 255 chip sequence to be extended by one chip is shown in Figure 7.5.
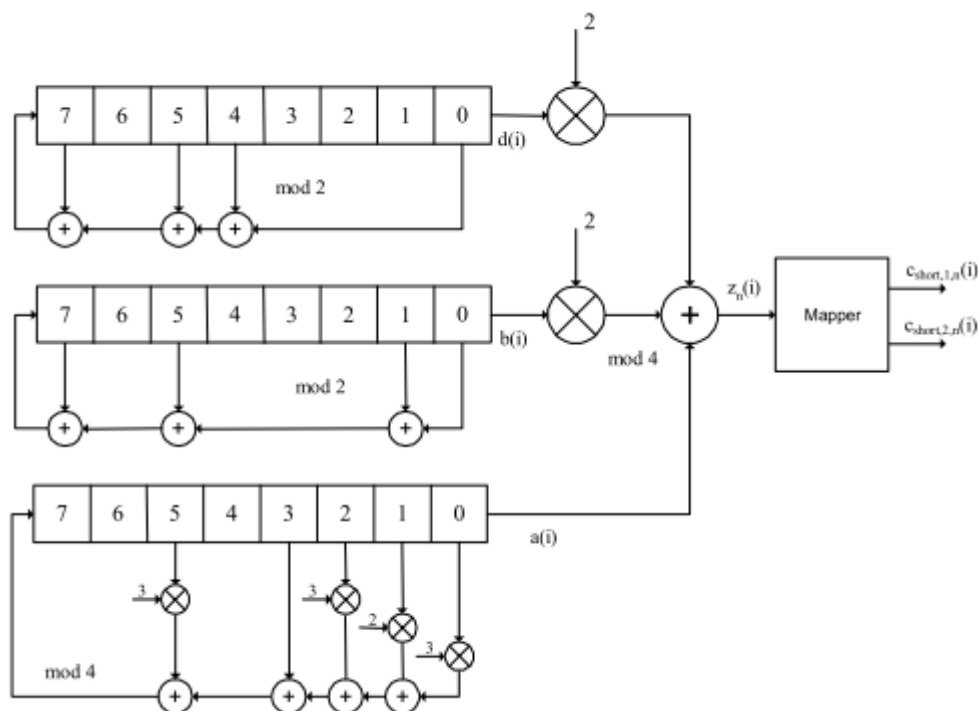
Figure 7.5: Scrambling sequence generator

7.2   Modulation and Pulse Shaping

The complex-valued chip sequence S generated by the spreading process (described in clause 7.1) is QPSK modulated as shown in Figure 7.6. For the PDRACH and PCRACH the preamble generated according to clause 5.1.3 shall be added.
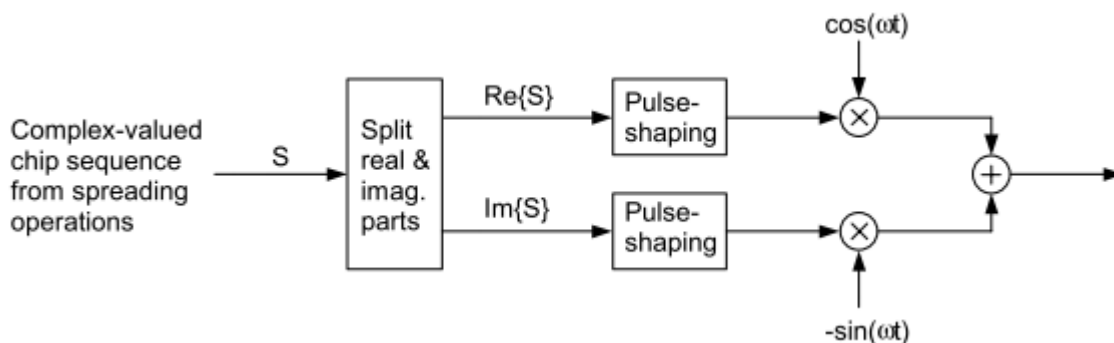
Figure 7.6: Modulation and pulse shaping

Pulse shaping is performed through square root raised cosine filters with roll-off $\alpha=0,22$ as shown in the figure.

The impulse response of the pulse shaping is thus equal to

$$p(t) = \frac{\sin\left(\pi\frac{t}{T_c}(1-\alpha)\right) + 4\alpha\frac{t}{T_c}\cos\left(\pi\frac{t}{T_c}(1+\alpha)\right)}{\pi\frac{t}{T_c}\left(1-\left(4\alpha\frac{t}{T_c}\right)^2\right)}$$

where Tc is the chip period.

8   Radio Transmission

8.1   Frequency bands and channel arrangement

The following channelisations shall be supported by the terminals:

- 5 MHz bandwidth channels (baseline);

- 625 kHz bandwidth channels;

- 312,5 kHz bandwidth channels.

Terminals shall be able to use any radio frequency channel available in the return link frequency band:
1 980 MHz to 2 010 MHz.

8.2   Stability and accuracy requirements

Stability and accuracy are partially dependent on synchronisation as described in clause 9.

8.2.1   Frequency and symbol timing stability and accuracy

The RMS carrier frequency error (measured at the satellite receiver input) for all QS-CDMA carriers shall be better than 5 Hz.

   NOTE: QS-CDMA carriers are used for dedicated physical channels (not the RACH).

The RMS chip frequency error (measured at the satellite receiver input) for all QS-CDMA carriers shall be better than 0,01 chip/s.

Terminals shall be able to apply carrier and chip frequency corrections with accuracy better than or equal to 1 Hz and $1/16 = 0,0625$ chip/s, respectively.

8.2.2   Time alignment accuracy

Terminals shall be able to apply time alignment corrections with accuracy better than or equal to $1/16 = 0,0625$ chips.

8.2.3   Power stability and accuracy

Terminals shall be able to apply power corrections with accuracy better than or equal to 0,2 dB.

8.3   Transmitter characteristics

8.3.1   Power output characteristics and power class

   NOTE: Typical EIRP values and power classes are defined in Part 1 [5].

8.3.2   Transmit polarization

Polarization in the return services may be either left-hand circular (LHCP) or right-hand circular (RHCP) fixed polarization.

8.3.3   Unwanted Emissions

ETSI MSS standards ([1] for wideband and [2] for narrowband systems) provide extensive regulation for the unwanted emissions. Since each document applies for different bandwidths, the requirements that would apply for each channelisation would be:

- 5 MHz (baseline): wideband systems requirements.

- 625 and 312,5 kHz: narrowband systems requirements.

Here is a summary of the requirements for the transmitters unwanted emissions defined in EN 302 574-2 [1] and EN 302 574-2 [2]:

Table 8.1: ETSI MSS unwanted emissions requirements

Wideband	Narrowband
Spectrum emission mask Adjacent Channel Leakage Power Ratio Transmitter spurious emissions Maximum output power Minimum output power	Unwanted emissions outside the band 1 980 MHz to 2 010 MHz (carrier on state) Unwanted emissions within the band 1 980 MHz to 2 010 MHz (carrier on state) Unwanted emissions in carrier off state UE Control and Monitoring Functions (CMF)

The detailed formulation of these requirements can be found in EN 302 574-2 [1] and EN 302 574-2 [2], along with the testing procedures associated to each requirement.

8.4   Power Control

The following power-control parameters need to be broadcast by the Hub periodically to all terminals in the system (statically configured unless otherwise noted):

- Expected FWD link SNIR for a terminal located at the edge of coverage with the worst case G/T in clear sky conditions: $SNIR_{total,FWD}^{\exp ected}(dB)$.

- RACH reference EIRP: $EIRP_{ref,SSA}$.

- RACH ΔEIRP: $\Delta EIRP_{SSA}$ *[dynamic.]*

- ULB retransmission parameters.

- Estimated difference between the pattern advantages of the satellite transmitter and receiver antenna over the coverage area (PA_{bias}).

- This parameter is only used by terminals without the knowledge of their position.

- Small (Δ_1) and large (Δ_2) closed-loop power control steps.

The static information is broadcast within the QSCT whereas dynamic information is distributed through the QSDT. These tables are defined in [6].

The selected power control policy maximises the power balance at the satellite level and adjusts the transmitted power to the minimum required to comply with PER requirements. The proposed power control mechanism consists of two main procedures:

- Open-loop power control: open loop estimation of the channel characteristics for the first terminal transmission (RACH).

- Closed-loop power control: subsequent periodic closed-loop adjustments of the terminal transmitter power by the Hub (DCH).

Figure 8.1 shows an overview of the power control mechanisms at the Hub and terminal sides. The power control mechanisms on the terminal side are described in the following clauses.
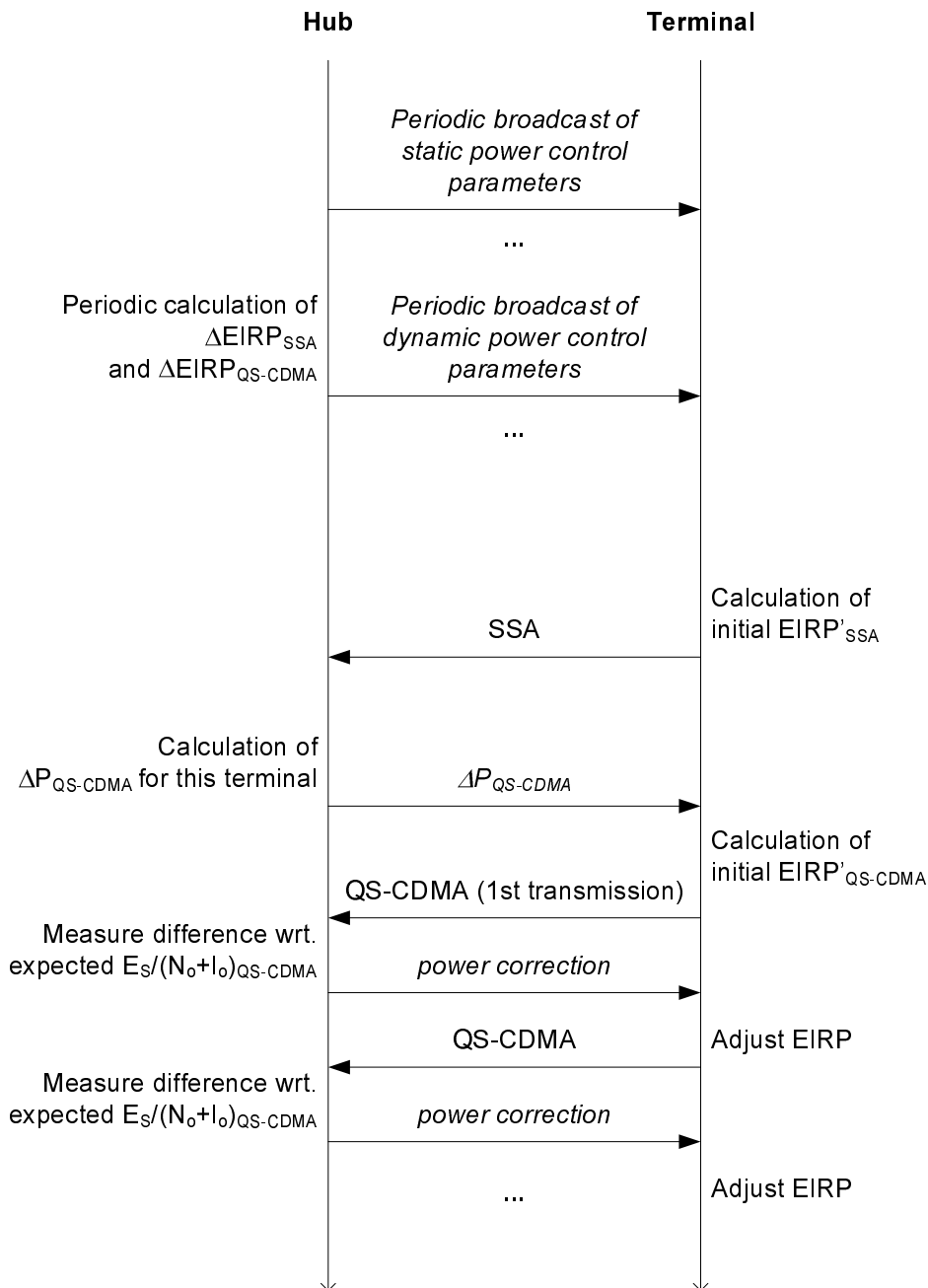
Hub   **Terminal**

Periodic broadcast of static power control parameters

...

Periodic calculation of $\Delta EIRP_{SSA}$ and $\Delta EIRP_{QS\text{-}CDMA}$

Periodic broadcast of dynamic power control parameters

...

Calculation of initial EIRP'$_{SSA}$

SSA

Calculation of $\Delta P_{QS\text{-}CDMA}$ for this terminal

$\Delta P_{QS\text{-}CDMA}$

Calculation of initial EIRP'$_{QS\text{-}CDMA}$

QS-CDMA (1st transmission)

Measure difference wrt. expected $E_S/(N_o+I_o)_{QS\text{-}CDMA}$

power correction

QS-CDMA   Adjust EIRP

Measure difference wrt. expected $E_S/(N_o+I_o)_{QS\text{-}CDMA}$

power correction

...   Adjust EIRP

Figure 8.1: Overview of power control mechanisms

8.4.1   Open-loop Power Control for RACH

The terminal estimates the *combined terminal loss*, L_{comb}, defined as the difference between the fading loss and the satellite transmission Pattern Advantage at its location. The calculation of the combined terminal loss is based on FWD link measurements, and is used to calculate the ULB power. The procedure is as follows:

1)   Measure the received forward link SNIR: $SNIR_{total,FWD}^{measured}\left(dB\right)$.

2)   Assuming that the overall forward link budget is governed by the user link, the combined terminal loss is calculated as:

$$L_{comb}\left(dB\right) = SNIR_{total,FWD}^{expected}\left(dB\right) - SNIR_{total,FWD}^{measured}\left(dB\right).$$

It must be noticed that $SNIR_{total,FWD}^{\exp ected}(dB)$ has been computed by the Hub for the worst-case terminal G/T. If the actual terminal G/T is different, the difference must be taken into account in the previous calculation.

3)   TheULB power level is calculated as follows:

$$EIRP_{SSA}^{'} = EIRP_{ref,SSA} + \Delta EIRP_{SSA} + L_{comb} + PA_{bias}$$

where PA_{bias} is the difference between PAtx and PArx (i.e. transmission and reception pattern advantage) and can be either known (if the terminal location is known) or replaced by an approximation (broadcast by the Hub). The transmitted ULB power is calculated based on this EIRP and the antenna and RF chain gains.

4)   If the ULB is not detected by the hub, the terminal will attempt retransmissions up to *N* times.

8.4.2   Closed-loop Power Control for RACH

In order to adjust the terminal transmitter power for the initial DCH transmission, the Hub sends the terminal a correction based on the received ULB $E_s/(N_0+I_0)$. The procedure is as follows:

1)   Upon receipt of an ULB with a Channel Request, the hub send an initial power correction $\Delta P_{QS-CDMA}$.

2)   The initial DCH carrier EIRP transmitted by the terminal is calculated as:

$$EIRP_{QS-CDMA}^{'} = EIRP_{SSA}^{'} + \Delta P_{QS-CDMA} + 10 \cdot \log 10 \left(SF_{\max} / SF_{QS-CDMA} \right).$$

where $SF_{QS-CDMA}$ is the spreading factor of the QS-CDMA carrier and SF_{max} the maximum spreading factor supported by the system.

3)   After this first transmission, the power transmitted by the terminal is adjusted remotely by the Hub through periodic corrections as illustrated in Figure 8.1.

9   Synchronisation

9.1   General description of synchronisation system

The S-MIM synchronous access is a connection-oriented system where all QS-CDMA carriers must be quasi-synchronous in time and frequency. Synchronisation involves two major tasks:

- Timing (chip phase and frequency) synchronisation.

- Carrier frequency synchronisation.

The RACH provides the ability for a terminal not only to log-on to the network or request capacity for a new connection, but also for it to pre-synchronise its transmitter before initiating QS-CDMA carrier transmission.

A closed-loop between the Hub and the terminals ensures proper synchronisation of QS-CDMA carriers when an end-to-end link is established.

9.2   Terminal requirements

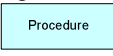The following terminals requirements shall be fulfilled:

- Terminals shall use the same reference clock for the RF up-converter and base-band modulator.

- The FWD link receiver tuner and base-band modules shall use the same reference clock as above.

- Terminals shall never transmit if they are not locked to the satellite FWD link signal.

- Terminals transmitter shall comply with the stability and accuracy requirements defined in clause 8.2.

- RACH bursts transmission shall comply with the following requirements:

  - Chip frequency errors at the Hub lower than ±3 chip/s.

  - Carrier frequency errors at the Hub lower than ±3 kHz.

  - Received E_b/N_t at the Hub above the target one. It must be noticed that specific information is broadcast by the system within the QSCT and QSDT tables in TS 102 721-6 [6] to allow terminals to calculate the required transmitted power level.

- During DCH transmission, terminals shall apply synchronisation (carrier frequency and chip phase and frequency) and power corrections computed by the Hub and distributed through the satellite FWD link within QSCM messages and QSPCT tables in TS 102 721-6 [6].
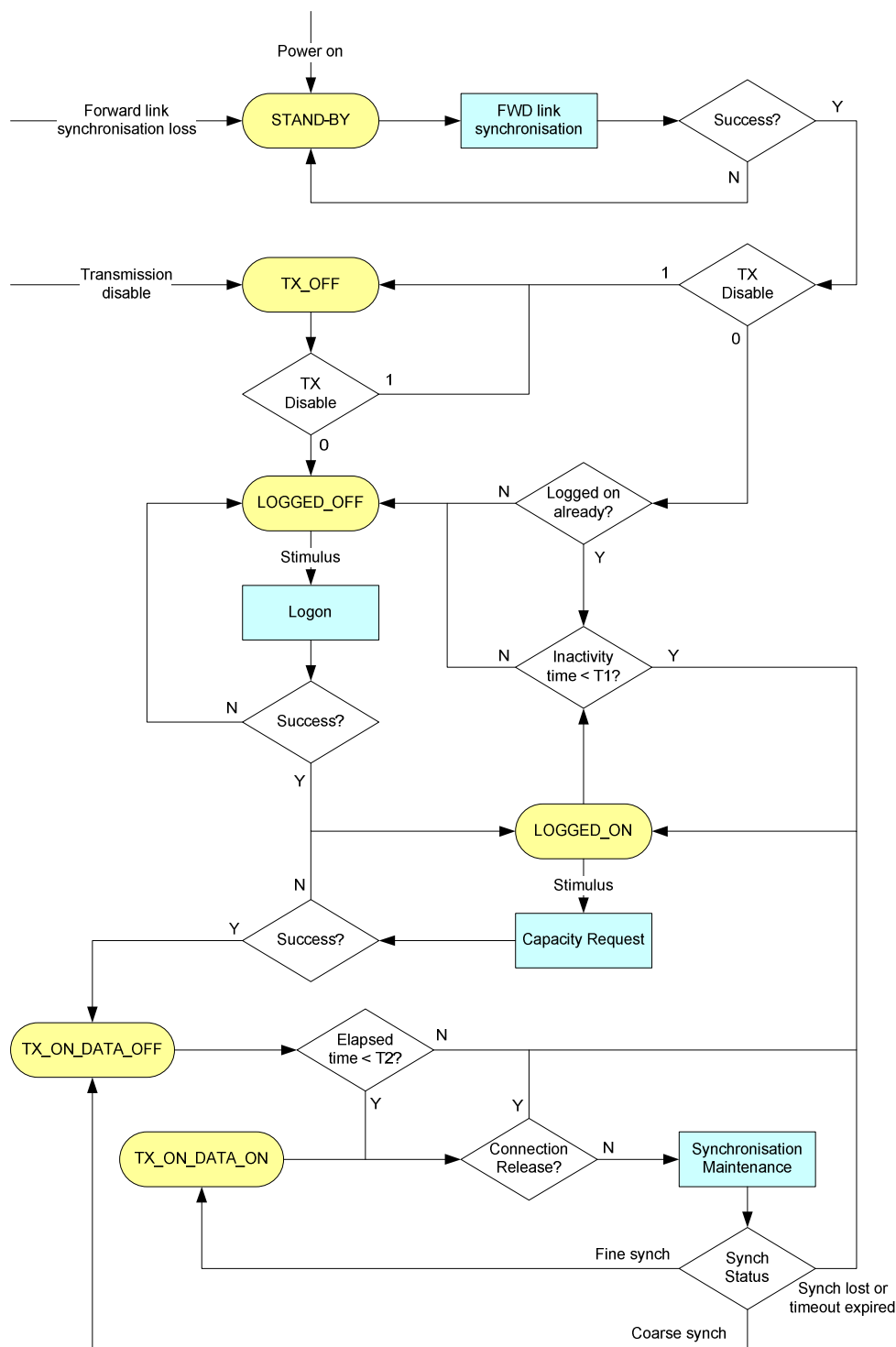
9.3 Synchronisation procedures

This clause defines the procedures to allow a terminal to logon on and initiate a data transmission.

9.3.1 Overall events sequencing

Terminal synchronisation states are defined in Table 9.1 and the terminal state flow diagram is shown in Figure 9-1, giving an overview of the overall events sequencing. In the figure, STATE represents terminal states, Procedure represents procedures.

Table 9.1: Terminal synchronisation states definition

Terminal state	Description	Transmission capabilities
STAND-BY	The terminal automatically starts the FWD link synchronisation procedure.	Transmission is not allowed.
LOGGED_OFF	The terminal is receiving the FWD link signal and has all the information required to access the QS-CDMA sub-system but must be logged on to the system for operation.	Transmission of RACH burst is allowed. Transmission of QS-CDMA carriers is not allowed.
LOGGED_ON	Terminal is logged on to the network but is not allowed to transmit a QS-CDMA carrier yet. It is allowed to request capacity though.	Transmission of RACH burst is allowed. Transmission of QS-CDMA carriers is not allowed.
TX_ON_DATA_OFF	The terminal transmits a QS-CDMA carrier without valid data in it (the terminal is not allowed to send signalling / traffic data). Note: In this state, the terminal transmission is aimed at allowing the Hub to properly estimate the synchronisation errors and check them against the corresponding synchronisation requirements.	Transmission of RACH burst is not allowed. Transmission of QS-CDMA carriers is done.
TX_ON_DATA_ON	The terminal transmits a QS-CDMA carrier with signalling / traffic data.	Transmission of RACH burst is not allowed. Transmission of QS-CDMA carriers is done.
TX_OFF	While in TX_OFF state, the terminal is not allowed to transmit. The terminal cannot access to the QS-CDMA sub-system until it is allowed to do so by the Hub. Note: A terminal that is in TX_OFF state will remain in this state after a power off or reset.	Transmission is not allowed.

Figure 9.1: Terminal synchronisation state diagram

9.3.2   FWD link synchronisation procedure

Following the power-up, the terminal shall proceed as detailed below:

- The terminal shall first synchronise the satellite FWD link carrier and extract the FWD link data.

- Control information (System tables) related to the operation of the S-MIM synchronous access shall be extracted and processed.

- FWD link carrier and timing frequency offsets and SNIR shall be continuously estimated.

If the previous procedure fails, the terminal shall remain in STAND-BY state and repeat the procedure again.

Previous steps must be done while the terminal is on. Upon a FWD link synchronisation loss event, the terminal shall go back to STAND-BY state and the previous procedure shall be initiated again.

A FWD link synchronisation loss event occurs when the satellite FWD link synchronisation is lost for a period of time longer than *FLSL_timeout*, where *FLSL_timeout* is a parameter broadcast by the Hub within the QSCT table.

9.3.3   Logon procedure

After the terminal has received all System tables related to the S-MIM synchronous access, it is ready to initiate a logon, in order to be admitted to the S-MIM synchronous access and be ready to request capacity to handle traffic.

The terminal shall proceed as follows:

- The terminal shall transmit a logon request by means of a RACH burst. In the absence of reply from the Hub in *LR_timeout* seconds, the terminal shall assume that the request is lost and the terminal shall retry after a randomly selected time interval between 0 and *LR_max_time_before_retry*. Up to *LR_max_retries* tries are allowed. *LR_timeout*, *LR_max_time_before_retry* and *LR_max_retries* are parameters distributed within the QSCT table. Terminals must comply with the RACH bursts synchronisation requirements defined in clause 9.2 in order to allow the proper RACH burst detection, demodulation and decoding at the Hub.

- The Hub receives the terminal logon request and checks if the administrative aspects are satisfied.

- The Hub shall send a specific message (confirming or denying the logon request) to the terminal through the satellite FWD link.

Upon success of the logon procedure, the terminal is ready to request capacity and shall go to LOGGED_ON state. If the logon procedure fails, the terminal shall remain in LOGGED_OFF state.

If the terminal is inactive (no transmission is done) for a period of time longer than *T1* (*T1* being determined by the Hub and sent to the terminal in the logon confirmation), the terminal shall go back to LOGGED_OFF state and the logon procedure must be repeated before requesting capacity.
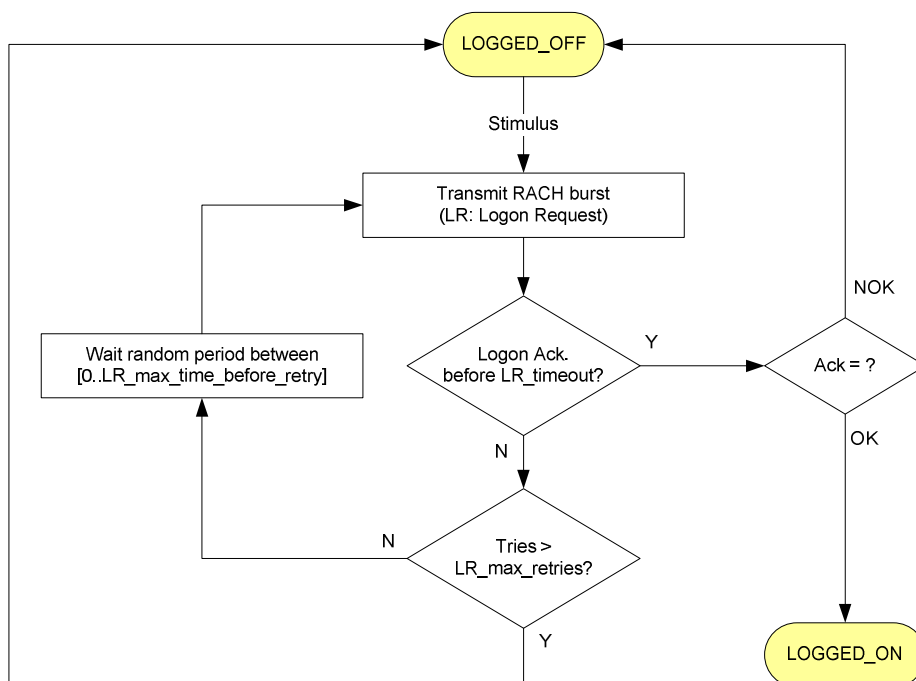

Figure 9.2: Logon procedure

9.3.4 Capacity request procedure

Once in LOGGED_ON state, the terminal is allowed to request capacity.

The capacity request procedure is either triggered by higher layers of the terminal or by the Hub, e.g. upon notification of an incoming call.

The terminal shall proceed as detailed below:

- The terminal shall transmit a capacity request by means of a RACH burst. In the absence of reply from the Hub in *CAR_timeout* seconds, the terminal shall assume that the request is lost and the terminal shall retry after a randomly selected time interval between 0 and *CAR_max_time_before_retry*. Up to *CAR_max_retries* tries are allowed. *CAR_timeout*, *CAR_max_time_before_retry* and *CAR_max_retries* are parameters distributed within the QSCT table.

- The Hub receives the terminal capacity request and checks if the administrative aspects are satisfied. RACH bursts synchronisation errors (carrier frequency and chip phase and frequency) and $E_s/(N_0+I_0)$.are also estimated by the Hub.

- The Hub shall send a specific message (confirming or denying the capacity request) to the terminal through the satellite FWD link. If capacity is allocated to the terminal, along with the resources parameters, the Hub shall send synchronisation (carrier frequency and chip phase and frequency) and power corrections to the terminal.

- The terminal shall apply the received synchronisation and power corrections.

Upon success of the capacity request procedure, the terminal shall go to the TX_ON_DATA_OFF state and start immediately the transmission of a QS-CDMA carrier with the resources allocated. If the capacity request procedure fails, the terminal shall remain in the LOGGED_ON state.

The parameter *T2* (see clause 9.3.5) is computed by the Hub and sent to the terminal in the capacity allocation confirmation.
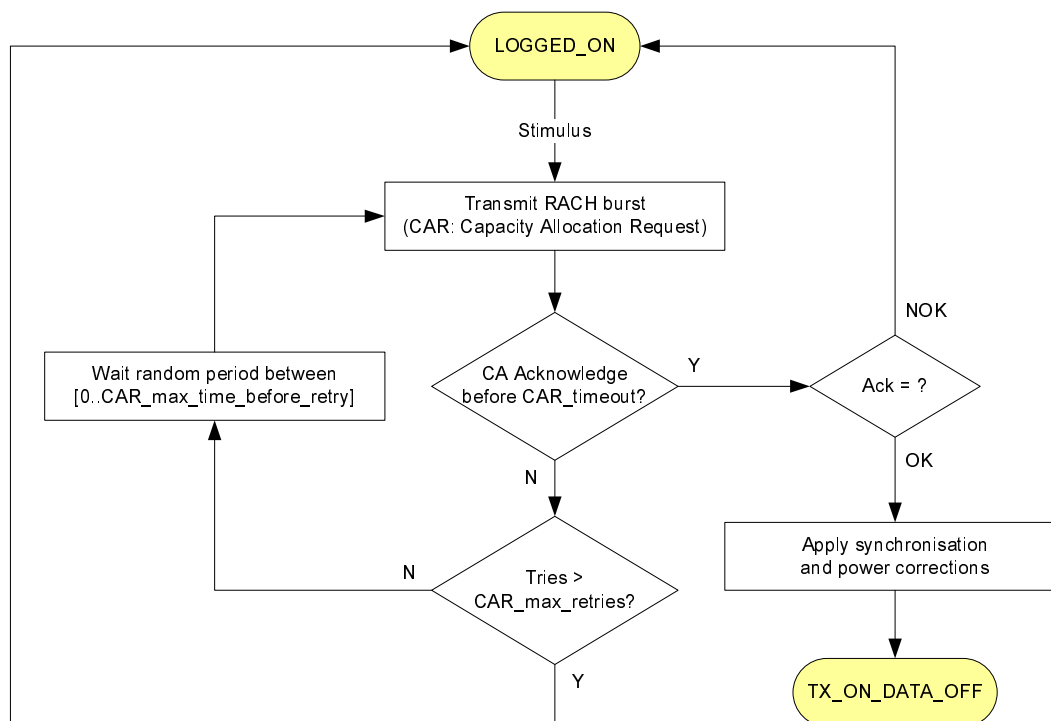

Figure 9.3: Capacity request procedure

9.3.5   Synchronisation maintenance procedure

While the terminal is in TX_ON_DATA_OFF or TX_ON_DATA_ON states, the terminal shall transmit a QS-CDMA carrier and execute the synchronisation maintenance procedure, which is detailed below:

- The Hub continuously estimates synchronisation errors and $E_s/(N_0+I_0)$.and sends synchronisation (carrier frequency and chip phase and frequency) and power corrections to the terminal.

- The terminal shall apply all synchronisation and power corrections sent by the Hub through the satellite FWD link.

- Two different levels of synchronisation requirements (referred as coarse and fine requirements) are used by the Hub to determine the terminal synchronisation status throughout a connection.

If the Hub detects that coarse synchronisation requirements are not met or the QS-CDMA signal is lost, it signals the terminal to stop transmitting and go back to LOGGED_ON state. Otherwise, the Hub checks if fine synchronisation requirements are met. If they are not, the terminal remains in / goes to TX_ON_DATA_OFF state. If fine synchronisation requirements are met, the terminal remains in / goes to TX_ON_DATA_ON state.

The Hub is in charge of signalling the previous terminal states transitions through the synchronisation status (*Synch Status* = {*Fine synch, Coarse synch, Synch lost*}), which is sent to the terminals along with the synchronisation and power corrections within QSCM messages.

- If no synchronisation and/or power corrections are received in a period of time longer than *max_time_without_corrections*, the terminal shall go to the LOGGED_ON state. The previous timeout is broadcast by the Hub within the QSCT table.

- If the terminal is in TX_ON_DATA_OFF state for a period of time longer than *T2*, the Hub shall signal the terminal to go to LOGGED_ON state.

Upon a FWD link synchronisation loss event, the terminal shall stop transmitting, release the resources assigned for the connection, go back to STAND-BY state and initiate the FWD link synchronisation procedure again.

Upon a connection release, initiated either by the terminal or the Hub, the terminal shall go to LOGGED_ON state.

9.3.6   Logoff procedure

Although it has not been represented in Figure 9.1 in order to make the diagram clearer, a logoff procedure is conceived. This procedure can be initiated by the Hub or by the terminal.

When initiated by the Hub, the procedure goes as follows:

- The procedure can be initiated anytime by the Hub. In this case, the Hub shall send a specific message to the terminal through the satellite FWD link. Upon reception of such message, the terminal shall go to the LOGGED_OFF state.

The logoff procedure, when initiated by the terminal, is detailed below:

- The terminal shall transmit a logoff request by means of a RACH burst. In the absence of reply from the Hub, the terminal shall go to the LOGGED_OFF state anyway.

- When the Hub receives the terminal logoff request, it sends a confirmation to the terminal through the satellite FWD link.

- Upon reception of the previous confirmation, the terminal shall go to the LOGGED_OFF state.

9.3.7   Transmission disable

The Hub can disable a terminal transmission by setting the *Transmission disable* flag to 1. The *Transmission disable* flag is a parameter sent to the terminal through the satellite FWD link. Along with the *Transmission disable* notification, a timeout *TD_timeout* is sent.

Upon reception of a *Transmission disable* = 1, the terminal shall go to TX_OFF state and remain in this state until transmission is enabled again (reception of a *Transmission disable* = 0) or the timeout expires. In both cases the terminal shall go to LOGGED_OFF state.

10   Physical layer measurements

Radio characteristics are measured and reported to higher layers and the network. Such measurements are for further study.

History

Document history		
V1.1.1	December 2011	Publication