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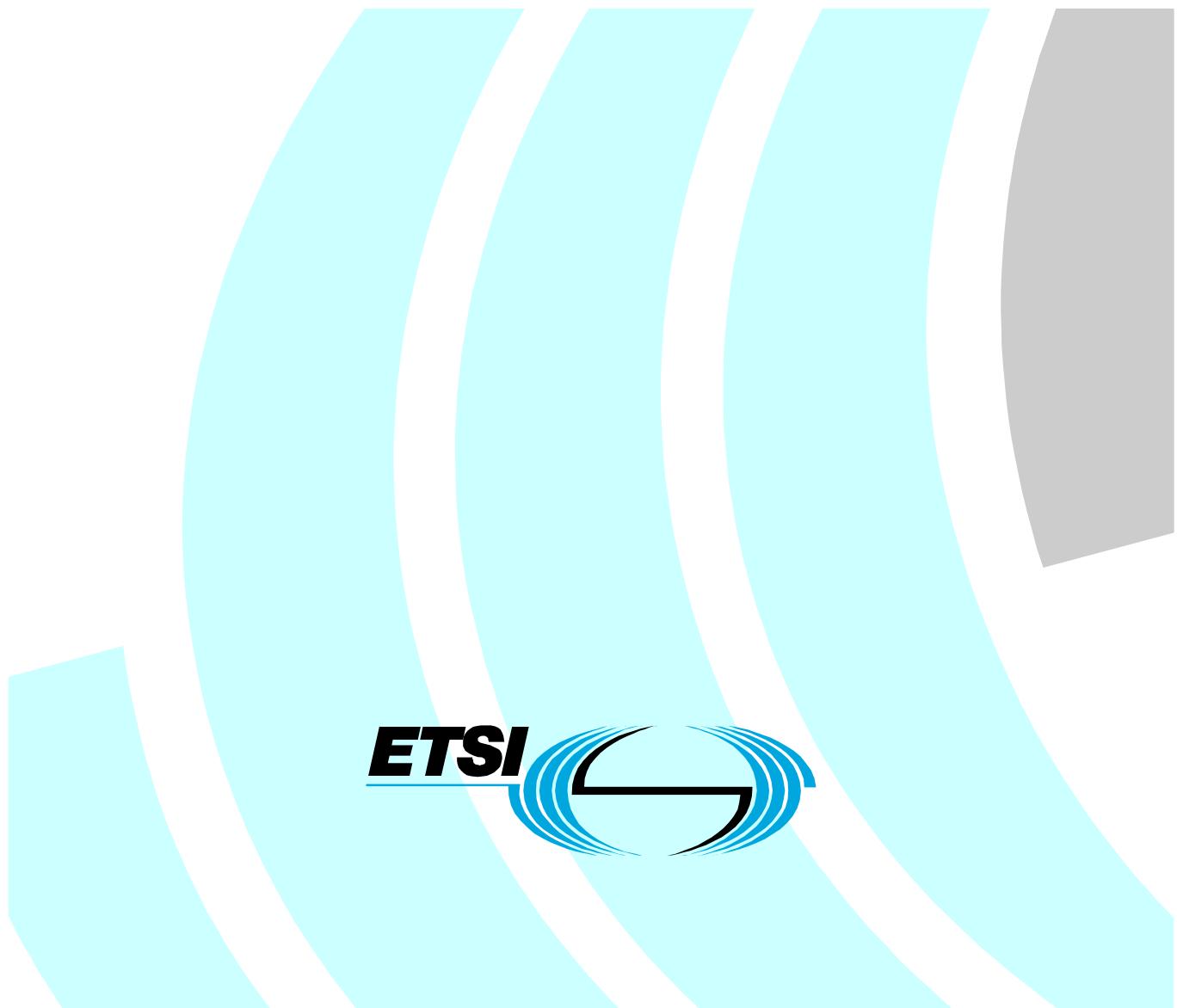
Technical Specification

**Terrestrial Trunked Radio (TETRA);
Voice plus Data (V+D);
Part 3: Interworking at the Inter-System Interface (ISI);
Sub-part 6: Speech format implementation for
circuit mode transmission**

ETSI

Reference

DTS/TETRA-03106

Keywords

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Foreword

This Technical Specification (TS) has been produced by ETSI Project Terrestrial Trunked Radio (TETRA).

The present document is part 3, sub-part 6 of a multi-part deliverable covering Voice plus Data (V+D), as identified below:

EN 300 392-1: "General network design";

EN 300 392-2: "Air Interface (AI)";

EN 300 392-3: "Interworking at the Inter-System Interface (ISI)";

> EN 300 392-3-1: "General design";
>
> EN 300 392-3-2: "Additional Network Feature Individual Call (ANF-ISIIC)";
>
> EN 300 392-3-3: "Additional Network Feature Group Call (ANF-ISIGC)";
>
> EN 300 392-3-4: "Additional Network Feature Short Data Service (ANF-ISISDS)";
>
> EN 300 392-3-5: "Additional Network Feature for Mobility Management (ANF-ISIMM)";
>
> **TS 100 392-3-6: "Speech format implementation for circuit mode transmission";**
>
> TS 100 392-3-7: "Speech Format Implementation for Packet Mode Transmission";

ETS 300 392-4: "Gateways basic operation";

EN 300 392-5: "Peripheral Equipment Interface (PEI)";

EN 300 392-7: "Security";

EN 300 392-9: "General requirements for supplementary services";

EN 300 392-10: "Supplementary services stage 1";

EN 300 392-11: "Supplementary services stage 2";

EN 300 392-12: "Supplementary services stage 3";

ETS 300 392-13: "SDL model of the Air Interface (AI)";

ETS 300 392-14: "Protocol Implementation Conformance Statement (PICS) proforma specification".

TS 100 392-15: "TETRA frequency bands, duplex spacings and channel numbering";

TS 100 392-16: "Network Performance Metrics";

TS 100 392-17: "TETRA V+D and DMO Release 1.1 specifications".

Introduction

There are two different speech format options defined for the TETRA InterSystem Interface (ISI) speech transmission one for circuit mode support and another for packet mode support.

The two options allow different techniques in designing and interconnecting TETRA SwMIs. Those based on packet mode transmission technology can use the complementary packet based option, and those based on circuit mode transmission technology can take advantage of the present subpart of the ISI.

The reason for having two options shall be found in the nature of existing TETRA SwMIs from various manufacturers. The existing SwMIs can generally be divided into two types: those that use packet switched technology and those which are using a circuit switched technology.

When connecting a circuit switched SwMI to a packet switched SwMI there must be a conversion performed from one technology to the other.

When a circuit switched and a packet switched SwMI is connected, a TETRA ISI Transport Converter (ISI-TC) is required. The ISI-TC does not necessarily need to be provided by the SwMI manufactures.

The location of the ISI-TC will be dependent on the backbone network that is used to interconnect the two systems. If a packet switched backbone is available, then the location of the ISI-TC is best in the circuit switched SwMI end. If a circuit switched backbone is available, then the location of the ISI-TC is best at the packet SwMI.

1 Scope

The present document specifies Speech Format Implementation for Circuit Mode Transmission in TETRA InterSystem Interface (ISI).

The present document defines the format of user information that is transported between two SwMIs using the TETRA ISI and supporting circuit mode speech transmission for ISI connections. It is complementary to the subpart of the ISI specification describing a packet mode approach.

The present document covers how speech frames are coded/decoded within digital circuit mode connection (2Mbit/s; G.703/G.704). That is the primary transport layer between those network elements within both SwMIs, which need to transfer/manipulate speech circuits.

The present document provides two options for speech transport called First Speech Transport Encoding format and Optimized Speech Transport Encoding format.

The present document does not cover any signalling issues (e.g. how speech circuits are reserved on the ISI interface, how call set-up is done).

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication and/or edition number or version number) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

[1] ETSI ETS 300 395-2: "Terrestrial Trunked Radio (TETRA); Speech codec for full-rate traffic channel; Part 2: TETRA codec".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

C-stolen sub block: sub block stolen from speech or circuit mode data by a signalling message

Mobile Station (MS): physical grouping that contains all of the mobile equipment that is used to obtain TETRA services

NOTE: By definition, a mobile station contains at least one Mobile Radio Stack (MRS).

U-stolen sub block: sub block stolen from speech or circuit mode data by a user application and intended for user to user signalling

3.2   Abbreviations

For the purposes of the present document, the following abbreviations apply:

ACELP   Algebraic CELP
BFI   Bad Frame Indicator
FEC   Forward Error Correction
FN   Frame Number
FSTE   First Speech Transport Encoding format
ISI   Inter-System Interface
MRS   Mobile Radio Stack
MS   Mobile Station
OSTE   Optimized Speech Transport Encoding format
STE   Speech Transport Encoding format
SwMI   Switching and Management Infrastructure

4   Overview of FSTE

4.1   Mapping structure of FSTE

TETRA voice codec encoded audio (speech) is mapped into First Speech Transport Encoding format (FSTE) used for voice signal transmission between SwMIs, see figure 1. The TETRA speech encoding is defined in ETS 300 395-2 [1] and the G.704 framing is defined in ITU-T Recommendation G.704.
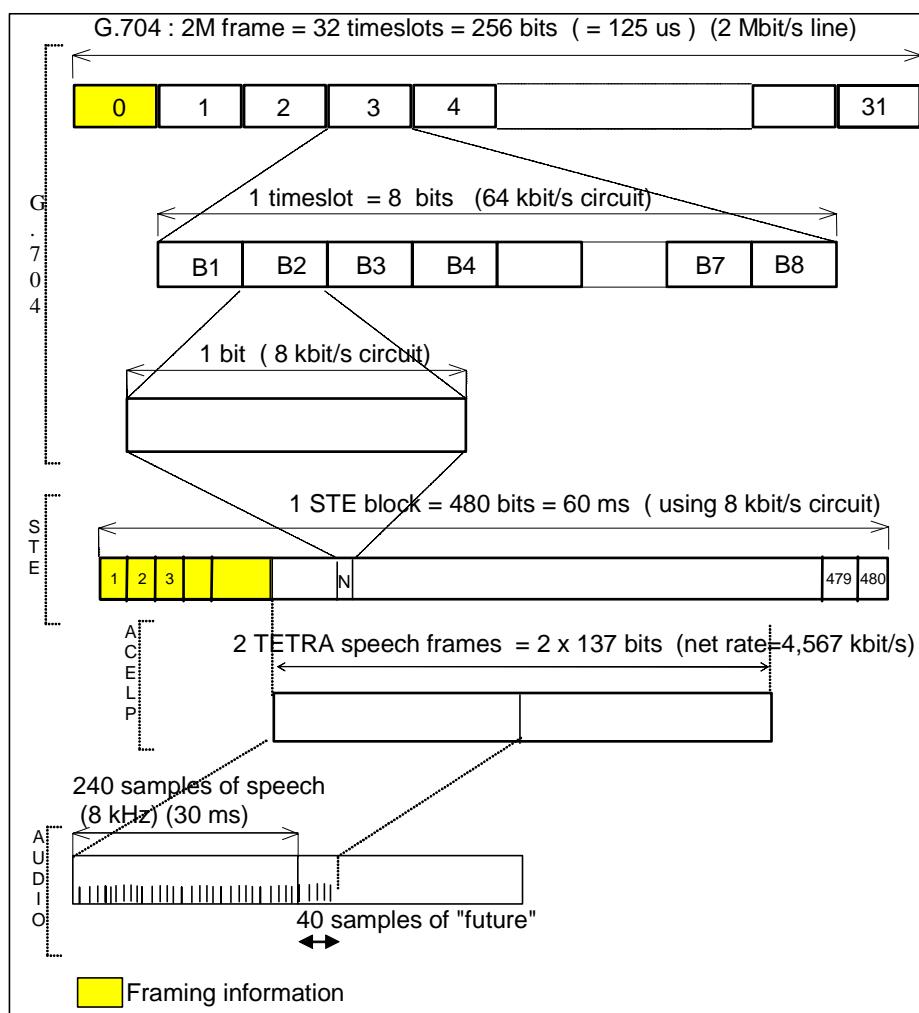
Figure 1: Mapping structure for FSTE

4.2   FSTE block layer

The TETRA speech frames are mapped to FSTE block format within 8 kbit/s circuit. Detailed specification of FSTE format is given on clause 5.

Also an optimized block format can be used, which reduces the need for buffering due to 18th frame gap. The optimized block format is presented in clauses 6 and 7 of the present document.

4.3   TETRA ACELP

Audio signal is coded with TETRA ACELP coding. The TETRA ACELP coding is a TETRA speech coding standard ETS 300 395-2 [1]. TETRA ACELP coding produces 137 coding bits from 30 ms length of audio speech frame, which consists of 240 speech audio samples taken with 8 kHz rate.

5   Block format and procedures for FSTE

5.1   General requirements for FSTE

FSTE is the STE block format that shall be used to carry TETRA ACELP coded speech frames within 8 kbit/s circuits over the TETRA ISI fulfilling requirements of the present document.

Each STE block shall incorporate block synchronization (clause 5.3), control bits (clause 5.5), data bits (=speech) and eventually spare bits (clause 5.6). The details of the FSTE block format are described in clause 5.2.

The STE blocks shall be transmitted as soon as available at 8 kbit/s on the physical link.

Receiver process shall use block synchronization as defined in clause 5.3.

Handling of block errors is described on clause 5.4.

5.2   FSTE block format

The FSTE block shall be encoded as presented in table 1. The bits of the block shall be sent over 8 kbit/s channel in octet order so that the octet "0" and its bit number "1" is sent first.

The meaning of different bits in the block is:

   C = control bits (see clause 5.5)

   D = data bits (i.e. TETRA ACELP coded speech bits)

   S = spare bits

   SYNC_1 = synchronization bits with value "1".

The FSTE block shall contain two sub-blocks as defined in clause 4.1.

Table 1: FSTE block format

Octet Nº	1	2	3	4	5	6	7	8
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	1	C1	C2	C3	C4	C5	D1	D2
5	D3	D4	D5	D6	D7	D8	D9	D10
6	D11	D12	D13	D14	D15	D16	D17	D18
7	SYNC_1	D19	D20	D21	D22	D23	D24	D25
8	D26	D27	D28	D29	D30	D31	D32	D33
9	D34	D35	D36	D37	D38	D39	D40	D41
10	SYNC_1	D42	D43	D44	D45	D46	D47	D48
11	D49	D50	D51	D52	D53	D54	D55	D56
12	D57	D58	D59	D60	D61	D62	D63	D64
13	SYNC_1	D65	D66	D67	D68	D69	D70	D71
14	D72	D73	D74	D75	D76	D77	D78	D79
15	D80	D81	D82	D83	D84	D85	D86	D87
16	SYNC_1	D88	D89	D90	D91	D92	D93	D94
17	D95	D96	D97	D98	D99	D100	D101	D102
18	D103	D104	D105	D106	D107	D108	D109	D110
19	SYNC_1	D111	D112	D113	D114	D115	D116	D117
20	D118	D119	D120	D121	D122	D123	D124	D125
21	D126	D127	D128	D129	D130	D131	D132	D133
22	SYNC_1	D134	D135	D136	D137	S1	S2	S3
23	S4	S5	S6	S7	S8	S9	S10	S11
24	S12	S13	S14	S15	S16	S17	S18	S19
25	SYNC_1	S20	S21	S22	S23	S24	S25	S26
26	S27	S28	S29	S30	S31	S32	S33	S34
27	S35	S36	S37	S38	S39	S40	S41	S42
28	SYNC_1	S43	S44	S45	S46	S47	S48	S49
29	S50	S51	S52	S53	S54	S55	S56	S57
30	S58	S59	S60	S61	S62	S63	S64	S65
31	SYNC_1	S66	S67	S68	S69	S70	S71	S72
32	S73	S74	S75	S76	S77	S78	S79	D1
33	D2	D3	D4	D5	D6	D7	D8	D9
34	SYNC_1	D10	D11	D12	D13	D14	D15	D16
35	D17	D18	D19	D20	D21	D22	D23	D24
36	D25	D26	D27	D28	D29	D30	D31	D32
37	SYNC_1	D33	D34	D35	D36	D37	D38	D39
38	D40	D41	D42	D43	D44	D45	D46	D47
39	D48	D49	D50	D51	D52	D53	D54	D55
40	SYNC_1	D56	D57	D58	D59	D60	D61	D62
41	D63	D64	D65	D66	D67	D68	D69	D70
42	D71	D72	D73	D74	D75	D76	D77	D78
43	SYNC_1	D79	D80	D81	D82	D83	D84	D85
44	D86	D87	D88	D89	D90	D91	D92	D93
45	D94	D95	D96	D97	D98	D99	D100	D101
46	SYNC_1	D102	D103	D104	D105	D106	D107	D108
47	D109	D110	D111	D112	D113	D114	D115	D116
48	D117	D118	D119	D120	D121	D122	D123	D124
49	SYNC_1	D125	D126	D127	D128	D129	D130	D131
50	D132	D133	D134	D135	D136	D137	S1	S2
51	S3	S4	S5	S6	S7	S8	S9	S10
52	SYNC_1	S11	S12	S13	S14	S15	S16	S17
53	S18	S19	S20	S21	S22	S23	S24	S25
54	S26	S27	S28	S29	S30	S31	S32	S33

Octet Nº	1	2	3	4	5	6	7	8
55	SYNC_1	S34	S35	S36	S37	S38	S39	S40
56	S41	S42	S43	S44	S45	S46	S47	S48
57	S49	S50	S51	S52	S53	S54	S55	S56
58	SYNC_1	S57	S58	S59	S60	S61	S62	S63
59	S64	S65	S66	S67	S68	S69	S70	S71
60	S72	S73	S74	S75	S76	S77	S78	S79

5.3   Block synchronization

During idle mode, when there is not any active call within that 8 kbit/s circuit, no block synchronization is done and the 8 kbit/s circuit shall be filled with all ones ("1").

The searching of block synchronization shall be started, when a new call request is accepted by the SwMI. The block synchronization (alignment) shall be acquired by searching the first instance of 24 contiguous "0"-bits followed by one "1"-bit in the 8 kbit/s circuit, see figure 2.

After a synchronization the block synchronization signal shall be continuously checked with the presumed block start position for the alignment.

If the block synchronization signal (during a call) is not found (e.g. due to transmission errors or due to PCM synchronization problem due to plesiochronous situation on transport network) from the presumed block start position (ones per 480 received bits within 8 kbit/s circuit), then re-synchronization should start immediately. The re-synchronization shall be considered completed, when next time 24 contiguous "0"-bits followed by one "1"-bit is received from the 8 kbit/s circuit.

While there is an ongoing call and block decoding process losses block synchronization, then the block decoding process shall behave as if it had received a block having control bits set to values "Sub block1 normal; sub block2 normal" and "Sub block1 BFI with error(s); sub block2 BFI with error(s)".

NOTE: The voice decoding process will use error concealment to minimize voice quality loss. Refer to ETS 300 395-2 [1].

In the general case, the synchronization pattern shall be as shown in figure 2. Bits marked with "x" can have any value.

Content:	00000000	00000000	00000000	1xxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
Octet N°	0	1	2	3	4	5	....

Figure 2: General format of synchronization pattern

5.4   Block error

Only when the decoder process is synchronized to block synchronization pattern, then block error have some meaning.

Block shall be defined to be erroneous, if the block decoder process receives at least one "SYNC_1" bit having value "0" in any of the octet numbers 6, 9,…, 54, 57.

For each sub block there shall be a specific sub block error indicator as defined in clause 5.5. This error indicator can be set at the previous "transmitter" point. The sub block error indicator shall inform, if the sub block content is valid or not.

Consequent actions in case of block error and/or sub block error indicators active are explained in clause 5.3.

5.5   Control bits

With control bits the coding process shall define if data bits have some meaning or not for the remote speech decoder process as defined in tables 2 and 3.

Table 2: Control bits C1, C2 and C3 in STE block format

C1	C2	C3	Explanation
0	0	0	Sub block1 normal; sub block2 normal
0	0	1	Sub block1 C stolen; sub block2 normal
0	1	0	Sub block1 U stolen; sub block2 normal
0	1	1	Sub block1 C stolen; sub block2 C stolen
1	0	0	Sub block1 C stolen; sub block2 U stolen
1	0	1	Sub block1 U stolen; sub block2 C stolen
1	1	0	Sub block1 U stolen; sub block2 U stolen
1	1	1	O&M ISI block; (see note)
NOTE:			The O&M block is reserved for future use.

NOTE 1:   Although the present document does not define contents of the O&M ISI block it is assumed that the same synchronization pattern will be applied in that block so that only the D and S bits are used for the O&M block data information and the "0", "1" and SYNC_1 bits are preserved.

Table 3: Control bits C4 and C5 in STE block format

C4	C5	Explanation
0	0	Sub block1 BFI no errors; sub BLOCK2 BFI no errors
0	1	Sub block1 BFI no errors; sub Block2 BFI with error(s)
1	0	Sub block1 BFI with error(s); sub block2 BFI no error(s)
1	1	Sub block1 BFI with error(s); sub block2 BFI with error(s)
NOTE:		The meaning of C4 and C5 is outside the scope of the present document, when the O&M ISI block is used.

Sub block1 shall refer to data bits D1 - D137 and SYNC_1 bits within octet numbers 3 to 21. Sub block2 shall refer to data bits D1 - D137 and SYNC_1 bits within octet numbers 31 to 49.

NOTE 2:   If the voice decoder process receives during a call either C- or U-stolen sub block(s) (or O&M ISI block), then the voice decoder will use error concealment the last correctly received speech frame(s) instead of this stolen sub block. Refer to ETS 300 395-2 [1].

5.6   Spare bits

The spare bits shall be filled with "1":s on the "transmitter" process, but receiver process should be tolerant to receive any values as in future versions of the present document the space bits may be used for any purpose.

6   Overview of OSTE

6.1   Mapping structure of OSTE

TETRA voice codec encoded audio (speech) is mapped into Optimized Speech Transport Encoding format (OSTE) used for voice signal transmission between SwMIs, see figure 3. The TETRA speech encoding is defined in ETS 300 395-2 [1] and the G.704 framing is defined in ITU-T Recommendation G.704.
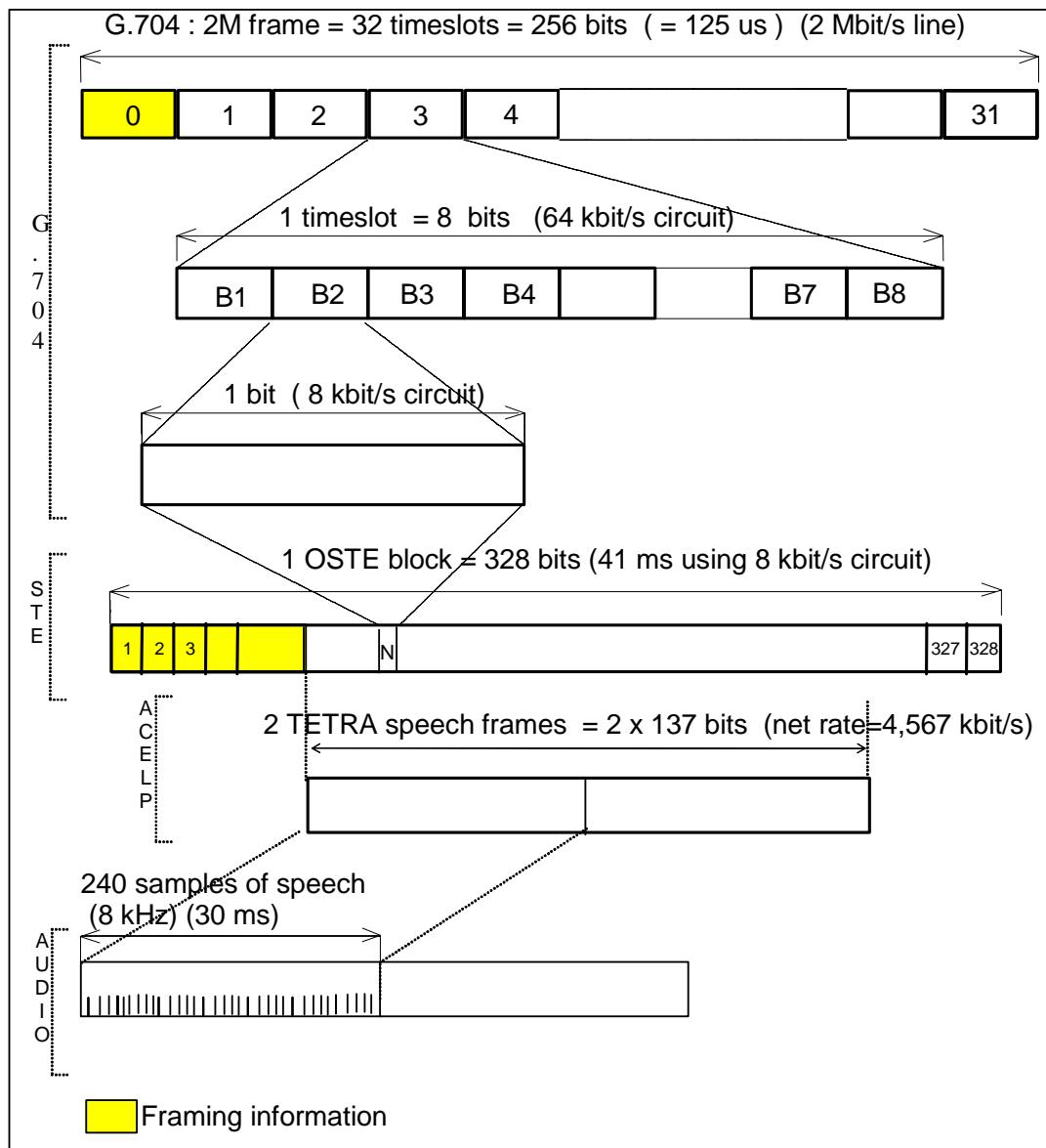
Figure 3: Mapping structure

6.2 OSTE block layer

The TETRA speech frames are mapped to OSTE block format within 8 kbit/s circuit. An optimized block format is used, which reduces the need for buffering due to 18th frame gap. Detailed specification of OSTE format is given on clause 7.

6.3 TETRA ACELP

Audio signal is coded with TETRA ACELP coding. The TETRA ACELP coding is a TETRA speech coding standard ETS 300 395-2 [1]. TETRA ACELP coding produces 137 coding bits from 30 ms length of audio speech frame, which consists of 240 speech audio samples taken with 8 kHz rate.

7   Block format and procedures for OSTE

7.1   General requirements

OSTE is the STE block format that shall be used to carry TETRA ACELP coded speech and U-stolen frames within 8 kbit/s circuits over the TETRA ISI fulfilling requirements of the present document.

Each STE block shall incorporate block synchronization, control bits, frame number bits, data bits (=speech or U-stolen bits), reserved bits and eventually idle bits. The details of the OSTE block format are described in clause 7.2.

The OSTE blocks should be transmitted as soon as available at 8 kbit/s on the physical link.

> NOTE: In an interface point, where the contents of the OSTE block needs to be understood, the OSTE block transmission can start after reception of SYNC_2 and possibly frame number bits.

Receiver process shall use block synchronization as defined in clause 7.3.

Handling of block errors is described on clause 7.4.

Control bits are defined in clause 7.5.

Frame number bit are defined in clause 7.6.

Idle bits are defined in clause 7.7.

7.2   OSTE block format

The OSTE block shall be encoded as presented in table 4 for speech frames transmission and as presented in table 5 for U-stolen frames transmission. The bits of the block shall be sent over 8 kbit/s channel in octet order so that the octet "1" and its bit number "1" is sent first.

The meaning of different bits in the block is:

> C = control bits (see clause 7.5);

> D = data bits (i.e. TETRA ACELP coded speech bits);

> FN = uplink Frame Number bits (see clause 7.6);

> I = idle bits;

> R = reserved bits;

> S = spare bits;

> SYNC_1 = synchronization bits with value "1"; and

> SYNC_2 = synchronization bits with value "0".

> NOTE: SYNC_2 bit actually indicates that the block is used for speech transmission, refer to clauses 4, 5 and annex A.

The OSTE block shall contain two TETRA ACELP coded speech or stolen frames as indicated by C control bits, see figure 3 and table 4.

Table 4: OSTE block format for speech transmission

Octet Nº	1	2	3	4	5	6	7	8
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	1	C1	C2	C3	C4	C5	D1	D2
5	D3	D4	D5	D6	D7	D8	D9	D10
6	D11	D12	D13	D14	D15	D16	D17	D18
7	SYNC_2	FN1	FN2	FN3	FN4	FN5	R1	R2
8	R3	R4	D19	D20	D21	D22	D23	D24
9	D25	D26	D27	D28	D29	D30	D31	D32
10	SYNC_1	D33	D34	D35	D36	D37	D38	D39
11	D40	D41	D42	D43	D44	D45	D46	D47
12	D48	D49	D50	D51	D52	D53	D54	D55
13	SYNC_1	D56	D57	D58	D59	D60	D61	D62
14	D63	D64	D65	D66	D67	D68	D69	D70
15	D71	D72	D73	D74	D75	D76	D77	D78
16	SYNC_1	D79	D80	D81	D82	D83	D84	D85
17	D86	D87	D88	D89	D90	D91	D92	D93
18	D94	D95	D96	D97	D98	D99	D100	D101
19	SYNC_1	D102	D103	D104	D105	D106	D107	D108
20	D109	D110	D111	D112	D113	D114	D115	D116
21	D117	D118	D119	D120	D121	D122	D123	D124
22	SYNC_1	D125	D126	D127	D128	D129	D130	D131
23	D132	D133	D134	D135	D136	D137	0	D1
24	D2	D3	D4	D5	D6	D7	D8	D9
25	SYNC_1	D10	D11	D12	D13	D14	D15	D16
26	D17	D18	D19	D20	D21	D22	D23	D24
27	D25	D26	D27	D28	D29	D30	D31	D32
28	SYNC_1	D33	D34	D35	D36	D37	D38	D39
29	D40	D41	D42	D43	D44	D45	D46	D47
30	D48	D49	D50	D51	D52	D53	D54	D55
31	SYNC_1	D56	D57	D58	D59	D60	D61	D62
32	D63	D64	D65	D66	D67	D68	D69	D70
33	D71	D72	D73	D74	D75	D76	D77	D78
34	SYNC_1	D79	D80	D81	D82	D83	D84	D85
35	D86	D87	D88	D89	D90	D91	D92	D93
36	D94	D95	D96	D97	D98	D99	D100	D101
37	SYNC_1	D102	D103	D104	D105	D106	D107	D108
38	D109	D110	D111	D112	D113	D114	D115	D116
39	D117	D118	D119	D120	D121	D122	D123	D124
40	SYNC_1	D125	D126	D127	D128	D129	D130	D131
41	D132	D133	D134	D135	D136	D137	0	I1
42	I2	I3	I4	I5	I6	I7	I8	I9
43	I10	I11	I12	I13	I14	I15	I16	etc…

Table 5: OSTE block format for U-stolen bits transmission

Octet Nº	1	2	3	4	5	6	7	8
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	1	C1	C2	C3	C4	C5	D1	D2
5	D3	D4	D5	D6	D7	D8	D9	D10
6	D11	D12	D13	D14	D15	D16	D17	D18
7	SYNC_2	FN1	FN2	FN3	FN4	FN5	R1	R2
8	R3	R4	D19	D20	D21	D22	D23	D24
9	D25	D26	D27	D28	D29	D30	D31	D32
10	SYNC_1	D33	D34	D35	D36	D37	D38	D39
11	D40	D41	D42	D43	D44	D45	D46	D47
12	D48	D49	D50	D51	D52	D53	D54	D55
13	SYNC_1	D56	D57	D58	D59	D60	D61	D62
14	D63	D64	D65	D66	D67	D68	D69	D70
15	D71	D72	D73	D74	D75	D76	D77	D78
16	SYNC_1	D79	D80	D81	D82	D83	D84	D85
17	D86	D87	D88	D89	D90	D91	D92	D93
18	D94	D95	D96	D97	D98	D99	D100	D101
19	SYNC_1	D102	D103	D104	D105	D106	D107	D108
20	D109	D110	D111	D112	D113	D114	D115	D116
21	D117	D118	D119	D120	D121	D122	D123	D124
22	SYNC_1	S1	S2	S3	S4	S5	S6	S7
23	S8	S9	S10	S11	S12	S13	0	D1
24	D2	D3	D4	D5	D6	D7	D8	D9
25	SYNC_1	D10	D11	D12	D13	D14	D15	D16
26	D17	D18	D19	D20	D21	D22	D23	D24
27	D25	D26	D27	D28	D29	D30	D31	D32
28	SYNC_1	D33	D34	D35	D36	D37	D38	D39
29	D40	D41	D42	D43	D44	D45	D46	D47
30	D48	D49	D50	D51	D52	D53	D54	D55
31	SYNC_1	D56	D57	D58	D59	D60	D61	D62
32	D63	D64	D65	D66	D67	D68	D69	D70
33	D71	D72	D73	D74	D75	D76	D77	D78
34	SYNC_1	D79	D80	D81	D82	D83	D84	D85
35	D86	D87	D88	D89	D90	D91	D92	D93
36	D94	D95	D96	D97	D98	D99	D100	D101
37	SYNC_1	D102	D103	D104	D105	D106	D107	D108
38	D109	D110	D111	D112	D113	D114	D115	D116
39	D117	D118	D119	D120	D121	D122	D123	D124
40	SYNC_1	S1	S2	S3	S4	S5	S6	S7
41	S8	S9	S10	S11	S12	S13	0	I1
42	I2	I3	I4	I5	I6	I7	I8	I9
43	I10	I11	I12	I13	I14	I15	I16	etc…

The OSTE block is constructed so that its length can be varied, e.g. to carry a different voice coding signal, as long as the SYNC_1 bits are transmitted as every 24th bit of the block to prevent accidental generation of the block synchronization bit string of 24 consecutive zeros. However in the present document the U-stolen frame is defined to have the same length as the speech frame by addition of spare bits.

If the OSTE sub block is indicated to be C-stolen, then the contents of the data bits in the sub slot are outside the scope of the present document. For an easier implementation of the receiver process it is recommended that the sub slot contains 137 data or spare bits followed by a "0" i.e. the length of the sub block is the same as for the speech transport.

7.3 Block synchronization

During idle mode, when there is not any active call within that 8 kbit/s circuit, no block synchronization is done and the 8 kbit/s circuit shall be filled with all ones ("1").

The searching of block synchronization shall be started, when a new call request is accepted by the SwMI. The block synchronization (alignment) shall be acquired by searching the first instance of 24 contiguous "0"-bits followed by "1" bit in the 8 kbit/s circuit, see figure 4.

After a synchronization the block synchronization signal shall be continuously checked at SYNC_1 positions. If at the assumed SYNC_1 position "0" is found, then a new block synchronization shall be started.

NOTE 1: The block synchronization is expected to not to study SYNC_2 for the block synchronization purposed.

If the block synchronization signal (during a call) is not found (e.g. due to transmission errors or due to PCM synchronization problem due to plesiochronous situation on transport network) close to the presumed block start position, then re-synchronization should start immediately. The re-synchronization shall be considered completed, when next time 24 contiguous "0"-bits followed by one "1"-bit is received from the 8 kbit/s circuit.

The presumed block start position depends whether the sending entity sends the blocks immediately as received at the air interface or whether the 18th frame cap of the air interface is smoothed out.

NOTE 2: In interworking with a packet mode SwMI the interval between speech blocks may in addition vary due to the nature of the packet data network.

While there is an ongoing call and block decoding process looses block synchronization, then the block decoding process shall behave as if it had received a block having control bits set to values "Sub block1 normal; sub block2 normal" and "Sub block1 BFI with error(s); sub block2 BFI with error(s)", refer to clause 7.5.

NOTE 3: The voice decoding process will use error concealment to minimize voice quality loss. Refer to ETS 300 395-2 [1].

In the general case, the synchronization pattern shall be as shown in figure 4. Bits marked with "x" can have any value.

Content:	00000000	00000000	00000000	1xxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
Octet N°	0	1	2	3	4	5	………….

Figure 4: General format of synchronization pattern

7.4 Block error

7.4.1 General on block errors

Only when the decoder process is synchronized to block synchronization pattern, then block error have some meaning.

A block error indicator can also be set at the previous "transmitter" point and should be preserved.

Consequent actions in case of block error and/or sub block error indicators are active are explained in clause 7.3.

7.4.2 Loss of synchronization

Block shall be defined to be erroneous, if the block decoder process receives "SYNC_2" having value "1" in octet number 7 or at least one "SYNC_1" bit having value "0" in any of the octet numbers 10, 13,…, 40 and the decoder shall set the control bits C1 to C3 to values "Sub block1 normal; sub block2 normal" and control bits C4 and C5 to values "Sub block1 BFI with error(s); sub block2 BFI with error(s)", refer to table 7.

7.4.3 Frame stealing

A sub block shall be defined to be erroneous, if the sub block is stolen. In the case of speech transport the stolen frame shall be identified stolen by control bits C1 to C3 bits and that it contains non-useful information for speech transport by control bits C4 and C5 indicating "Sub block1 BFI with error(s)" and/or "sub block2 BFI with error(s)", refer to table 7.

7.5   Control bits

With control bits the coding process shall define if data bits have some meaning or not for the remote speech decoder process as defined in tables 6 and 7.

Table 6: Control bits C1, C2 and C3 in STE block format

C1	C2	C3	Explanation
0	0	0	Sub block1 normal; sub block2 normal
0	0	1	Sub block1 C stolen; sub block2 normal
0	1	0	Sub block1 U stolen; sub block2 normal
0	1	1	Sub block1 C stolen; sub block2 C stolen
1	0	0	Sub block1 C stolen; sub block2 U stolen
1	0	1	Sub block1 U stolen; sub block2 C stolen
1	1	0	Sub block1 U stolen; sub block2 U stolen
1	1	1	O&M ISI block; (see note)
NOTE:			The O&M block is reserved for future use.

NOTE 1: Although the present document does not define contents of the O&M ISI block it is assumed that the same synchronization pattern will be applied in that block so that only the D and S bits are used for the O&M block data information and the "0", "1", SYNC_1 and SYNC_2 bits are preserved, but length can be any.

Table 7: Control bits C4 and C5 in STE block format

C4	C5	Explanation
0	0	Sub block1 BFI no errors; sub BLOCK2 BFI no errors
0	1	Sub block1 BFI no errors; sub Block2 BFI with error(s)
1	0	Sub block1 BFI with error(s); sub block2 BFI no error(s)
1	1	Sub block1 BFI with error(s); sub block2 BFI with error(s)
NOTE:		The meaning of C4 and C5 is outside the scope of the present document, when the O&M ISI block is used.

Sub block1 shall refer to data bits D1 - D137 within octet numbers 4 to 23 (data bit D1 in octet 23 excluded). Sub block2 shall refer to data bits D1 - D137 within octet numbers 23 to 41 (data bits D132 to D137 in octet 23 excluded).

NOTE 2: If the voice decoder process receives during a call either C- or U-stolen sub block(s) (or O&M ISI block) where is should have received a speech sub block, then the voice decoder will use error concealment. Refer to ETS 300 395-2 [1].

7.6   Frame number bits

The uplink Frame Number bits indicate which frame in the air interface or equivalent carried the information in the present frame as defined in table 8.

Table 8: Coding of up link frame number

Frame number bits	Meaning
00000	Frame number and rate unknown
00001	TDMA frame 1 at TDMA rate
etc.	etc.
10001	TDMA frame 17 at TDMA rate
10010	Reserved (Frame 18 position indicator)
10011	Reserved (Unnumbered frame, only one 30ms speech sample is included)
10100	Reserved (Unnumbered frame at TDMA rate)
10101	Reserved (Unnumbered frame at 60ms rate)
10110	Reserved
etc.	etc.
11111	Reserved

7.7   Block end and idle bits

The block ends at the "0" after the D137 bit in octet 41.

One or more idle bits shall be added at the end of the OSTE block, if the next OSTE block is not immediately followed by next one. The number of the additional idle bits can be any. The idle bits shall be filled with "1":s on the "transmitter" process.

NOTE: If no idle bits are added, then there will be one "0" adjacent to the synchronization pattern and the first "1" is preceded by 25 zero bits.

Optionally the sender may use at least nine idle bits so that the "failing" SYNC_1 bit position is also first possible position of the block synchronization pattern as defined in clause 7.3. That option allows the receiver process to start block synchronization search without looking "backwards" to idle bits I1 to I9 for possible synchronization pattern.

Annex A (informative):
Support of circuit mode services

A.1   Background

The same principle as used for speech transmission can be extended to cover circuit mode data transmission. The present document identifies how that can be done.

The circuit mode services in TETRA have features that indirectly may affect to the circuit mode data transmission at ISI:

- number of timeslots;

- Forward Error Correction (FEC) level; and

- interleaving depth.

The number of timeslots and FEC affects to the amount data available for transmission in each frame of the air interface. For simpler implementation the present document use the same amount of ISI resources as used at the air interface allocating one 8 kbit/s circuit for each time timeslot of the air interface frame. No special arrangements are used to minimize transmission delay in ISI is proposed.

The interleaving depth affects to the delay of the data transmission as the interleaving and FEC is applied only over the air interface. Notably all timeslots interleaved at the air interface need to be completely received before transmission of that circuit mode data part can commence.

A.2   Block format and procedures

A.2.1   Mapping structure

Figure A.1 presents the general frame structure for data transmission for a single 8 kbit/s circuit. It is outside the scope of the present document how multi-slot circuit mode data is transmitted.
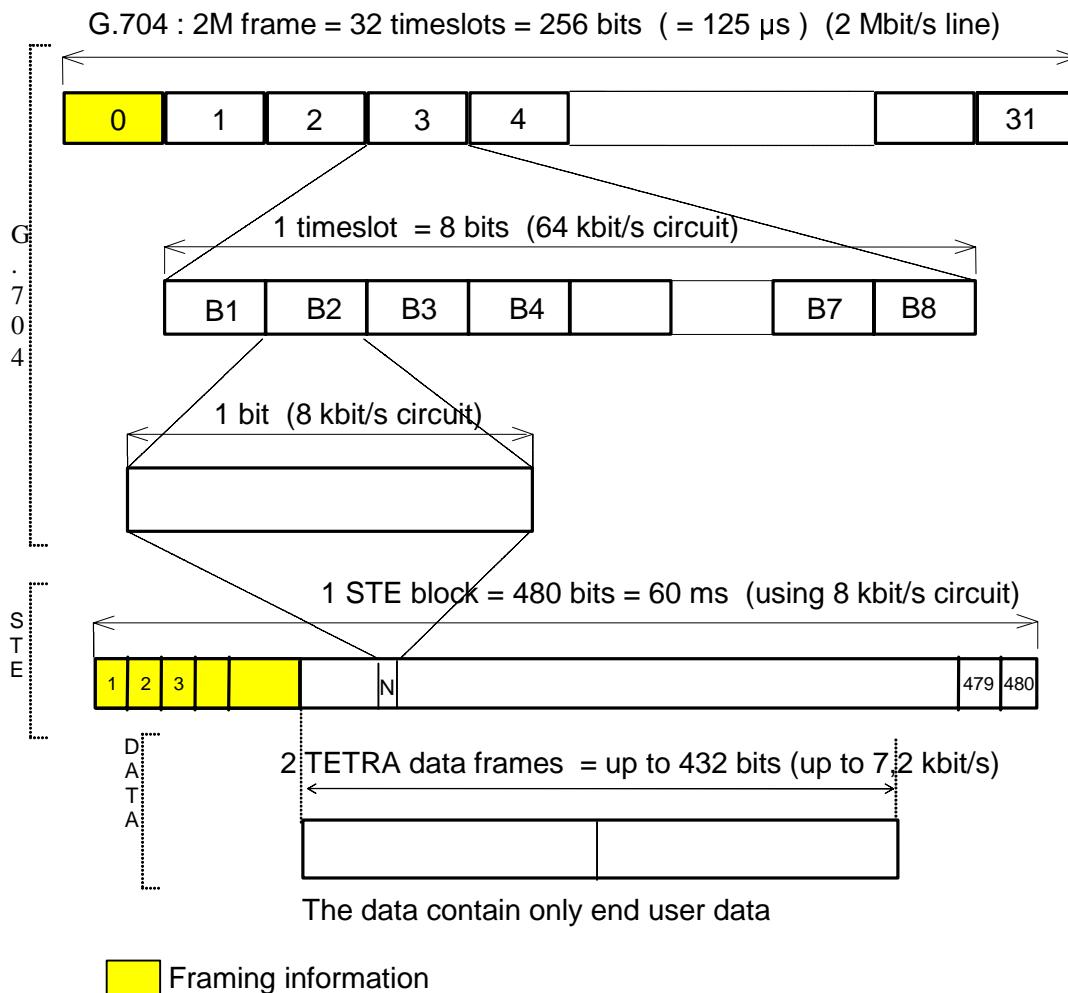
Figure A.1: Circuit mode data mapping structure

A.2.2   FSTE block format

The FSTE block shall be encoded as presented in table A.1 for 4,8 kbit/s case. The bits of the block shall be sent over 8 kbit/s channel in octet order so that the octet "1" and its bit number "1" is sent first.

The meaning of different bits in the block is:

   C = control bits (see clause 5.5)

   D = data bits

   S = spare bits

   SYNC_1 = synchronization bits with value "1".

The FSTE block shall contain two sub-blocks of the air interface equivalent to 60 ms of time, when the frames 1 to 17 of the air interface are spread over time of the frames 1 to 18 of the air interface.

Table A.1: FSTE block format

Octet Nº	1	2	3	4	5	6	7	8
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	1	C1	C2	C3	C4	C5	D1	D2
5	D3	D4	D5	D6	D7	D8	D9	D10
6	D11	D12	D13	D14	D15	D16	D17	D18
7	SYNC_1	D19	D20	D21	D22	D23	D24	D25
8	D26	D27	D28	D29	D30	D31	D32	D33
9	D34	D35	D36	D37	D38	D39	D40	D41
10	SYNC_1	D42	D43	D44	D45	D46	D47	D48
11	D49	D50	D51	D52	D53	D54	D55	D56
12	D57	D58	D59	D60	D61	D62	D63	D64
13	SYNC_1	D65	D66	D67	D68	D69	D70	D71
14	D72	D73	D74	D75	D76	D77	D78	D79
15	D80	D81	D82	D83	D84	D85	D86	D87
16	SYNC_1	D88	D89	D90	D91	D92	D93	D94
17	D95	D96	D97	D98	D99	D100	D101	D102
18	D103	D104	D105	D106	D107	D108	D109	D110
19	SYNC_1	D111	D112	D113	D114	D115	D116	D117
20	D118	D119	D120	D121	D122	D123	D124	D125
21	D126	D127	D128	D129	D130	D131	D132	D133
22	SYNC_1	D134	D135	D136	D137	D138	D139	D140
23	D141	D142	D143	D144	S1	S2	S3	S4
24	S5	S6	S7	S8	S9	S10	S11	S12
25	SYNC_1	S13	S14	S15	S16	S17	S18	S19
26	S20	S21	S22	S23	S24	S25	S26	S27
27	S28	S29	S30	S31	S32	S33	S34	S35
28	SYNC_1	S36	S37	S38	S39	S40	S41	S42
29	S43	S44	S45	S46	S47	S48	S49	S50
30	S51	S52	S53	S54	S55	S56	S57	S58
31	SYNC_1	S59	S60	S61	S62	S63	S64	S65
32	S66	S67	S68	S69	S70	S71	S72	D1
33	D2	D3	D4	D5	D6	D7	D8	D9
34	SYNC_1	D10	D11	D12	D13	D14	D15	D16
35	D17	D18	D19	D20	D21	D22	D23	D24
36	D25	D26	D27	D28	D29	D30	D31	D32
37	SYNC_1	D33	D34	D35	D36	D37	D38	D39
38	D40	D41	D42	D43	D44	D45	D46	D47
39	D48	D49	D50	D51	D52	D53	D54	D55
40	SYNC_1	D56	D57	D58	D59	D60	D61	D62
41	D63	D64	D65	D66	D67	D68	D69	D70
42	D71	D72	D73	D74	D75	D76	D77	D78
43	SYNC_1	D79	D80	D81	D82	D83	D84	D85
44	D86	D87	D88	D89	D90	D91	D92	D93
45	D94	D95	D96	D97	D98	D99	D100	D101
46	SYNC_1	D102	D103	D104	D105	D106	D107	D108
47	D109	D110	D111	D112	D113	D114	D115	D116
48	D117	D118	D119	D120	D121	D122	D123	D124
49	SYNC_1	D125	D126	D127	D128	D129	D130	D131
50	D132	D133	D134	D135	D136	D137	D138	D139
51	D140	D141	D142	D143	D144	S1	S2	S3
52	SYNC_1	S4	S5	S6	S7	S8	S9	S10
53	S11	S12	S13	S14	S15	S16	S17	S18
54	S19	S20	S21	S22	S23	S24	S25	S26
55	SYNC_1	S27	S28	S29	S30	S31	S32	S33
56	S34	S35	S36	S37	S38	S39	S40	S41
57	S42	S43	S44	S45	S46	S47	S48	S49
58	SYNC_1	S50	S51	S52	S53	S54	S55	S56
59	S57	S58	S59	S60	S61	S62	S63	S64
60	S65	S66	S67	S68	S69	S70	S71	S72

For various TETRA air interface FEC cases the division of data and spare bits in each half block is presented in table A.2.

Table A.2: Number of data and spare bits in each half block

Data rate bit/s	Data bits	Spare bits
2 400	72	144
4 800	144	72
7 200	216	0
U-stolen	124	92
U-stolen + 2 400	124 + 72	20

If the circuit mode data bits are stolen, then the stolen bits occupy 124 data bits and the rest of the bits are spare bits as defined in the table A.2 on the row U-stolen. In the case of data rate of 2 400 bit/s and suitable interleaving and forward error correction the circuit mode data may be recovered and may be added at the end of the U-stolen part replacing the first 72 spare bits.

A.2.3   Block synchronization

During idle mode, when there is not any active call within that 8 kbit/s circuit, no block synchronization is done and the 8 kbit/s circuit shall be filled with all ones ("1").

The searching of block synchronization shall be started, when a new call request is accepted by the SwMI. The block synchronization (alignment) shall be acquired by searching the first instance of 24 contiguous "0"-bits followed by one "1"-bit in the 8 kbit/s circuit, see figure 2.

After a synchronization the block synchronization signal shall be continuously checked with the presumed block start position for the alignment.

If the block synchronization signal (during a call) is not found (e.g. due to transmission errors or due to PCM synchronization problem due to plesiochronous situation on transport network) from the presumed block start position (ones per 480 received bits within 8 kbit/s circuit), then re-synchronization should start immediately. The re-synchronization shall be considered completed, when next time 24 contiguous "0"-bits followed by one "1"-bit is received from the 8 kbit/s circuit.

While there is an ongoing call and block decoding process looses block synchronization, then the block decoding process shall behave as if it had received a block having control bits set to values "Sub block1 normal; sub block2 normal" and "Sub block1 BFI with error(s); sub block2 BFI with error(s)".

In the general case, the synchronization pattern shall be as shown in figure 2 in clause 5.3. Bits marked with "x" can have any value.

A.2.4   Block error

A.2.4.1   General on block errors

Only when the decoder process is synchronized to block synchronization pattern, then block error have some meaning.

A block error indicator can also be set at the previous "transmitter" point and should be preserved.

Consequent actions in case of block error and/or sub block error indicators in the case of circuit mode data transport are outside the scope of the present document.

A.2.4.2   Loss of synchronization

Block shall be defined to be erroneous, if the block decoder process receives at least one "SYNC_1" bit having value "0" in any of the octet numbers 7, 10, 13,…, 40 and the decoder shall set the control bits C1 to C3 to values "Sub block1 normal; sub block2 normal" and control bits C4 and C5 to values "Sub block1 BFI with error(s); sub block2 BFI with error(s)", refer to table 7.

A.2.4.3   Frame stealing

Generally a sub block shall be defined to be erroneous, if the sub block is stolen. In the case of 2 400 bit/s data rate and long interleaving a stealing of a sub block may not generate any errors to the circuit mode data due to the strength of the forward error correction. If the sub block was C-stolen and the forward error correction potentially recovered the circuit mode data, then the ISI interface need not to indicate that at all and send the circuit mode data as if no stealing took place. If the sub block was U-stolen and the forward error correction potentially recovered the circuit mode data, then the ISI may put the circuit mode data bits after the U-stolen data bits and indicate by control bits C1 to C3 that the sub block was stolen and by control bits C4 and C5 "Sub block BFI no errors". Refer to table A.2 and clause A.2.2.

In the case of circuit mode data transport the stolen frame shall be identified stolen by control bits C1 to C3 bits and that it contains non-useful information for circuit mode data transport by control bits C4 and C5 indicating "Sub block1 BFI with error(s)" and/or "sub block2 BFI with error(s)", refer to table 7.

A.2.5   Control bits

Clause 5.5 applies. Sub block1 shall refer to data bits D1 up to D216 within octet numbers 3 to 32 (D1 in octet 32 excluded). Sub block2 shall refer to data bits D1 up to D216 within octet numbers 32 to 60 (D210 - D216 in octet 32 excluded).

NOTE: In the case of 2 400 bit/s data rate both the stolen data and the circuit mode data may be recovered and that special case uses combination of values "Sub block stolen" and "Sub block BFI no errors", which is not normally a valid combination.

Annex B (informative):
Bibliography

ITU-T Recommendation G.703: "Physical/electrical characteristics of hierarchical digital interfaces".

ITU-T Recommendation G.704: "Synchronous frame structures used at 1 544, 6 312, 2 048, 8 448 and 44 736 kbit/s hierarchical levels".

History

Document history		
V1.1.1	December 2003	Publication