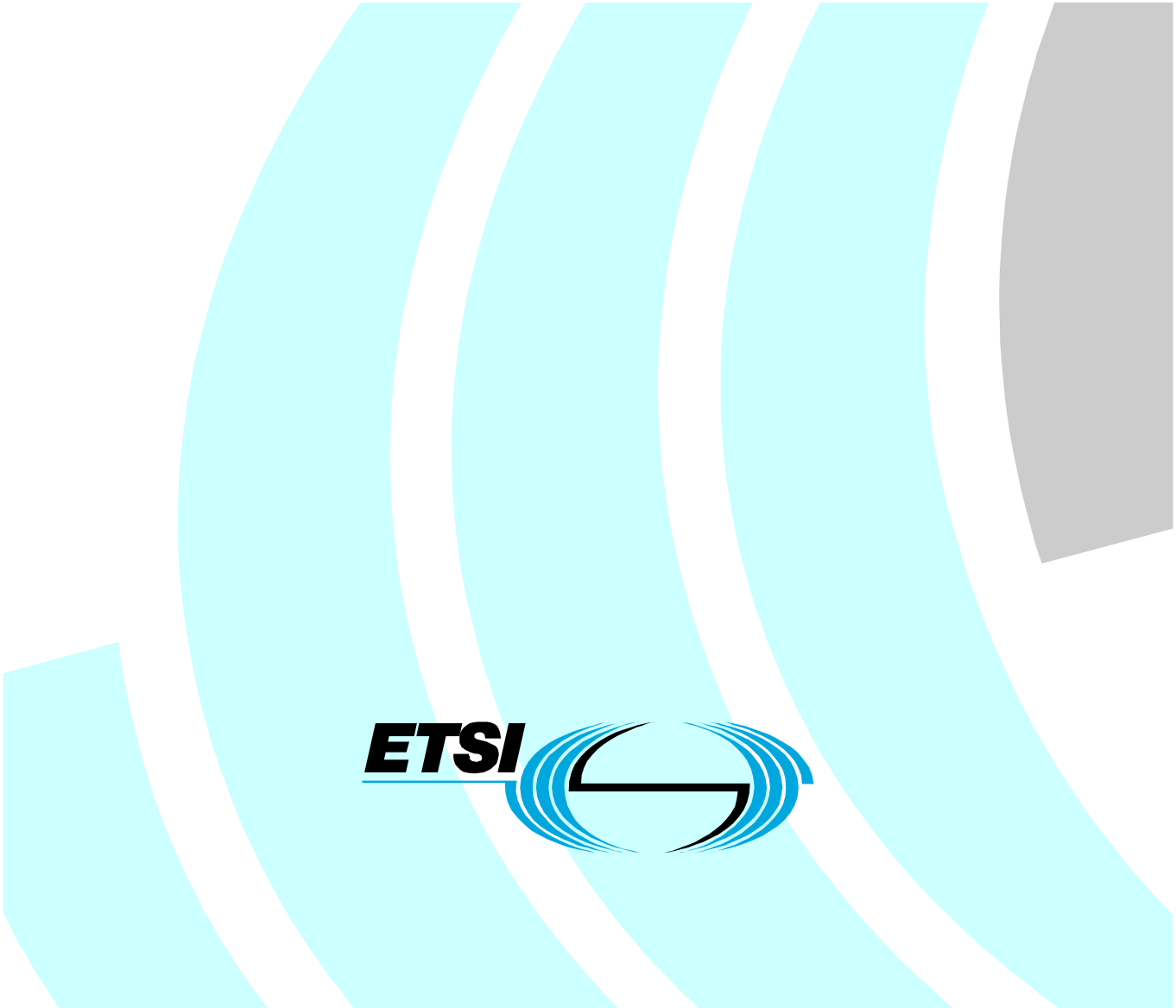
ETSI TR 101 953-2-1 V1.1.1 (2003-12)

Technical Report

Access network xDSL transmission filters;
Part 2: VDSL splitters for European deployment;
Sub-part 1: Specification of Testing methods
for low pass part of VDSL/POTS splitters



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ETSI

650 Route des Lucioles
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C
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Foreword

This Technical Report (TR) has been produced by ETSI Technical Committee Access and Terminals (AT).

- AT Analogue of Technical Committee Access and Terminals (AT); and
- TM6 of Technical Committee Transmission and Multiplexing (TM).

The present document is part 2, sub-part 1 of a multi-part deliverable supporting different aspects of European Specific DSL splitters, as identified below:

Part 1: "ADSL splitters for European deployment";

Part 2: "VDSL splitters for European deployment";

Sub-part 1: "Specification of Testing methods for low pass part of VDSL/POTS splitters";

Sub-part 2: "Specification of Testing methods for high pass part of VDSL/POTS splitters";

Sub-part 3: "Specification of Testing methods for VDSL/ISDN splitters".

NOTE: The choice of a multi-part format for this deliverable is to facilitate maintenance and future enhancements.

1 Scope

The present document describes test methods for the low pass section of VDSL/POTS splitters. These splitters are intended to be installed at the Local Exchange side of the local loop and at the user side near the NTP. In the case of splitters at the user side, the present document describes test methods for the master splitter that is intended for use at the demarcation point of the customer premises. Distributed filters are not concerned by the present document.

2 References

For the purposes of this Technical Report (TR) the following references apply:

[1] ETSI TS 101 270 (all parts): "Transmission and Multiplexing (TM); Access transmission systems on metallic access cables; Very high speed Digital Subscriber Line (VDSL)".

[2] ETSI TS 101 952-2-1: "Access network xDSL transmission filters; Part 2: VDSL splitters for European deployment; Sub-part 1: Specification of the low pass part of VDSL/POTS splitters".

[3] ETSI TS 101 952-1-1: "Access network xDSL transmission filters; Part 1: ADSL splitters for European deployment; Sub-part 1: Specification of the low pass part of ADSL/POTS splitters".

[4] ETSI TR 101 953-1-1: "Access and Terminals (AT); Unified and Generic Testing Methods for European Specific DSL splitters; Part 1: ADSL splitters for European deployment; Sub-part 1: Specification of Testing methods for Low Pass part of ADSL/POTS splitters".

[5] ETSI TR 102 139: "Compatibility of POTS terminal equipment with xDSL systems".

[6] ETSI TR 101 728: "Access and Terminals (AT); Study for the specification of low pass filter section of POTS/ADSL splitters".

[7] ITU-T Recommendation O.9: "Measuring arrangements to assess the degree of unbalance about earth".

[8] ITU-T Recommendation O.42: "Equipment to measure non-linear distortion using the 4-tone intermodulation method".

[9] ETSI TBR 038: "Public Switched Telephone Network (PSTN); Attachment requirements for a terminal equipment incorporating an analogue handset function capable of supporting the justified case service when connected to the analogue interface of the PSTN in Europe".

[10] ETSI TBR 021: "Terminal Equipment (TE); Attachment requirements for pan-European approval for connection to the analogue Public Switched Telephone Networks (PSTNs) of TE (excluding TE supporting the voice telephony service) in which network addressing, if provided, is by means of Dual Tone Multi Frequency (DTMF) signalling".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

A-wire and B-wire: wires in the 2-wire local loop connection provided from the exchange to the NTP

on-hook: state of the POTS equipment at either end of a POTS loop connection when the NTP terminal equipment is in the quiescent state

NOTE: In the case where there are multiple TE present at the customer end of the loop, then only when all of these are on-hook should the CPE be considered to be on hook from the perspective of testing the splitter.

off-hook: state of the POTS equipment at either end of a loop connection when the NTP terminal equipment is in the steady loop state

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ADSL	Asymmetric Digital Subscriber Line
CO	Central Office (Local Exchange)
CPE	Customer Premises Equipment
dBm	absolute power level expressed in decibels relative to 1 mW
dBmp	absolute power level weighted psophometrically
dBV	absolute voltage level expressed in decibels relative to 1 Volt
dBVp	absolute voltage level weighted psophometrically
DSLAM	Digital Subscriber Line Access Multiplexer
DUT	Device Under Test
HPF	High Pass Filter
ISDN-BA	Integrated Services Digital Network-Basic Access
ITU	International Telecommunication Union
LCL	Longitudinal Conversion Loss
LCTL	Longitudinal Conversion Transfer Loss
LE	Local Exchange (Central Office)
LPF	Low Pass Filter
LT	Line Termination
NF	Narrow-band Frequency
NT	Network Termination
NTP	Network Termination Point
POTS	Plain Old Telephone Service
rms	root mean square
TE	Terminal Equipment (e.g. telephone, fax, voice band modem, etc.)
THD	Total Harmonic Distortion
VDSL	Very high speed Digital Subscriber Line

4 Introduction

The present document is part 2 of a multi-part deliverable supporting different aspects of European Specific DSL splitters.

It has been produced based on the activities of ETSI STF 248.

The current document describes test methods for the low pass part of VDSL/POTS splitters.

The test methods of this Technical Report are based on requirements of the following document:

- TS 101 952-2-1 [2].

Furthermore certain aspects of the following documents have been considered as to provide a document which is consistent with the specifications of the other sub parts of TR 101 953:

- TS 101 952-1-1 [3];
- TR 101 953-1-1 [4].

For each test, the document describes:

- Title of the test;
- Requirement in reference to the specifications;
- Purpose of the test;

- Test configuration;
- Test set up;
- Test parameters;
- Test matrix;
- Test procedure note;
- Test Result;
- Measuring notes.

5 Test conditions and general notes

For each test, feeding bridge and holding circuit must comply to the requirements as specified in TBR 038 [9] with respect to the low frequency range. Similar performance is required for the high frequency range (up to 12 MHz). An equivalent accuracy may be obtained by calibrating the feeding bridge and holding circuit across the relevant frequency range.

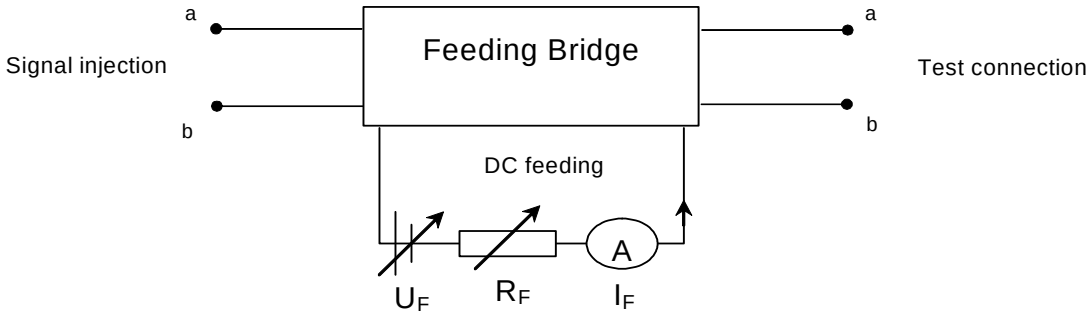


Figure 1: External circuitry for feeding bridge

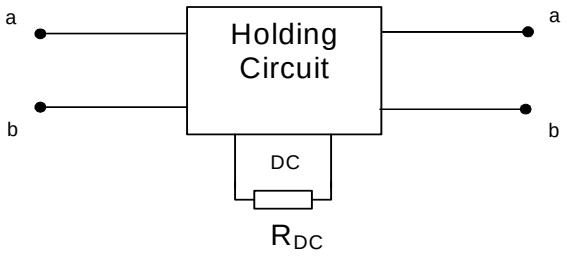


Figure 2: External circuitry for holding circuit

General notes:

Polarity of the feeding voltage and with this the direction of the feeding current may impact the additional insertion loss caused by feeding bridge and holding circuit. A calibration/normalization measurement need to be taken before each single measurement step.

For active splitters the connection of the DC feeding is essential i.e. for LE splitters the feeding bridge should be connected to the POTS port and the holding circuit should be connected to the LINE port. For TE splitters the feeding bridge should be connected to the LINE port and the holding circuit should be connected to the POTS port.

Test set-ups as given in the present document show TE test set-ups unless stated otherwise. Tests for LE splitter evaluation should be set up considering the aforementioned. Accordingly, ringing and metering signals shall be provided to the relevant port of the tested splitter (LE splitter: signal source connected to POTS port and load connected to LINE port; TE splitter: signal source connected to LINE port and load connected to POTS port).

The inaccuracy of the measurement which results from tolerances in the test set-up and its containing equipment should be carefully considered. When giving a verdict on the test results with respect to the requirement in the related standard this tolerance in the test results need to be taken into account.

Z_{VDSL} as given in the current version of TS 101 952-2-1 [2] is likely to be changed in co-operation between ETSI AT and ETSI TM6. The termination as referenced to in the present document reflect the current specification, however, when performing tests Z_{VDSL-1} and Z_{VDSL-2} and all related parameters shall be checked carefully with the then-current TS 101 952-2-1 [2].

Before splitters are tested the class of splitter should be categorized. Basis for this could be the schematic of the splitter or a statement of the manufacturer. The following classes have been identified so far in the course of this project:

- **passive:** splitters which do exclusively contain passive components.
- **passive with current/voltage detection:** splitters which perform NF filtering using passive components, which are enhanced by detection circuits based on the DC voltage and/or the DC current.
- **active:** splitters which contain active components (like OP amplifier) to perform the NF filtering.

NOTE: The splitters which have been evaluated during the validation of the test methods described herein are to be classified in cluster "passive". Although the STF 248 has not had a splitter classified in cluster "passive with current/voltage detection" at hand for the validation, the experience from STF 215 allowed to assess the test methods for that type, too. No "active" splitters could be made available for evaluation. The results of the STF 248 work could be validated for the first two classes, for the third class (active splitters) theoretical test case validations have been discussed.

At some test cases in the present document, a difference is made between splitters which do not break the DC path and splitters which do break the DC path. The following drawings should give a guidance for the separation of this two different types.

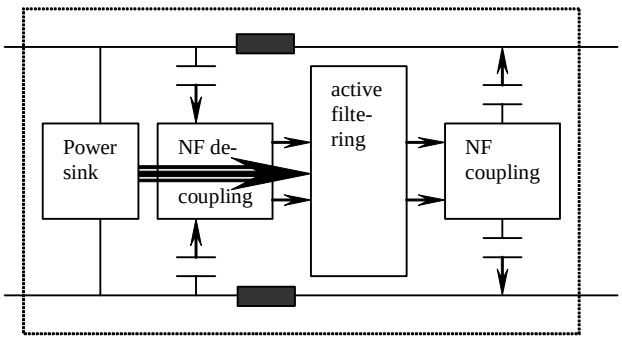


Figure 3: Example for a splitter not breaking the DC path

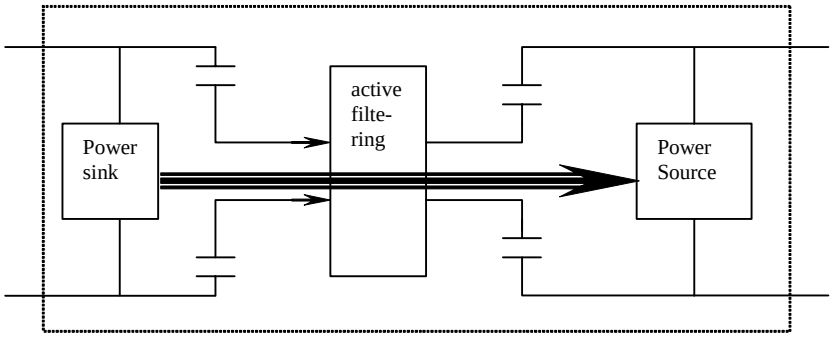


Figure 4: Example for a splitter breaking the DC path

Filters with current/voltage detection must be classified under the first type of splitters for their operating range (e.g. DC current above detection limit) and under the second type of splitters in the blocking range (e.g. DC current below detection limit).

6 List of test cases for the low pass part of the VDSL over POTS splitter

6.1 Tests for DC requirements

6.1.1 Tests for DC resistance to earth

Table 1

Test case name:	DC Resistance to Earth
Reference:	TS 101 952-2-1 [2], clause 6.2.1
Test purpose:	To evaluate the DC resistance between a-wire and earth as well as b-wire and earth. This test only applies to splitters which provide a terminal which is connected to ground. (see note)
Test configuration:	See Test Set-up; DUT not configured
NOTE: A splitter is considered to provide a earth connection, as soon as there is a specific terminal which might lead to the reasonable assumption that it could be connected to ground. Furthermore, this test is to be performed, when there are non-insulated conducting parts at the enclosure.	

Test set-up:

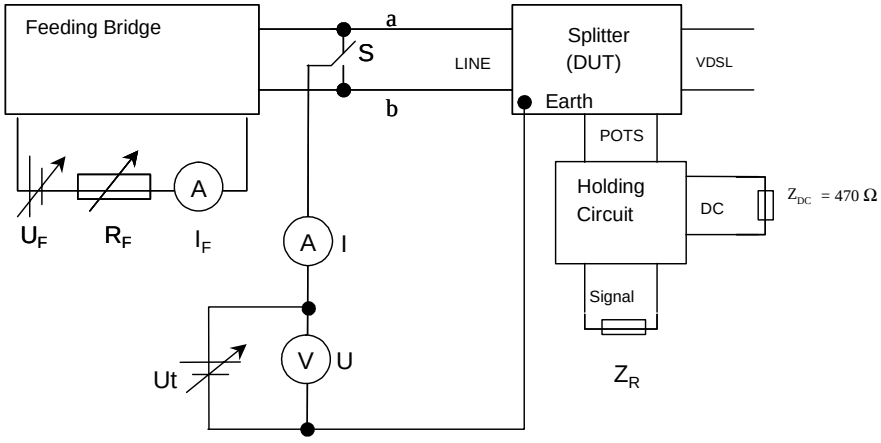


Figure 5: Test set-up for DC resistance between terminal and earth when testing LINE port

Test parameters:

Table 2

Parameter	Value
DC test voltage Ut	100 VDC -100 VDC
Feeding voltage U_F	50 VDC -50 VDC
Feeding current I_F in off-hook state	0 mA 13 mA 30 mA 60 mA 80 mA
Position of switch S	a-wire b-wire
Termination at POTS port	Z_R, R_{DC} = 470 Ω open circuit
Termination at VDSL port	open circuit
Ports to be tested (probe to be connected to)	LINE POTS (only for splitters breaking the DC path in any way) VDSL

Test matrix:

Table 3

	TS 101 952-2-1 [2]	Essential tests	Optional tests
DC test voltage Ut: +100 VDC	X	X	
DC test voltage Ut: -100 VDC	X	X	
Ut applied to LINE port	X	X	
Ut applied to POTS port (for splitters breaking the DC path only!)	X	X	
Ut applied to VDSL port	X	X	
Switch in position a	X	X	
Switch in position b	X	X	
Feeding voltage U_F: +50 VDC	X	X	
Feeding voltage U_F: -50 VDC	X	X	
Feeding current I_F: 0 mA	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 30 mA	X	X	
Feeding current I_F: 60 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Termination at POTS port: Z_R, R_{DC} = 470 Ω	X	X	
Termination at POTS port: open circuit	X	X	
Number of tests	32 tests (48 for splitters breaking the DC path)	32 tests (48 for splitters breaking the DC path)	

Test procedure notes:

NOTE 1: When a DC current is flowing, the difference in the test results between the measurements from a-wire to earth and b-wire to earth is negligible (only the R_{DC} and the series resistance of the holding circuit is added to the result). With this, at the LINE port and the POTS port testing only one wire against earth is sufficient when there is no break in the DC path.

NOTE 2: Splitters breaking the DC path should be tested completely (all three ports), splitters not breaking the DC path can use a reduced test which only requires testing at the xDSL port and the LINE port.

NOTE 3: At the xDSL port a- and b- wire should be tested separately, however, a DC current need not be applied.

NOTE 4: Verification of the test result: To verify the test result, a well-known resistor of about 5 MΩ (measured independently at an uncertainty of less than 0,1 %) should be connected to the test set-up and the resulting current should be compared with the theoretically expected result.

NOTE 5: When the resistance from wire to earth is measured when RDC is connected, one roughly sees the two resistances (one from a-wire to earth and the other from b-wire to earth) in parallel. The test result must be assessed accordingly. When RDC is not connected (0 mA measurement) the resistances from each wire to earth is seen as a single one.

Test results:

Test Result has to be recorded in two ways:

when RDC is not connected:

- I in µA, where: I is the value of the observed current, which is flooding into the tip under test;
- $R_{(DC\text{-}wire\text{-}earth)}$, where $R_{(DC\text{-}wire\text{-}earth)} = Ut/I$.

when RDC is connected:

- I in µA, where: I is the value of the observed current, which is flooding into the tip under test;
- $R_{(DC\text{-}a/b\text{-}wire\text{-}earth)}$, where $R_{(DC\text{-}a/b\text{-}wire\text{-}earth)} \approx 2Ut/I$.

NOTE 6: The result for $R_{(DC\text{-}a/b\text{-}wire\text{-}earth)}$ when R_{DC} is connected assumes that both resistances are of the same magnitude. If this is not the case, this will be visible at the measurements where R_{DC} is not connected (compare $R_{(DC\text{-}wire\text{-}earth)}$).

Measuring notes:

See general notes.

6.1.2 Tests for DC insulation resistance between A-wire and B-wire

Table 4

Test case name:	DC Insulation resistance between a-wire and b-wire (open ports)
Reference:	TS 101 952-2-1 [2], clause 6.2.2
Test purpose:	To evaluate the DC series resistance between a-wire and b-wire of the various ports when all the ports are left open
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

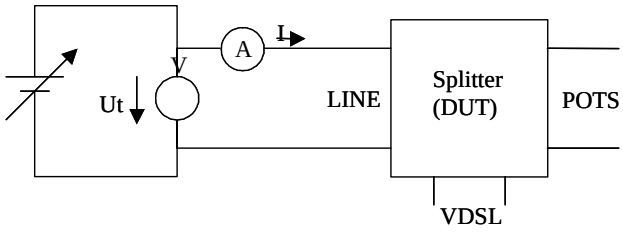


Figure 6: Test Set-up for DC insulation between a-wire and b-wire measurements

Test parameters:

Table 5

Parameter	Value
DC test voltage Ut	100 VDC -100 VDC
Termination at ports under test	open circuit
Termination at ports not under test (while testing at another one)	open circuit
Ports to be tested (probe to be connected to)	LINE POTS (only for splitters breaking the DC path in any way)

Test matrix:

Table 6

	TS 101 952-2-1 [2]	Essential tests	Optional tests
DC test voltage Ut: +100 VDC **DC test voltage Ut: -100 VDC**	X X	X X	
Ut applied to LINE port **Ut applied to POTS port (for splitters breaking the DC path only!)** **Ut applied to VDSL port**	X X	X X	
Number of tests	2 tests (4 for splitters breaking the DC path)	2 tests (4 for splitters breaking the DC path)	

Test procedure notes:

NOTE 1: If the splitter is not breaking the DC path, it is sufficient to measure at one port (the LINE port). If the splitter is breaking the DC path, both ports (LINE and POTS) should be measured.

NOTE 2: Verification of the test result: To verify the test result, a well-known resistor of about 5 MΩ (measured independently at an uncertainty of less than 0,1 %) should be connected to the test set-up and the resulting current should be compared with the theoretically expected result.

NOTE 3: Testing the xDSL port with respect to the DC resistance between open wires has been cancelled as it is not to be expected that a DC of that level occurs in normal operation at the xDSL port. Even if the DC resistance is lower than 5 MΩ this need not necessarily lead to a performance loss on the DSL path.

Test results:

Test Result has to be recorded in two steps:

- I in µA, where: I is the value of the observed current, which is flooding into the tip under test;
- $R_{DC\text{-}wire\text{-}wire}$, where $R_{DC\text{-}wire\text{-}wire} = Ut/I$.

Measuring notes:

See general notes.

6.1.3 Tests for DC series resistance

Table 7

Test case name:	DC series resistance
Reference:	TS 101 952-2-1 [2], clause 6.2.3
Test purpose:	To evaluate the DC series resistance between wires at the LINE port, and the wires at the POTS port with an open circuit applied to the VDSL port
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

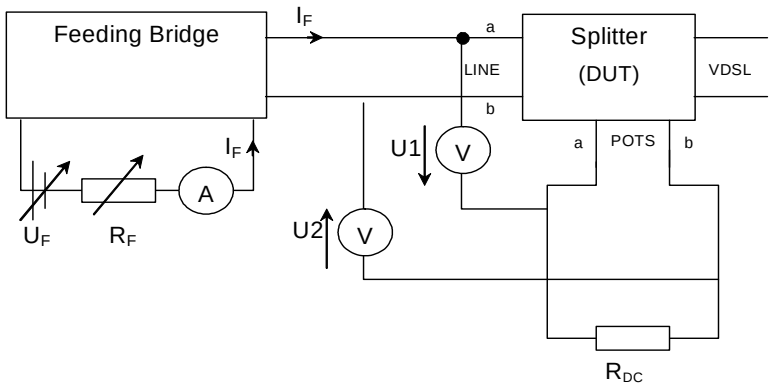


Figure 7: Test set-up for DC resistance measurements

Test parameters:

Table 8

Parameter	Value
Feeding voltage U_F	50 V_{DC}
Feeding current I_F	13 mA 30 mA 60 mA 80 mA
Polarity of feeding voltage	Alternating
Termination at VDSL port	open circuit
Termination at POTS port	R_{DC} = 470 Ω
Ports to be tested	LINE

Test matrix:

Table 9

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Feeding voltage U_F: 50 V_{DC}	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 30 mA	X	X	
Feeding current I_F: 60 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Polarity of feeding voltage	alternating	alternating	
Termination at POTS port: R_{DC}	X	X	
Termination at VDSL port: open circuit	X	X	
Number of tests	4 tests	4 tests	

Test procedure notes:

NOTE 1: The DC series resistance of passive splitters without current/voltage detection does not change with the value of the current. Furthermore, the DC series resistance of passive splitters without current/voltage detection usually does not change but may change with the polarity of the current. Therefore, it is recommended to test half of the tests using normal polarity and half the tests using reversed polarity.

NOTE 2: The DC series resistance of passive splitters with current/voltage detection changes significantly (or at least may change significantly) with the value of the current. However, the DC series resistance of passive splitters with current/voltage detection does not change its tendency with the polarity of the current.

NOTE 3: The current leakage which is present for passive splitters with current/voltage detection and for active splitters is not defined in TS 101 952, yet. A validation of the test is not possible without having specific knowledge on the splitters implementation as long as the (current/voltage dependent) power consumption of the splitter itself is not clear. Until clarification this test case does not apply for passive splitters with current/voltage detection and for active splitters.

NOTE 4: Splitters that do break the DC path cannot be assessed using this type of test. The assessment of active splitters and splitters that break the DC path in any way is for further study.

NOTE 5: Verification of the test result: To verify the test result, two well-known resistors of about 25 Ω (measured independently at an uncertainty not more than of 0,1 %) should be connected to the test set-up, simulating two DC branches of the splitter. The resulting current should be compared with the theoretically expected result.

Test results:

Test Result has to be recorded in three steps:

- U1 and U2 in V, where: U1 is the voltage drop between a-wire of the LINE port and the a-wire of the POTS port and U2 is the voltage drop between b-wire of the LINE port and the b-wire of the POTS port.
- I_F in mA, where I_F is the resulting feeding current.
- $R_{DC\text{-}series}$, where $R_{DC\text{-}series} = (U1 + U2)/I_F$.

Measuring Notes:

See general notes.

6.2 Tests for ringing frequency requirements

6.2.1 Tests for voltage drop at 25 Hz and 50 Hz

Table 10

Test case name:	Voltage Drop at 25 Hz and 50 Hz
Reference:	TS 101 952-2-1 [2], clause 6.3.1
Test purpose:	To measure the voltage drop at 25 Hz and 50 Hz when tested with the test parameters as given in the related standards
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

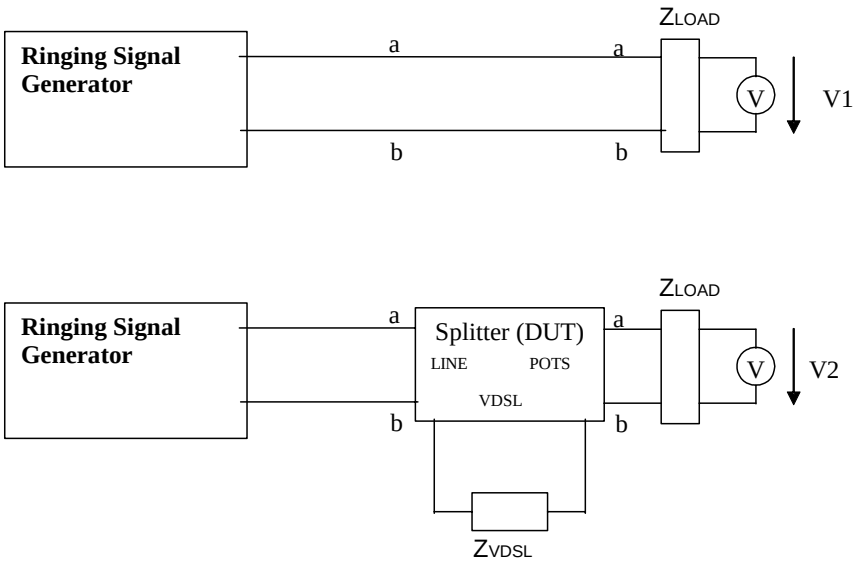


Figure 8: Test Set-up for voltage drop at 25 Hz and 50 Hz measurements

Test parameters:

Table 11

Parameter	Value
Frequency of the test signal	(i) 25 Hz (ii) 50 Hz
Amplitude of the test signal	35 Vrms superimposed on 60 VDC
Source impedance Z_{SOURCE}	850 Ω resistive
Load impedance Z_{LOAD}	(i) 2,7 kΩ + 2,2 µF for 25 Hz (ii) 2,7 kΩ + 1,0 µF for 50 Hz
VDSL termination	Z_{VDSL} open circuit

Test matrix:

Table 12

	TS 101 952-2-1 [2]	Essential tests	Optional tests
25 Hz signal frequency	X	X	
50 Hz signal frequency	X	X	
35 Vrms superimposed on 60 VDC	X	X	
35 Vrms superimposed on -60 VDC	X	X	
Source impedance Z_{SOURCE} = 850 Ω	X	X	
Termination at VDSL port: Z_{VDSL}	X	X	
Termination at VDSL port: open circuit	X	X	
Number of tests	8 tests	8 tests	

Test procedure notes:

Test results:

The voltage drop measured should be recorded.

- voltage drop = V1 - V2

Measuring notes:

Suggested configuration for Z_{LOAD} (approx. modulus 4 000 Ω, angle -45°):

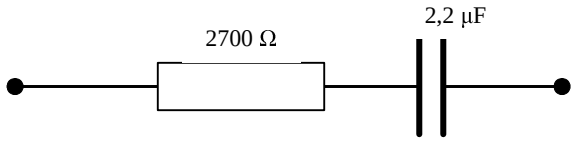


Figure 9: Z_{LOAD} for 25 Hz

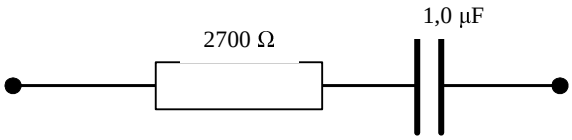


Figure 10: Z_{LOAD} for 50 Hz

6.2.2 Tests for impedance at 25 Hz and 50 Hz

Table 13

Test case name:	Impedance at 25 Hz and 50 Hz
Reference:	TS 101 952-2-1 [2], clause 6.3.2
Test purpose:	To evaluate the splitter return impedance at 25 Hz and 50 Hz when tested with the test parameters as given in the related standards
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

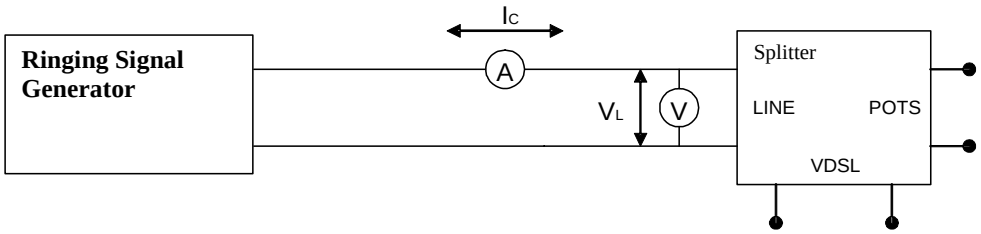


Figure 11: Test Set-up for impedance measurements at the LINE port

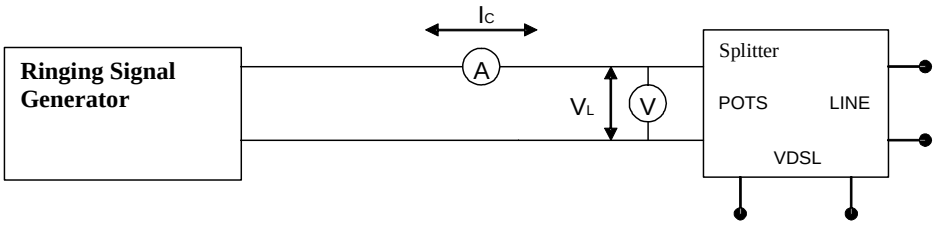


Figure 12: Test Set-up for impedance measurements at the POTS port

NOTE: Figure 12 requires that there is DC feeding of the splitter from the POTS port. If the splitter is sensitive to which port is power fed, feeding has to be done via the LINE port. A holding circuit is to be used to inject the test signal at the POTS port in that situation.

Test parameters:

Table 14

Parameter	Value
Level of the test signal	25 Hz at 60 Vrms superimposed on 60 VDC 50 Hz at 60 Vrms superimposed on 60 VDC
Termination at VDSL port	no VDSL load

Test matrix:

Table 15

	TS 101 952-2-1 [2]	Essential tests	Optional tests
25 Hz at 60 Vrms, 60 VDC, LINE port	X	X	
25 Hz at 60 Vrms, 60 VDC, POTS port	X	X	
50 Hz at 60 Vrms, 60 VDC, LINE port	X	X	
50 Hz at 60 Vrms, 60 VDC, POTS port	X	X	
Number of tests	4 tests	4 tests	

Test procedure notes:

- Ringing Impedance Circuit:
  - Configure the circuit as per figure 11 (for LINE Port test) or figure 12 (for POTS Port test) as required.
  - For each test case, set the ringing signal at the signal generator in accordance with the Test Parameters.
  - Measure the current $\boldsymbol{I}_C$ and the voltage $\boldsymbol{V}_L$ dropped across the splitter port under test.
- Ringing impedance is calculated thus:

$$R_L = \frac{V_L}{I_C}$$

Test results:

Table 16

	Ringing impedance (kΩ)
25 Hz ringing signal at Line port	
50 Hz ringing signal at Line port	
25 Hz ringing signal at POTS port	
50 Hz ringing signal at POTS port	

Measuring notes:

See general notes.

6.2.3 Tests for total harmonic distortion at 25 Hz and 50 Hz

Table 17

Test case name:	Total Harmonic Distortion at 25 Hz and 50 Hz
Reference:	TS 101 952-2-1 [2], clause 6.3.3
Test purpose:	To evaluate the splitters ability to transfer ringing signals without significant distortion
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

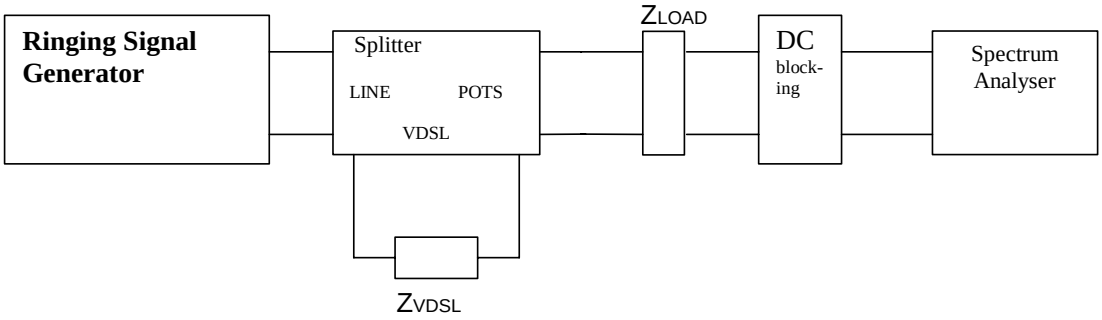


Figure 13: Test set-up for total harmonic distortion measurements

Test parameters:

Table 18

Parameter	Value
Frequency of the test signal	25 Hz 50 Hz
Amplitude of the test signal	100 Vrms superimposed on 50 VDC 50 Vrms superimposed on 78 VDC
Source impedance Z_{SOURCE}	850 Ω resistive
Load impedance Z_{LOAD}	2,7 kΩ + 2,2µF for 25 Hz 2,7 kΩ + 1,0µF for 50 Hz
VDSL termination	ZVDSL open circuit

Test matrix:

Table 19

	TS 101 952-2-1 [2]	Essential tests	Optional tests
25 Hz signal frequency **50 Hz signal frequency**	X X	X X	
100 Vrms superimposed on 50 VDC **50 Vrms superimposed on 78 VDC**	X X	X X	
Termination at VDSL port: ZVDSL **Termination at VDSL port: open circuit**	X X	X X	
Number of tests	8 tests	8 tests	

Test procedure notes:

NOTE 1: The total harmonic distortion of the test set-up should be less or equal to 2 %.

NOTE 2: For each test case, measure the spectral amplitude in Vrms of the fundamental (ringing) frequency $U0$ and all the harmonic frequencies, Un up to the fifth harmonic, across the load impedance $ZLOAD$.

The harmonic distortion expressed as a percentage is calculated as follows:

$$\%\ \text{Total Harmonic Distortion}\ (THD) = \frac{\sqrt{(U_1)^2 + (U_2)^2 + (U_3)^2 + ...(U_n)^2}}{\sqrt{(U_0)^2 + (U_1)^2 + (U_2)^2 + (U_3)^2 + ...(U_n)^2}} \times 100$$

Where terms $U1$ to Un are the levels of the harmonic frequencies and term $U0$ is the level of the fundamental (ringing signal) frequency.

Test results:

Table 20

Ringing signal amplitude	Ringing frequency	
	25 Hz	50 Hz
100 Vrms + 50 VDC THD (%)		
50 Vrms + 78 VDC THD (%)		

Measuring notes:

NOTE 3: This test requires as a very pure signal source. This has to be considered when setting up the test. Note that most standard signal generators do not provide sufficiently pure sinusoidal signals for the purpose of this test. Furthermore, operational amplifiers often cause significant distortion in achieving the test levels required.

NOTE 4: Assuming standard terminal equipment it is not expected that distortion of the ringing signal do cause any problem to the TE.

See also General Notes.

6.3 Tests for pass band loss requirements (on-hook)

6.3.1 Tests for on-hook requirement for the case of high impedance injection

Table 21

Test case name:	On hook requirement for the case of high impedance injection
Reference:	TS 101 952-2-1 [2], clause 6.4.1
Test purpose:	To evaluate the magnitude of voltage gain of the splitter in the range 200 Hz to 2 800 Hz for the on-hook case with high impedance injection
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

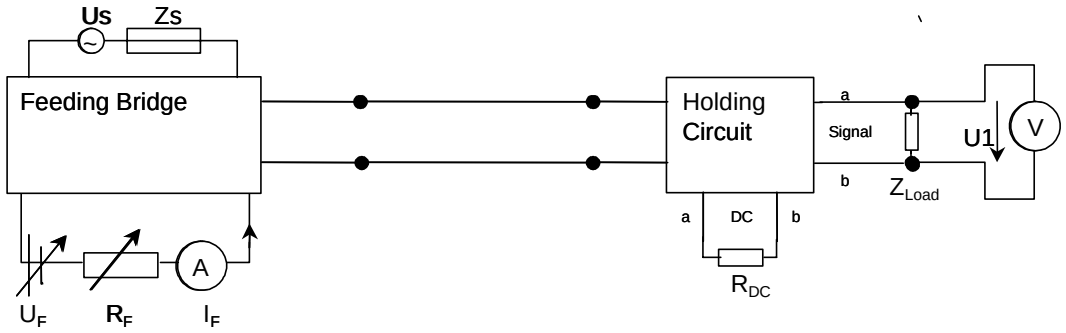


Figure 14: Test set-up for measurement calibration

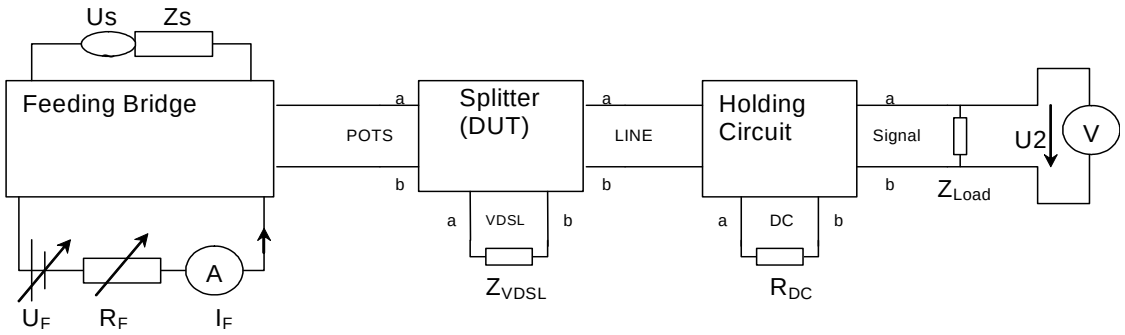


Figure 15: Test set-up for voltage gain measurements for LE splitters

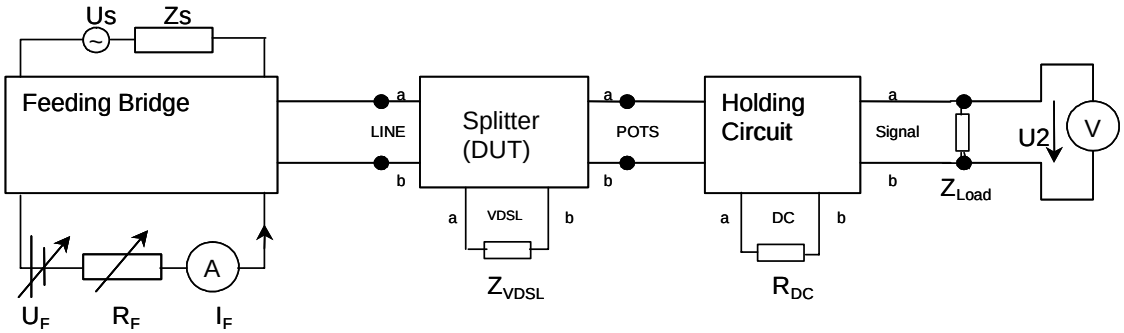


Figure 16: Test set-up for voltage gain measurements for TE splitters

Test parameters:

Table 22

Parameter	Value
Level of the test signal U_S	-4 dBV emf
Frequency of the test signal	200 Hz to 2 800 Hz
Feeding voltage U_F	50 V DC - 50 V DC
Feeding current I_F	0,4 mA (R_{DC} to be adjusted accordingly) 2,5 mA (R_{DC} to be adjusted accordingly)
Impedance of the signal source Z_S	Z_R
Impedance of the load Z_{LOAD}	Z_{ON}
VDSL termination	Z_{VDSL} open circuit
Direction of transmission	passive splitters: LINE - POTS passive splitters with current/voltage detection: LINE - POTS active splitters: LINE - POTS and POTS - LINE

Test matrix:

Table 23

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal U_S: -4 dBV emf	X	X	
Frequency range: 200 Hz to 2 800 Hz	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 0,4 mA	X	X	
Feeding current I_F: 2,5 mA	X	X	
Polarity of the DC feeding	alternating	alternating	
Termination at VDSL port: ZVDSL	X	X	
Termination at VDSL port: open circuit	X	X	
Direction LINE - POTS	X	X	
Direction POTS - LINE	(for active splitters only)	(for active splitters only)	
Number of tests	4 tests for passive splitters and 8 tests for active splitters	4 tests for passive splitters and 8 tests for active splitters	

Test procedure notes:

NOTE 1: Polarity of the feeding voltage and with this the direction of the feeding current should not impact the insertion loss of splitters.

NOTE 2: For passive splitters and for passive splitters with current/voltage detection it is sufficient to measure insertion loss in one direction (LINE to POTS or POTS to LINE). Differences in the insertion loss in the two directions might be visible due to differences in the impedance matching, however, this will anyhow be seen in the return loss measurement. For active splitters it is necessary to measure both directions.

NOTE 3: When verifying the test set-up, a verification measurement should not just be taken with 0 Ω, but also with a resistor which leads to an insertion loss of about 1 dB.

NOTE 4: If necessary, the feeding voltage can be increased to achieve the specified feeding current.

NOTE 5: The feeding conditions for active splitters and for passive splitters with current/voltage detection need to be determined and are for further study.

NOTE 6: It need to be clarified, if a specific signal (e.g. ringing signal) must be sent to the device under test before performing on-hook tests on active splitters or passive splitters with current/voltage detection.

NOTE 7: For active and for passive splitters it is sufficient to measure at the lowest and the highest specified current for on-hook condition.

Test results:

Test Result should be recorded in dB, where: VG = 20 lg (U2/U1), where U2 is the voltage observed when the splitter is connected as in Test set-up and where U1 is the voltage observed when the splitter is replaced by a direct wire connection of less than 0,01 Ω.

6.3.2 Tests for on-hook requirement for the case of low impedance injection

Table 24

Test case name:	On hook requirement for the case of low impedance injection
Reference:	TS 101 952-2-1 [2], clause 6.4.2
Test purpose:	To evaluate the insertion loss and the insertion loss distortion of the splitter in the range 200 Hz to 2 800 Hz for the on-hook case with low impedance injection
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

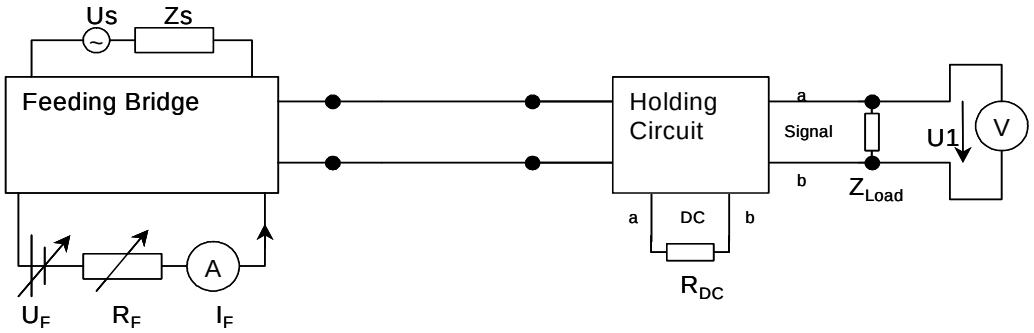


Figure 17: Test set-up for measurement calibration

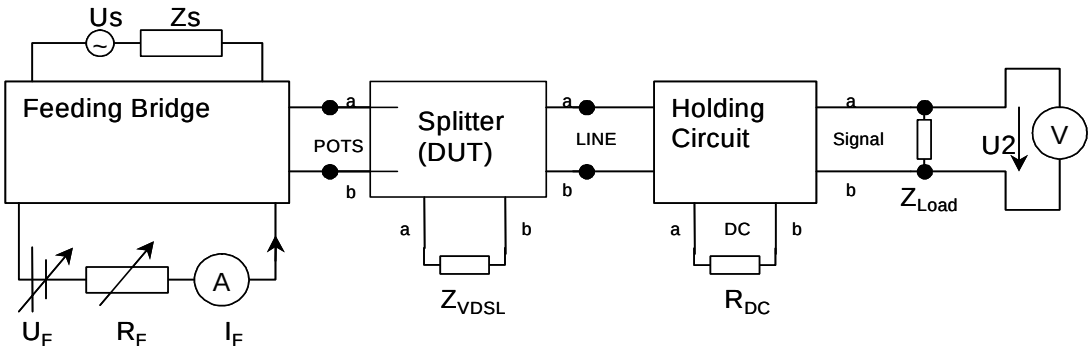


Figure 18: Test set-up for voltage gain measurements for LE splitters

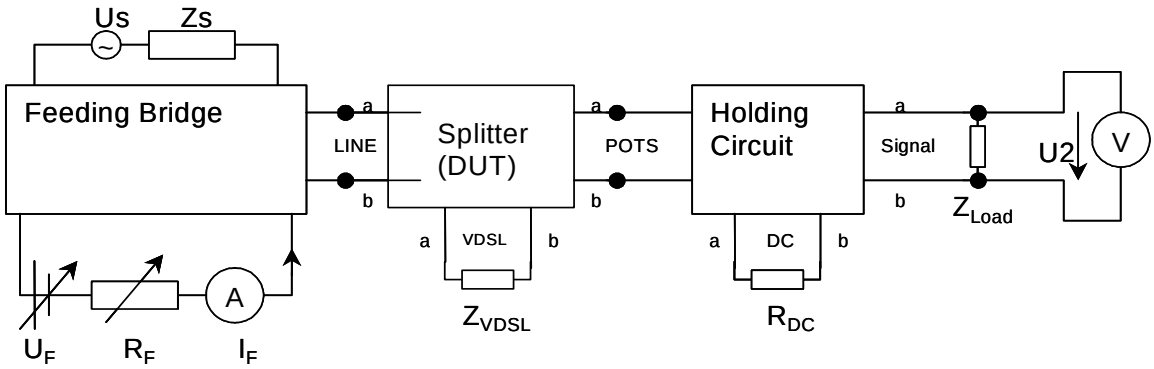


Figure 19: Test set-up for voltage gain measurements for TE splitters

Test parameters:

Table 25

Parameter	Value
Level of the test signal U_S	-4 dBVemf
Frequency of the test signal	1 000 Hz (for insertion loss) 200 Hz to 2 800 Hz (for insertion loss distortion)
Feeding voltage U_F	50 VDC - 50 VDC
Feeding current I_F	0,4 mA (R_{DC} to be adjusted accordingly) 2,5 mA (R_{DC} to be adjusted accordingly)
Impedance of the signal source	600 Ω
Impedance of the load	600 Ω
VDSL termination	Z_{VDSL} open circuit
Direction of transmission	passive splitters: LINE - POTS passive splitters with current/voltage detection: LINE - POTS active splitters: LINE - POTS and POTS - LINE

Test matrix:

Table 26

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal U_S: -4 dBV emf	X	X	
Frequency of the test signal: 1 kHz **Frequency range: 200 Hz to 2 800 Hz (for distortion measurement)**	X X	X X	
Feeding voltage $U_{F:}$ 50 VDC	X	X	
Feeding current $I_{F:}$ 0,4 mA **Feeding current $I_{F:}$ 2,5 mA**	X X	X X	
Polarity of the DC feeding	alternating	alternating	
Termination at VDSL port: ZVDSL **Termination at VDSL port: open circuit**	X X	X X	
Direction LINE - POTS **Direction POTS - LINE**	X (for active splitters only)	X (for active splitters only)	
Number of tests	8 tests for passive splitters and 16 tests for active splitters	8 tests for passive splitters and 16 tests for active splitters	

Test procedure notes:

NOTE 1: Polarity of the feeding voltage and with this the direction of the feeding current should not impact the insertion loss of splitters.

NOTE 2: For passive splitters and for passive splitters with current/voltage detection it is sufficient to measure insertion loss in one direction (LINE to POTS or POTS to LINE). Differences in the insertion loss in the two directions might be visible due to differences in the impedance matching, however, this will anyhow be seen in the return loss measurement. For active splitters it is necessary to measure both directions.

NOTE 3: When verifying the test set-up, a verification measurement should not just be taken with 0 Ω, but also with a resistor which leads to an insertion loss of about 1 dB. For a 600 Ω source/load impedance, a simple way to set-up such an attenuation is by inserting 2×75 Ω resistors instead of the DUT.

NOTE 4: If necessary, the feeding voltage can be increased to achieve the specified feeding current.

NOTE 5: The feeding conditions for active splitters and for passive splitters with current/voltage detection need to be determined and are for further study.

NOTE 6: It need to be clarified, if a specific signal (e.g. ringing signal) must be sent to the device under test before performing on-hook tests on active splitters or passive splitters with current/voltage detection.

NOTE 7: For active and for passive splitters it is sufficient to measure at the lowest and the highest specified current for on-hook condition.

Test results:

Test Result should be recorded in dB, where: IL = 20 lg (U1/U2), where U2 is the voltage observed when the splitter is connected as in Test set-up and where U1 is the voltage observed when the splitter is replaced by a direct wire connection of less than 0,01 Ω.

6.4 Tests for pass band loss requirements (off-hook)

6.4.1 Tests for off-hook pass band insertion loss

NOTE: To maintain the same structure as in TS 101 952-2-1 [2] this clause has been added. However, it will be kept empty as the tests for off-hook pass band insertion loss are covered by the tests for off-hook pass band insertion loss distortion.

6.4.2 Tests for off-hook pass band insertion loss distortion

Table 27

Test case name:	Off-hook pass band insertion loss and insertion loss distortion
Reference:	TS 101 952-2-1 [2], clauses 6.5.1 and 6.5.2
Test purpose:	To evaluate the insertion loss in the off-hook case
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

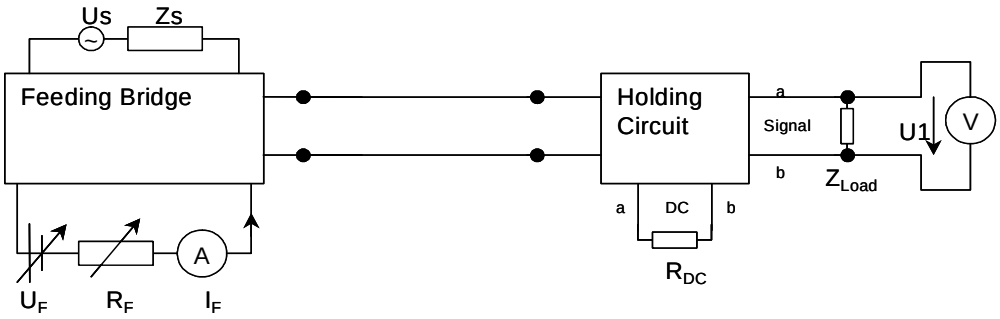


Figure 20: Test set-up for measurement calibration

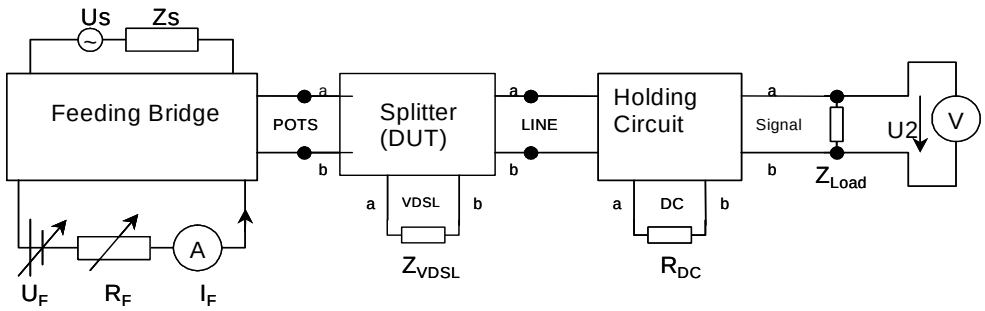


Figure 21: Test set-up for insertion loss measurements for LE splitters

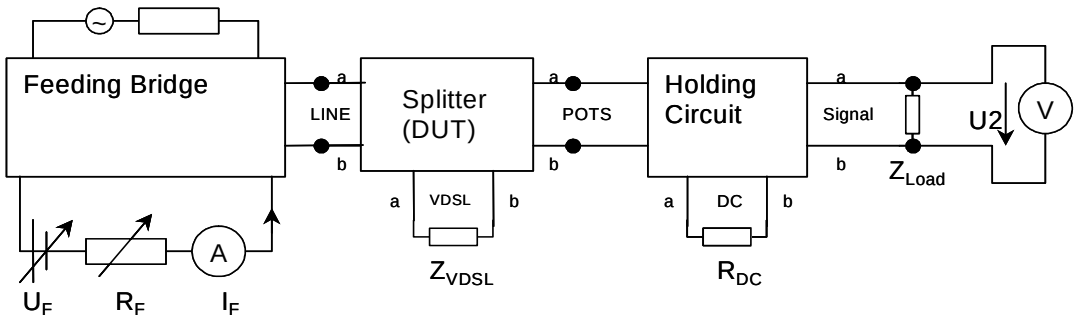


Figure 22: Test set-up for insertion loss measurements for TE splitters

Test parameters:

Table 28

Parameter	Value
Level of the test signal U_S	-4 dBV emf
Frequency of the test signal	1000 Hz (for insertion loss) 200 Hz to 4 000 Hz (for insertion loss distortion)
Feeding voltage U_F	50 V_{DC} -50 V_{DC}
Feeding current I_F	13 mA (R_{DC} and Rf to be adjusted accordingly) 80 mA (R_{DC} and Rf to be adjusted accordingly)
Impedance combinations	combination 1: source impedance: Z_R; load impedance: Z_R combination 2: source impedance: 600 Ω; load impedance: 600 Ω
VDSL termination	Z_{VDSL} open circuit
Direction of transmission	passive splitters: LINE - POTS passive splitters with current/voltage detection: LINE - POTS active splitters: LINE - POTS and POTS - LINE

Test matrix:

Table 29

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal U_S: -4 dBV emf	X	X	
Frequency of the test signal: 1 kHz **Frequency range: 200 Hz to 4 000 Hz (for distortion measurement)**	X X	X X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 13 mA **Feeding current I_F: 80 mA**	X X	X X	
Impedance combination 1 **Impedance combination 2**	X X	X X	
Polarity of the DC feeding	alternating	alternating	
Termination at VDSL port: Z_{VDSL} **Termination at VDSL port: open circuit**	X X	X X	
Direction LINE - POTS **Direction POTS - LINE**	X (for active splitters only)	X (for active splitters only)	
Number of tests	16 tests for passive splitters and 32 tests for active splitters	16 tests for passive splitters and 32 tests for active splitters	

Test procedure notes:

NOTE 1: Polarity of the feeding voltage and with this the direction of the feeding current should not impact the insertion loss of splitters.

NOTE 2: For passive splitters and for passive splitters with current/voltage detection it is sufficient to measure insertion loss in one direction (LINE to POTS or POTS to LINE). Differences in the insertion loss in the two directions might be visible due to differences in the impedance matching, however, this will anyhow be seen in the return loss measurement. For active splitters it is necessary to measure both directions.

NOTE 3: When verifying the test set-up, a verification measurement should not just be taken with 0 Ω, but also with a resistor which leads to an insertion loss of about 1 dB. For a 600 Ω source/load impedance, a simple way to set-up such an attenuation is by inserting 2×75 Ω resistors instead of the DUT.

NOTE 4: If necessary, the feeding voltage can be increased to achieve the specified feeding current.

NOTE 5: The feeding conditions for active splitters and for passive splitters with current/voltage detection need to be determined and are for further study.

NOTE 6: For active and for passive splitters it is sufficient to measure at the lowest and the highest specified current for off-hook condition.

Test results:

Test Result should be recorded in dB, where: IL = 20 lg (U1/U2), where U2 is the voltage observed when the splitter is connected as in Test set-up and where U1 is the voltage observed when the splitter is replaced by a direct wire connection of less than 0,01 Ω.

When reporting the insertion loss distortion (200 Hz to 4 000 Hz) the absolute difference of the insertion loss at any frequency and the insertion loss at 1 kHz shall be evaluated. The insertion loss distortion equals:

$$ild = 20\lg(\frac{U_{2(1kHz)}}{U_{2(f)}}) = 20\lg(\frac{U_{1(f)}}{U_{2(f)}}) - 20\lg(\frac{U_{1(1kHz)}}{U_{2(1kHz)}}) = il(f) - il(1kHz)$$

Measuring notes:

See general notes.

6.5 Tests for return loss requirements

6.5.1 Tests for return loss requirements options A and B

Table 30

Test case name:	Return Loss Requirements for option A and B
Reference:	TS 101 952-2-1 [2], clause 6.6
Test purpose:	To evaluate the splitter return loss when tested with the test parameters as given in the related standards
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

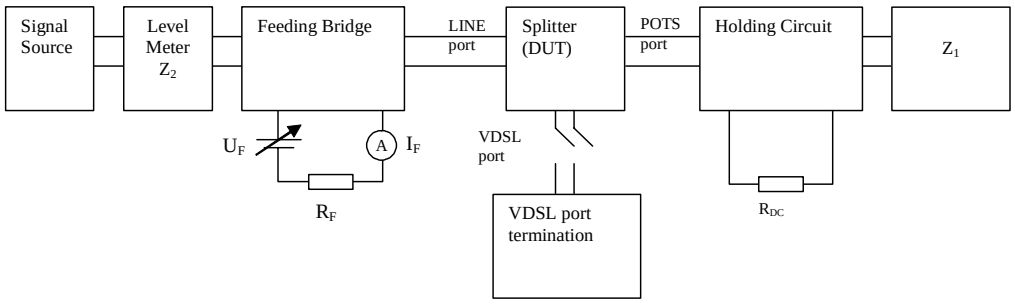


Figure 23: Test set-up for return loss testing on a splitter (at the line port)

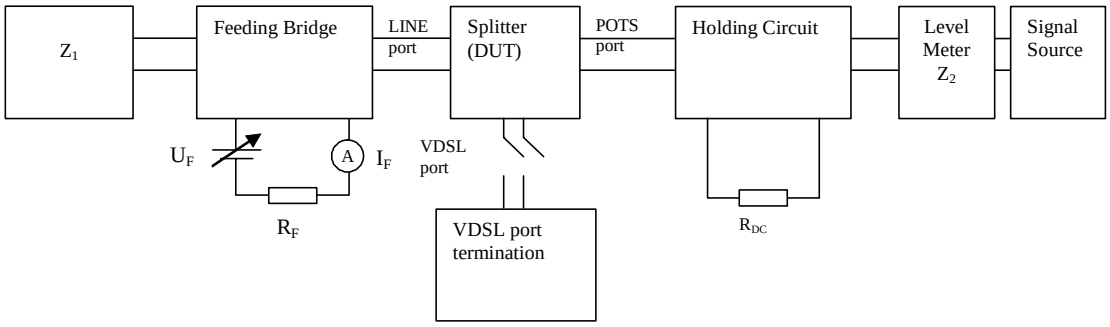


Figure 24: Test set-up for return loss testing on a splitter (at the POTS port)

Test parameters:

Table 31

Parameter	Value
Level of test signal	-10 dBV
Frequency range of test signal	300 Hz to 4 000 Hz
Combination of port and load impedances	Option A combination 1: Z_R / LINE Port test combination 2: Z_R / POTS Port test combination 3: Z_{SL} / LINE Port test combination 4: Z_{SL} / POTS Port test Option B combination 1: Z_R / LINE Port test combination 2: Z_R / POTS Port test
Termination at VDSL port	VDSL load = Z_{VDSL} VDSL load = open circuit
Feeding voltage U_F	+50 V_{DC} -50 V_{DC}
Load resistance R_{DC}	470 Ω in off-hook state
DC feeding current I_F in off-hook state	I_{DC} = 13 mA I_{DC} = 80 mA (see note)
NOTE: These values of DC current are set by adjusting the values of the external circuitry (namely U_F, R_F and R_{DC}) shown in figures 23 and 24. For the return loss only DC for off-hook cases need to be considered according to TS 101 952-2-1 [2], clause 6.6.	

Test matrix:

Table 32

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal: -10 dBm	X	X	
Frequency range: 300 Hz to 4 000 Hz	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Impedance of a splitter (Option A)			
combination A1: Z_R / LINE Port test	X	X	
combination A2: Z_R / POTS Port test	X	X	
combination A3: Z_{SL} / LINE Port test	X	X	
combination A4: Z_{SL} / POTS Port test	X	X	
Impedance of a splitter (Option B)			
combination B1: Z_R / LINE Port test	X	X	
combination B2: Z_R / POTS Port test	X	X	
Polarity of the DC feeding	alternating	alternating	
Termination at VDSL port: Z_{VDSL}	X	X	
Termination at VDSL port: open circuit	X	X	
Number of tests (Option A) **(Option B)**	16 tests 8 tests	16 tests 8 tests	

Test procedure notes:

None.

Test result:

Test result should be the return loss following the definition:

$$R_L = 20 \lg \frac{|Z_1 + Z_2|}{|Z_1 - Z_2|}$$

Measuring notes:

NOTE 1: The reduction of line feeding currents to just 13 mA and 80 mA has shown to be appropriate as no significant differences were evident between the various current results.

NOTE 2: Positive and negative feed voltages produced no significant differences in the return loss results. However, it is suggested that the positive/negative aspect of the test should still be present. Consequently, it is recommended that the results are measured with half of the tests performed with +50 V and the remaining half performed with -50 V (alternating polarity).

6.6 Tests for requirements relating to metering pulses

6.6.1 Tests for requirements relating to metering pulses at 12 kHz or 16 kHz

Table 33

Test case name:	Requirements relating to metering pulses at 12 kHz or 16 kHz
Reference:	TS 101 952-2-1 [2], clauses 6.5.1 and 6.5.2
Test purpose:	To evaluate the insertion loss in the off-hook case
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

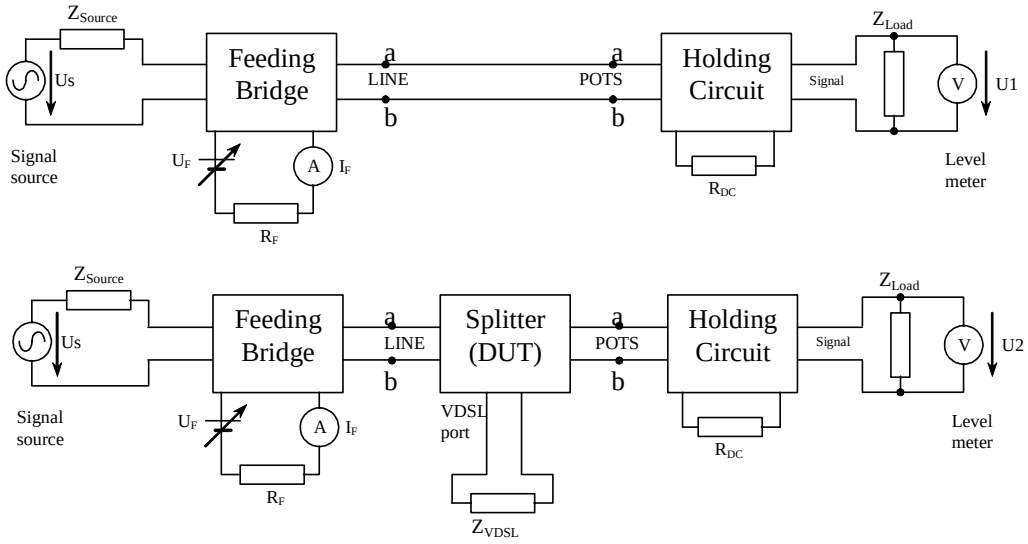


Figure 25: Test set-up for insertion loss measurements at splitters

Test parameters:

Table 34

Parameter	Value
Level of the test signal U_S	3,53 Vrms
Frequency of the test signal U_S	12 kHz ± 1 % 16 kHz ± 1 %
Feeding current I_F	13 mA 80 mA (see note)
Direction of current I_F	Alternating
Source impedance Z_{SOURCE}	200 Ω
Load impedance Z_{LOAD}	200 Ω
Termination at V_{DSL} port	Z_{VDSL} open circuit
Feeding voltage U_F	50 V_{DC}
NOTE: The values of I_F are set by adjusting the values of the external circuitry (U_F, R_F and R_{DC}).	

Test matrix:

Table 35

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal U_S: 3,53 Vrms	X		X
Feeding voltage U_F: 50 VDC	X		X
Feeding current I_F: 13 mA	X		X
Feeding current I_F: 80 mA	X		X
Source impedance Z_{SOURCE}: 200 Ω	X		X
Load impedance Z_{LOAD}: 200 Ω	X		X
Polarity of the DC feeding	alternating		alternating
Termination at V_{DSL} port: Z_{VDSL}	X		X
Termination at V_{DSL} port: open circuit	X		X
Number of tests	8 tests	none	8 tests

Test procedure notes:

NOTE 1: The test frequency of 12 kHz or 16 kHz is dependent on the network operator specific requirement.

NOTE 2: Polarity of the feeding voltage and with this the direction of the feeding current does not impact the insertion loss of splitters.

NOTE 3: Polarity of the feeding voltage and with this the direction of the feeding current may impact the additional insertion loss caused by feeding bridge and holding circuit. A calibration/normalization measurement need to be taken before each single measurement step.

NOTE 4: It is sufficient to measure insertion loss in one direction as metering pulses are transmitted from LE to NTP only. Hence, insertion loss shall be measured from POTS port to LINE port for LE splitters and from LINE port to POTS port for TE splitters.

NOTE 5: A test case verification measurement should be taken using a flat attenuation leading to an insertion loss of about 3 dB. A simple way to set-up such an attenuation is by adding 165 Ω instead of the unit under test.

NOTE 6: If necessary, the feeding voltage can be increased to achieve the specified feeding current.

NOTE 7: The feeding conditions for active splitters and for passive splitters with current/voltage detection need to be determined.

NOTE 8: There is a recognizable difference (about 0,5 dB) in the test result when measuring with and without Z_{VDSL}. Both conditions are likely to occur in real life as modems do change their input impedance when switched off. Both conditions with and without Z_{VDSL} should be tested.

Test results:

Test result shall be recorded in dB, where $I_L = 20 \log (U1/U2)$, where U2 is the voltage observed when the splitter is connected as in Test set-up and where U1 is the voltage observed when the splitter is replaced by a direct wire connection of less than 0,01 Ω.

Table 36

Frequency (kHz)	Maximum Insertion loss (dB)
12 ± 1 % or 16 ± 1 %	

Measuring Notes:

See general notes.

6.7 Tests for unbalance about earth

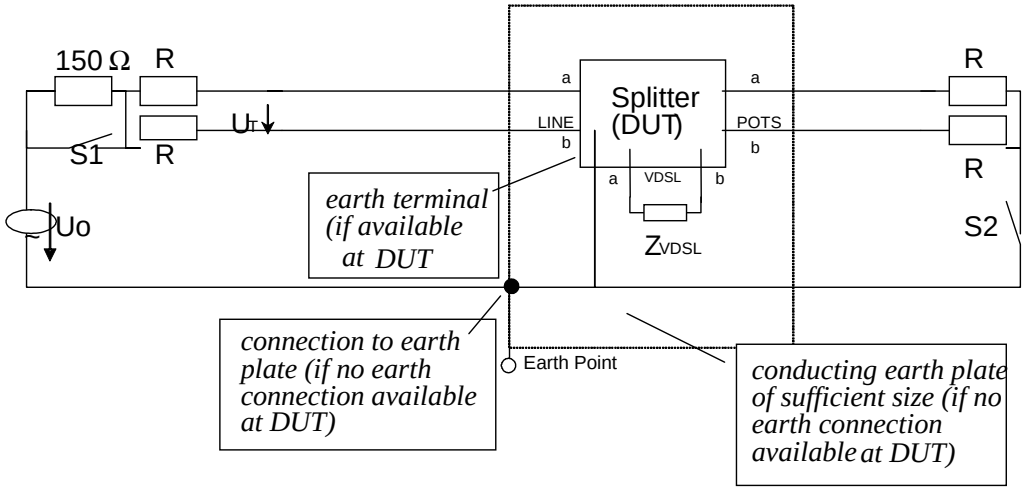
TS 101 952-2-1 [2] requires the unbalance about earth to be measured up to 12 MHz under the application of DC feeding. Applying a feeding bridge and a holding circuit to an unbalance test set-up means a significant impact to the set-up´s balance about earth, especially at higher frequencies. However, the evaluation of the unbalance of splitters should be done with a DC feeding applied, as the impedance of splitter components might vary upon the feeding current. To achieve both a valid LCL/LCTL test result as well as a prove of the splitters behaviour under the influence of the DC current it is recommended by STF 248 to test this characteristic in two steps (see clauses 6.7.1 and 6.7.2).

6.7.1 Tests for the unbalance about earth (LCL/LCTL) without feeding

Table 37

Test case name:	Unbalance about earth without feeding
Reference:	TS 101 952-2-1 [2], clause 6.8.1
Test purpose:	To evaluate the longitudinal conversion (transfer) loss of a splitter when no feeding is applied
Test configuration:	See Test Set-up; DUT not configured

Test set-up:



NOTE: Special care need to be taken to achieve a test set-up of sufficient balance about earth. It is highly recommended to perform a calibration/normalization measurement before the test where the balance of the test set-up without DUT (DUT replaced by straight connection between feeding bridge and holding circuit).

Figure 26: Test set-up for measuring LCL/LCTL at splitters

Test parameters:

Table 38

Parameter	Value
Level of the test signal U_O	-10 dBm
Frequency of the test signal U_O	frequency range 1: 50 Hz to 4 kHz frequency range 2: 4 kHz to 12 MHz
Combination of source and load impedances	combination 1: R = 600 Ω/2 = 300 Ω; combination 2: R = 50 Ω (see notes 1 and 2)
Status of S1	open closed
Status of S2	open closed
Termination at VDSL port	Z_{VDSL} (see note)
Feeding voltage/current	no feeding applied

NOTE 1: Currently there are some tendencies to change the VDSL termination impedance. This could also have an effect to the further impedances and resistors given in this figure. It is highly recommended to carefully check the actual values with the then-current TS 101 952-2-1 [2] or its succeeding document when performing the tests.

NOTE 2: R is in principle half the value of the resistive part of ZVDSL at very high frequencies.

Test matrix:

Table 39

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal U_O: - 10 dBm	X	X	
Frequency range of the test signal: 50 Hz to 4 kHz 4 kHz to 12 MHz	 X X	 X X	
Impedance combination 1 **Impedance combination 2**	X X	X X	
S1 open **S1 closed**	X X	X X	
S2 open **S2 closed**	X X	X X	
measured at POTS port **measured at LINE port**	X X	X X	
Termination at VDSL port: Z_{VDSL}	X	X	
Number of tests	3 tests	3 tests	

Test procedure notes:

There is a study point pending at ETSI TM6 on the question, if a measurement with a middle-earthened termination at the LINE or POTS port respectively (LCTL measurement) is appropriate.

Test results:

Test Result shall be recorded in dB, where: unbalance = 20 lg (Uo/U_T), where Uo is the longitudinal voltage fed in by the generator and where U_T is the differential voltage observed at the input of the DUT.

Measuring Notes:

Special care need to be taken to achieve a test set-up of sufficient balance about earth. It is highly recommended to perform a calibration/normalization measurement before the test where the balance of the test set-up without DUT (DUT replaced by straight connection between feeding bridge and holding circuit). See also general notes.

6.7.2 Tests for the unbalance about earth with DC feeding on basis of the branch impedances

Table 40

Test case name:	Unbalance about earth; comparison of branch impedances
Reference:	TS 101 952-2-1 [2], clause 6.8.1
Test purpose:	To evaluate the unbalance of the splitter by comparing the branch impedances of the splitter under application of a DC feeding
Test configuration:	See Test Set-up; DUT not configured

Background information:

Testing the unbalance about earth using the LCTL test method as described in ITU-T Recommendation O.9 [7] when also feeding bridges and/or holding circuits are connected to the test set-up is not easy, as commonly available feeding bridges and holding circuits are specified for voice frequencies. While the insertion loss is still acceptable at higher frequencies, a sufficient balance about earth cannot be guaranteed. The dynamic range of a measurement with feeding bridge and holding circuit is unlikely to be high enough to prove a balance of about 30 dB at high frequencies.

Therefore, this test case investigates that part of the splitters behaviour that is mainly responsible for an unbalance about earth.

Measurements using the LCL method show, that the layout of splitters usually has a good balance about earth. However, as soon as the LCTL method is used (the termination at the non-measured port is built up as a symmetrical termination having an earth connection at the "middle" point) one observes significant variations in the test result, which cannot be caused by the splitter layout. Reason for this behaviour is the tolerance of the splitter components in the a-wire and b-wire. As soon as a component in the a-wire behaves different to its counterpart in the b-wire, there will be a significant impact to the LCTL result. Especially when a DC current is applied, the variances in the branch impedance can be significant because of loading effects in the inductances. Therefore an alternative test method is proposed in this clause.

The principle of this test lies in the comparison of the two branches' impedance over frequency for different DC currents. Validation tests of STF 248 have shown that this approach is valid. However, currently there is no requirement defined in TS 101 952-2-1 [2] which could easily be transferred to this method. Nevertheless, this test is proposed in conjunction with the request to the responsible technical body (ETSI AT) to work out a related requirement.

Having in mind the test set-up for the LCTL measurement in combination with the investigation of the branch impedances, one could imagine calculating the LCTL from the information gained in this test. However, STF 248 does recommend to create a new type of requirement.

Test set-up:

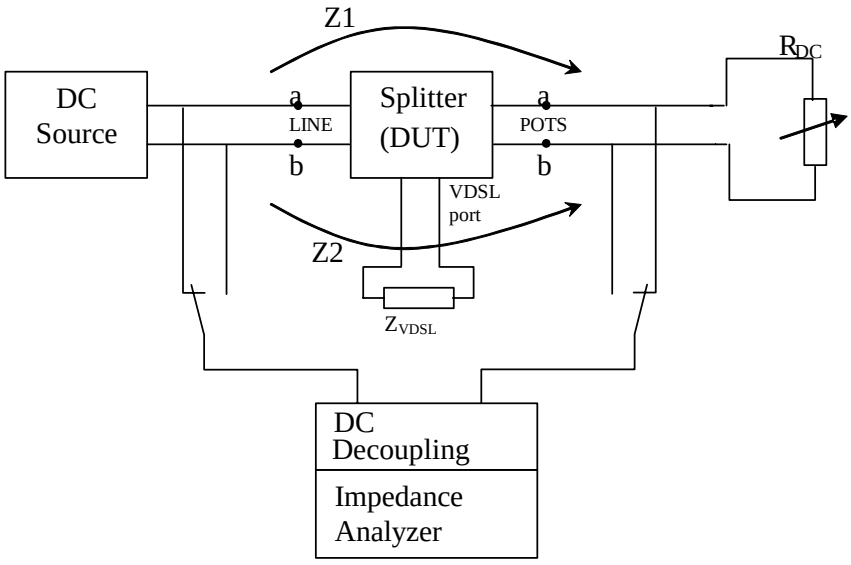


Figure 27: Test set-up for impedance comparison measurements

Test parameters:

Table 41

Parameter	Value
Frequency of the test signal Us	frequency range 1: 50 Hz to 4 kHz frequency range 2: 4 kHz to 12 MHz
Termination at VDSL port	Z_{VDSL} (see note 1)
Feeding voltage U_F	100 V
Feeding current I_F	13 mA 80 mA (see note 2)
Impedances to be measured	Z1 Z2
Polarity of feeding voltage/current	normal (the polarity of the feeding voltage must not be changed between two measurements (Z1 and Z2) which belong together).
NOTE 1: Currently there are some tendencies to change the VDSL termination impedance. This could also have an effect to the further impedances and resistors given in this figure. It is highly recommended to carefully check the actual values with the then-current TS 101 952-2-1 [2] or its succeeding document when performing the tests. NOTE 2: The feeding current is to be adjusted by varying R_{DC}.	

Test matrix:

Table 42

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Frequency range of the test signal U_S:			
50 Hz to 4 kHz	X		X
4 kHz to 12 MHz	X		X
Impedance combination 1	X		X
Impedance combination 2	X		X
Feeding voltage U_F: 100 V	X		X
Feeding current I_F: 13 mA	X		X
Feeding current I_F: 80 mA	X		X
Polarity of feeding voltage: normal	X		X
Impedance to be measured: Z1 (a-wire)	X		X
Impedance to be measured: Z2 (b-wire)	X		X
Termination at VDSL port: Z_{VDSL}	X		X
Number of tests	4 tests		4 tests

Test procedure notes:

NOTE 1: Until a related requirement is formulated by ETSI AT this test case shall be seen as an optional test.

NOTE 2: It is required that the current in a-wire and b-wire are equal with respect to their level as there might be a common mode choke implemented in the splitter.

NOTE 3: When using a DC decoupling at the impedance analyzer the impact of that decoupling over frequency need to be compensated before performing any impedance measurement at the splitter.

Test results:

Resistance and phase of the two branch impedances shall be recorded. As long as there is no exact definition in TS 101 952-2-1 [2] or its succeeding document the two impedances should be compared graphically.

The following formula gives a measure to compare the measured impedance with the LCTL result this would mean when testing according to ITU-T Recommendation O.9 [7] and test case 6.7.1 of the present document. However, the accuracy of the impedance measurement must be carefully considered when entering this formula. This formula is for information an non-mandatory use. Under no circumstances it shall be seen as a decision of AT-a on a related splitter requirement.

$$\text{unbalance} = 20 \log ((Z1+2R) \times (Z2+2R)/(R \times (Z1-Z2)))$$

where:

- Z1 is the impedance measured at the a-wire.
- Z2 is the impedance measured at the b-wire.
- R is the terminating impedance R as shown is figure 26 of clause 6.7.1 (R = 300 Ω for frequency range 1 and R = 1/2 x (resistive part of ZVDSL at high frequencies) for frequency range 2).

Measuring Notes:

See general notes.

NOTE: It is recognized that there is a risk of a high degree of measurement uncertainty in both the old and proposed alternative test methods especially at high frequencies. Further study is recommended in this area.

6.8 Tests for VDSL band requirements

6.8.1 Tests for On-hook loss for VDSL over POTS splitters

Table 43

Test case name:	On-hook loss for VDSL over POTS splitters
Reference:	TS 101 952-2-1 [2], clause 6.9.1
Test purpose:	To evaluate the on-hook loss (voltage drop) of the splitter from LINE to POTS for signals in the VDSL frequency range
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

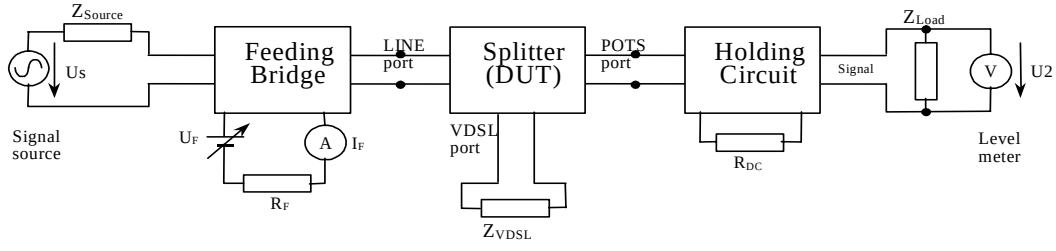


Figure 28: Test set-up for on-hook loss measurements

Test parameters:

Table 44

Parameter	Value
Level of the test signal U_S	-6 dBVemf provided at LINE port
Frequency range of the test signal	fL ... 12 MHz
Feeding voltage U_F	50 VDC
Feeding current I_F	0,4 mA 2,5 mA (see note)
Polarity of current I_F	Alternating
Load impedance Z_{Load}	Z_{ON}
Termination at VDSL port	Z_{VDSL}
DC resistance RDC	R_{DC} shall be adjusted to meet the 0,4 mA to 2,5 mA requirement R_{DC} = 20 kΩ to 125 kΩ
NOTE: The values of I_F are set by adjusting the values of the external circuitry as well as the DC load resistor (U_F, R_F and R_{DC}).	

Test matrix:

Table 45

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of test signal U_S: -6 dBV emf	X	X	
Impedance combinations combination 1: (Z_{load} = Z_{ON}, VDSL port = Z_{VDSL})	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 0,4 mA **Feeding current I_F: 2,5 mA**	X X	X X	
Polarity of the DC feeding	alternating	alternating	
Load impedance: Z_{ON}	X	X	
Termination at VDSL port: Z_{VDSL}	X	X	
Number of tests	2 tests	2 tests	

Test Procedure Notes:

Test Result:

The test result shall meet the requirement of TS 101 952, figure 14. The graph given in TS 101 952-2-1 [2] does not clearly specify the dimensions, further clarification required. A reasonable assumption is that the x-axis carries a logarithmic scaling for the frequency and the y-axis carries a linear scaling for the output voltage in dBV (meaning a logarithmic scaling for the output voltage in V).

Measuring Notes:

NOTE 1: The reduction of line feeding currents to just 0,4 mA and 2,5 mA has shown to be appropriate as no significant differences were evident between the various current results.

NOTE 2: Positive and negative feed voltages produced no significant differences in on-hook loss results. However, it is suggested that the positive / negative aspect of the test should still be present. Consequently, it is recommended that the results are measured with half of the tests performed with +50 V and the remaining half performed with -50 V (alternating polarity).

NOTE 3: The stability of the signal source over frequency need to be considered carefully when performing this tests. If the variation of the signal source voltage is too high over frequency a single step measurement is recommended, where the signal source voltage is adjusted to the specified value at each measurement step.

NOTE 4: Commonly available feeding bridges and holding circuits seem to be appropriate for performing this test, however, special care needs to be taken at higher frequencies (see also note 3).

6.8.2 Tests for Off-hook isolation

Table 46

Test case name:	Off-hook isolation
Reference:	TS 101 952-2-1 [2], clause 6.9.2
Test purpose:	To evaluate the isolation of the POTS port to VDSL signals and vice versa in the upper frequency range, when POTS is off-hook
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

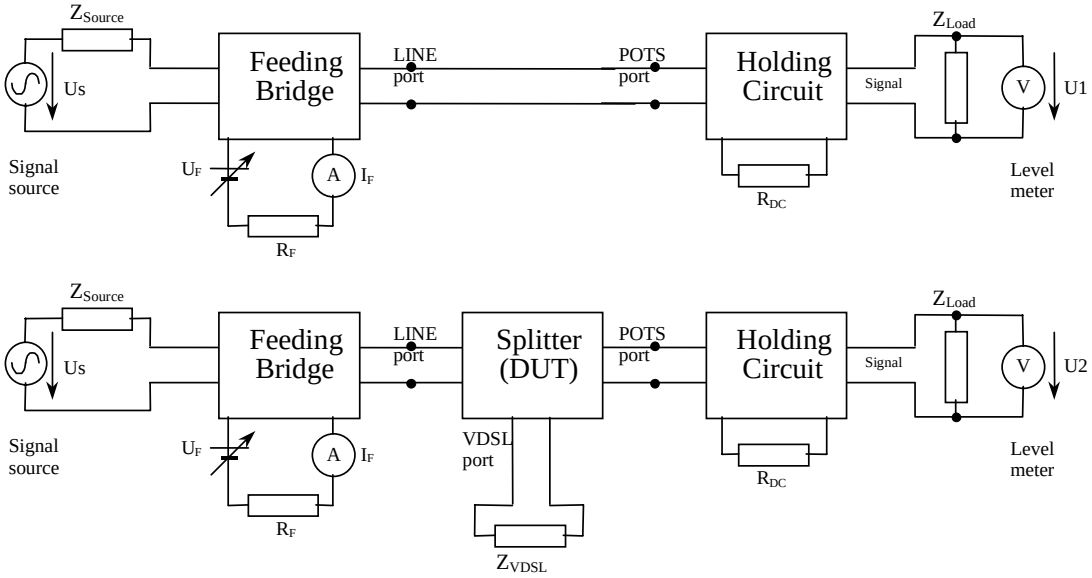


Figure 29: Test set-up for Isolation testing on a splitter from LINE port to POTS port

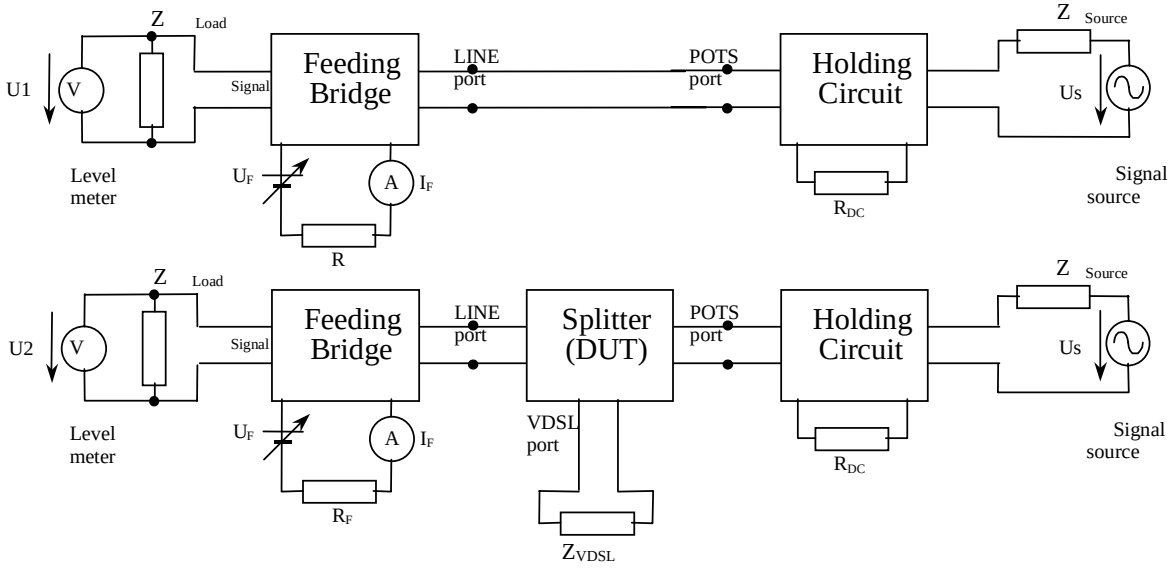
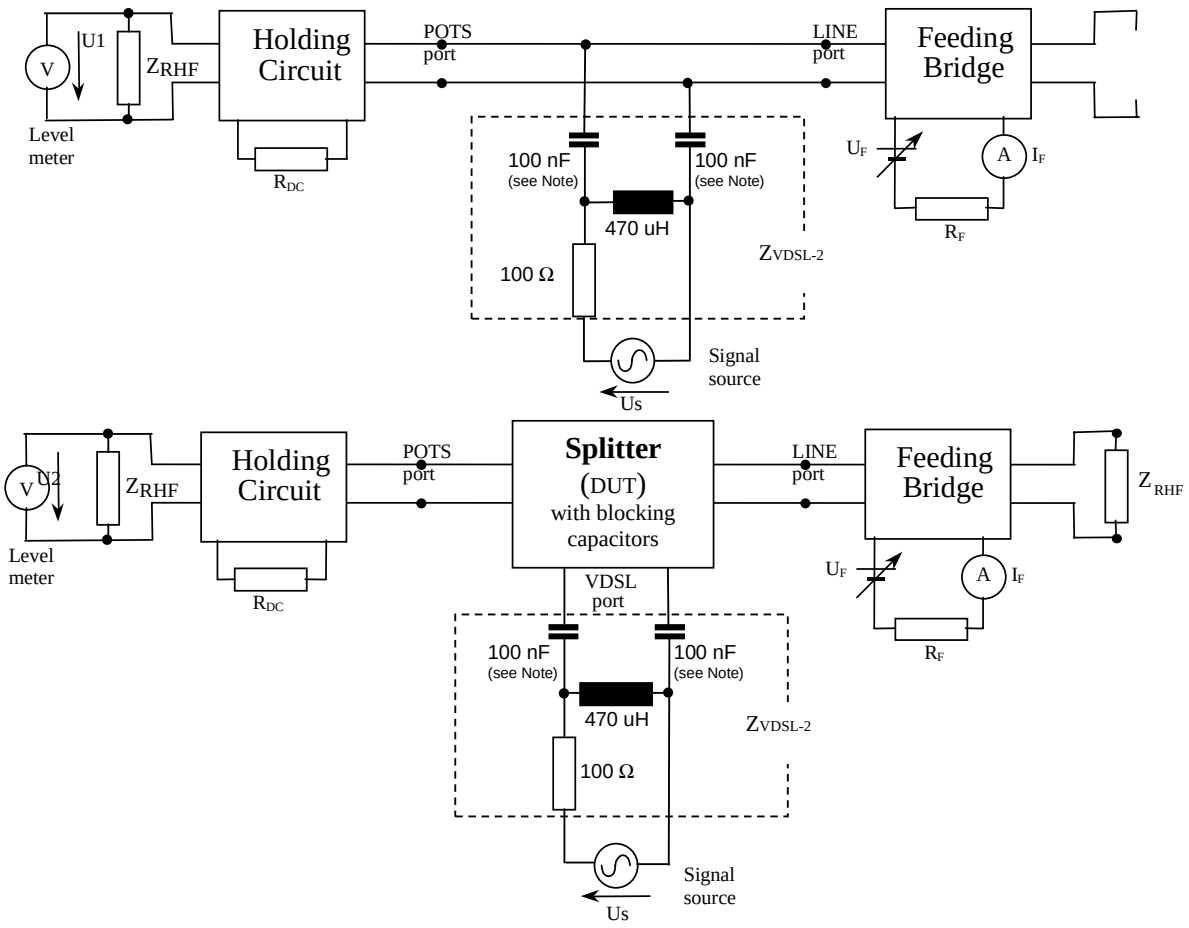


Figure 30: Test set-up for Isolation testing on a splitter from POTS port to LINE port



NOTE: The figure is given for testing a splitter with two blocking capacitors of 120 nF included. In cases where no blocking capacitors are implemented in the DUT, Z_{VDSL-1} is to be applied.

Z_{VDSL} is likely to be changed in co-operation between ETSI AT and ETSI TM6. The values given above reflect the current specification, however, when performing tests Z_{VDSL-1} and Z_{VDSL-2} shall be checked carefully with the then-current TS 101 952-2-1 [2] or its succeeding document.

Figure 31: Test set-up for isolation testing on a splitter from VDSL port to POTS port

Test parameters:

Table 47

Parameter	Value
Level of test signal U_S	-6 dBV emf
Frequency range of test signal	fL ... 12 MHz
Impedance combinations	combination 1 (used for LINE to POTS tests): LINE (source): Z_{RHF}; POTS (load): Z_{RHF}; VDSL: Z_{VDSL} combination 2 (used for POTS to LINE tests): LINE (load): Z_{RHF}; POTS (source): Z_{RHF}; VDSL: Z_{VDSL} combination 3: (used for VDSL to POTS tests): LINE: Z_{RHF}; POTS (load): Z_{RHF}; VDSL (source): Z_{VDSL} (see note 1)
Feeding voltage U_F	50 V_{DC}
DC load resistance R_{DC}	470 Ω
Feeding current I_F in off-hook state	13 mA 80 mA (see note 2)
NOTE 1: All source impedances shall be implemented symmetrically. NOTE 2: These values of DC current are set by adjusting the values of the external circuitry (namely Uf, Rf).	

Test matrix:

Table 48

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of test signal U_S: -6 dBV emf	X	X	
Impedance combinations:			
combination 1	X	X	
combination 2	X	X	
combination 3	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Polarity of the DC feeding	alternating	alternating	
Number of tests	6 tests	6 tests	

Test Procedure Notes:

The source impedance Z_{SOURCE} shall be implemented in a symmetrical way.

Test Result:

The test result shall meet the requirement of TS 101 952, table 10 for an Option A splitter and table 11 for an Option B splitter. The result shall be given in a = 20 log (U1/U2) where U1 is the output voltage measured without splitter connected to the set-up (see first figure for each set-up) and U2 is the observed voltage when the splitter is inserted in the set-up.

Measuring Notes:

NOTE 1: The reduction of line feeding currents to just 13 mA and 80 mA has shown to be appropriate as no significant differences were evident between the various current results.

NOTE 2: Positive and negative feed voltages produced no significant differences in on-hook loss results. However, it is suggested that the positive / negative aspect of the test should still be present. Consequently, it is recommended that the results are measured with half of the tests performed with +50 V and the remaining half performed with -50 V (alternating polarity).

NOTE 3: When testing the VDSL to POTS isolation the following problem occurs: During the calibration measurement the impedances at the POTS port and the LINE port would be seen in parallel as there is no isolation between LINE and POTS when no splitter is added. When the splitter is added, the blocking of the low pass would de-couple these two impedances at higher frequencies. The calibration measurement would therefore assume other relations than the measurement with splitter. Theoretically, it is the POTS impedance which needed to be disconnected (e.g. replaced by a high impedance). This however, would be a rather uncommon measurement, which would also be very different to a similar measurement which has already been defined in the ADSL-over-ISDN case (see TR 101 953-1-3). It was decided to disconnect the impedance at the LINE port instead during the calibration measurement.

NOTE 4: Feeding bridge and holding circuit are expected to have an insertion loss which is higher than 1 dB at higher frequencies. Therefore, feeding bridge and holding circuit are to be considered carefully before entering the tests. An insertion loss of more than 1 dB is acceptable, as long as the dynamic range of the entire test set-up is appropriate to prove an isolation of 55 dB. The dynamic range shall be taken into account when the assessment of the test results is done. It is recommended to have a margin of at least 20 dB between the dynamic range of the test set-up and the required isolation which is to be proved.

6.9 Tests for noise

6.9.1 Tests for audible noise level

Table 49

Test case name:	Audible noise level
Reference:	TS 101 952-2-1 [2], clause 6.10.1
Test purpose:	To evaluate the unwanted noise signal which is produced in the splitter itself without any other signals applied
Test configuration:	See Test Set-up; DUT not configured
NOTE: This test only applies, if the splitter under test does contain active elements.	

No active splitter for the validation measurement could be supplied to STF248. However, it could be proven that the test can be performed at reasonable effort. The required accuracy to asses a system under test according to the requirements as stated in TS 101 952-2-1 [2] can be achieved.

Test set-up:

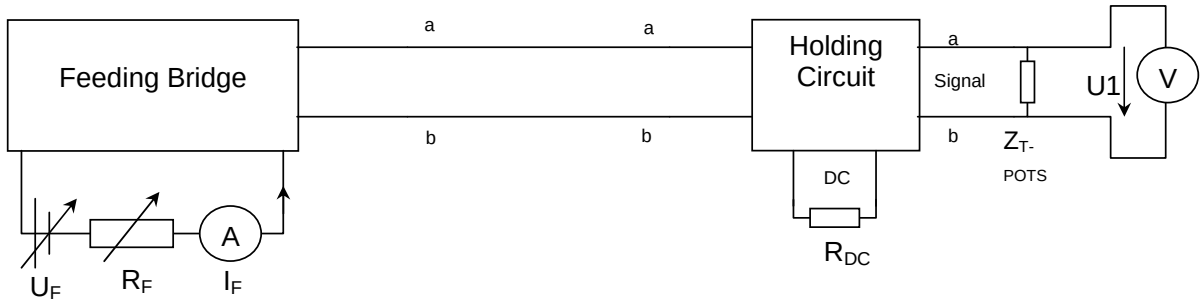


Figure 32: Test set-up for the verification of the test set-up self-noise

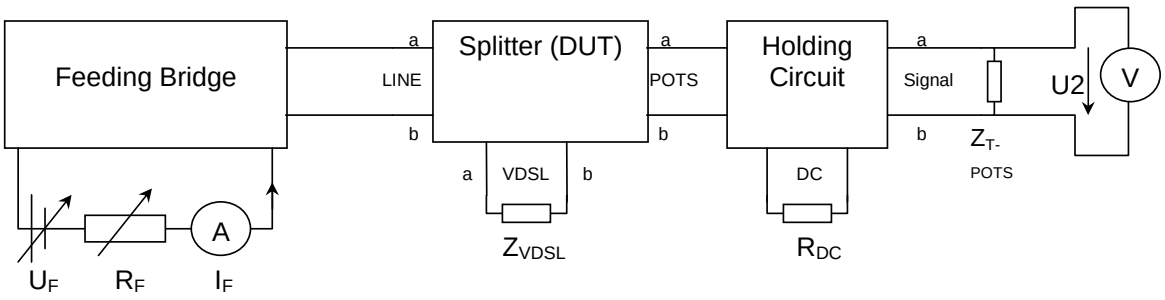


Figure 33: Test set-up for noise measurements at the POTS port of splitters

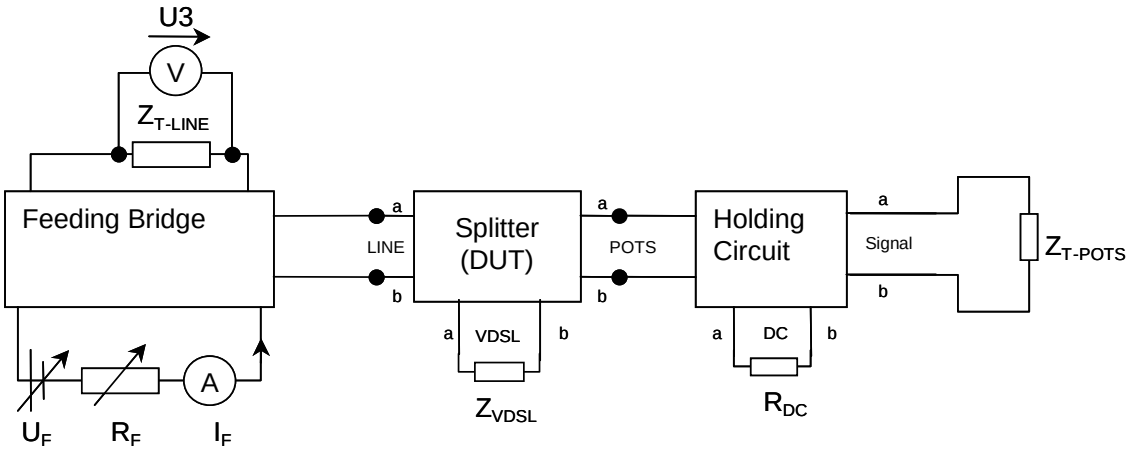


Figure 34: Test set-up for noise measurements at the LINE port of splitters

Test parameters:

Table 50

Parameter	Value
Frequency range	300 Hz to 4 000 Hz
Termination at VDSL port	Z_{VDSL}
Termination at LINE port: Z_{T-LINE}	Z_R
Termination at POTS port: Z_{T-POTS}	Z_R
Feeding voltage U_F	50 V_{DC}
Load resistance R_{DC}	470 Ω in off-hook state 10 kΩ in on-hook state
Feeding current I_F in on-hook state	0,4 mA 2,5 mA
Feeding current I_F in off-hook state	13 mA 80 mA
Ports to be tested	LINE POTS
Weighting of the measured noise	Psophometric

Test matrix:

Table 51

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Frequency range: f_L ... 12 MHz	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 0,4 mA	X	X	
Feeding current I_F: 2,5 mA	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X		
Polarity of feeding voltage	alternating	alternating	
DC load resistor: 470 Ω	X	X	
DC load resistor: 10 kΩ	X	X	
measured at LINE port	X	X	
measured at POTS port	X	X	
Weighting of the measured noise	psophometric	psophometric	
Number of tests	8 tests	8 tests	

Test procedure notes:

Before starting the measurements the test set-up shall be verified with respect to the noise present when having the DC source as well as the holding circuit present in the set-up but not having connected the splitter under test. Measuring P1 as shown in the test set-up is an appropriate way to do so. The observed value for P1 (in dBmp) shall be at least 10 dB lower than the value which is to be proven.

Test results:

The test result shall be presented in dBmp, where P2 = $(U_2)^2/Z_R$ and P3 = $(U_3)^2/Z_R$ is the power observed and weighted psophometrically, when the splitter is connected as in the Test set-up.

Measuring Notes:

See general notes.

6.9.2 Tests for VDSL band noise level

Table 52

Test case name:	VDSL band noise level
Reference:	TS 101 952-2-1 [2], clause 6.10.2
Test purpose:	To evaluate the unwanted noise signal which is produced in the splitter itself without any other signals applied
Test configuration:	See Test Set-up; DUT not configured
NOTE: This test only applies, if the splitter under test does contain active elements.	

No active splitter for the validation measurement could be supplied to STF 248. However, it could be proven that the test can be performed at reasonable effort. The required accuracy to asses a system under test according to the requirements as stated in TS 101 952-2-1 [2] can be achieved.

Test set-up:

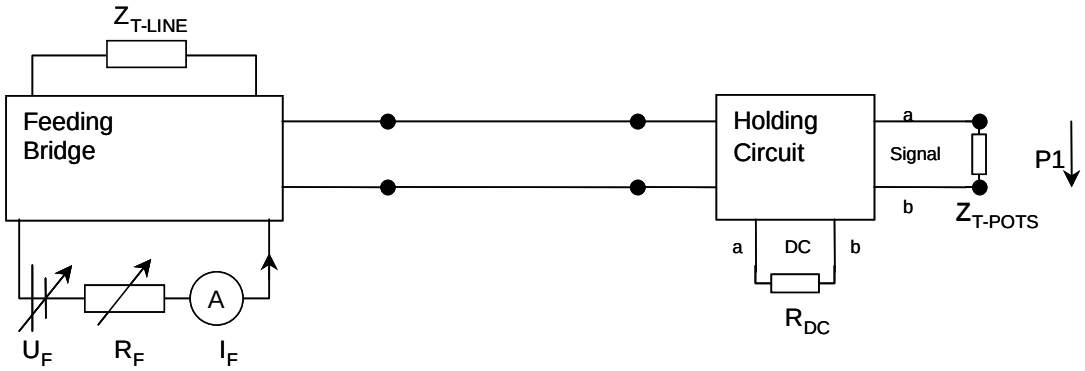


Figure 35: Verification of the test set-up

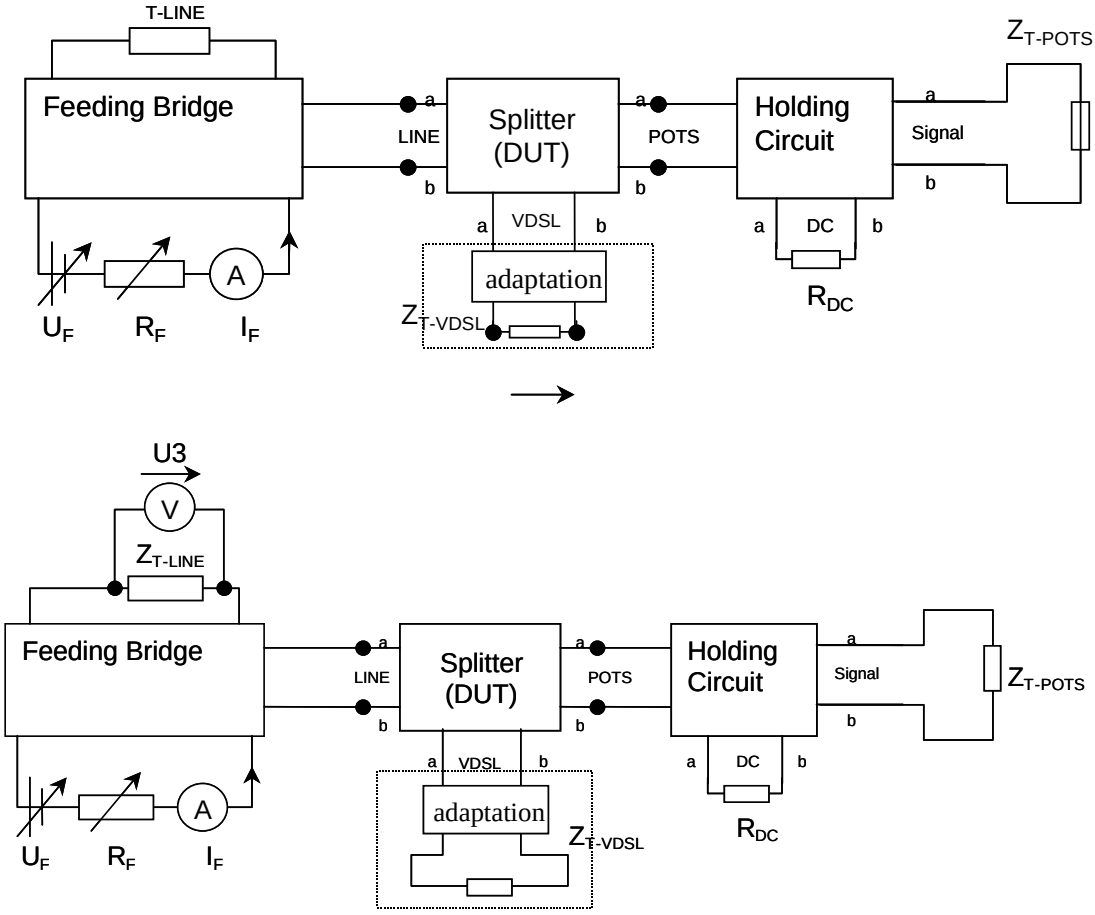


Figure 36: Test set up for noise testing in the VDSL band on a splitter at the xDSL port

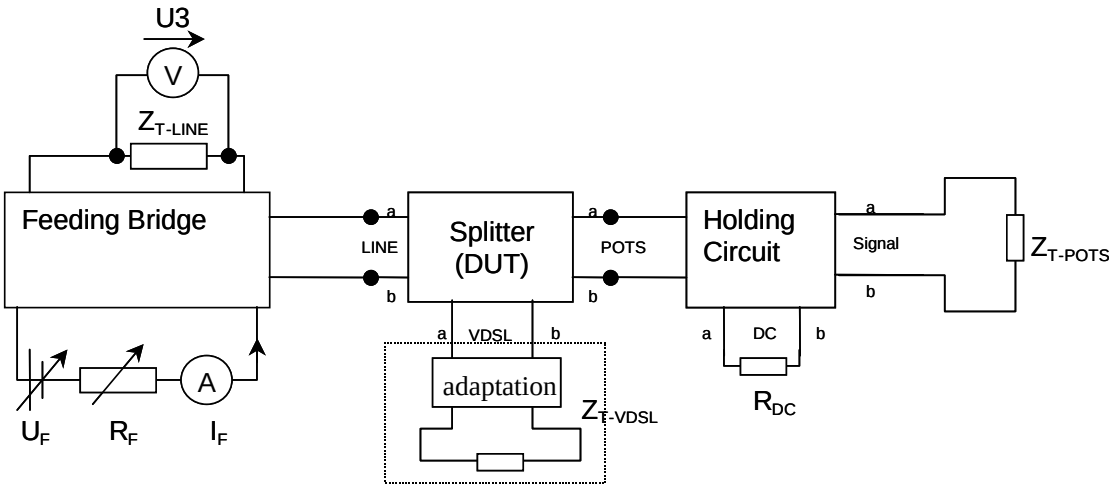


Figure 37: Test set up for noise testing in the VDSL band on a splitter at the LINE port

Test parameters:

Table 53

Parameter	Value
Frequency range	f ... 12 MHz
Termination at VDSL port: Z_{T-VDSL}	Z_{VDSL} (see note)
Termination at LINE port: Z_{T-LINE}	100 Ω (see note)
Termination at POTS port: Z_{T-POTS}	100 Ω (see note)
Feeding voltage U_F	50 V_{DC}
Load resistance R_{DC}	470 Ω in off-hook state 10 kΩ in on-hook state
Feeding current I_F in on-hook state	0,4 mA 2,5 mA
Feeding current I_F in off-hook state	13 mA 80 mA
Ports to be tested	LINE VDSL
Resolution bandwidth of analyzer	10 kHz
NOTE: The termination of ports in the parameters list as well as in the figures above are given on basis of TS 101 952-2-1 [2]. Currently it is under investigation to change the VDSL termination impedance which would also lead to a change in impedances of this test case. When performing the tests of this clause the termination impedances should be checked carefully with the then current TS 101 952-2-1 [2] or its succeeding document.	

Test matrix:

Table 54

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Frequency range: f_L ... 12 MHz	X	X	
Feeding voltage U_F: 50 VDC	X	X	
esolution bandwidth of analyzer: 10 kHz	X	X	
Feeding current I_F: 0,4 mA	X	X	
Feeding current I_F: 2,5 mA	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X		
Polarity of feeding voltage	alternating	alternating	
DC load resistor: 470 Ω	X	X	
DC load resistor: 10 kΩ	X	X	
measured at LINE port	X	X	
measured at VDSL port	X	X	
Number of tests	8 tests	8 tests	

NOTE: The feeding bridge and holding circuit shall not only be considered with respect to their self-noise, but also with respect to their insertion loss. As the noise produced by a splitter will be attenuated by the feeding bridge's and the holding circuit's insertion loss, this attenuation has to be taken into account when presenting the test result.

Test procedure notes:

Before starting the measurements the test set-up shall be verified with respect to the noise present when having the DC source as well as the holding circuit present in the set-up but not having connected the splitter under test. Measuring P1 as shown in the test set-up is an appropriate way to do so. The observed value for P1 (in dBm/Hz) shall be at least 10 dB lower than the value which is to be proven.

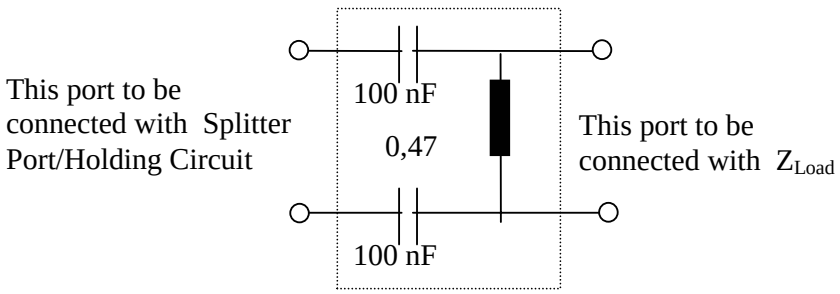
Test results:

The test result shall be presented in dBm/Hz, where P2 = $(U_2)^2/100\ \Omega$ and P3 = $(U_3)^2/100\ \Omega$ is the power observed, when the splitter is connected as in the Test set-up. Note that if the specification for Z_{VDSL} is changed also the 100 Ω in the aforementioned formulas are likely to be changed.

Measuring Notes:

When testing with a selective power measurement method, at least 120 measuring points should be selected over the frequency band. When testing with a frequency sweep mode, one needs to carefully take into account of the choice of resolution bandwidth, video bandwidth and frequency range when defining the sweep time.

The adaptation that is given in figures of the test set-up for this clause should be as follows:



NOTE: This adaptation circuit is based on the specification for Z_{VDSL} of the current TS 101 952-2-1 [2]. Currently it is under investigation to change the VDSL termination impedance which would also lead to a change in the components of this adaptation. When performing the tests of this clause the termination impedances should be checked carefully with the then current TS 101 952-2-1 [2] or its succeeding document.

Figure 38: Adaptation circuit

See also general notes.

6.10 Tests for distortion

6.10.1 Tests for POTS band intermodulation distortion

Table 55

Test case name:	POTS band intermodulation distortion
Reference:	TS 101 952-2-1 [2], clause 6.11.1
Test purpose:	To evaluate the unwanted POTS signal distortion caused by intermodulation effects in the splitter
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

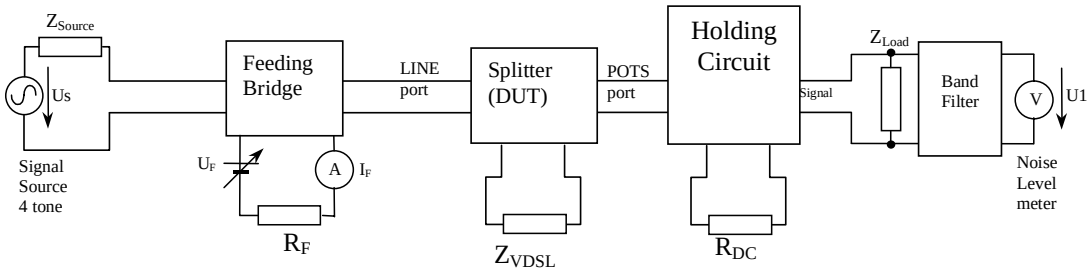


Figure 39: Test set-up for measuring POTS band intermodulation distortion

Test parameters:

Table 56

Parameter	Value
Level of the 4 tone POTS test signal Us	-9 dBV into Z_R according to ITU-T Recommendation O.42 [8]
Feeding current I_F	13 mA 80 mA (see note)
Source impedance Z_{Source}	Z_R
Load impedance Z_{Load}	Z_R with filters: 1 900 Hz, 520 Hz and 2 240 Hz
VDSL termination	Z_{VDSL}
NOTE: The values of I_F are set by adjusting the values of the external circuitry (U_F, R_F and R_{DC}).	

Test matrix:

Table 57

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the 4 tone POTS signal U_S: -9 dBV	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Polarity of feeding voltage	alternating	alternating	
Number of tests	2 tests	2 tests	

Test procedure notes

NOTE 1: In comparison to the related ADSL-over-POTS test case (see TR 101 953-1-1 [4]) this test does not contain an xDSL upstream or downstream signal representation. Reason for this is, that TS 101 952-2-1 [2] currently does not require such a signal. However, TS 101 952-2-1 [2] states that a methodology to test in the presence of a VDSL signal is currently under study. STF248 has performed such a study and has come to the conclusion, that adding a VDSL signal does not lead to a significantly changed test result as long as passive splitters or passive splitters with current/voltage detection are concerned. Intermodulation of these splitters is mainly caused by the saturation of inductive components. Usually splitters are laid out not to get into saturation at the specified DC currents. Furthermore, usually there is a certain gap between the highest specified DC current and the minimum saturation current. The additional load by the VDSL signal is that small that the effect of it is falling into usually achievable measuring tolerances. Active components in splitters may cause intermodulation independently of the DC loading. Consequently, for active splitters a test with VDSL signal provision should be kept under study.

Test results:

Table 58

Order of harmonic distortion	Maximum Intermodulation product (dB)
Second order harmonic distortion	
Third order harmonic distortion	

Measuring Notes:

NOTE 2: To evaluate 3rd order distortion, the total power due to the six 3rd order intermodulation products in a narrow band centred at 1,9 kHz is measured and expressed in dB below the received signal. For 2nd order distortion, the power due to the four 2nd order intermodulation products in a narrow band centred at 520 Hz and the power nominally due to the four 2nd order intermodulation products in a narrow band centred at 2 240 Hz are also measured. These two 2nd order distortion product powers are then averaged and the result expressed in dB below the received signal.

See also general notes.

6.11 Tests for signal delay Impacts

6.11.1 Tests for group delay distortion

Table 59

Test case name:	Group delay distortion
Reference:	TS 101 952-2-1 [2], clause 6.12
Test purpose:	To measure the increase in group delay distortion in the POTS band caused by the splitter with VDSL load, relative to the lowest measured delay without the splitter, when tested with the test parameters as given in the related standards
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

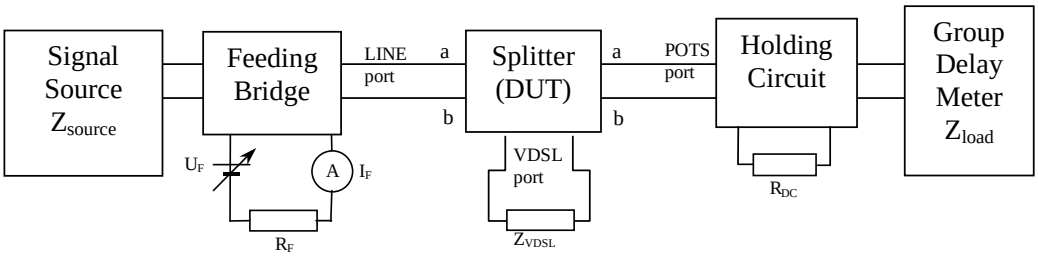


Figure 40: Test set-up for group delay distortion measurements

Test parameters:

Table 60

Parameter	Value
Level of the test signal	-10 dBV
Feeding current I_F	13 mA 80 mA (see note)
Source impedance Z_{Source}	Balanced 600 Ω resistive (test 1) ZR (test 2)
Load impedance Z_{Load}	Balanced 600 Ω resistive (test 1) ZR (test 2)
Termination at VDSL port	Z_{VDSL}
NOTE: The values of I_F are set by adjusting the values of the external circuitry (U_F, R_F and R_{DC}).	

Test matrix:

Table 61

	TS 101 952-2-1 [2]	Essential tests	Optional tests
Level of the test signal: -10 dBV	X	X	
Feeding voltage U_F: 50 VDC	X	X	
Feeding current I_F: 13 mA	X	X	
Feeding current I_F: 80 mA	X	X	
Polarity of feeding voltage	alternating	alternating	
Source impedance: 600 Ω	X	X	
Source impedance: Z_R	X	X	
Load impedance: 600 Ω	X	X	
Load impedance: Z_R	X	X	
Number of tests	4 tests	4 tests	

Test Procedure Notes:

GDD_f formula is as follows:

$$GDD_f = GD_{nf} - GD_{\min}$$

where:

GDD_f is the Group Delay Distortion at frequency *f*.

GD_{nf} is the normalized Group Delay at frequency *f*.

GD_{min} is the minimum normalized Group Delay for all frequencies for that load.

Measuring notes:

For each test case, the normalized group delay is to be obtained by subtracting the group delay values without the splitter from the group delay values with the splitter at each measured frequency point:

$$GD_{nf} = GD_{sf} - GD_{0f}$$

where:

GD_{nf} is normalized Group Delay at frequency *f*.

GD_{sf} is measuref Group Delay at frequency *f* with splitter in circuit.

GD_{0f} is measured Group Delay at frequency *f* without splitter in circuit.

NOTE: It was noted that the requirement states that the increase in group delay distortion caused by the splitter must be less than 200 µs to 250 µs. This seems excessively large. In practice the increase in GDD indicated results in the order of 40 µs worst case (lower frequency range).

6.12 Tests for requirements related to POTS effects

6.12.1 Tests for requirements related to POTS transient effects

Table 62

Test case name:	Requirements related to POTS transient effects
Reference:	TS 101 952-2-1 [2], clause 6.13
Test purpose:	To measure the increase in group delay distortion in the POTS band caused by the splitter with VDSL load, relative to the lowest measured delay without the splitter, when tested with the test parameters as given in the related standards
Test configuration:	See Test Set-up; DUT not configured

Test set-up:

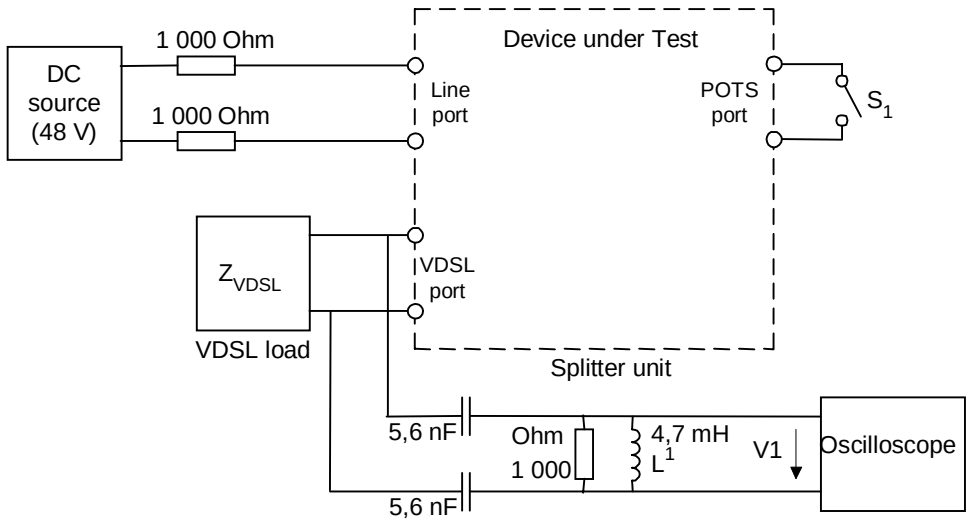


Figure 41: Test Set-up for investigating POTS transient effects

Test parameters:

Table 63

Parameter	Value
S1 transition time	< 2 µs
Termination at VDSL port	Z_{VDSL} in parallel to additional components as given in the set-up
Feeding Voltage U_F	48 VDC (see note)
Type of transient	S1 from closed to open S1 from open to closed
NOTE: The feeding voltage should be provided via a DC source not containing high inductances (as for instance feeding bridges).	

Test matrix:

Table 64

	TS 101 952-2-1 [2]	Essential tests	Optional tests
S1 transition time < 2 µs	X	X	
Feeding voltage U_F: 48 VDC	X	X	
S1 transition from open to closed **S1 transition from closed to open**	X X	X X	
Peak voltage measurement **Main lobe frequency (resonance)**	X X	X X	
Number of tests	4 tests	4 tests	

Test Procedure Notes:

NOTE 1: A possible implementation of the switch S1 can be found in TR 101 728 [6].

NOTE 2: The feeding voltage should be provided via a DC source not containing high inductances (as for instance feeding bridges) as an inductance in the DC source would significantly change the test result.

Test results:

Test results should be given in two ways:

- The maximum peak voltage of V1 should be given in V.
- The frequency of the main lobe of the Fourier Transform of V1 (resonance frequency) should be given in kHz.

Table 65

	maximum peak voltage V1 (Vpp)	main lobe of Fourier transformed V1 (kHz)
S1 transient from open to closed		
S1 transient form closed to open		

Measurement notes:

See general notes.

NOTE 3: During the validation work of STF 248 it could be found that proper working VDSL-over-POTS splitters do provide a resonance frequency higher than the specified one. It could not be proven why the specified resonance frequency was selected at 15 kHz. One outcome of STF 248 validation work was to inform AT about this aspect and to ask for re-considering the requirement.

History

Document history		
V1.1.1	December 2003	Publication