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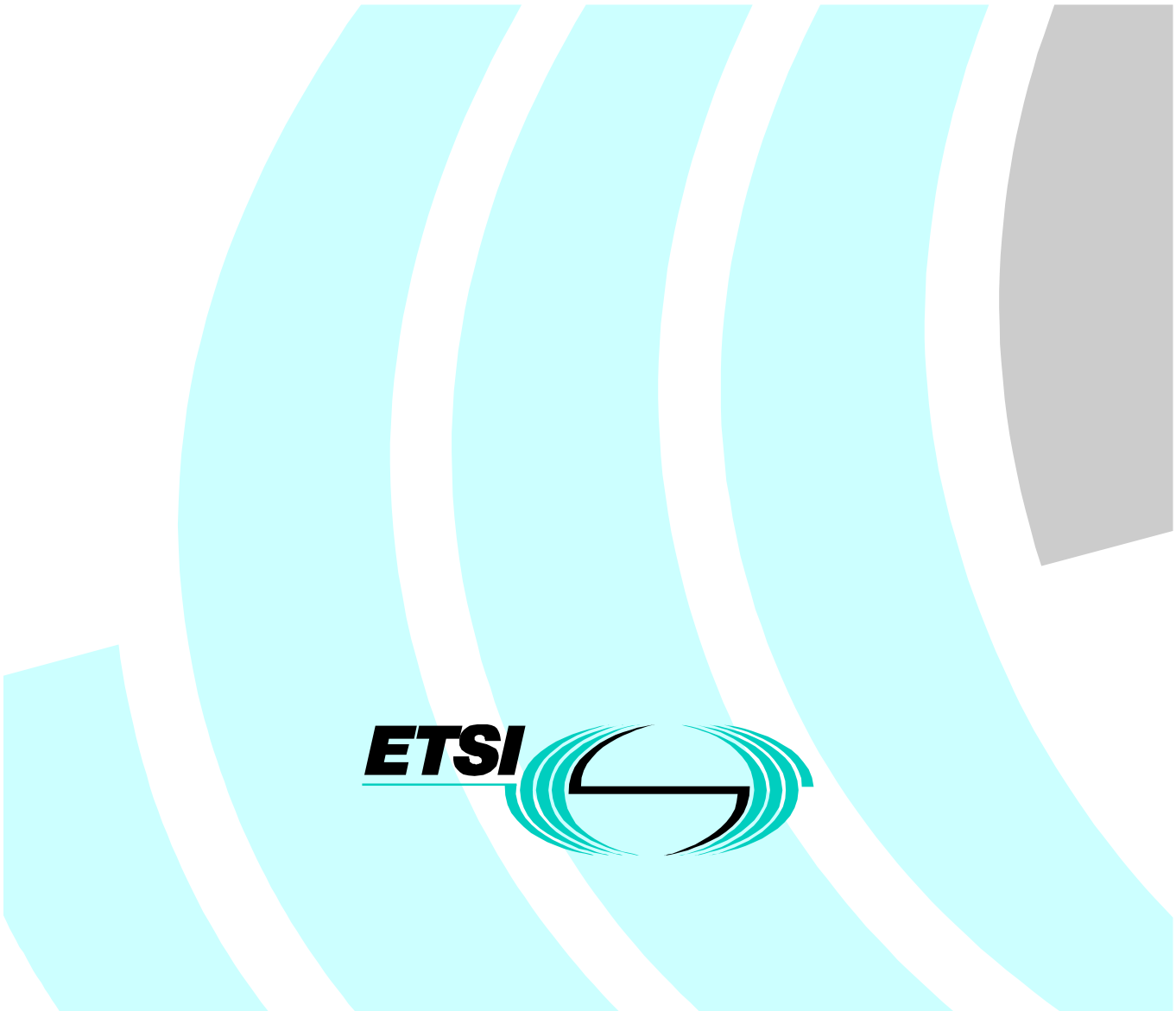
Technical Report

Transmission and Multiplexing (TM); Timing and synchronization aspects of Asynchronous Transfer Mode (ATM) networks



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Foreword

This Technical Report (TR) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

1 Scope

The present document gives guidance on timing and synchronization aspects and defines requirements for ATM Networks. This includes a model of network interactions as well as a simplified model of the function on which most requirements will be assigned, i.e., the Interworking Function (IWF). In relation to the models and requirements, different synchronization methods are described on an overview level. The present document provides recommendations on the applications when different methods are most suitable.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] ITU-T Recommendation I.363.1 (1996): "B-ISDN ATM Adaptation Layer specification: Type 1 AAL".

[2] EN 300 462-3-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks".

[3] EN 300 462-4-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4-1: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

[4] EN 300 462-5-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[5] EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[6] ETS 300 300 (Edition 2): "Broadband Integrated Services Digital Network (B-ISDN); Synchronous Digital Hierarchy (SDH) based user network access; Physical layer User Network Interfaces (UNI) for 155 520 kbit/s and 622 080 kbit/s Asynchronous Transfer Mode (ATM) B-ISDN applications".

[7] I-ETS 300 353: "Broadband Integrated Services Digital Network (B-ISDN); Asynchronous Transfer Mode (ATM); Adaptation Layer (AAL) specification - type 1".

[8] ITU-T Recommendation G.823 (1993): "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".

[9] EN 302 084: "Transmission and Multiplexing (TM); The control of jitter and wander in transport networks".

[10] ITU-T Recommendation G.813 (1996): "Timing characteristics of SDH equipment slave clocks (SEC)".

[11] ITU-T Recommendation G.114 (1996): "One-way transmission time".

[12] ITU-T Recommendation I.363 (1993): "B-ISDN ATM Adaptation Layer specification".

[13] CCITT Recommendation G.702 (1988): "Digital hierarchy bit rates".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply.

Network-Synchronous Operation: synchronization of the physical layer (usually by a timing distribution of a timing signal traceable to a Primary Reference Clock PRC, see EN 300 462-3-1 [2] and EN 300 462-6-1 [5])

Service Synchronization: synchronization of a specific service carried over an ATM network

NOTE: There may exist situations when Network-Synchronous operation is required and service synchronization is not needed (for example at the network interface between different operators).

ATM Island: collection of interconnected ATM equipment with AAL functionality at the edges

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AAL	ATM Adaptation Layer
ATM	Asynchronous Transfer Mode
B-TE	Broadband Terminal Equipment
CBR	Constant Bit Rate
CDV	Cell Delay Variation
CSI	Convergence Sub-layer Indication
CTD	Cell Transfer Delay
ISDN	Integrated Services Digital Network
IWF	Interworking Function
PDH	Plesiochronous Digital Hierarchy
PRC	Primary Reference Clock
STM	Synchronous Transfer Mode
TDM	Time Division Multiplex
UNI	User Network Interface
VBR	Variable Bit Rate

4 General

As ATM is essentially a packet oriented transmission technology, the ATM network nodes do not require any synchronization of the ATM layer. At any entrance point of an ATM multiplexer or an ATM switch, an individual device shall provide cell timing adaptation of the incoming signal to the internal timing. The principle in ATM networks to cater for frequency differences is to use idle cell stuffing. Transmission links therefore in principle need not to be synchronized with each other.

However, ATM network shall be able to integrate STM-based applications. When transporting a CBR stream over an ATM network and when interworking with PSTN networks, the ATM network shall provide correct timing at the service interfaces.

This means that the requirements on synchronization functions in ATM networks, especially on the boundary of the ATM networks, are depending on the services carried over the ATM network. For STM based services, the IWF may require network-synchronous operation in order to provide acceptable performance.

It can also be noted that if network-synchronous operation is applied for other purposes, it can simplify ATM switch or IWF design. Further, cell loss performance can be improved in high loaded ATM networks.

In other applications, however, where the services do not need synchronization, the implementation of network-synchronous operation could be a waist of resources. It shall be noted however that the physical layer of B-ISDN has been generally defined to be synchronous (see related physical layer recommendations, for example ETS 300 300 [6]).

The timing and synchronization issues addressed in the present document concerns only the protocol layers of the standard B-ISDN reference model which is composed of:

- Physical Layer;
- ATM Layer;
- AAL Layer.

In the context of the present document, all layers above those are considered as applications transported over ATM. Real time applications have relatively tight timing requirements concerning delay and delay variation. Some applications might resolve their timing issues within higher layers (e.g., MPEG2), other applications rely on the timing support provided by one or more of the above mentioned layers. Specifically, AAL1 has been provided with means to achieve this.

The present document aims at describing different methods to obtain the synchronization related requirements. Additionally, the requirements for interfaces and equipment which are part of an ATM network, are described. It also gives recommendations when to apply different types of synchronization methods (Network-synchronous operation, SRTS or adaptive timing).

5 ATM Network Reference Models

5.1 Reference interfaces, Equipment and Synchronization

Figure 1 shows the reference configuration for ATM Network interworking with private or public circuit switched networks (generally called STM Network) and with Broadband Terminal Equipment (B-TE). The ATM network comprises a number of ATM switches and multiplexors.

The IWFs shown in figure 1 are those relevant for synchronization aspects.

It is assumed that an arbitrarily large number of IWFs could be connected to the ATM network.

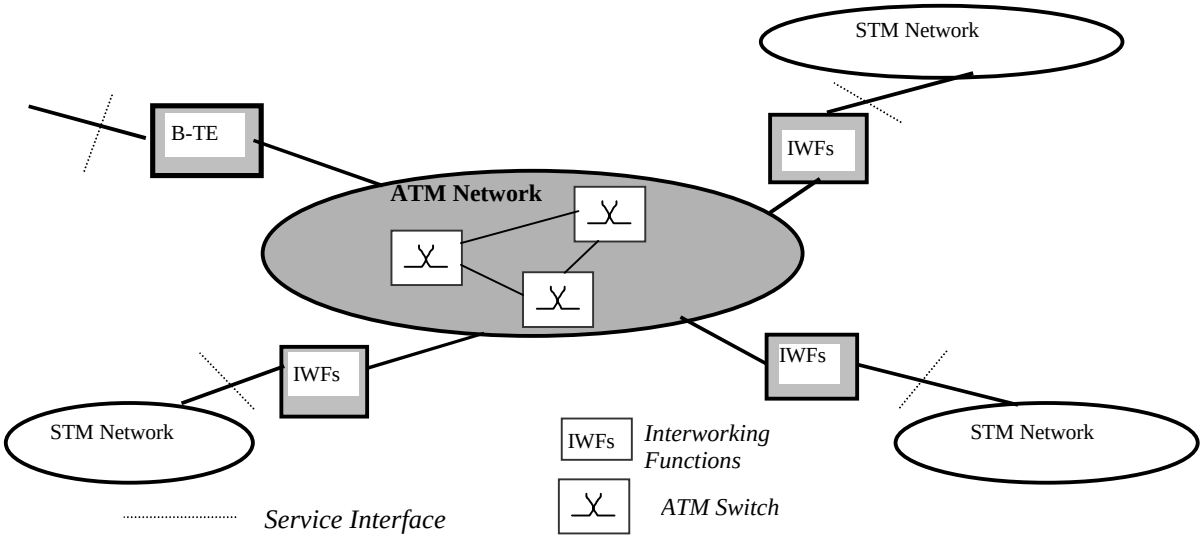


Figure 1: Reference interfaces and equipment

The synchronization related functions of IWF, B-TE and ATM switches will be analyzed in clause 8.

One of the most common cases of interworking for an ATM network is when providing transport layer capability between several traditional public STM networks (PSTN, PLMN, etc.) and/or between a public STM network and private networks (e.g. through connection with a PABX).

As result of the considerations done in the next chapters, in this case a fully synchronized network is recommended (PSTN and ATM network both traceable to PRC) in order to fulfil requirements related to PDH interfaces (see figure 2).

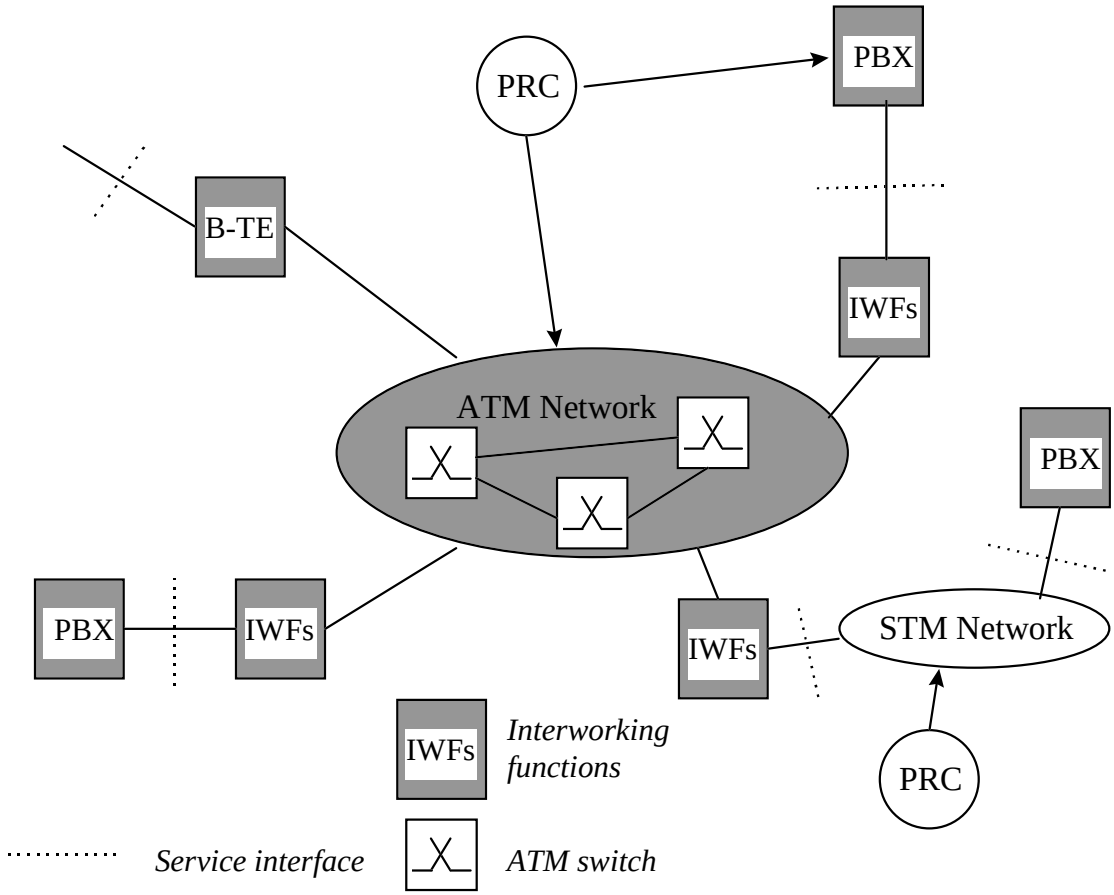


Figure 2: Reference interfaces, equipment and synchronization

5.2 Hypothetical Networks Connection Reference Model

Figure 3 shows a hypothetical network connection reference model used to analyze jitter and wander performance of services carried over ATM.

A chain of *M* islands is considered each containing a chain of *N* ATM switches.

N and *M* are for further study.

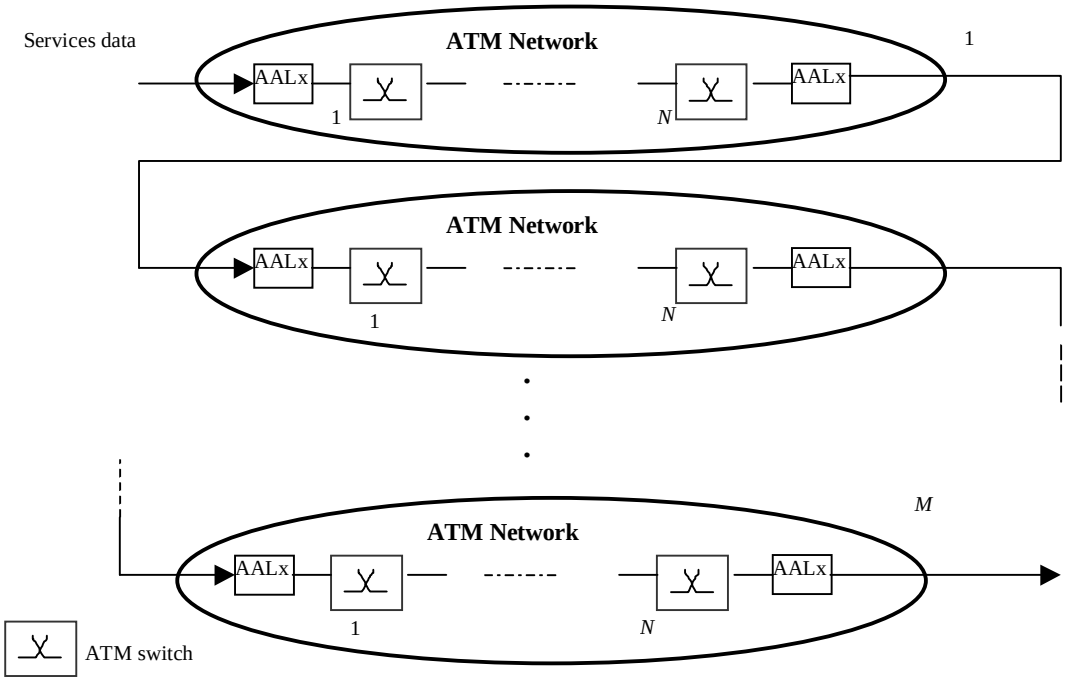


Figure 3: ATM Networks connection reference model

6 Parameters Related to Synchronization Aspects of ATM Networks

6.1 General

The synchronization related characteristics of the service synchronization (wander and jitter in particular) depend on the characteristics of the ATM network itself, that is mainly CDV. In the following, the relationship between CDV, jitter and wander of the services and the used clock recovery method is discussed.

6.2 Synchronization Related Characteristics

6.2.1 Cell Delay Variation (CDV)

When a constant bit rate stream is fed into an ATM network the stream is mapped into the ATM cell payload and the ATM cells passed to the physical layer at regular intervals (ignoring waiting time jitter etc.).

On traversing the ATM network, in the absence of cell delay variation, the cells would arrive with constant inter-interval time and could be played out immediately upon receipt on the constant bit rate interface. Just as the buffer is about to empty the next cell would arrive to replenish the buffer.

However, if each cell is subjected to a different delay through the network and, for example, if the second cell arrives late the buffer would empty and have no more bits to send. If the second cell arrives early the 47 byte buffer would overflow. Therefore, the play-out buffer needs to be dimensioned and operated in such a way as to allow for late or early cell arrivals. The usual technique is to delay playout of the initial cell by the calculated maximum cell delay variation allowance. This has the effect of ensuring no buffer depletion even when the first cell arrives very early and the second cell arrives very late (figure 4a). However, the buffer now needs to be enlarged to at least the payload size plus the number of cells that could be delivered in an interval equal to twice peak-to-peak CDV. This ensures that if the first cell actually arrives very late and is additionally delayed by the peak-to-peak CDV before playout and subsequent cells arrive very early there will still be space available for them in the buffer (figure 4b). In this latter case the buffer level needs, ideally, to be optimized over a period of time to ensure the cells are delayed in the buffer for a period not in excess of the peak-to-peak cell delay variation.

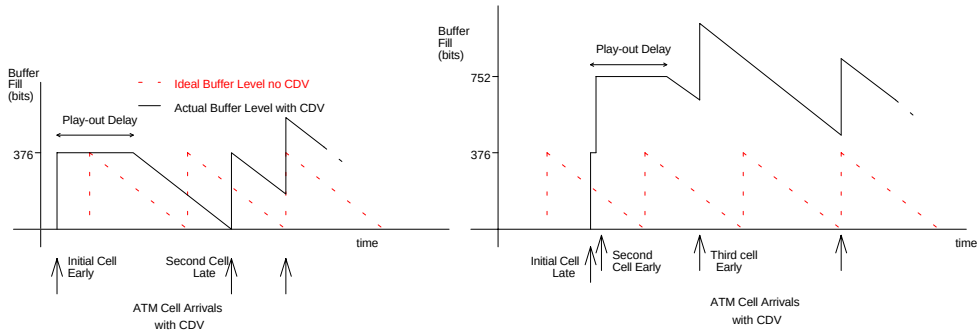


Figure 4a **Figure 4b**

Where a receiver's clock takes time to lock to the transmitter, or where the receive clock varies in a time dependant fashion, the buffer level will vary beyond that influenced by CDV and the time taken to lock and the frequency difference over time should be taken into account when specifying the delay needed before initial playout and total buffer size. The delay in the buffer can be thought of as the elimination of variable delay by an increase in total fixed delay, the total fixed delay of the ATM network thus becomes the fixed transmission propagation delay plus the peak–to–peak CDV.

The main mechanism, among many, responsible for cell delay variation within an ATM network is output port contention. Given independent traffic streams on each input port (and given an output-port buffered, non-blocking, switch design) cells arriving at the switch at a regular rate will have to wait varying amounts of time in the output buffer dependant on the number of cells instantaneously contending for the same output port. The regularity of the input traffic stream is thus disrupted and cells arrive at their destination at irregular intervals. Other mechanisms that can contribute to CDV include that of waiting time jitter where the inter-cell period dictated by the transmitting service clock does not map exactly to the cell interval available on the physical transmission line, and variation in delay experienced through the switching fabric of an ATM switch.

The main parameter affecting buffer dimensioning at the receiver and initial play-out delay is thus peak-to-peak cell delay variation. However, when using an adaptive clock recovery synchronization technique the time dependence of CDV can adversely affect the purity of the recovered clock leading to larger play-out buffer dimensions (or in the absence of a larger play-out buffer, cell loss) and jitter and wander of the output bit stream.

In annex B, the characteristics of cell delay variations for various network reference models, loads and traffic are discussed.

6.2.2 Wander Limits

The limit for long term phase wander for a 2Mbit/s PDH CBR stream, as defined by ITU-T Recommendation G.823 [8], is 36, 9 UI at 1, 2×10^{-5} Hz (daily wander limit) down to 18 UI between 0,01 Hz and 1,667 Hz.
An adaptive method as described in subclause 7.3, has been used in some tests.
Given any change in network load with periodicity greater than the time constant of the adaptive clock's phase locked loop the received clock phase will directly track the rms switch delay. A test has been performed using a worst case queuing technique on an STM-1 output interface and applying a short term network load changes by 93,2 % on a single ATM switch. This test showed that the receive clock phase would change by ~32 UI against a downstream equipment tolerance limit of only 18 UI (see figure 5). Worst still, not all of this tolerance limit could be apportioned to the ATM network. It seems likely therefore that for a network comprising a number of ATM switches passing through busy hours and idle periods that excessive wander, beyond the ITU-T Recommendation G.823 [8] limits, will be exhibited by the exiting CBR cell stream.

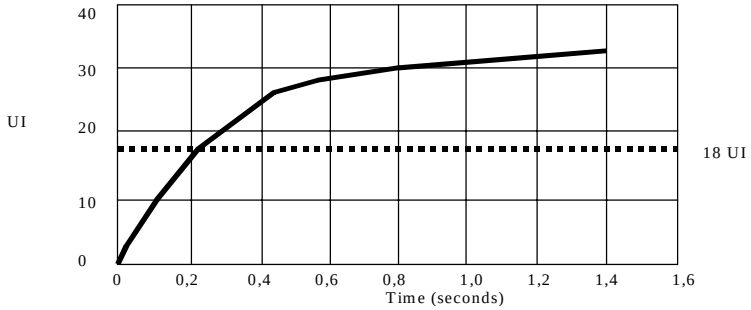


Figure 5: Output phase variations vs output wander limit

Indeed the measurements performed on the ATM switch and 2 Mbit/s CBR transmission interface show that, for a single priority queue output port switch, the long term phase of the 2 Mbit/s CBR output stream will follow the slow delay changes of the switch queue caused by varying network load.

Given that the limits in ITU-T Recommendation G.823 [8] for 2 Mbit/s wander lie between 36,9 UI and 18 UI, it appears impossible to guarantee such limits when using a single priority queue in association with adaptive clock recovery. This is particularly so where the CBR streams are made to contend with large bursty data loads, and the fact that not all of the downstream equipment wander tolerance limit can be apportioned to the ATM network. Thus any downstream equipment which relies on the ITU-T Recommendation G.823 [8] limits for wander being met could not be connected through such an ATM switch and adaptive clock recovery configuration and be guaranteed compliant wander behaviour.

It may be possible to reduce excessive wander by use of a separate priority queue for CBR cell streams. For example, in the case considered where only one CBR stream exists, if this were to be serviced by a separate priority output buffer it would suffer little CDV and thus cause virtually no wander at the output of the adaptive clock circuit. However, even here further study is required since the effects of waiting time jitter, effects of dissimilar CBR rate contention at higher CBR loads and contention with real time VBR video traffic if placed in same buffer would need to be studied.

6.2.3 Jitter Limits

The jitter limit for a 2 Mbit/s PDH CBR stream, as defined by ITU-T Recommendation G.823 [8], is 1,5 UI Peak to Peak between 20 Hz and 100 kHz.

An adaptive method has been considered also in this case for some tests. The time constant of the adaptive method is approximately 0,8 s.

The amount of jitter above 20 Hz is limited by the rate of change allowed by the adaptive clock's phase locked loop. The amount of jitter that could be imparted by the experiment described in subclause 6.2.2, has been estimated by passing the measured responses through a 20 Hz highpass filter. The related results are shown in figure 6.

Here the measured characteristic has been fitted to an exponential and the curve fit subjected to 20 Hz high pass filtering. This result shows that even in the worst case a step change in network load will not cause excessive jitter (phase noise above 20 Hz) on the output stream.

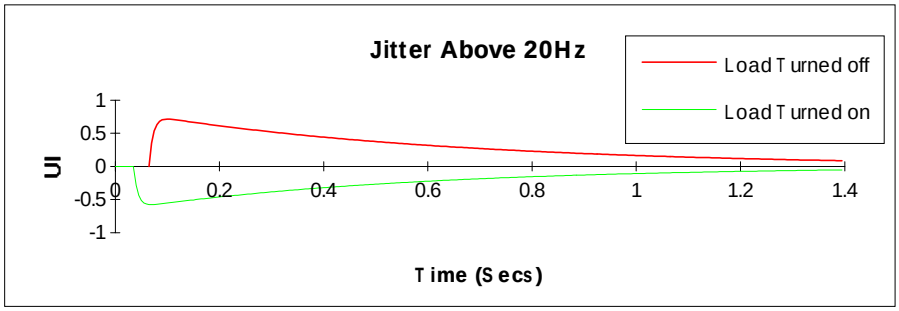


Figure 6

7 Clock Recovery for Constant Bit Rate Services Transported over ATM Networks

Three solutions exist to eliminate or reduce the effects of CDV from constant bit rate connections.

These comprise:

a) fully network-synchronous operation by using a network derived clock as the service clock;

b) the use of Synchronous Residual Time Stamps (SRTS) to transmit service clock information, and finally;

c) adaptive clock recovery.

Additionally, where the network is solely responsible for transporting ATM cells, rather than delivering a constant bit stream to the user, the receiving higher level application layer can have the added responsibility for service clock derivation.

These aspects are reviewed in more detail below.

7.1 Network - Synchronous Operation

In forcing an end-station (the CBR equipment in figure 7) to operate in synchronism with the network clock the effects of CDV can be completely eliminated. As shown in figure 7 (the figure indicates the principle for one direction only, the same applies in the opposite direction) the service clock is derived directly from the network clock. Given the presence of a network clock at both the transmitting and receiving end-stations, the service bit stream can simply be clocked out of the playout buffer at the service bit rate, fully independent of the cell delay variations caused by the ATM network. A playout buffer with correct dimensions and initial delay in playout is still required to ensure that CDV does not cause cell loss or bit stuffing. In the event of network clock failure the buffer will also require either a buffer slip algorithm with the receive clock placed in hold-over mode or the receiver shall revert to an adaptive clocking algorithm.

The network clock is distributed through the synchronization of the physical layer connecting the ATM network elements. These ATM network elements may themselves be synchronized via an external physical timing interface or as a slave of another ATM network element via the physical layer connection.

- ***Network Synchronous Operation***

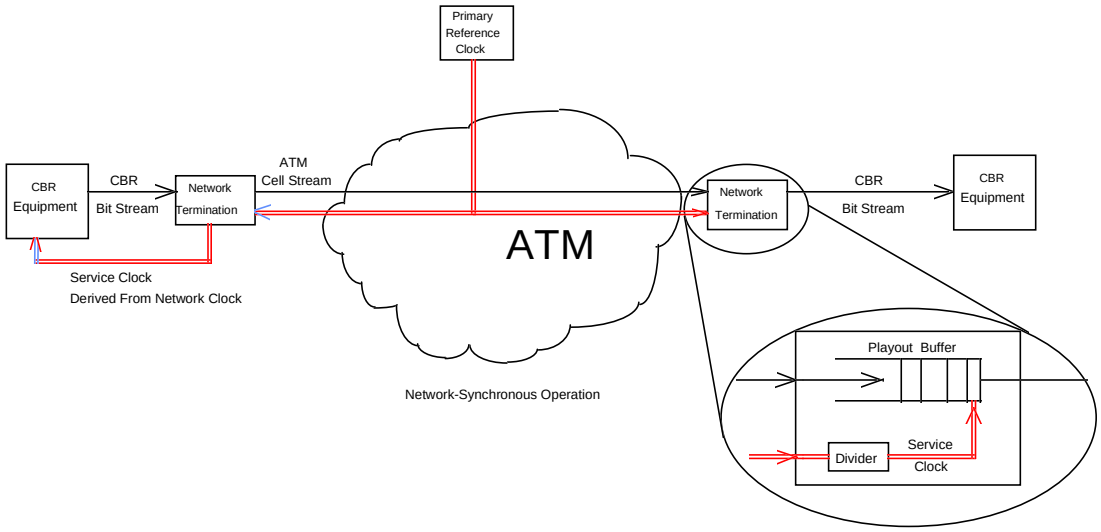


Figure 7

NOTE: The distribution of the network clock, from the Primary Reference Clock to the IWFs, is not conveyed by the ATM layer network. It can be done either via the physical transport layer or via a separate synchronization network. Anyway, the network clock is in principle only needed at the edges of the ATM network, where the CBR streams are processed.

7.2 Synchronous Residual Time Stamps (SRTS) Method

The above network synchronous option has the drawback that not all end-stations and CBR sources would wish to synchronize to the network clock. In these instances one option is to transport information about the source clock across the ATM network to eliminate playout buffer depletion or overflow. The technique adopted for this is called the Synchronous Residual Time Stamp (SRTS) technique which is closely associated with the ATM Adaptation Layer Type 1 protocol. To allow SRTS to work accurately the network needs to distribute a good quality network clock to the network interface.

Some general features of the SRTS method are:

- essentially insensitive to CDV;
- robust against cell losses.

The SRTS method of timing delivery together with the network synchronous operation, is the preferred option for timing delivery of CBR services which require compliance with ITU-T Recommendation G.823 [8] jitter and wander requirements.

Further details on SRTS method are given in I-ETS 300 353 [7] and in annex C of present document.

7.3 Adaptive Methods

Where ATM cells traverse a number of different ATM networks, it may not be possible to provide a common network clock to the transmitting and receiving end-stations. Also, some services may not require the purity of clock available from the above network synchronous or SRTS schemes. In these instances it may only be possible or more cost effective to use an adaptive clock recovery technique.

The adaptive clock method is actually a collective designation for a large number of end-to-end clock recovery methods using particular adaptive algorithms. Since all adaptive methods are based on the fact that the mean rate of cell arrivals is a measure of the source clock frequency, they are sensitive to the cell delay variation (CDV) induced in the network. A good adaptive algorithm should:

- track the transmit service clock whilst at the same time not tracking changes implied erroneously by the CDV of the network;
- have a reasonable convergence time;
- respond fast to a phase or frequency transient in the transmit service clock;
- generate a clock signal which is stable in phase, has a slew rate and tolerance corresponding to the transmit service clock and remains within the bounds of the service specific jitter-wander limits;
- control the buffer fill so it doesn't deviate too much from its defined nominal fill level.

Various algorithms may exhibit different behavior under the same conditions so their characteristics should be studied carefully before taking into use. The adaptive method should be used only for wander insensitive services.

In annex D some details of the method are further described.

8 Impact of network clock impairment on service clock recovery

During normal operation, the transport of a CBR signal using SRTS or network synchronous operation, depends on the timing signals at the AAL1 transmitter and receiver being either PRC traceable or traceable to a common network clock. When one or both timing signals are traceable to clock(s) in holdover, equipment at the terminating ends of the CBR service will experience (uncontrolled) frame slips.

This occurs because any frequency offset between the transmitter and receiver is added to the recreated nominal frequency of the CBR signal egressing the ATM network. This results in a difference between the rate at which data enters the AAL1 receiver buffer and the rate at which it is read from the AAL1 receiver buffer, which leads to buffer over/under-flows in the receiver. This in turns could cause slips and reframing events (as buffer over/under-flows are often not aligned with the CBR services frame boundaries) in the connected STM equipment.

The rate of (uncontrolled) slips at the AAL1 receiver buffer depends on the frequency offset, whether and how the buffer is recentered following a slip and the statistics of CDV. Large CDV will, in general, increase the slip rate compared to the slip rate caused by frequency offset only. This is because the CDV gives rise to a random component of buffer fill variation that is added to the deterministic component due to frequency offset. Any model shall account for whether or not buffer recentering is implemented.

Consider for example immediate buffer recentering following the (uncontrolled) slip. If 2B is the size of slip buffer, y is the frequency offset between the AAL-1 transmitter and receiver, the time to the next (uncontrolled) slip is given by:

$$T = B/y$$

This result assumes there is no CDV.

In the following table some examples are given with a three milliseconds and one millisecond AAL1 buffer.

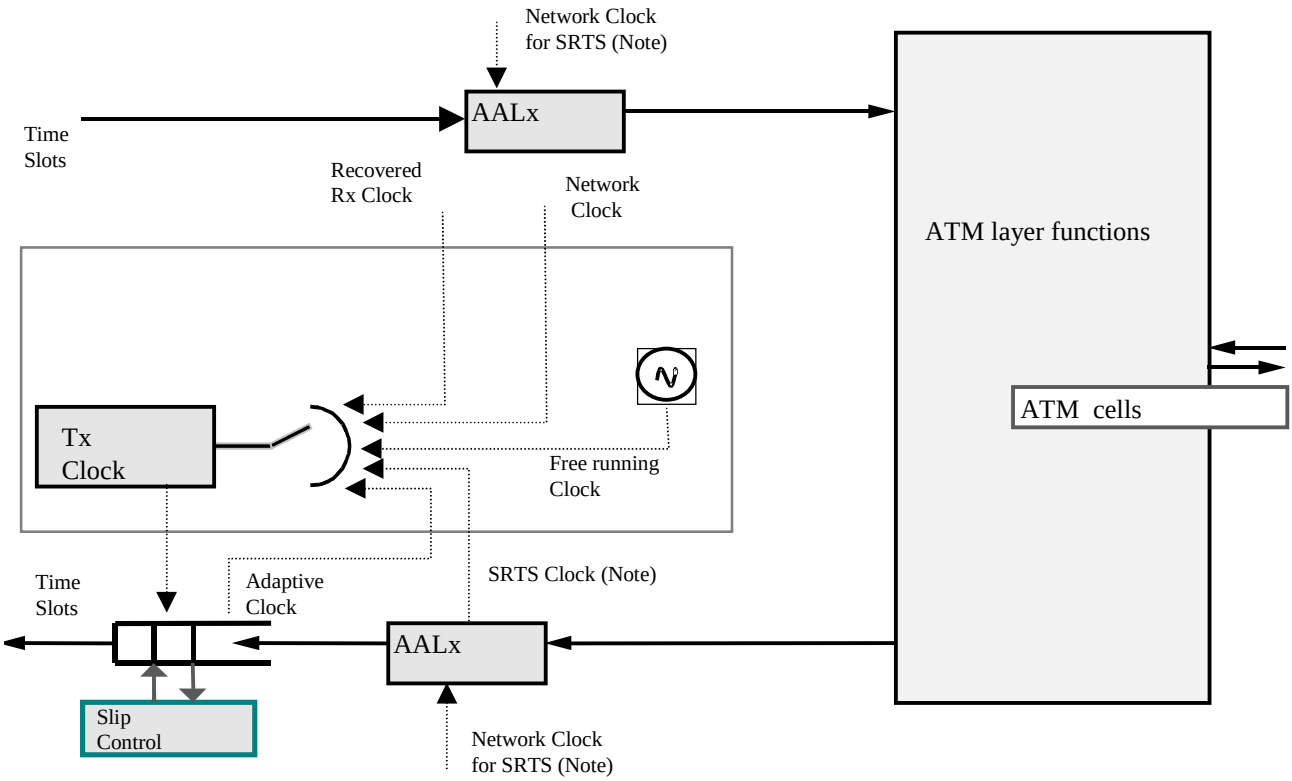
Table 1

Synchronization Fractional Frequency offset (y)	Time between slips (T) B = 3 ms	Time between slips (T) B = 1 ms
2,08 ppm = $2{,}08 \times 10^{-6}$ (EN 300 462-5-1 [4] after 3 days)	0,4 hour	0,13 hour
0,08 ppm = 8×10^{-8} (EN 300 462-5-1 [4] without temperature variation after 3 days)	10,4 hours	3,47 hours
0,0031 ppm = $3{,}1 \times 10^{-9}$ (EN 300 462-4-1 [3] after 3 days)	11,2 days	3,73 days
NOTE: Increasing the buffer size would lead to an increased time between slips but also to an increased amount of data deleted/repeated per slip.		

9 Equipment Synchronization Related Requirements

9.1 Interworking Function (IWF) for CBR Services

In the context of the present document, the Interworking Function (IWF) provides necessary adaptations of CBR bit streams to cell streams and vice versa.



Rx = Receiving side from CBR equipment
Tx = Transmitting side to CBR equipment

NOTE: SRTS is only supported by AAL1.

Figure 8: IWF Equipment model

Supported timing options for the Tx clock are:

- Timing from recovered source clock (loop-timing);
- Timing from the network clock (the network clock can be derived either from the physical layer of the traffic links from the ATM network or through an external physical timing interface, e.g., 2 048 kHz);
- Timing from a free running clock (shall provide an accuracy according to relevant CBR service interface, e.g. 2 048 kbit/s shall comply to ITU-T Recommendation G.703 §6, ±50 ppm);
- SRTS;
- Adaptive timing.

Which timing option(s) to be supported are dependent on the services to be provided.

It is recommended to have slip control in the Tx direction to control possible over/underflow in the playout buffer. Slip shall be performed on $n \times 125$ microsecond frames.

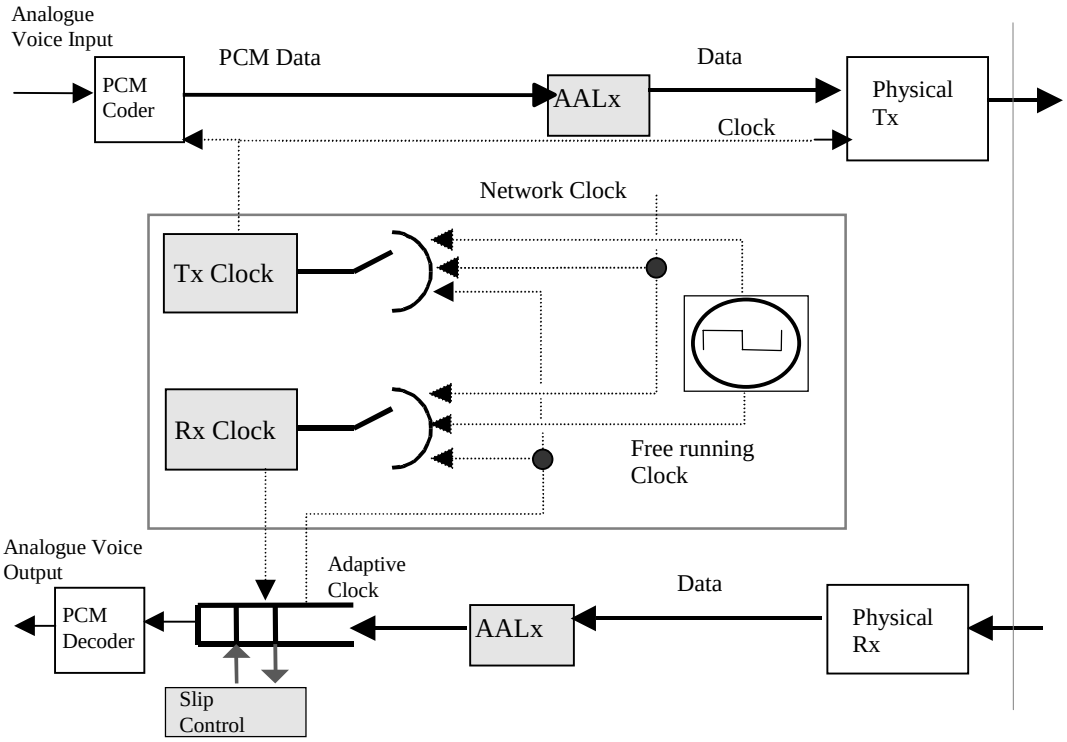
When AAL1 transmitter and/or receiver clocks are in holdover or are traceable to clocks in holdover, and a synchronous clock recovery technique (SRTS or Network synchronous operation) is used, slips (most likely uncontrolled) result. A back-up method based on the use of adaptive method may be used in order to avoid an excessive rate of slips. As mentioned in subclause 7.3, the adaptive clock recovery technique shall be properly designed.

The definition of a buffer threshold could be used to detect degraded synchronization function. However it shall be noted that large CDV could negatively affect this detection method.

9.2 Broadband Terminal Equipment (B-TE)

For the purposes of the present document, the native terminal equipment (B-TE) is defined as a device able to establish a communication through a B-ISDN on a per call basis.

In the example shown in figure 9 the main B-TE synchronization related functions for a voice service are described.



Rx = Receiving side to B-TE from the ATM Network
Tx = Transmitting side from B-TE to the ATM Network

Figure 9: B-TE Equipment model

There are three possible timing options for the operation of the PCM codec in the B-TE:

- Network Synchronous;
- Adaptive Method;
- Free Running.

The B-TE is required to have a free running clock. It may be used in a situation where a network clock signal is not available.

If the B-TE has access to a network clock, it shall synchronize both the Receiver and the Transmitter clock.

When no network clock is available, and

- if the B-TE does not receive any indication from the other end that it will use adaptive timing recovery, the B-TE shall perform adaptive timing recovery on both its RX and TX clocks if it has the capability to do so;
- if the B-TE receives an indication from the other end that it will perform adaptive timing recovery, the B-TE shall use the free running clock on its TX clock to avoid a timing loop. If the B-TE has two distinct clocks for the TX and the RX, it shall perform adaptive timing recovery on the RX clock if it has the capability to do so. If the B-TE only has one clock (RX and TX clocks are the same), the RX/TX clock shall be free running;
- if the B-TE does not have the ability to perform adaptive timing recovery, it shall use the free running clock on both RX and TX. This is the minimum requirement.

A B-TE using a free running clock requires provisions to cope with overflow or underflow in the CDV and reassembly buffer. The buffer is read out using the local free running clock but may be filled by the AAL receiver at higher or lower bit rate which is determined by the IWF or the other B-TE.

9.3 ATM Switch

Devices included in ATM network are ATM Switches and ATM multiplexors.

Two aspects are important in the ATM equipment regarding the synchronization of the physical layer: the possibility to be connected to a Synchronization Network and the possibility to maintain a defined quality level of the timing in case of failure in the synchronization distribution.

The timing for physical layer of ATM switches is derived from either an external synchronization interface (typically 2 048 KHz) or from the incoming traffic link(s).

The timing transported is normally PRC traceable. In case of failure of all the incoming timing reference signals, the quality of the timing, should fulfill the requirements of the relevant physical layer (see physical layer B-ISDN recommendation): that gives recommendation on the accuracy required for the clocks present in the equipment.

10 Results and Consequences of the Different Synchronization methods over multiple ATM Islands

In this clause are presented the main performances of the SRTS and Adaptive Clock synchronization methods when multiple ATM islands are crossed. No specific problems have been identified when Network Synchronous operation is employed.

10.1 SRTS Clock Recovery

Of the two methods currently recommended in ITU-T Recommendation I.363 [12] for the transfer of CBR service timing information between source and destination, i.e. SRTS *(Synchronous Residual Time Stamp*) and *Adaptive Clock*, only the first one has been specified in some detail: a description of the method can be found in ITU–T Recommendation I.363.1 [1] and I-ETS 300 353 [7]; more consideration to design aspects is given in "Synchronous Techniques for Timing Recovery in BISDN" (see Bibliography). Because of the intrinsic mechanism of SRTS, jitter and wander are introduced on the reconstructed service clock at the receiver, in a way very similar to conventional pulse stuffing. The accumulation of jitter and wander on E1 CBR service clock reconstructed at the output of multiple ATM islands that use SRTS method has been investigated by computer simulation, as described in the following clauses.

10.1.1 Simulations Models

Jitter Accumulation

In order to evaluate the jitter introduced in CBR services because of SRTS mechanism it is possible to resort to a fairly simple mathematical model "DS1 and DS3 Jitter Accumulation in a Network of ATM Islands with SRTS Timing Recovery - Initial Results" (see Bibliography). In reference "DS1 and DS3 Jitter Accumulation in a Network of ATM Islands with SRTS Timing Recovery - Initial Results" (see Bibliography) equations are given that allow to calculate unfiltered recovered time stamp intervals TC at the output of the ATM island: in order to simulate cascaded ATM islands it is necessary to take into account the source clock frequency recovery filtering as well. Therefore an unfiltered total phase is obtained integrating the sequence of TCs and then is filtered through a first order linear PLL: the first difference of PLL output (sampled at the nominal TS interval) eventually gives the filtered TCs.

Figure 10 shows the overall scheme of the simulations carried out based on the above ATM island model. The Service Clock block generates time stamp intervals of 3 008 service clock periods, taking into account possible frequency offset of the source: the source clock in the simulations was assumed to be noise free. Instead of performing a large number of independent simulations as in "DS1 and DS3 Jitter Accumulation in a Network of ATM Islands with SRTS Timing Recovery - Initial Results" (see Bibliography), a worst case approach was used, selecting a source clock frequency offset capable to produce a stuffing ratio ρ value close to 0 (or 1): it is well known, from the analysis of Duttweiler (see Bibliography), that this condition corresponds to the largest peak of waiting time jitter root mean square amplitude. For the simulations
ρ = 0,997 was chosen.

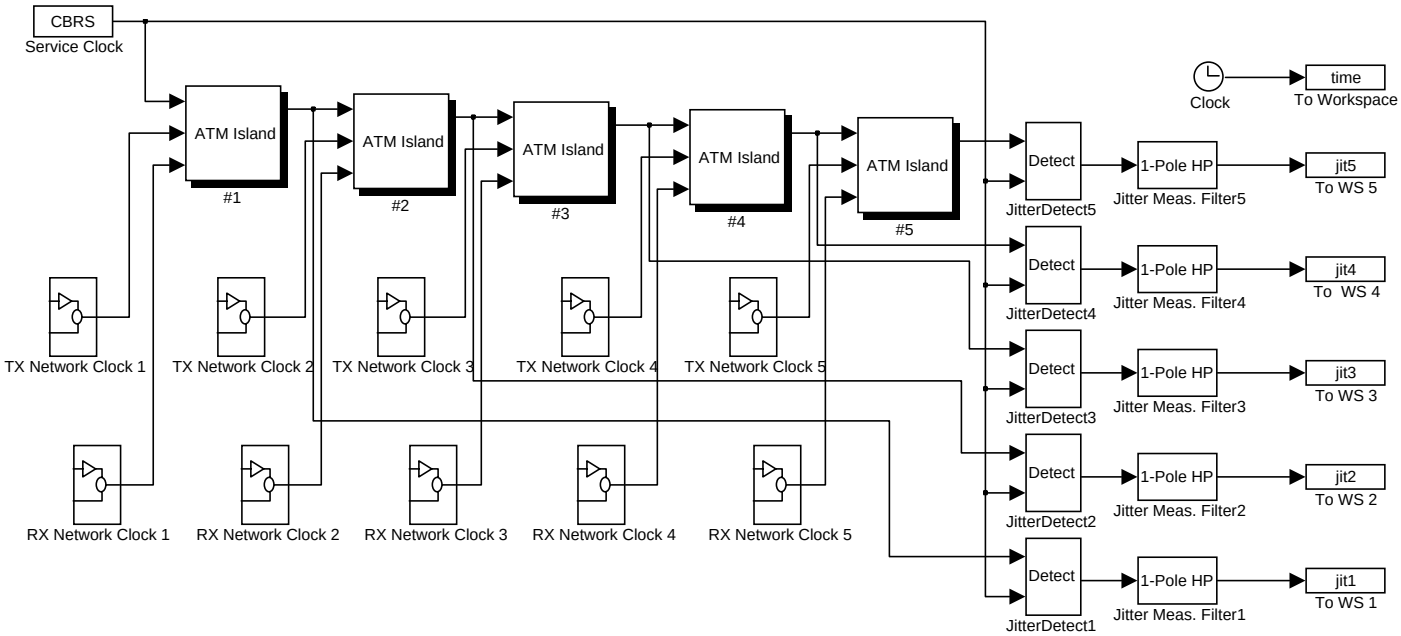


Figure 10: Overall scheme of the simulation for five cascaded ATM islands

Both transmit (TX) and receive (RX) Network Clock blocks generate time stamp intervals affected by phase noise that meets the mask in figure 11. This mask reproduces the network limit specification given in ITU–T Recommendation G.813 [10] for Option 2 clocks, which is roughly of the same value as the wander mask given in Recommendation EN 300 462-3-1 [2] at the output of SEC clocks. The noisy reference signal is passed through a 10 Hz low pass filtering: this cut-off frequency represents the upper limit of allowed SEC bandwidth according to EN 300 462-5-1 [4].

NOTE: Further simulation work is required in order to obtain a more accurate estimation of the distributed peak to peak wander.

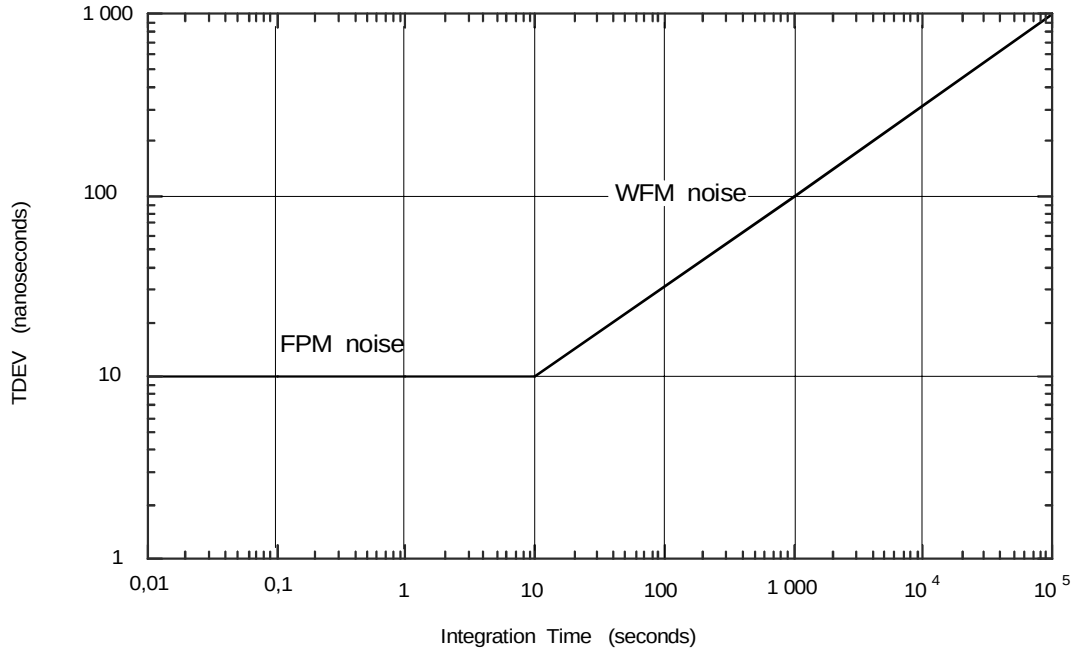


Figure 11: TDEV mask at the output of the Network Clock blocks in the simulation model

Finally, the Jitter Detect blocks calculate phase differences between each ATM island output and the source service clock, passing them on to 10 Hz high pass filters that remove any wander component prior to the peak-to-peak measurement: this last step is carried out off-line, during post-processing of stored data. An observation interval of 100 seconds was found a suitable compromise between execution time and data sample size to meet both manageable processing requirements and acceptable confidence level of the obtained results.

Wander accumulation

The evaluation of wander performance over observation intervals in the order of 24 hours using the above model would require unacceptably long run times, due to the sampling period equal to 1 time stamp interval: even for the bit rate of the E1 service, the time stamp interval is less than 2 milliseconds. However, it can be shown that at a first degree of approximation, the wander "waveform" resulting on the recovered service clock is roughly given by the differential wander waveform applied between TX and RX Network Clocks. Therefore it is possible to utilize a far simpler model for the accumulation of wander, as depicted in figure 12. Each island's operation on the incoming wander reduces to merely adding the difference between TX and RX Network Clock wander. Furthermore, due to the small bandwidth of wander waveforms it is possible to greatly reduce the sampling rate at which simulations can run with little degradation of peak-to-peak wander estimates: in deriving the results reported in subclause 9.1.3 a 1 second sampling period was chosen.

It is worthwhile noticing that the above wander accumulation model is independent of the service bit rate.

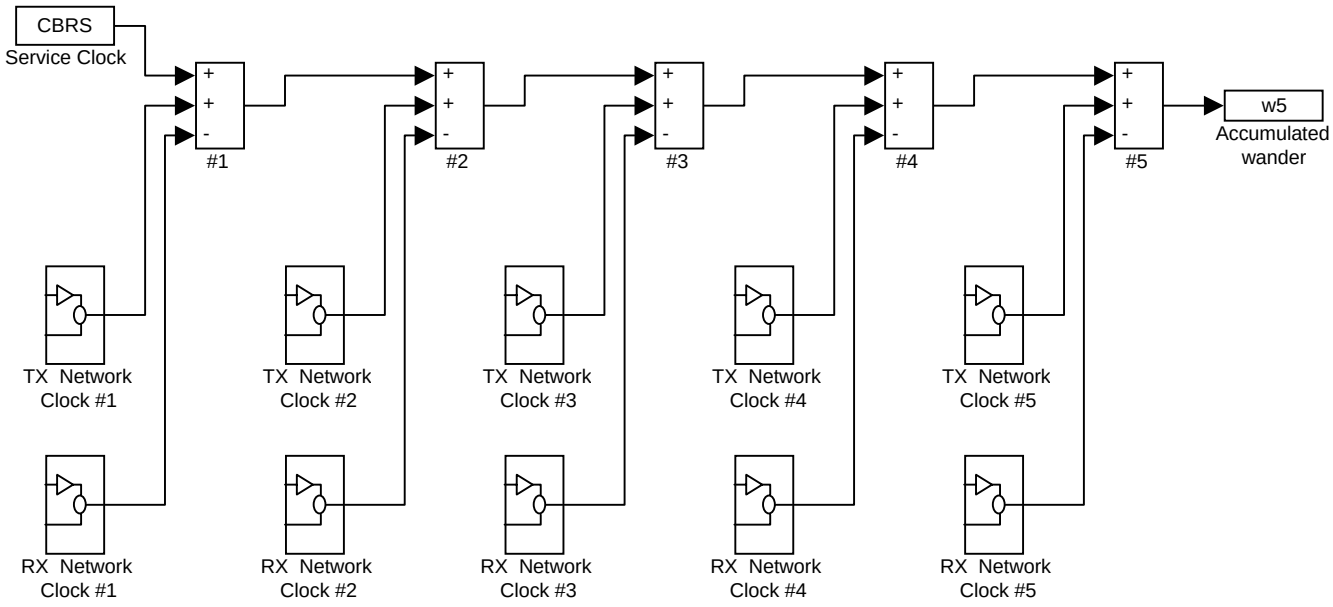


Figure 12: Simplified wander accumulation model of five cascaded ATM islands: each island simply adds to the incoming wander the difference between TX and RX Network Clock wander

10.1.2 Jitter Accumulation Results

For the E1 service transport, the following values apply:

$$N = 3\,008, \qquad F_s = 2\,048\,000, \qquad F_{nx} = 2\,430\,000 \tag{1}$$

$$M = \frac{NF_{nx}}{F_S\,(1+\delta)} \tag{2}$$

By numerical solution of the equation:

$$M - \lfloor M \rfloor = \rho \tag{3}$$

for $\rho = 0{,}997$, $\delta = 18{,}352$ ppm is found. Results for the peak-to-peak jitter are shown in figure 12 as a function of number of cascaded ATM islands, with source clock frequency recovery PLL bandwidth as a parameter. Taking into account the stringent requirement of 1,5 UI peak-to-peak jitter that applies for E1 service in existing ITU-T Recommendation G.823 [8], the results in figure 13 indicate that careful design is required in order to prevent exceeding total jitter limits that have already been specified.

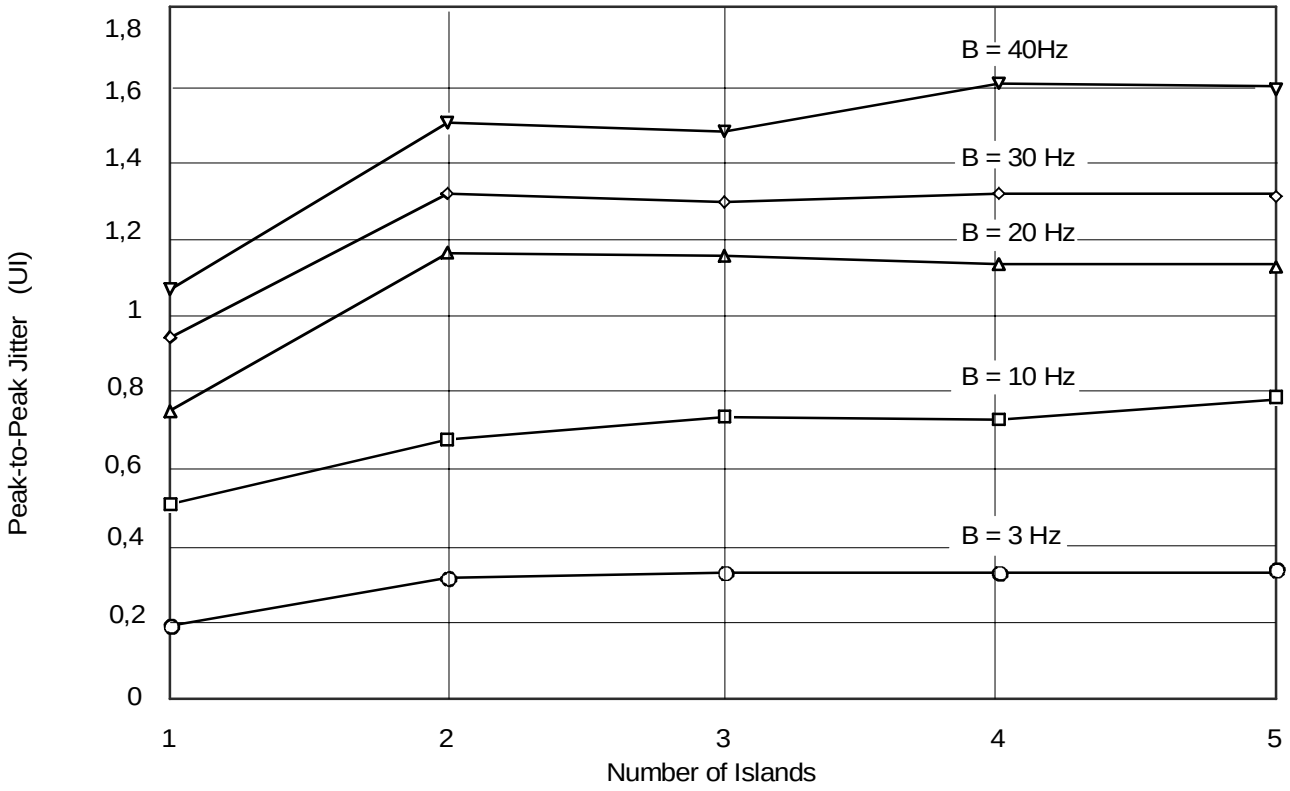


Figure 13: Results of peak-to-peak jitter on reconstructed E1 service at the output of cascaded ATM islands: the parameter for the set of five plots is source clock frequency recovery bandwidth

10.1.3 Wander Accumulation Results

To validate the simulation model for diurnal wander accumulation the case in which only WPM clock noise is present was first considered: this case has been investigated analytically by G. M. Garner (see Bibliography). In figure 14 results from 10 independent simulation runs are compared with analytical results from G. M. Garner showing that simulation results for one ATM island are well centered around the average and closely range from the 5th and the 95th Percentiles derived by mathematical analysis. The figure shows also that results well outside the theoretical range may occur for multiple cascaded islands even if a small number of trials (10 in the case at hand) is performed: this confirms that for a meaningful estimation of the distribution of peak-to-peak wander a much larger number of simulations (or measurements) should be carried out.

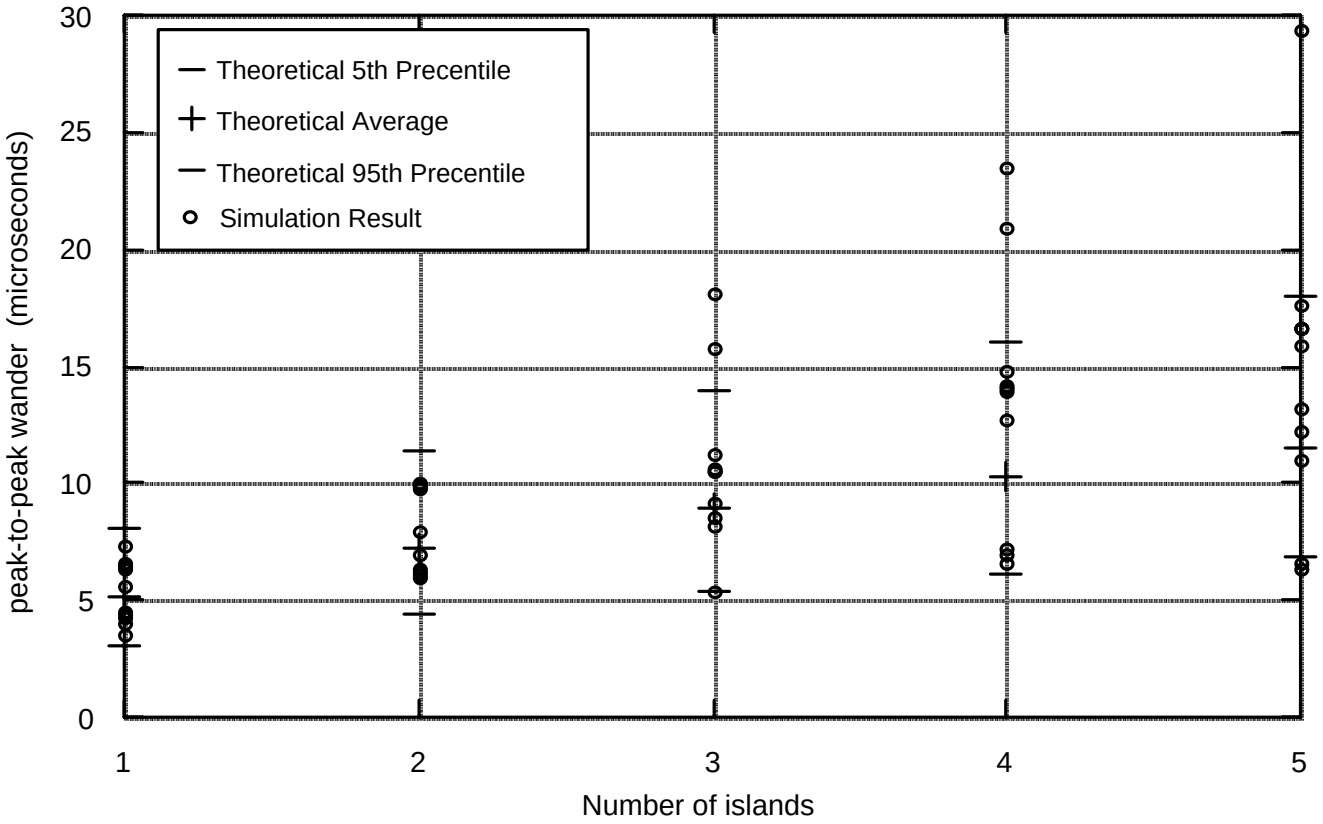


Figure 14: Results of peak-to-peak wander over a 24 hour observation interval at the output of cascaded ATM islands: WFM noise model

The wander accumulation model was run using the WFM + FPM clock noise of figure 11: results are shown in figure 15 against analytical results for WFM noise. The presence of FPM noise, at the level specified in current standards, slightly increases peak-to-peak wander measured over a 24 hours interval. Therefore, it is reasonable to use analytical results obtained for WFM noise as a first approximation.

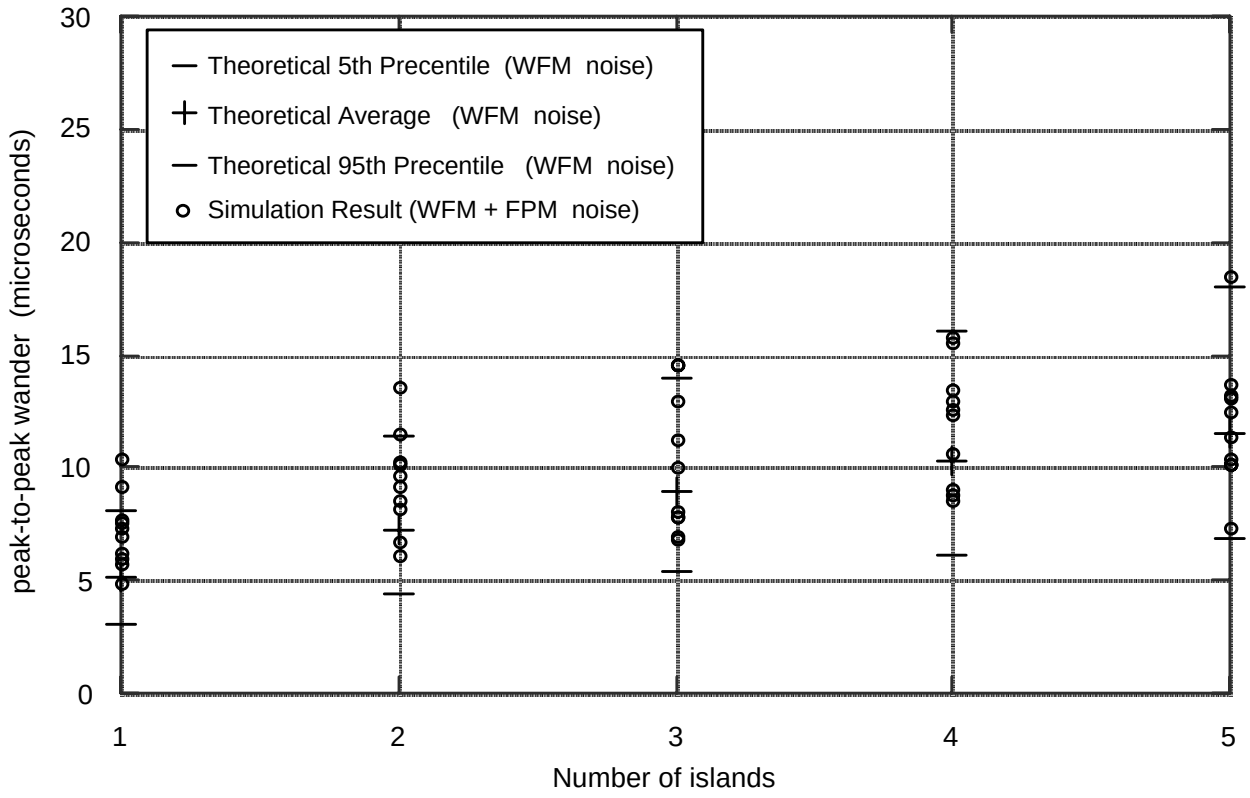


Figure 15: Results of peak-to-peak wander over a 24 hour observation interval at the output of cascaded ATM islands: WFM+FPM noise model

The major conclusion that can be drawn from results in figures 14 and 15 is that at the output of 3 multiple cascaded ATM islands a peak-to-peak wander as large as 15 microseconds may affect transported CBR services: recalling the 18 microseconds wander network limit specified in ITU-T Recommendation G.823 [8] to meet the wander tolerance requirement of slip buffering interfaces it is clear that transport of CBR services over ATM poses severe constraints on wander budgets from other portion of the network (i.e., PDH and SDH).

10.2 Adaptive Method Clock Recovery

The performance of ATM networks in transporting Constant Bit Rate (CBR) services with assigned quality of service is strongly dependent on a number of factors intimately connected with switch fabric design (such as switch architecture, buffering scheme and buffer discipline), traffic control mechanisms at different levels (connections, bursts, cells), and statistical characteristics of Variable Bit Rate (VBR) traffic contending with CBR traffic for the utilization of ATM switch resources (output buffers and links).

Two meaningful scenarios have been analyzed in the following chapters. The case of CBR and VBR traffic sharing the same ATM switch output buffer (subclause 9.2.1), and the case of dedicated output buffer for the CBR traffic (subclause 9.2.2).

10.2.1 CBR and VBR traffic sharing the same output buffer

Initial simulation results have been obtained based on the model shown in figure 16. In this figure it is shown a single ATM switch with one buffer per output port, five input ports (port #1 - #5) with 155,52 Mbit/s interfaces and one input port (port #6) with 2,048 Mbit/s interface. Port #1 is loaded with a VBR source multiplexed with a 2,048 Mbit/s CBR source (CBR1), port #2 - #5 are loaded with VBR traffic only, while port #6 is loaded with a 2,048 Mbit/s CBR source (CBR2).

All VBR sources generate bursts of cells of length and arrival time randomly distributed. All the incoming CBR and VBR cells are switched to the **same output buffer** (port #1) which is a simple infinite length FIFO without cell priority

management. The CBR1 cells are dropped from the outgoing stream and the associated time delay variations are "smoothed" through a low-pass filter simulating the action of a clock recovery circuit based on the adaptive method.

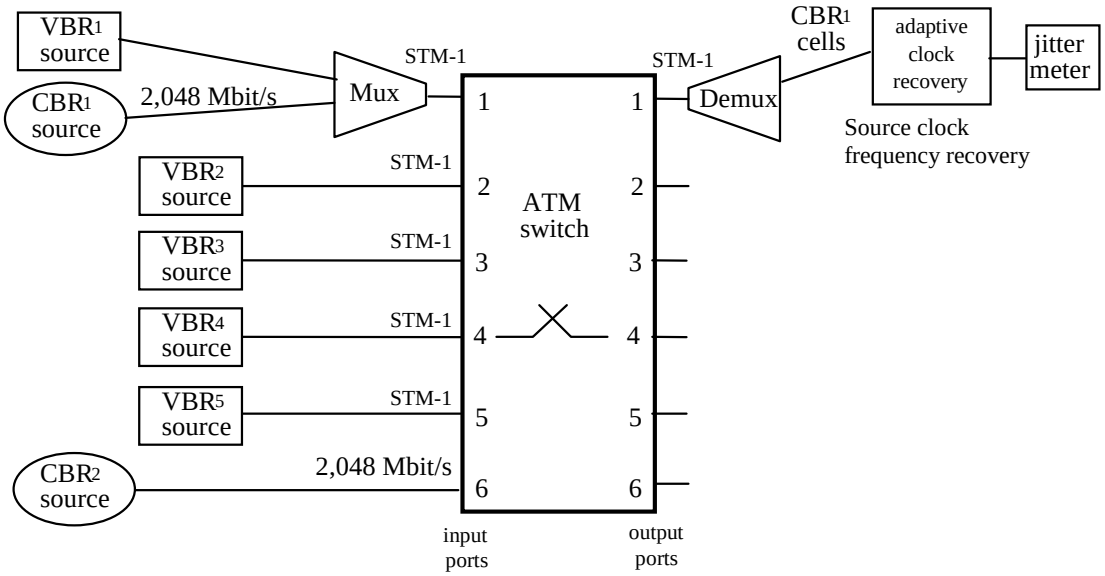


Figure 16: Simulation model

For the case considered, it appears that there is a strong influence of highest switch load (approaching the 90 % of the total traffic) and of the VBR traffic characteristics on CBR service jitter performance. It results in intrinsic difficulty in satisfying ITU-T Recommendation G.823 [8] jitter limit requirements, especially in case of bursty VBR traffic.

10.2.2 CBR traffic with dedicated output buffer

Some simulation results both for jitter and wander are provided for the case when CBR services use a dedicated output buffer in order to minimize cell delay variations. The simple structure of one single ATM switch has been considered.

At a first level of approximation the behaviour of the source clock frequency recovery, i. e. the equipment that implements the service clock recovery, has been modeled by means of a simple first or second order low pass filter.

A number of cases were considered assuming different CBR service rates and input port CBR traffic load, as summarized below:

- Case 1 - One single 2 Mbit/s service;
- Case 2 - Two 2,048 Mbit/s services;
- Case 3 - Six 2,048 Mbit/s services;
- Case 4 - One 2,048 Mbit/s service plus one 34 Mbit/s service;
- Case 5 - One 2,048 Mbit/s service plus two 34 Mbit/s services;
- Case 6 - One 2,048 Mbit/s service plus three 34 Mbit/s services.

The example of case 3 scenario is shown in figure 17 below. The clock sources for the six 2,048 Mb/s services have different frequencies but all of them are within the 50 ppm frequency accuracy limit.

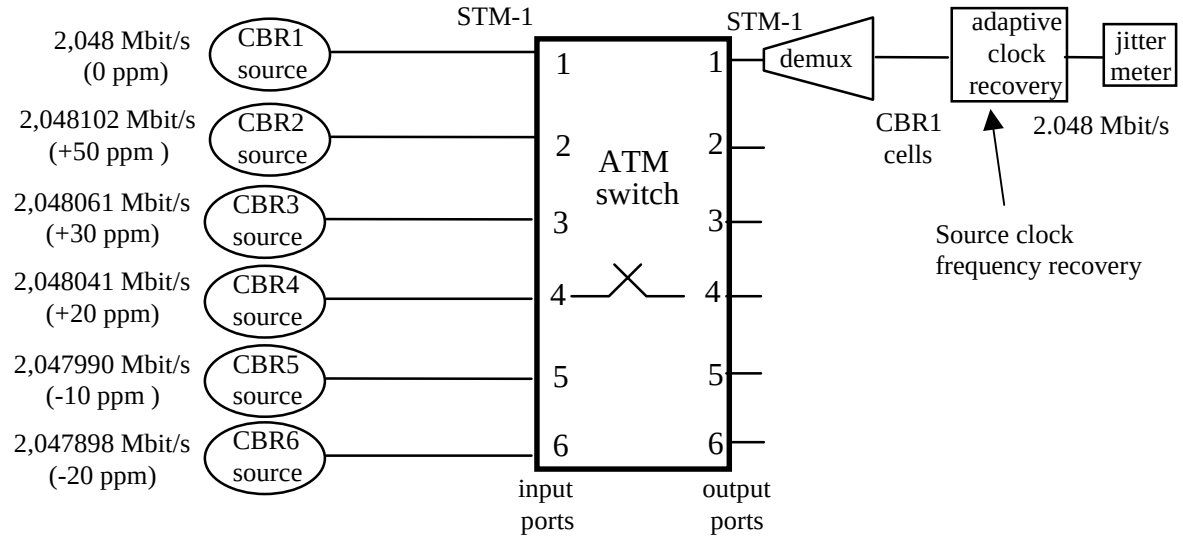


Figure 17: Simulation model for case 3

In figure 18 the peak-to-peak jitter results obtained in the case of first order source clock frequency recovery for the six cases considered are shown aiming at comparing the impact of different situations. From the figure we deduce that case 3 is the worst case for the jitter generation. This case (six 2,048 Mbit/s services) corresponds to a situation of low load at the output port of the switch (for this case equal to 8 %), with few input sources characterized by similar, but not equal, bit rates and with CBR service cells that contend the same switch output buffer. We further observe that in the case of higher traffic load at the output port of the switch (case 4, 5 and 6) the jitter magnitude maintains smaller values than those obtained for lower traffic load case.

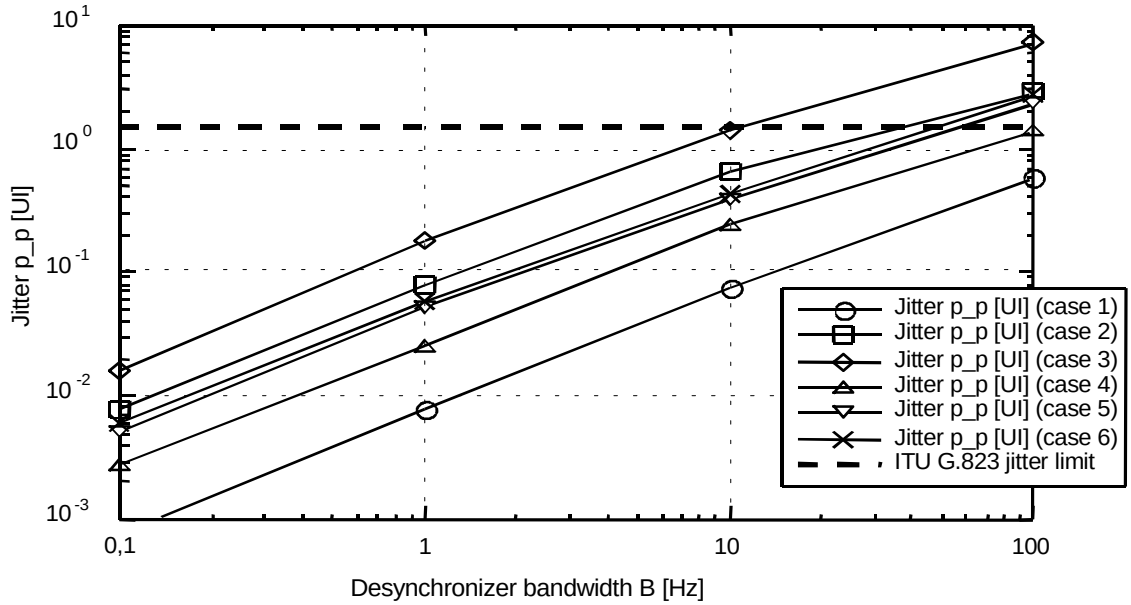


Figure 18: Comparison of peak-to-peak jitter values for the six considered cases as a function of the source clock frequency recovery bandwidth (first order source clock frequency recovery)

Preliminary wander measurements on the same 20 s long waveforms produced for the jitter analysis has been done.

This first partial results are reported in figure 19 for the case of a first order source clock frequency recovery. In the figure peak-to-peak wander performance are expressed in seconds. For comparison purpose the 9 µs value, currently set in EN 302 084 [9] for 2,048 Mbit/s interface as MRTIE limit for observation interval between 0,2 s and 32 s, is reported in the figure (dashed line).

From this initial results we can observe that the wander value obtained are not far from the wander limit currently standardized: we can argue that the wander performance in this case can be critical for a proper operation of the network and further analysis of the wander accumulation law for this case is necessary.

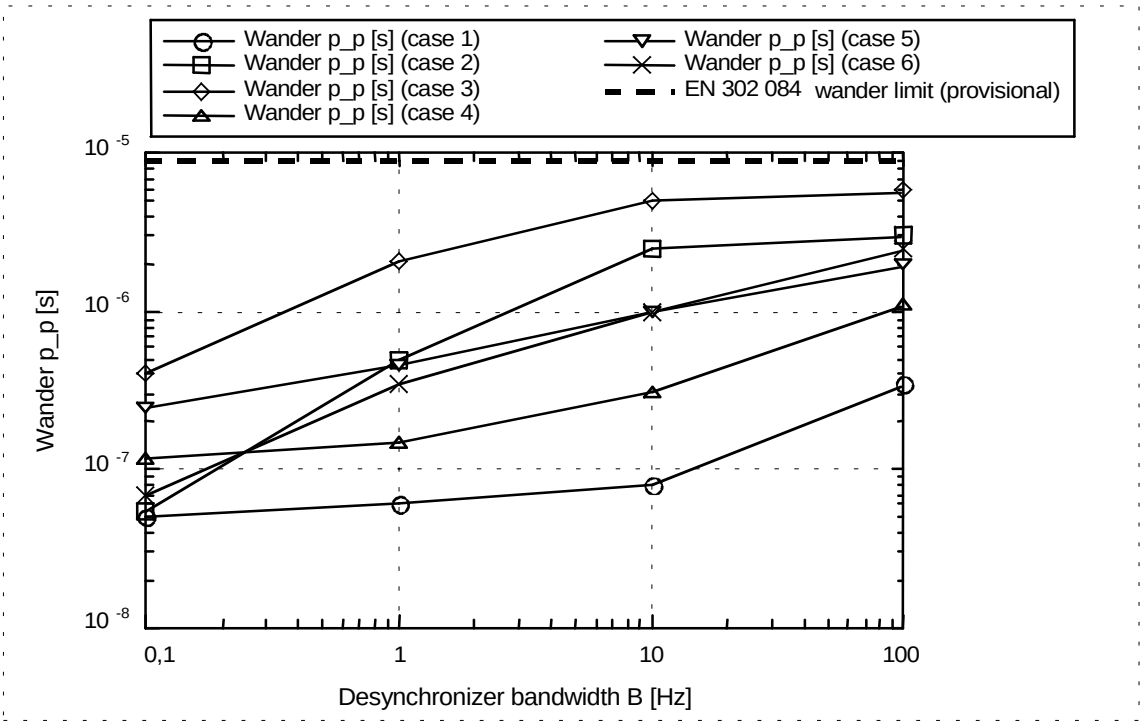


Figure 19: Comparison of peak-to-peak wander values for the six considered cases as a function of the source clock frequency recovery bandwidth (first order source clock frequency recovery)

NOTE: Further analysis would be required for the case of interconnection of ATM switches and ATM islands according to the reference model described in figure 3.

11 Application of the Synchronization Methods

The following synchronization options have been identified within an ATM network:

- Network-synchronous operation:

  this is the recommended method when traffic streams shall be merged and when interworking with PSTN. It is also the recommended method when a network clock is available at the IWF and the service user does not require timing transparency.

- SRTS synchronization:

  this is the recommended method when frequency transparency is required through an ATM network. It is also suitable for limiting the wander caused by CDV.

- Adaptive Timing:

  this method is recommended when long term frequency transparency through ATM network is required and there are no strong requirements on wander and temporary frequency offset (due to wander) at the service interfaces.

Annex A (informative): Services Requirements

A.1 Voice Services

In the design of the CBR connection, the max delays shall be contained according to the relevant recommendation (see for example ITU-T Recommendation G.114 [11] for requirements related to delays in the telephone connections). In the design of the ATM network, the total CTD and the added delay due to the buffering of the service data in the IWF, shall be accordingly considered.

A.1.1 Echo Canceller Requirements

Echo cancellation is a function typically implemented within STM network equipment, however when implementing an ATM network, echo canceller requirements shall also be considered.

Cell Transfer Delay (CTD) is the parameter mainly determining if echo cancellers are required. The clock recovery technique is also related to echo canceller requirements.

When an ATM network falls inside the echo tail of a voice connection, as in figure A.1, the CDV induced phase noise may be restricted to that of contemporary TDM networks by use of the appropriate synchronization technique (i.e. Network Synchronous operation or Synchronous Residual Time Stamp (SRTS)). However, recognizing that both techniques require the delivery of a relatively pure reference clock to both ends of the ATM network, and that in some instances this may not be possible - the use of adaptive timing may be considered provided that the residual phase wander is within the bounds of the echo canceller's phase noise tolerance. Further work is needed to check whether adaptive clock recovery techniques and the resultant residual phase wander will be compatible with echo canceller operation.

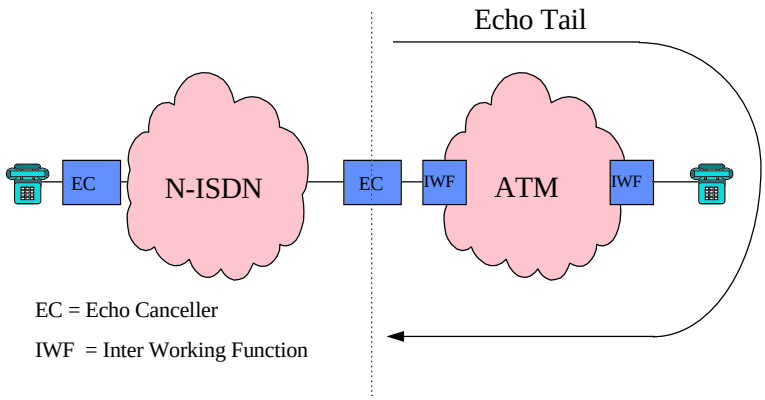


Figure A.1

Annex B (informative): Characteristics of Cell Delay variations for various loads and traffic

Many published papers model the characteristics of cell delay variation for various network reference models, network loads and traffic characteristics. Many make use of analytical queuing models, such as N × D/D/1 or M/D/1 models for a single switch, as a basis for network evaluation, others use numerical simulation techniques, and yet others attempt to load prototype ATM switches with 'real' traffic in an attempt to characterize the CDV likely to be incurred in a 'real' network. No one technique can exactly predict the performance expected of real networks since the network's characteristics will be dynamic and strongly influenced by the network operator's traffic management policies. For example, such a policy may dictate the traffic loads allowed by connection admission control (CAC), the service partitions, traffic shaping functions and the service dependant buffer management algorithms to be enacted for different services and differing qualities of service. For networks with switch output ports lightly loaded, little or no CDV would be incurred, whereas in networks where constant bit rate traffic is made to contend with large and varying switch loads, large cell delay variation can be expected. For each specific case the peak-to-peak CDV incurred by the service and its time-dependant characteristics will be very different. The onus is therefore on each network operator to ensure that its traffic management policy and simulation studies evolve towards a network design capable of meeting the requirements of each specific service that it offers on its ATM network.

For simulations attempting a worst case analysis, the M/D/1 queuing model, which assumes poisson arrivals and deterministic service time, is viewed by many as adequate for predicting worst case CDV.

As an example the waiting time distribution of an M/D/1 queue is given by:

$$Q(x) = \sum_{n>x}^{\infty} \frac{(\rho(n-x))^n}{n!} e^{-\rho(n-x)}(1-\rho)$$

and for ρ = 0,9 (i.e. a 90 %) switch load the peak to peak CDV (defined here as the 10^{-3} quantile for comparison with figure B.1a which comprises ~1 000 samples) is calculated as x = 34 cell times. For an STM-1 output port this equates to a peak to peak CDV of 96µs.

Such pessimistic results can be used to engineer robust buffer management policies. However, such analytical techniques give little information on the expected time-dependence of CDV since by default the models imply an essentially 'white' frequency spectrum for a static load. Numerical simulation techniques and 'real' measurements therefore provide the best opportunity to understand the frequency characteristics of CDV. The cell delay characteristics and CDV power spectral density resulting from a simulation of 2 Mbit/s CBR connection multiplexed with 15 other bernoulli traffic sources for a fixed total output buffer load of 90 % is shown in figures B.1a and B.1b below.

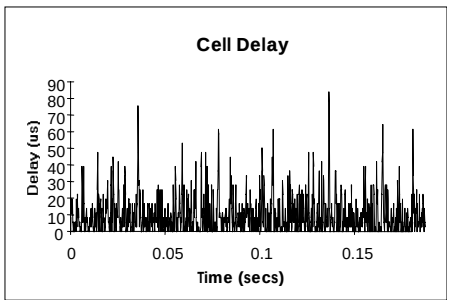


Figure B.1a

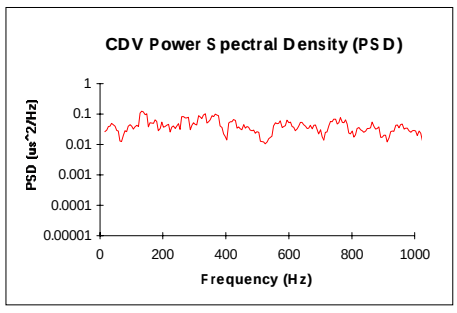


Figure B.1b

The limited results of the simple numerical model support the analytical model results in that an essentially 'white' power spectral density is predicted. However, caution has to be applied to such simplistic modelling. Models such as these again generally tend to evaluate the effects of a static load on the output buffer. Any slow changes in network load over the day could result in strong spectral lines at low frequencies. Any step changes in network load, contention of CBR streams with bursty variable bit rate streams or dissimilar rate CBR streams, or the effects of waiting time jitter can also result in strong spectral characteristics at both low and high frequencies. As an example figures B.2a and B.2b show the

effect of a step change in network load from 70 % to 90 % on the power spectral density. Low frequency components are now seen to dominate.

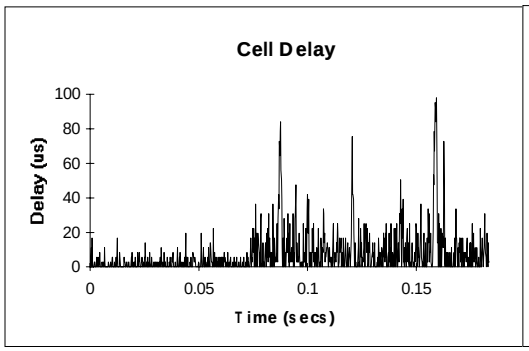


Figure B.2a

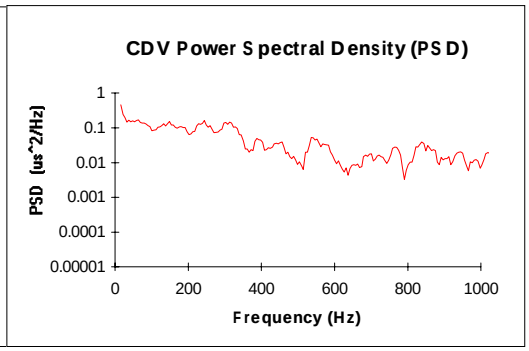


Figure B.2b

It is important therefore that not only are the cell level effects at static load understood but equally important is an understanding of the effects of network load statistics. Such effects can restrict adaptive clock recovery techniques to only selected CBR services in which the higher levels of jitter and wander can be tolerated.

Annex C (informative): SRTS

General implementation of SRTS method is shown pictorially in figures C.1 and C.2.

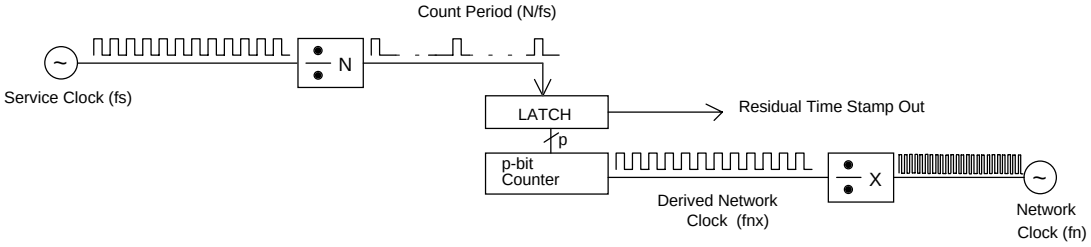


Figure C.1

- ***Synchronous Residual Time Stamp (SRTS)***

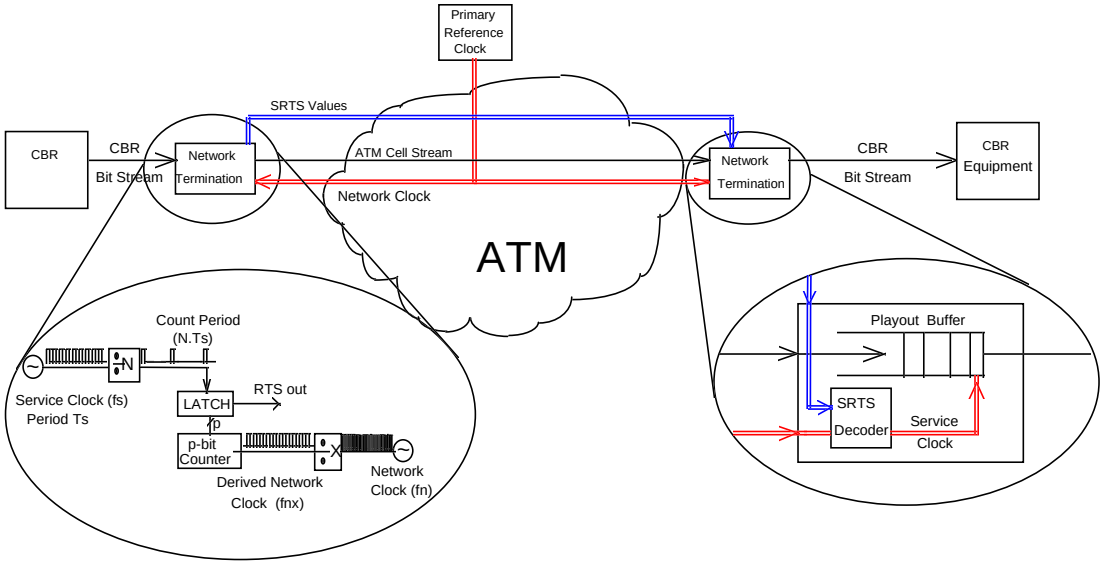


Figure C.2

NOTE: It should be noted that the distribution of the network clock, from the Primary Reference Clock to the IWFs, is not conveyed by the ATM layer network. It can be done either via the physical transport layer or via a separate synchronization network.

With SRTS the number of derived network clock cycles (fn/X) in N cycles of Service clock is counted in a p-bit counter and this p-bit SRTS value transmitted across the network to the receiving network terminating point. At the receiving terminal the local service clock can be adjusted against the reference network clock to ensure that the same number of derived network clock cycles are counted over the same N cycles of local service clock, thus locking the local service clock to the transmitter service clock by use of the received residual time stamps and the reference network clock.

For CCITT Recommendation G.702 [13], 1,544 Mbit/s and 2,048 Mbit/s based CBR hierarchies the value of N = 3 008 and a p = 4-bit SRTS value has been agreed and specified in ITU-T Recommendation I.363.1 [1].

The derived network clock f_{nx} is specified uniquely by assuming the existence of an 8 kHz clock derived from the network frame rate and constraining f_{nx} by the following:-

$$f_{nx} = 8\ \text{kHz} \times 19\ 440/2^{k} \text{ where } k = 0, 1, 2.....11$$

$$1 \leq f_{nx}/(f_s) < 2$$

The 4-bit SRTS value is transported over the ATM network as Convergence Sub-layer Indication (CSI) bits distributed alternately over 8 consecutive ATM cells using ATM Adaptation Layer Type 1 (figure C.3).

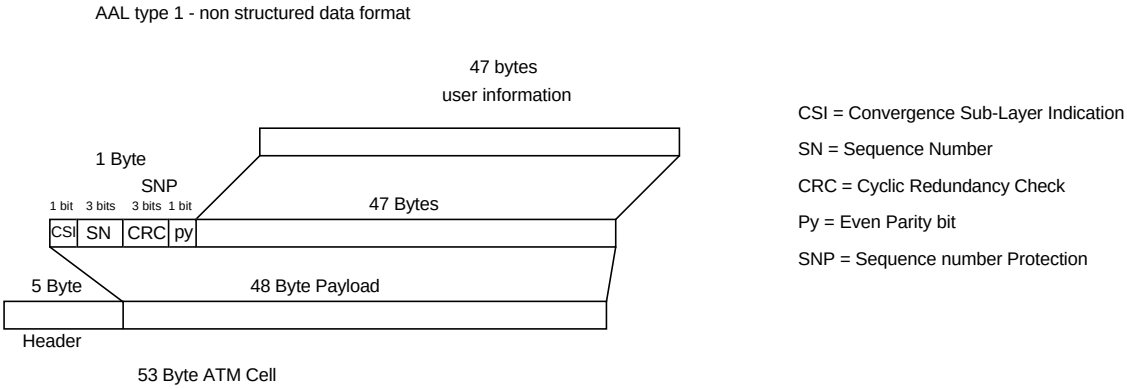


Figure C.3

The value of N = 3 008 has been chosen which corresponds to the number of AAL-type 1 user information bits in 8 ATM cells.

Since the nominal service clock frequency is known by both transmitter and receiver the full derived network clock count need not be sent. Hence the use of only 4 bits as a 'residual', or off-set, rather than full count. This residual count gives an indication of offset from nominal clock frequency. The use of 4-bits allows up to a ±200 ppm offset from nominal clock frequency.

The quantized nature of the residual time stamp will lead to slight clock imperfections at the receiver. The effect of quantization may be visualized by examining the implementation details for a specific service such as a 2,048 Mbit/s CBR service. In this particular implementation the derived network clock is specified, from the constraints given above, as 2,43 MHz. The number of derived network clock cycles in 3 008 service clock cycles is counted in 4-bit modulo 16 counter. For a 10 ppm offset service frequency the total count would be 3569,0268 derived network clock cycles. The 4-bit residual time stamp truncates this to 3 569 and sends the residual modulo-16 count of 0001 binary. With knowledge of the nominal service frequency the truncated derived-network-clock count of 3 569 can then be generated at the far end on reception of the RTS value 0001 binary. The service clock generated from this truncated value is given by 2,43 MHz × (3 008/3 569) = fs = 2,048 MHz + 17,5 ppm i.e. some 7,5 ppm in error due to the RTS quantization. This static frequency error and thus increasing phase error will continue until the partial clock counts of 0,0268 cycles per RTS period accumulate (over 1/0,0268 = 37 RTS periods) to greater than unity giving a 3 570 clock count and implied service clock frequency for this RTS value of fs = 2,048 MHz -262,6 ppm, this time -272,6 ppm in error from the transmit service clock. However, in this case over the long term of 37 RTS periods the average frequency information given = (37 × 17,5 ppm) - 262,6 ppm = +10,128 ppm, which begins to close in the true transmit service frequency. Thus by taking the longer term average of the RTS values the true underlying transmitted service frequency can be determined and tracked. The overall effect is best viewed by looking at the time dependant phase difference of the received service clock implied by the RTS values to the actual transmit clock. This is shown in figure C.4a below for the example just given. The induced phase transients in this particular case are sufficiently frequent that if necessary they could be reduced by a sufficiently long time constant in the phase locked loop being used to derive the receive service clock.

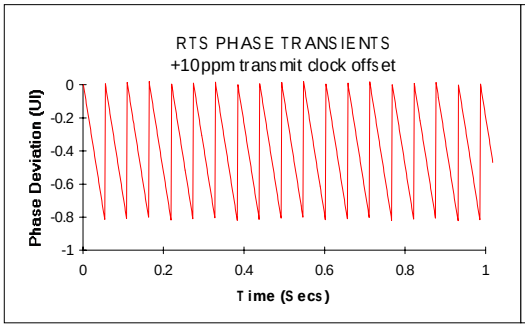


Figure C.4a

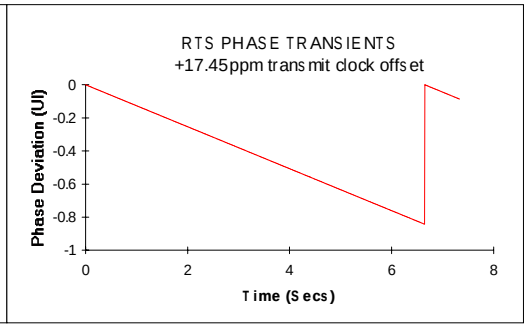


Figure C.4b

For certain values of service frequency, particularly where the derived network count is close to an integral number, the phase transients will become so infrequent that it becomes more difficult to filter them out, as shown in figures C.4b and C.5. It should be noted that figure C.5 represents a simulation and measurement comparison for a commercial Data Service Unit (DSU) with an E3 ATM UNI and an E1 circuit emulation interface. This DSU utilizes an early ITU-T Recommendation I.363 [12] implementation of SRTS.

In earlier versions of ITU-T Recommendation I.363 [12] the derived network reference clock frequency was not fully specified and this unit appears to use a now non-standard 34,368 MHz/16 = 2,148 MHz derived network reference clock. This gives rise to a slightly larger potential peak phase deviation of 0,9 UI which is exhibited by both the simulation and the measurement. The use of 2,148 MHz rather than the more recently defined 2,43 MHz for the derived network reference clock would make early ITU-T Recommendation I.363 [12] SRTS circuit emulation implementations incompatible with their more recent counterparts.

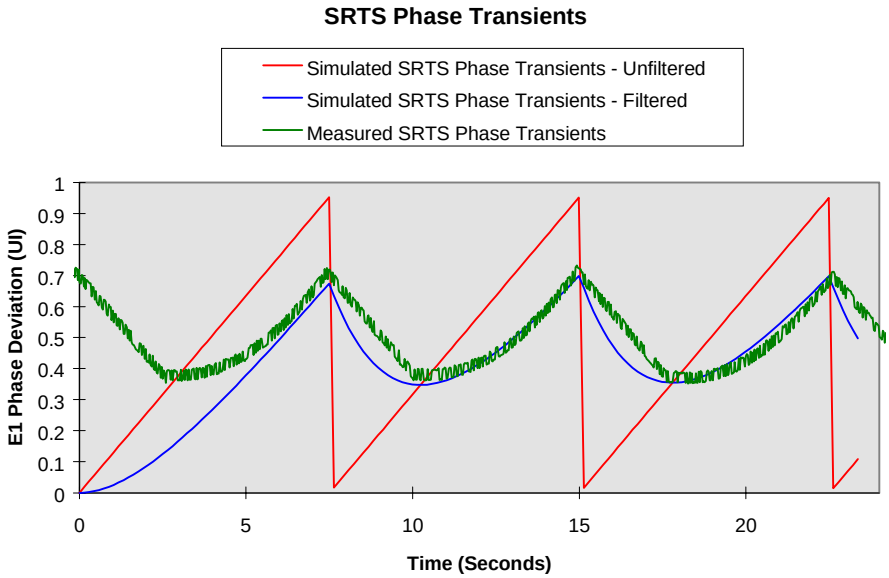


Figure C.5

Even for the case of the isolated phase transients the peak phase deviation falls inside of the ITU-T Recommendation G.823 [8] recommendation limits for wander and jitter on PDH interfaces. Therefore, provided a good quality network clock is delivered to the network interfaces the SRTS technique is capable of delivering third party timing across the ATM network within the jitter and wander constraints imposed by ITU-T Recommendation G.823 [8]. Such imperfections and the additive effect of service clock and network clock imperfections may however, make SRTS unsuitable for the transport of equipment clock quality signals - this is for further study. Also for further study is the actual specified quality level of the network clock needed at the ATM node responsible for Circuit emulation timing.

Annex D (informative): Adaptive Clock Method

The technique of adaptive clock recovery is depicted in figures D.1 and D.2 that serve as an introduction to the basic theme.

- ***Adaptive Clock Recovery***

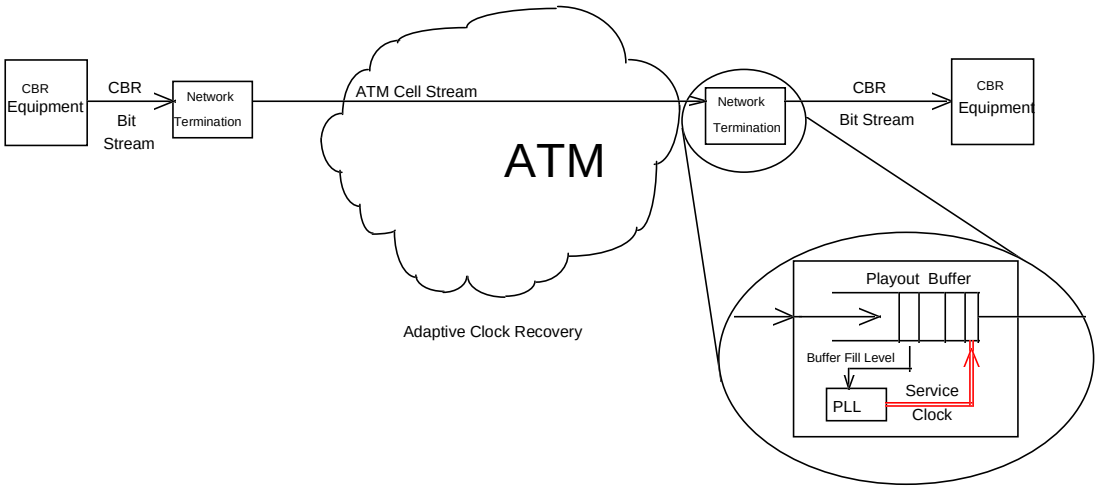


Figure D.1

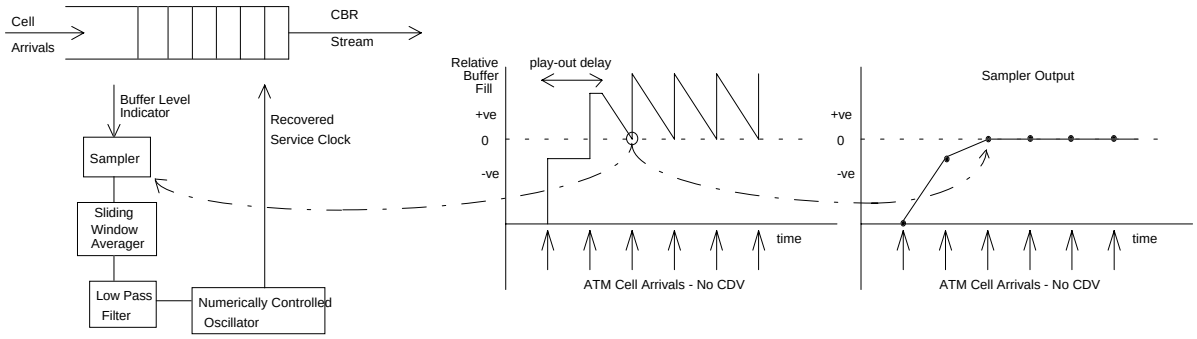


Figure D.2a **Figure D.2b** **Figure D.2c**

In general, adaptive clock recovery relies on the fact that, irrespective of the amount of delay variation experienced in the network, the CBR cell stream has an underlying average inter-arrival time. The job of any adaptive clock recovery mechanism is to extract this longer term average inter-arrival time from the 'noise' produced by both CDV and cell loss, and to use this as a basis for received service clock derivation.

The data buffer acts as phase comparator of the incoming cell stream and outgoing bit stream - the buffer fill level being the output of the phase comparison. Since on cell arrival the service bits are delivered 'in bulk' by the ATM payload the buffer fill varies in a 'saw-tooth' fashion as in figure D.2b, even in the absence of CDV.

If this waveform is sampled at the cell arrival rate, in the absence of CDV and/or waiting time jitter, and with the transmitting and receiving clocks locked the sampled values will be of constant value as in figure D.2c.

If the receiving clock is too slow compared to the transmitter the average buffer level will rise with time and the sample values would gradually increase in value as in figure D.3.

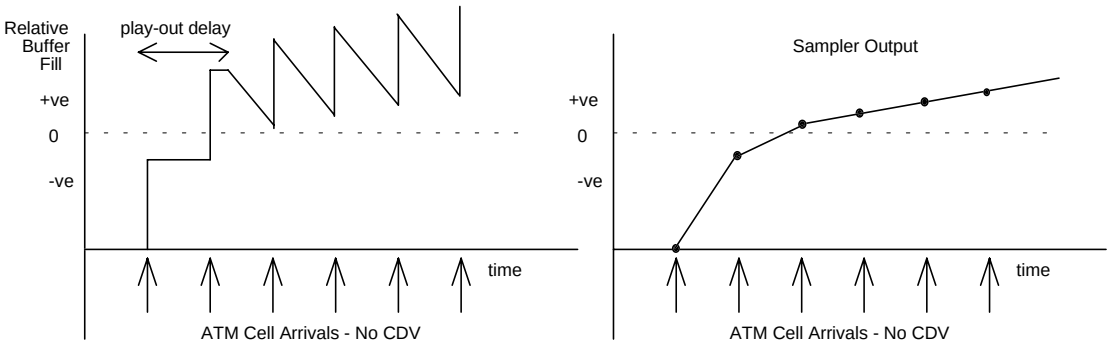


Figure D.3a **Figure D.3b**

This trend, once detected, can be used to increase the receive clock frequency to bring the buffer level back to a nominal value and lock-in the receiving clock to that of the transmitter. Unfortunately, the presence of CDV can obscure the underlying trend as shown in figure D.4 below.

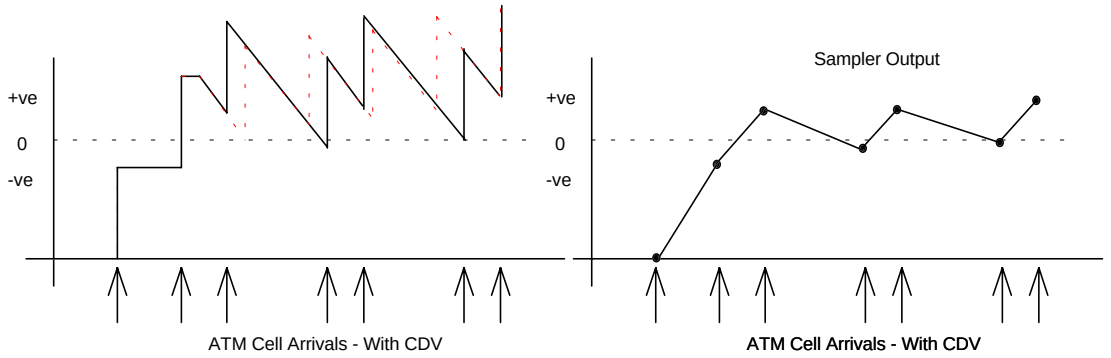


Figure D.4a **Figure D.4b**

The buffer level sample values cannot therefore be used directly but shall be filtered in such a way as to allow the recovered clock to react only to a mismatch of the transmitter to receiver clocks. In general such a mismatch would result in a continued increase or decrease in average buffer fill level over the averaging period. The adaptive recovery algorithm should ignore the relatively more rapid fluctuations around the longer term average due to CDV.

The adaptive clock recovery scheme therefore acts as a low pass filter. As a result low frequency CDV, as may occur due to a slowly cyclic or step change in network load, will be misinterpreted as a frequency mismatch, as shown in figure D.5. With low frequency CDV the buffer level will increase or decrease over the averaging period of the adaptive algorithm in much the same way as that due to transmitter-receiver mismatch. The adaptive recovery circuit will erroneously respond to low frequency CDV producing low frequency phase variation of the recovered clock in concert with the CDV.

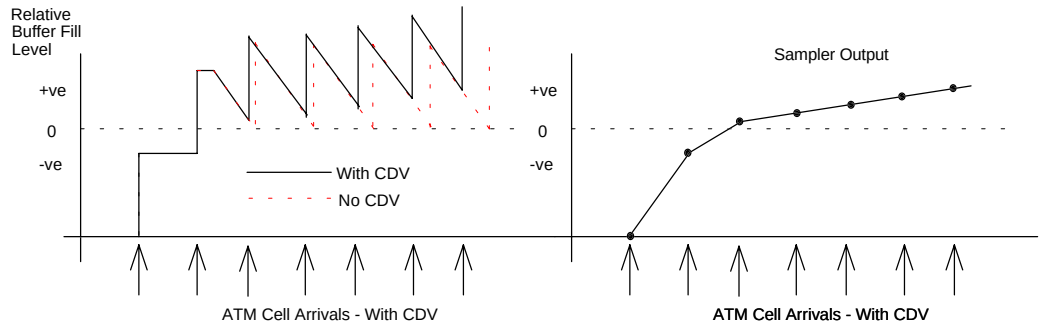
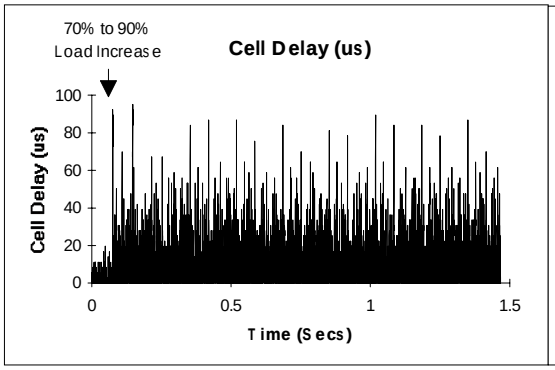


Figure D.5a **Figure D.5b**

To demonstrate this, the effect of the CDV characteristic of figure B.1a (and reproduced over a longer time period in figure D.6a) on a simulated 2,048 MHz adaptive clock recovery scheme is shown below in figures D.6a through D.7c.



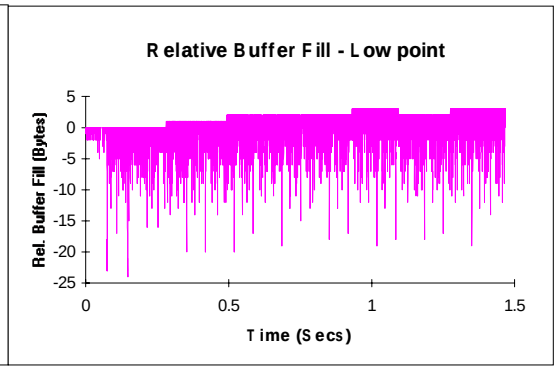
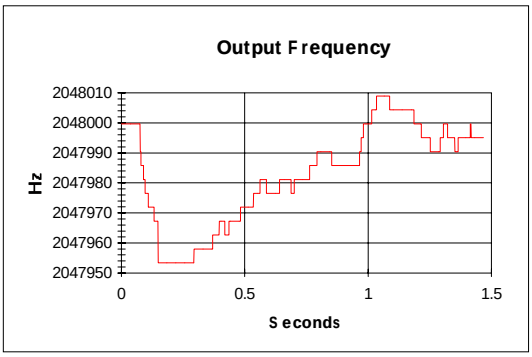


Figure D.6a **Figure D.6b**

The late cell arrivals in figure D.6a are reflected as low buffer levels in figure D.6b.

The output frequency deviation, total output phase deviation (wander) and jitter above 20Hz is shown in figures D.7a through D.7c respectively.



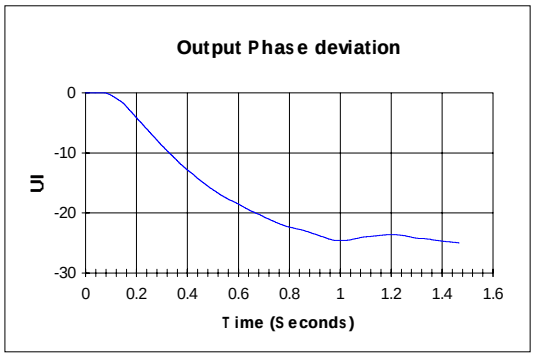


Figure D.7a **Figure D.7b**

The adaptive clock recovery mechanism can be seen to respond to the rms increase in cell delay when the switch load instantaneously increases from 70 % to 90 %. The rms increase in delay causes a general lowering of the buffer level and the output frequency is decreased momentarily to bring the mean buffer level back to normality. The frequency transient in this case causes a peak-peak jitter above 20 Hz of 0,5 unit intervals (UI) (figure D.7c) and a total output phase deviation equivalent to the increase in rms transport delay of 24,4 UI = 11,9 µs (figure D.7b). These results are for a single switch, in general the load characteristics for all switches through which the CBR cell stream pass shall be taken into account by the simulation and the peak to peak phase deviations due to network load variations will easily exceed the values shown here.

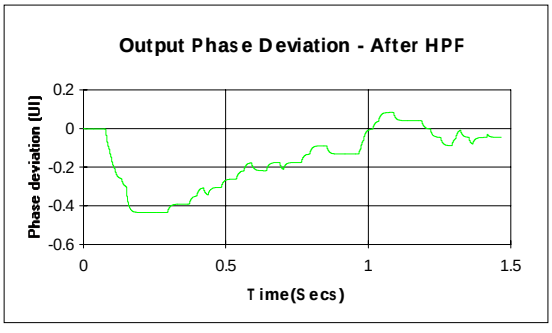
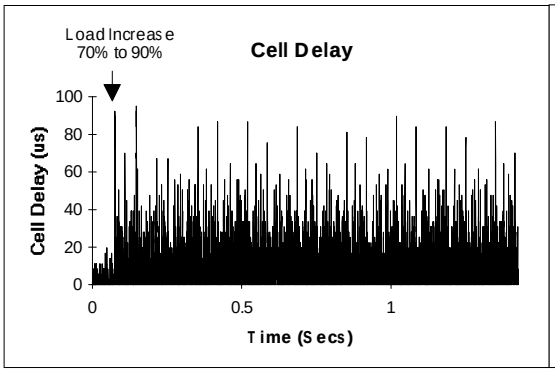


Figure D.7c

The numerical simulation model above had shown the 2Mbit/s output clock to track the slow changes in switch delay due to changing network load. The model had shown that for an increase in output port load from 70 % to 90 % the rms switch delay, for an STM-1 output port, would increase by 11,9 µs and that the 2,048 Mbit/s output clock phase would track this increased rms delay as shown in figures D.8 and D.9 respectively.

NOTE: 11,9 µs = 24,4 Unit Intervals (UI = Bit Periods) at 2,048MBit/s.



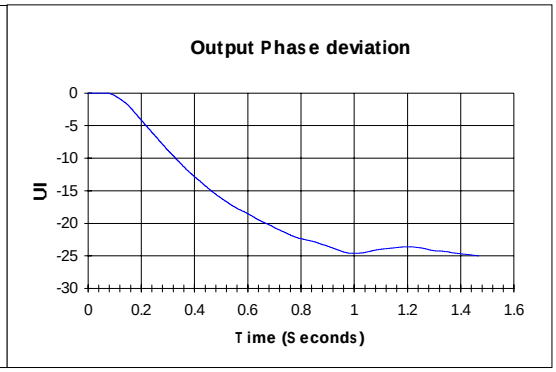


Figure D.8 **Figure D.9**

The mean (rather than rms) switch delay at 90 % load exhibited by the numerical model in figure D.8 was 10,1 µs. This result is supported by analytical analysis for an M/D/1 queue which gives the worst-case mean delay, $\lambda(\rho)$ in switch cell times, for a given load (ρ) as:

$$\lambda(\rho) = \frac{\rho}{2(1-\rho)} \quad (1)$$

Thus by equation (1) the increase in mean delay expected from a load of 90 % = $\lambda(0,9)$ = 4,5 cells = 4,5 × 2,83µs for an STM-1 output port = 12,75µs = 26 UI at 2,048 MHz.

It was expected therefore that if an output port of the ATM switch could be artificially loaded to, say 90 %, phase tracking, similar to that shown in figure D.8, ought to occur on the 2,048 Mbit/s CBR output of the adaptive clock recovery module thus causing the 2,048 Mbit/s output phase to wander in concert with longer term (sub. 1 Hz) load variations.

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History

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