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Contents

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Foreword

This European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunication Standards Institute (ETSI) in order to provide requirements for synchronization networks that are compatible with the performance requirements for digital networks. It is one of a family of ETSs covering various aspects of synchronization networks:

Part 1: "Definitions and terminology for synchronization networks" (ETS 300 462-1).

Part 2: "Synchronization network architecture" (ETS 300 462-2).

Part 3: "The control of jitter and wander within synchronization networks" (ETS 300 462-3).

Part 4: "Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment" (ETS 300 462-4).

Part 5: "Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment" (ETS 300 462-5).

Part 6: "Timing characteristics of primary reference clocks" (ETS 300 462-6).

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1 Scope

This third part of ETS 300 462 outlines requirements for the control of jitter and wander within synchronization Networks that are constructed according to the architectural principles described in ETS 300 462-2 [2]. A synchronization network that complies with the network limits for jitter and wander specified in this ETS will be suitable for the synchronization of Synchronous Digital Hierarchy (SDH) and Public Switched Telephone Network (PSTN) networks. It combines the short term stability requirements of SDH networks with the long term stability requirements of the PSTN. The values specified in this ETS refer to the design of new synchronization networks. They do not necessarily represent the performance of existing PSTN synchronization networks.

The network limits specified in this ETS form the network requirements from which the clock specifications in ETS 300 462-4 [3], ETS 300 462-5 [4] and ETS 300 462-6 [5] have been derived.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] prETS 300 462-1 (1996): "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1: Definitions and terminology for synchronization networks".

[2] ETS 300 462-2 (1995): "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2: Synchronization network architecture".

[3] prETS 300 462-4: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

[4] ETS 300 462-5 (1995): "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[5] prETS 300 462-6: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6: Timing characteristics of primary reference clocks".

[6] ITU-T Recommendation G.822: "Controlled slip rate objectives on an international digital connection".

[7] ITU-T Recommendation G.823: "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".

[8] ITU-T Recommendation O.171: "Timing jitter measuring equipment for digital systems".

[9] ITU-T Recommendation G.783: "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this ETS, the definitions given in ETS 300 462-1 [1] apply.

3.2 Symbols

For the purposes of this ETS the symbols and diagrammatic conventions described in ETS 300 462-1 [1] apply.

3.3 Abbreviations

MTIE	Maximum Time Interval Error
PDH	Plesiochronous Digital Hierarchy
PSTN	Public Switched Telephone Network
PRC	Primary Reference Clock
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SSU	Synchronization Supply Unit
STM-N	Synchronous Transport Module, level N
TDEV	Time DEViation
UTC	Universal Time Co-ordinated

4 Basic philosophy for the control of jitter and wander

The 300 462 series of ETSs describes the synchronization network as a logically distinct network layer with its own planning rules and performance requirements. The philosophy for the control of jitter and wander in the synchronization network layer is the same as applied to the payload carrying layers of the transport network, which can be found in ITU-T Recommendation G.823 [7]. It is based on the need to recommend a maximum network limit that should not be exceeded at any synchronization interface. This network limit represents the worst case accumulation of jitter and wander within the synchronization network reference chain shown in figure 5 of ETS 300 462-2 [2]. The main purpose for defining a network limit is that it provides the maximum amount of jitter and wander that any synchronization element in the network may experience at its input, since the network limit should not be exceeded at the output of a synchronization element anywhere in the network. The network limits therefore provide indirectly the requirements for the lower limit of maximum tolerable jitter and wander at the input of synchronization elements.

The wander tolerance of the large installed base of 64 kbit/s digital switches, i.e. the differential wander that a switch will tolerate before giving rise to controlled slip, together with the slip performance objectives stated in ITU-T Recommendation G.822 [6], have to be respected when introducing new transport technologies in the network. This differential wander is the cumulative effect of wander in the synchronization network and the wander that the transport of the data between switches may introduce. In the case of SDH, in most implementations, the latter is dependent on the wander that the SDH network elements experience at their synchronization inputs. The wander in a synchronization network that is also suitable for the synchronization of SDH therefore needs to be controlled to a level that is compatible with the slip performance objectives of the 64 kbit/s switched network.

It should be noted that the implication of the network limit definition is, that in practical networks the jitter and wander values at most synchronization interfaces should be well within the network limits, because the network limits will only appear at the end of a synchronization chain that is as long as the reference chain.

5 Synchronization interfaces

The synchronization interfaces that are specified in this ETS are depicted in figure 1. This figure is an expanded version of figure 6 of ETS 300 462-2 [2] showing examples of actual physical interfaces that may appear in synchronization networks. Universal Time Co-ordinated (UTC) is indicated in the figure as the reference relative to which all network limits are specified. Because of the way it is defined, there is no physical entity or interface associated with UTC. Two alternative synchronization distribution methods may be used between Synchronization Supply Unit (SSUs), and between Primary Reference Clock (PRC) and SSUs. SDH distribution makes use of the SDH section layer and may be a cascade of sections with at most 20 intermediate SDH network elements, each containing an SDH Equipment Clock (SEC). Plesiochronous Digital Hierarchy (PDH) distribution makes use of a 2 Mbit/s PDH path that may be traversing a number of intermediate PDH multiplexing stages and PDH line systems. These are not shown explicitly, because they do not contain clocks that are subject to this ETS.

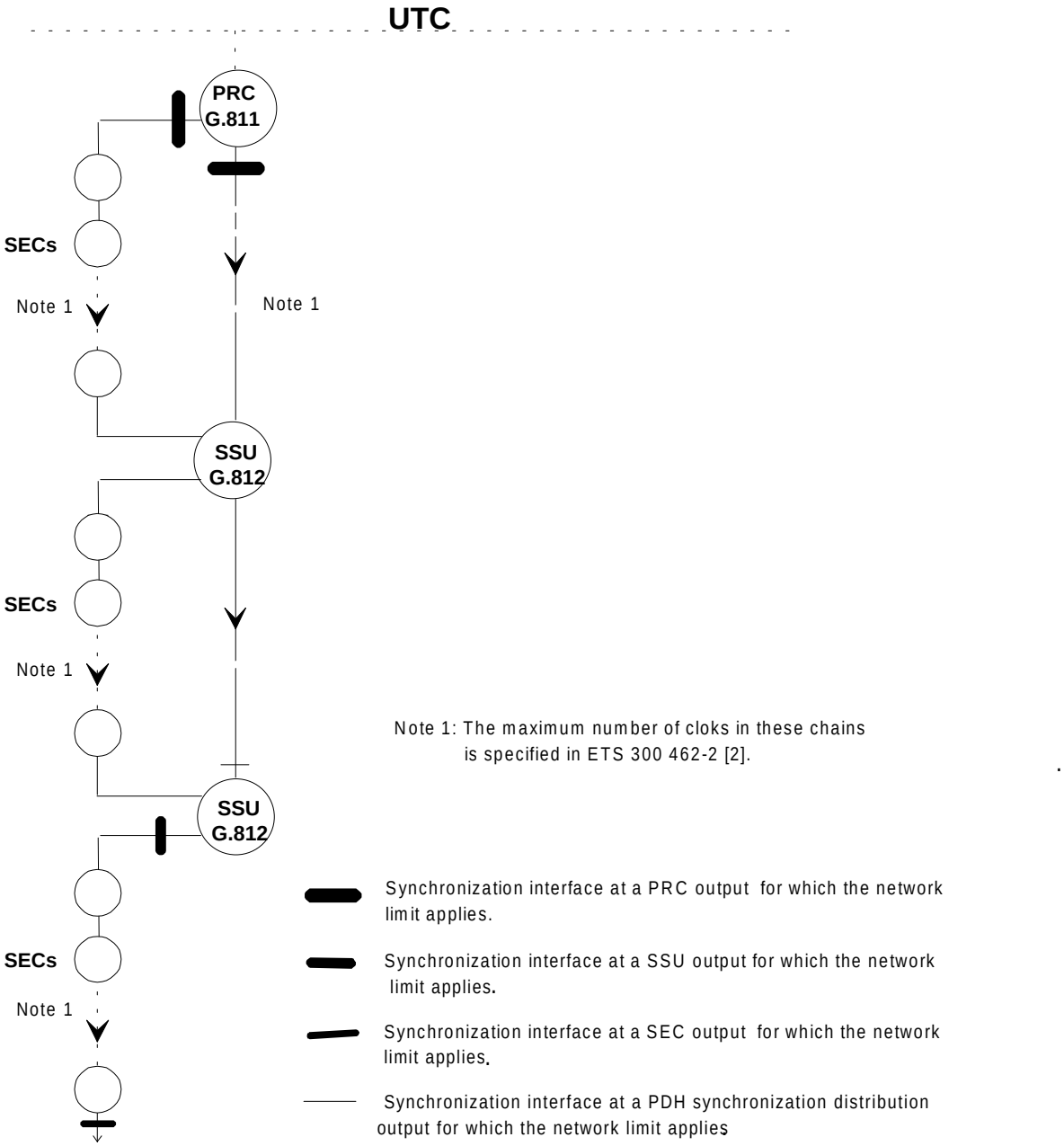


Figure 1: Synchronization reference chain showing where the network limits apply

Figure 1 shows that four types of synchronization interfaces can be distinguished in the synchronization network:

- synchronization interfaces at PRC outputs;
- synchronization interfaces at SSU outputs;
- synchronization interfaces at SEC outputs;
- synchronization interfaces at PDH distribution outputs.

This ETS therefore provides four sets of network limit requirements, one for each type of interface.

6 Synchronization reference network

The synchronization reference chain defined in figure 5 of ETS 300 462-2 [2] has to support not only a homogeneous SDH transport network, to which the transport network will evolve sooner or later, but also the evolution towards an all SDH transport network. In the transitional period, a mixed situation will exist where data paths may traverse both PDH and SDH sub-networks. The additional PDH/SDH mappings give rise to an increase of the wander that the data path is experiencing because the wander that appears at the output of one SDH island is passed on transparently through subsequent islands via the asynchronous mapping process. It is therefore the transitional period which puts the most stringent requirements on the performance of the synchronization network.

To provide for consistency between the specifications of the individual synchronization elements and the network limits an iterative process has been followed. The accumulation of wander in the synchronization reference network has been calculated based on a set of assumptions on:

- the number and performance of individual synchronization elements;
- the number and size of transients in the synchronization network;
- the level of diurnal wander.

The resulting quality of the synchronization network has then been applied to a reference model for the data path of four synchronous islands. Subsequently, the set of assumptions has been varied until a combination was found that met the requirement for the average differential wander experienced by a slip buffer terminated equipment (e.g. a 64 kbit/s exchange) of less than 18 μs measured over one day. The assumptions that were found to meet this requirement are documented in annex B.

It is stressed however that many other combinations of assumptions are conceivable that will comply with the network limits resulting from the set given in annex B. These are elaborated in this informative annex for guidance only. Provided these assumptions are fulfilled, the 18 μs wander limit will be met also across multiple operator domains.

A network operator may use a different set of rules, e.g. with a different number of SSUs and other assumptions about the transients in the synchronization chain, provided the synchronization network limits for jitter and wander specified in this standard are adhered to.

7 Network limits for jitter and wander at synchronization interfaces

The specification of network limits for synchronization interfaces is primarily intended to reflect the results of a theoretical analysis of the worst case accumulation of jitter and wander in a synchronization network. These values then serve to specify tolerance requirements for synchronization equipment. It should, however, also be possible to verify through measurements in a real network that a particular interface does not exceed the specified limits. The location of the interface in the synchronization chain of that network determines what margin may be expected with reference to the network limits.

As shown in figure 1, an SSU may receive its timing via SDH or PDH distribution. The network limit at the output of these distribution chains represents the amount of jitter and wander that an SSU may experience at its input. Since there is more jitter allowed at PDH interfaces than at SDH Synchronous Transport Module, level N (STM-N) interfaces, the network limit for the PDH distribution outputs represents the worst case that the SSU should tolerate at its inputs. The jitter and wander tolerance of a SEC should be (at least) the amount of jitter at the input of the last SEC of a synchronization chain. Since the contribution of the last SEC in the chain to the network limit at SEC outputs- that is the amount of jitter and wander that may be expected at the output of the last SEC of the chain - is small, the network limit in the SEC output can be used as the jitter and wander tolerance requirement for a SEC.

From the large number of available timing characteristics a subset has been selected to constrain both the standardization as well as the operational verification effort. The selected characteristics are considered to provide sufficient information to ensure satisfactory operation of PSTN and SDH networks.

7.1 Network limits for jitter

The maximum allowable high frequency noise components of a timing signal are specified by the network limits for jitter.

The theoretical arrangement for measuring output jitter at a synchronization interface is illustrated in figure 2. This figure does not imply an implementation. Jitter is measured using measurement bandwidths of f1-f4 and f3-f4 with first-order 20 dB/decade roll-off characteristics and shall not exceed the limits B1 and B2 indicated in table 1 when measured over a 60 second interval. More details about the measurement set-up can be found in ITU-T Recommendation O.171 [8].

Table 1: Network limits for jitter at PRC, SSU, SEC and PDH distribution outputs

Network limits at:	f1 [Hz]	f3 [Hz]	f4 [kHz]	B1 [UIpp]	B2 [UIpp]
PRC outputs	20	-	100	0,05	-
SSU outputs	20	-	100	0,05	-
SEC outputs	20	49	100	0,5	0,2
PDH distribution outputs	20	18 000	100	1,5	0,2
NOTE: For 2 Mbit/s and 2 MHz synchronization interfaces, UIpp refers to the reciprocal of the bit rate. For interfaces at other bit rates carrying synchronization the corresponding value in units of time applies.					

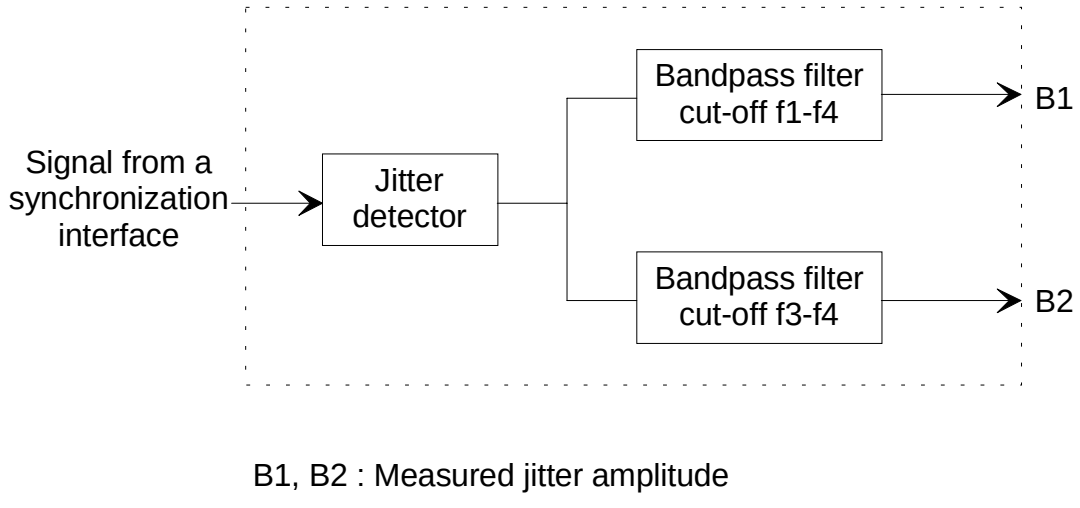


Figure 2: Theoretical measurement arrangement for jitter at a synchronization interface

7.2 Network limits for wander

The two timing parameters that have been selected to characterize transients and low frequency noise on a synchronization interface are Maximum Time Interval Error (MTIE) and Time Deviation (TDEV). Detailed definitions of MTIE and TDEV can be found in ETS 300 462-1 [1]. MTIE is considered useful to capture the phase transients in a timing signal, since it describes the maximum phase variation of a timing signal over a time period. MTIE is inadequate to show the underlying noise on the timing signal, because of its sensitivity to phase transients. Random noise is better characterized by TDEV which is an RMS power estimator instead of a peak estimator. TDEV tends to remove transients in a timing signal, and is therefore a better estimator of the underlying noise processes. To be strictly correct, transients and periodic components should be removed from data prior to calculating TDEV. This is not appropriate however for measurements on network interfaces since there is no a priori knowledge of the types of disturbances experienced in the timing signal. This means that it cannot be guaranteed that the TDEV results from processing of raw phase data truly reflect the random noise processes in a timing signal on a network interface, but they can provide a good estimate (refer to clause B.3, annex B, of ETS 300 462-1 [1]).

Wander is the result of random processes and therefore measurement results will vary over time and over the population of interfaces that is being considered. The network limits which are specified in this standard represent the 2 σ value of a set of measurements for a particular interface. In other words, 95 % of all measurements at any interface should be below the network limit masks for that interface.

The sampling time τ_0 and the anti-aliasing filter to be used for the measurement of MTIE and TDEV are provided in annex A**.**

At very low frequencies also, synchronization networks are transparent to wander. Consequently, two signals received in the same node that derive their timing from the same source but over different paths may in the worst case have opposite phase deviation. The minimum wander tolerance in the frequency range where relevant equipment is affected by the differential phase variation between two inputs is therefore higher than the network limit for absolute wander. The performance of a clock is only influenced by the phase variations that it is experienced at the selected synchronization input. That is why the absolute network limits in the subsequent sections can be used directly to specify jitter and wander tolerance of the SSU and SEC.

7.2.1 Network limits for wander at PRC outputs

The maximum wander that may be generated at the output of a PRC, expressed in MTIE shall not exceed the limits given in table 2.

Table 2: Network limit for wander at PRC outputs expressed in MTIE

MTIE	Observation Interval
25 ns	$0{,}1 < \tau \leq 83$ s
$0{,}3\ \tau$ ns	$83 < \tau \leq 1\,000$ s
300 ns	$1\,000 < \tau \leq 30\,000$ s
$0{,}01\ \tau$ ns	$\tau > 30\,000$ s

The resultant overall specification is illustrated in figure 3.

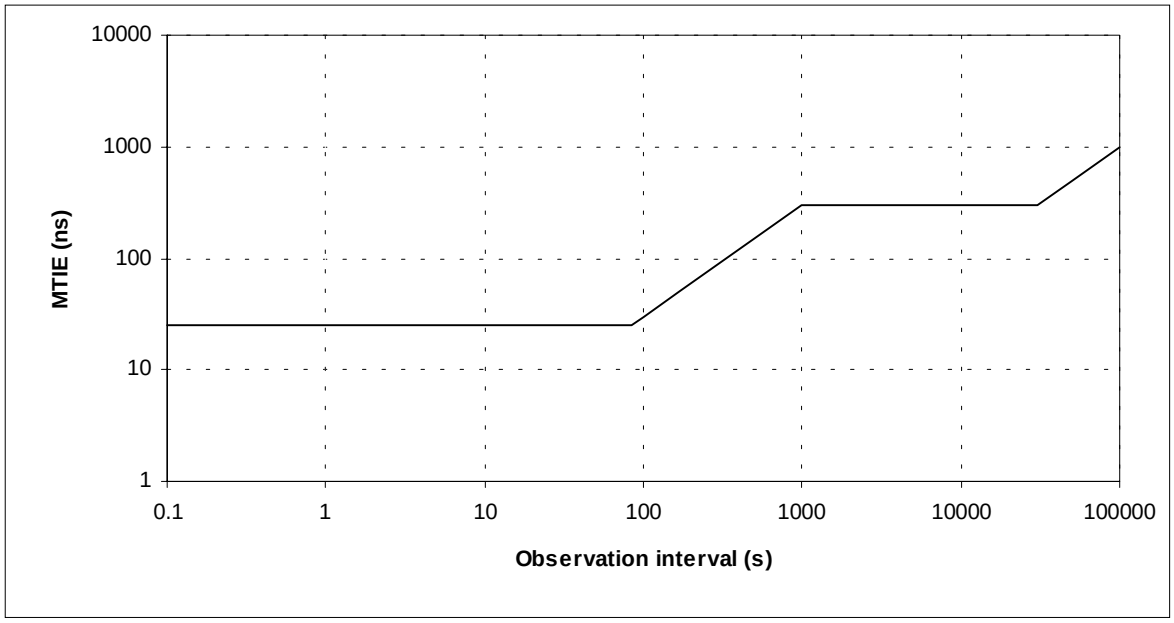


Figure 3: Network limit for wander at PRC outputs expressed in MTIE

The maximum wander that may be generated at the output of a PRC, expressed in TDEV shall not exceed the limits given in table 3.

Table 3: Network limit for wander at PRC outputs expressed in TDEV

TDEV	Observation Interval
3 ns	$0,1 < \tau \leq 100$ s
$0,03\ \tau$ ns	$100 < \tau \leq 1\ 000$ s
$29,7 + 0,000\ 3\ \tau$ ns	$1\ 000 < \tau \leq 1\ 000\ 000$ s

At observation intervals larger than 1 million seconds other effects than covered by the formula above play a role in PRCs. For this reason the TDEV specifications in this standard are truncated at 1 million seconds. For longer observation intervals the network limits are sufficiently characterized by the MTIE specification.

The overall specification expressed in TDEV is shown in figure 4.

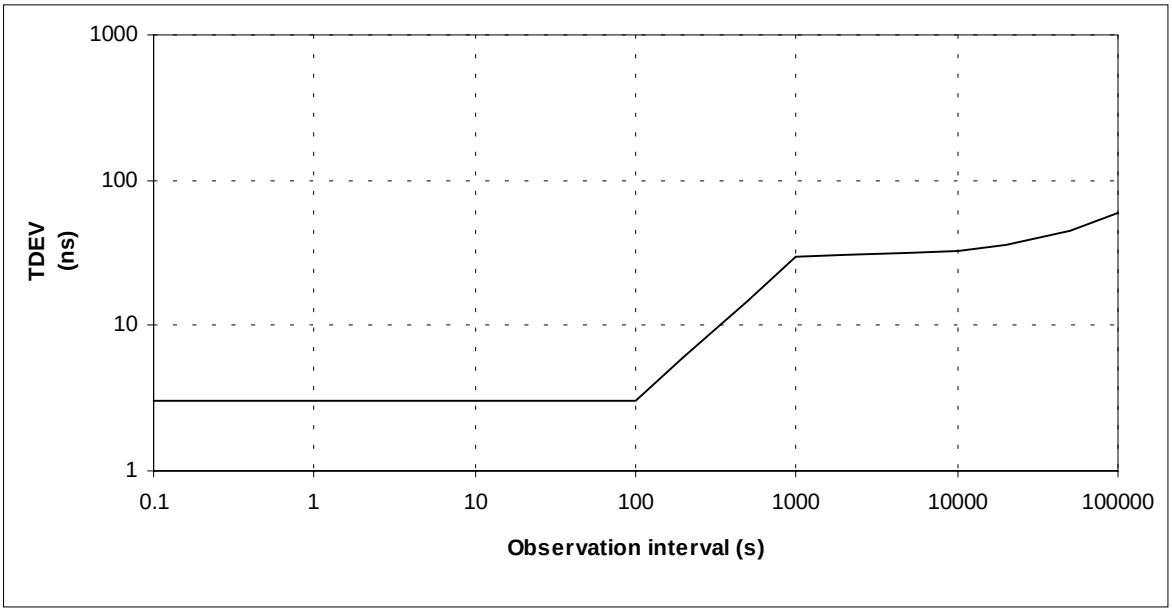


Figure 4: Network limit for wander at PRC outputs expressed in TDEV

7.2.2 Network limits for wander at SSU outputs

The maximum wander that may be generated at the output of an SSU, expressed in MTIE shall not exceed the limits given in table 4.

Table 4: Network limit for wander at SSU outputs expressed in MTIE

MTIE	Observation Interval
25 ns	$0,1 < \tau \leq 2,5$ s
$10\ \tau$ ns	$2,5 < \tau \leq 200$ s
2 000 ns	$200 < \tau \leq 2\ 000$ s
$433\ \tau^{0,2} + 0,01\ \tau$ ns	$\tau > 2\ 000$ s

The resultant overall specification is illustrated in figure 5. Note that the values are relative to UTC, i.e. they include the wander of the PRC.

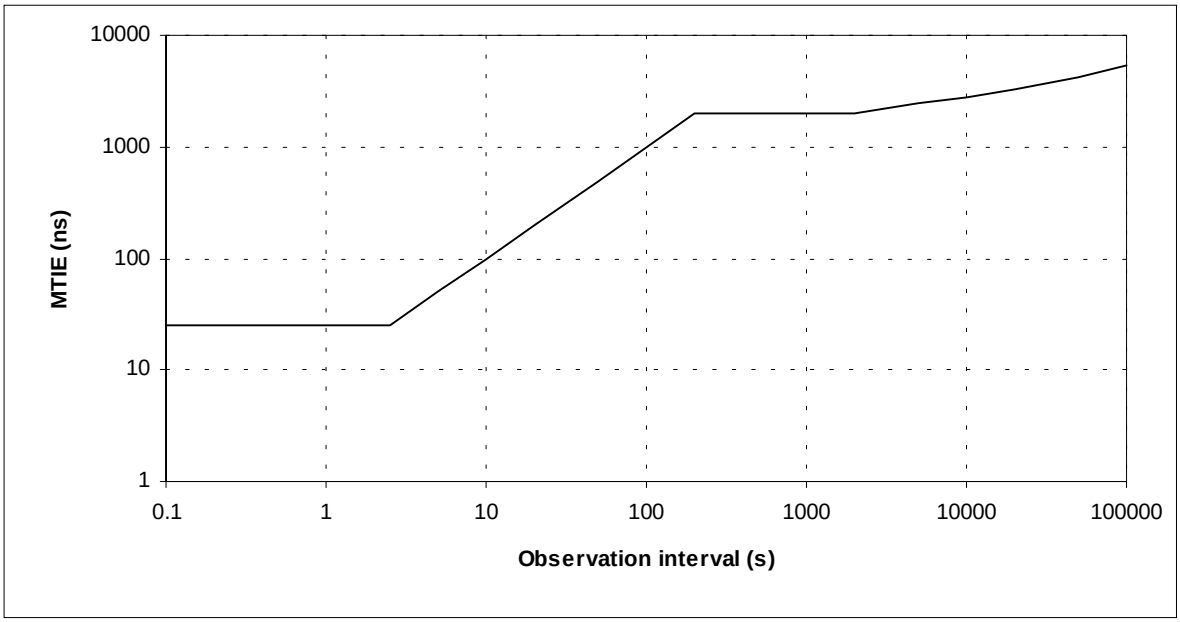


Figure 5: Network limit for wander at SSU outputs expressed in MTIE

The maximum wander that may be generated at the output of an SSU, expressed in TDEV shall not exceed the limits given in table 5.

Table 5: Network limit for wander at SSU outputs expressed in TDEV

TDEV	Observation Interval
3 ns	$0,1 < \tau \leq 4,3$ s
$0,7\ \tau$ ns	$4,3 < \tau \leq 100$ s
$58 + 1,2\ \tau^{1/2} + 0,000\ 3\ \tau$ ns	$100 < \tau \leq 1\ 000\ 000$ s

The resultant overall specification is illustrated in figure 6.

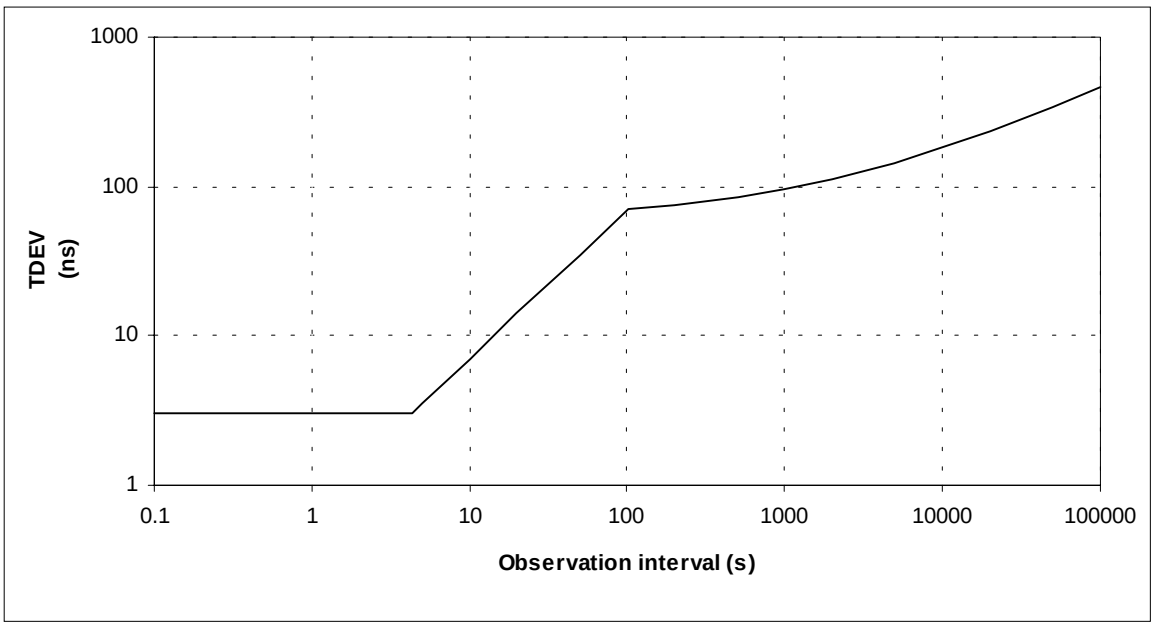


Figure 6: Network limit for wander at SSU outputs expressed in TDEV

7.2.3 Network limits for wander at SEC outputs

The maximum wander that may be generated at the output of a SEC, expressed in MTIE shall not exceed the limits given in table 6.

Table 6: Network limit for wander at SEC outputs expressed in MTIE

MTIE	Observation Interval
250 ns	$0,1 < \tau \leq 2,5$ s
$100\ \tau$ ns	$2,5 < \tau \leq 20$ s
2 000 ns	$20 < \tau \leq 2\ 000$ s
$433\ \tau^{0,2} + 0,01\ \tau$ ns	$\tau > 2\ 000$ s

The resultant overall specification is illustrated in figure 7. Note that the values are relative to UTC, i.e. they include the wander of the PRC.

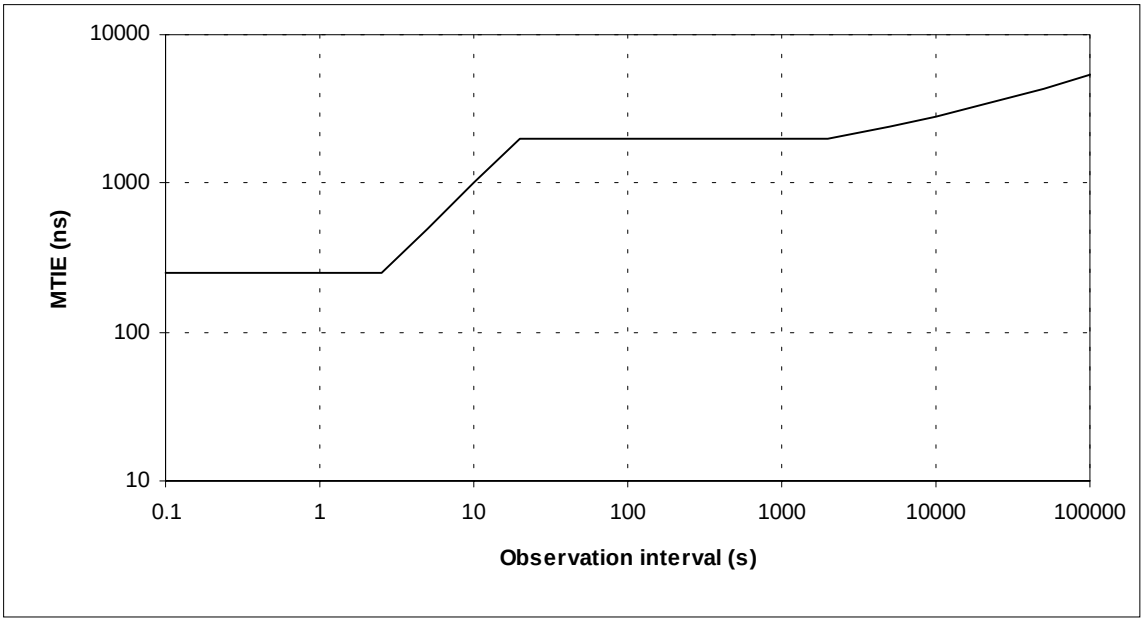


Figure 7: Network limit for wander at SEC outputs expressed in MTIE

The maximum wander that may be generated at the output of a SEC, expressed in TDEV shall not exceed the limits given in table 7.

Table 7: Network limit for wander at SEC outputs expressed in TDEV

TDEV	Observation Interval
12 ns	$0,1 < \tau \leq 17,14$ s
$0,7\ \tau$ ns	$17,14 < \tau \leq 100$ s
$58 + 1,2\ \tau^{1/2} + 0,000\ 3\ \tau$ ns	$100 < \tau \leq 1\ 000\ 000$ s

The network limit for wander at a SEC output expressed in TDEV is shown in figure 8.

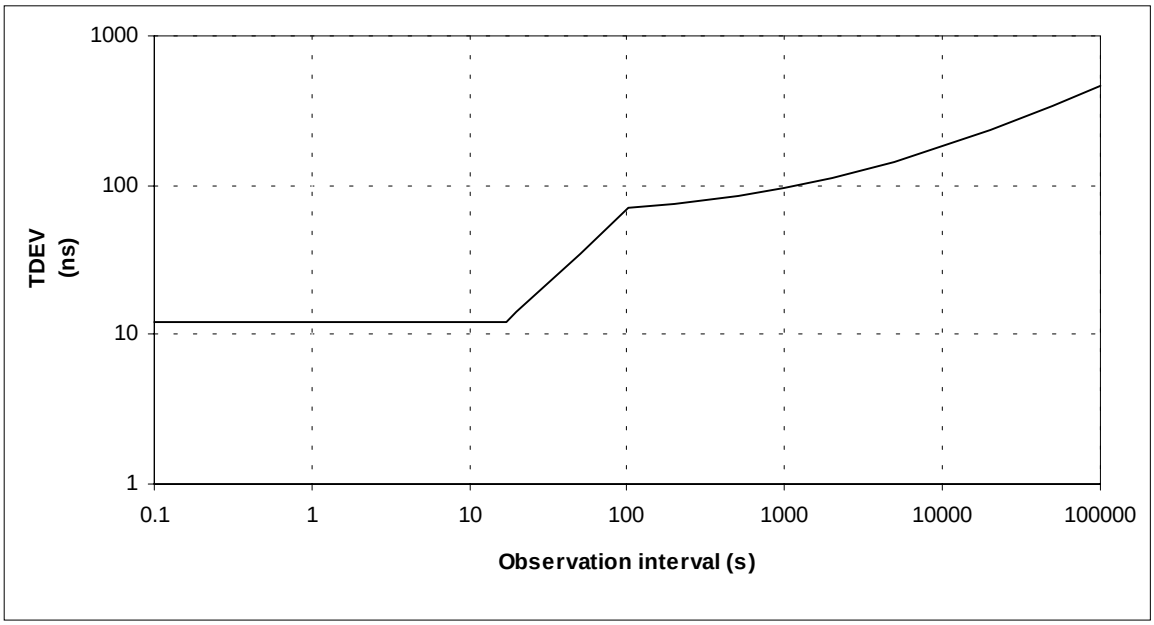


Figure 8: Network limit for wander at SEC outputs expressed in TDEV

7.2.4 Network limits for wander at PDH distribution outputs

The maximum wander that may be experienced at the output of the PDH distribution outputs, expressed in MTIE shall not exceed the values given in table 8.

Table 8: Network limit for wander at PDH distribution outputs expressed in MTIE

MTIE	Observation Interval
732 ns	$0{,}1 < \tau \leq 7{,}3$ s
$100\ \tau$ ns	$7{,}3 < \tau \leq 20$ s
2 000 ns	$20 < \tau \leq 2\,000$ s
$433\ \tau^{0,2} + 0{,}01\ \tau$ ns	$\tau > 2\,000$ s

The resultant overall specification is illustrated in figure 9.

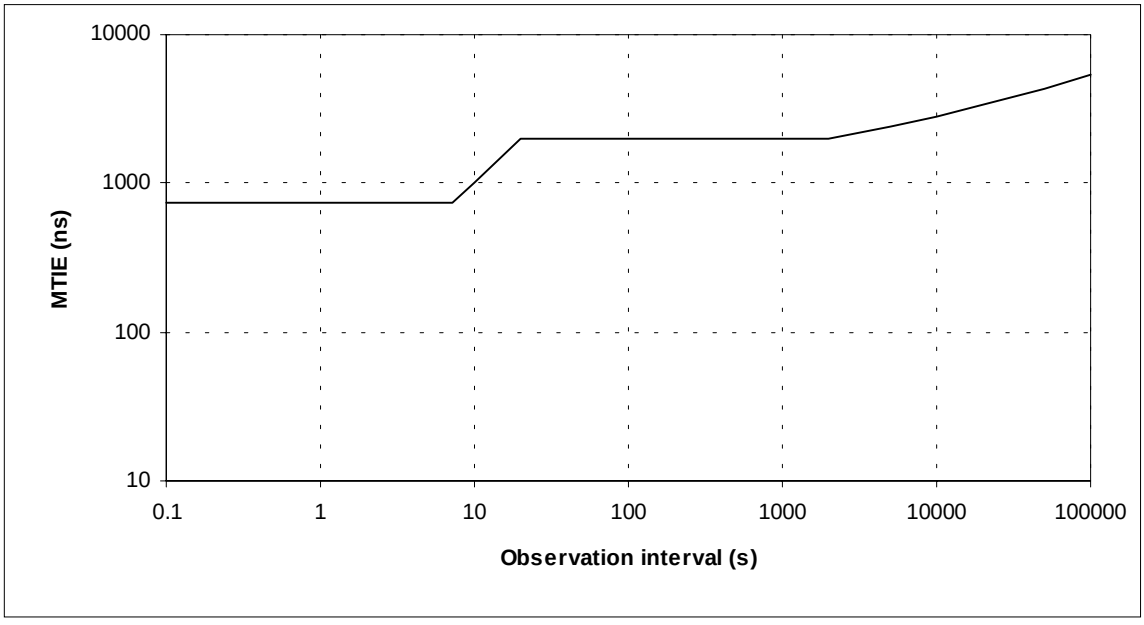


Figure 9: Network limit for wander at PDH distribution outputs expressed in MTIE

The maximum wander that may be generated at PDH distribution outputs expressed in TDEV shall not exceed the limits given in table 9.

Table 9: Network limit for wander at PDH distribution outputs expressed in TDEV

TDEV	Observation Interval
34 ns	$0{,}1 < \tau \leq 48$ s
$0{,}7\ \tau$ ns	$48 < \tau \leq 100$ s
$58 + 1{,}2\ \tau^{1/2} + 0{,}000\ 3\ \tau$ ns	$100 < \tau \leq 1\ 000\ 000$ s

The network limit for wander at PDH distribution outputs expressed in TDEV is shown in figure 10.

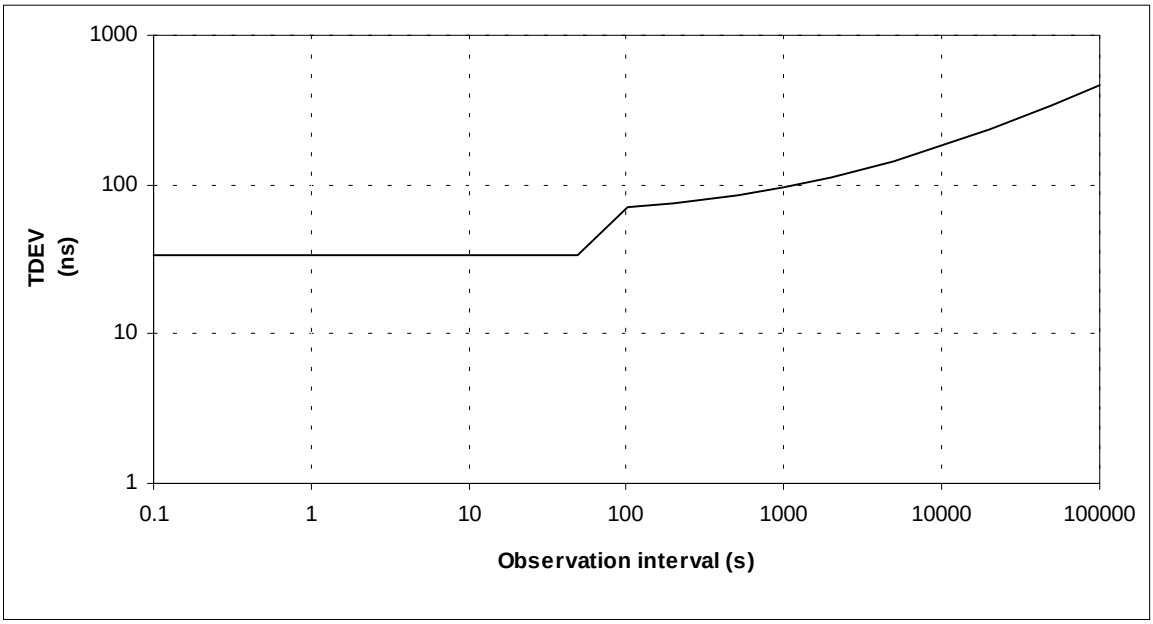


Figure 10: Network limit for wander at PDH distribution outputs expressed in TDEV

Annex A (normative): Anti-aliasing filter to be used for the measurement of MTIE and TDEV

A.1 Measurement philosophy

The measurement of TDEV of a timing signal on a network interface is intended to characterize the random noise processes in the signal. To be strictly correct, transients and periodic components should be removed from the measurement data prior to calculating TDEV, to get as good an estimate of the random processes as possible. This is however not practical for measurements on network interfaces since there is no a priori knowledge of the type of disturbances to be expected. Furthermore, the use of individual judgement to remove certain components from the timing data would lead to ambiguous results which is undesirable for the specification of network interfaces.

For this reason TDEV shall be calculated from the raw measurement data. It is also important for consistency in measuring MTIE and TDEV parameters that an anti-aliasing filter, maximum sampling time and measurement interval are specified. These are given below.

A.2 Filter specification, sampling time and measurement interval

For observation intervals of 0,1 s to 1 000 s, MTIE and TDEV shall be measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period T for TDEV is twelve times the observation interval τ.

For observation intervals of 10 s to 100 000 s, MTIE and TDEV shall be measured through an equivalent 0,1 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 3,3 seconds. The minimum measurement period T for TDEV is twelve times the observation interval τ.

Note that for any other range of observation intervals the maximum sampling time τ_0 and the measurement filter cut-off frequency f_c should have the same ratio to the minimum observation interval τ_{min} as used above, i.e. $\tau_0 = \tau_{min} / 3$ and $f_c = 1 / \tau_{min}$ Hz.

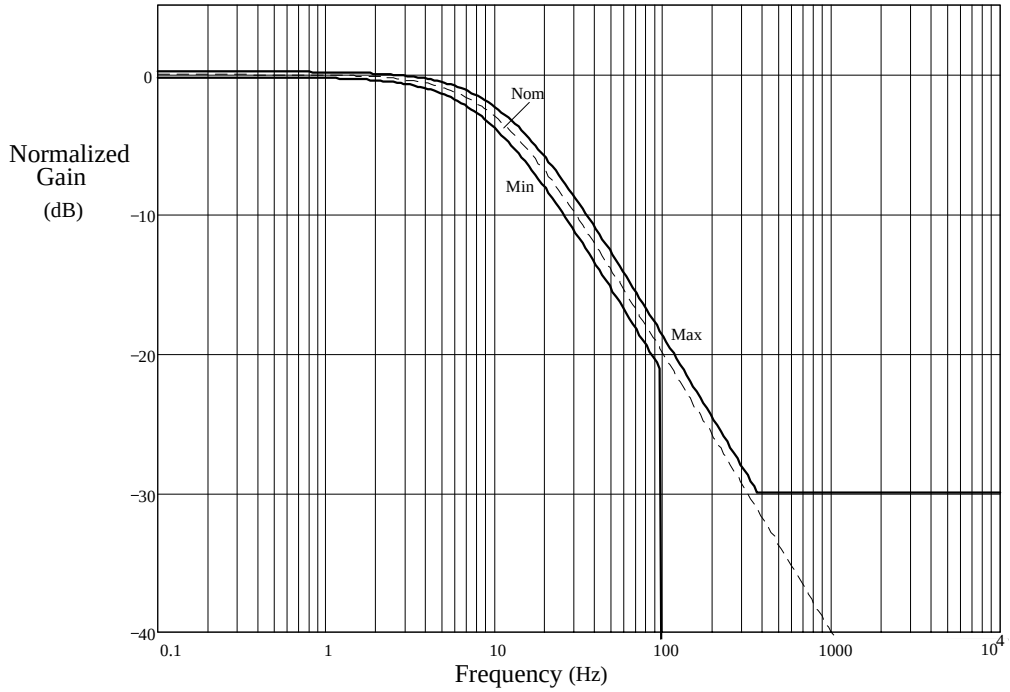
The anti-aliasing measurement filter characteristic shall, for the purpose of testing conformance to the masks in this standard be designed to ensure that measurement accuracy due to the variance in filter performance for flicker phase noise is better than 8 % with respect to an ideal first order low pass filter. Note that overall measurement accuracy is also affected by a number of other factors, such as test equipment gain accuracy, measurement time, temperature stability, MTIE/TDEV calculation algorithm, and so on.

The following 10 Hz anti-aliasing filter tolerance specification has been demonstrated to meet the 8 % accuracy requirement. It is provided for guidance only:

Amplitude of passband ripple ± 0,2 dB (excluding constant gain factors);

- 3 dB cut-off frequency, f_c = 10 Hz ± 15 %.

The tolerance is illustrated as maximum and minimum response masks in figure A.1.



f_c = 10 Hz

$$H_{Max}(f) = 0{,}2 + 20\log_{10}\sqrt{\frac{1}{\left(\frac{f}{1{,}13\,f_c}\right)^2 + 1}} \quad \text{dB} \quad \text{for } f < 36{,}3\,f_c$$

$$H_{Max}(f) = -30 \quad \text{dB} \quad \text{for } f \geq 36{,}3\,f_c$$

$$H_{Min}(f) = -0{,}2 + 20\log_{10}\sqrt{\frac{1}{\left(\frac{f}{0{,}87\,f_c}\right)^2 + 1}} \quad \text{dB} \quad \text{for } f < 10\,f_c$$

$$H_{Min}(f) = -\infty \quad \text{dB} \quad \text{for } f \geq 10\,f_c$$

Figure A.1: Wander measurement filter characteristic and tolerance limits

Annex B (informative): Network model underlying the network limit

B.1 Introduction

The method of deriving network limits is based on numerical simulations carried out on a certain network model, that is representative of a "reasonable worst case" network from the point of view of synchronization. A description of this reference network and other assumptions that went into the composition of the network limits, are outlined in this annex.

B.2 Considerations on the network model

The synchronization network limits are a compromise between several conflicting requirements, since one needs to align specifications of the individual equipment with the performance criteria that are applicable to the network as a whole. The number of possible networks that are and can be built is almost without bounds, therefore a reference network is needed that is "worse" than the large majority of the real networks from a synchronization point of view. The list below contains the most important elements that need to be considered when a reference network is constructed:

- the first element is the specification of individual clocks that are part of the synchronization trail to a network element: the more phase noise each clock is allowed to produce the higher the network limit will be. These noise specifications are those that can be found in ETS 300 462-4 [3], ETS 300 462-5 [4] and ETS 300 462-6 [5], for SSUs, SECs and PRCs, respectively;

- the composition of the complete synchronization chain in terms of how many clocks of each type (PRC, SSU or SEC) are cascaded and in what order is the second important element. Such a synchronization reference chain is defined in ETS 300 462-2 [2] and consists of 1 PRC followed by 10 SSUs and 20 SECs (there may be 40 more SECs between the SSUs but those are of no consequence for the problem at hand);

- apart from the noise generated by the individual clocks, also diurnal wander and the phase transients that occur on the synchronization links are a factor. The (conservative) assumption was that between any two SSUs there will be on average 1 transient per 25 days. The size of each transient was taken to be 1 μs with random polarity. Compared to the cumulative effect of clock noise and transients, the effect of diurnal wander is negligible if the synchronization trail is in the main transported over buried optical cable.

The three items mentioned above completely determine the network limit for synchronization interfaces. However, a data reference network is needed to verify whether these limits are consistent with existing performance requirements:

- the important aspects of the architecture of the reference data connection are those that influence the wander accumulation of the data signal, hence the number of SDH islands on the link and the number of pointer processors inside each island. This reference data connection should be representative for any 2 048 kbit/s link between two equipments that have slip-buffer termination (e.g. two international gateway switches), this is because an equipment with slip-buffer termination completely re-times the signal. The reference data connection was chosen to consist of 4 SDH islands, each having 8 TU-12 pointer processors, in an otherwise PDH connection. The network model also (conservatively) assumes that each node that needs timing is synchronized via an independent worst case synchronization chain;

- finally, the performance requirements against which the resulting differential wander on the receiving slip-buffer is to be evaluated are specified in ITU-T Recommendations G.822 [6] and G.823 [7]. ITU-T Recommendation G.823 [7] prescribes a maximum amount of differential input wander of 18 μs over a time period that was decided to be 24 hours. ITU-T Recommendation G.822 [6] specifies a slip performance better than 0,3 per day (98,9 % of the time) for the national part of a 27 500 km reference connection. This national part was considered to be the right benchmark for the proposed network.

The elements in the list above lead to the network shown in figure B.1. This model is derived from figure C.1 of ITU-T Recommendation G.823 [7], but it includes multiple PRCs to make it applicable for data paths that traverse multiple PRC timing domains.

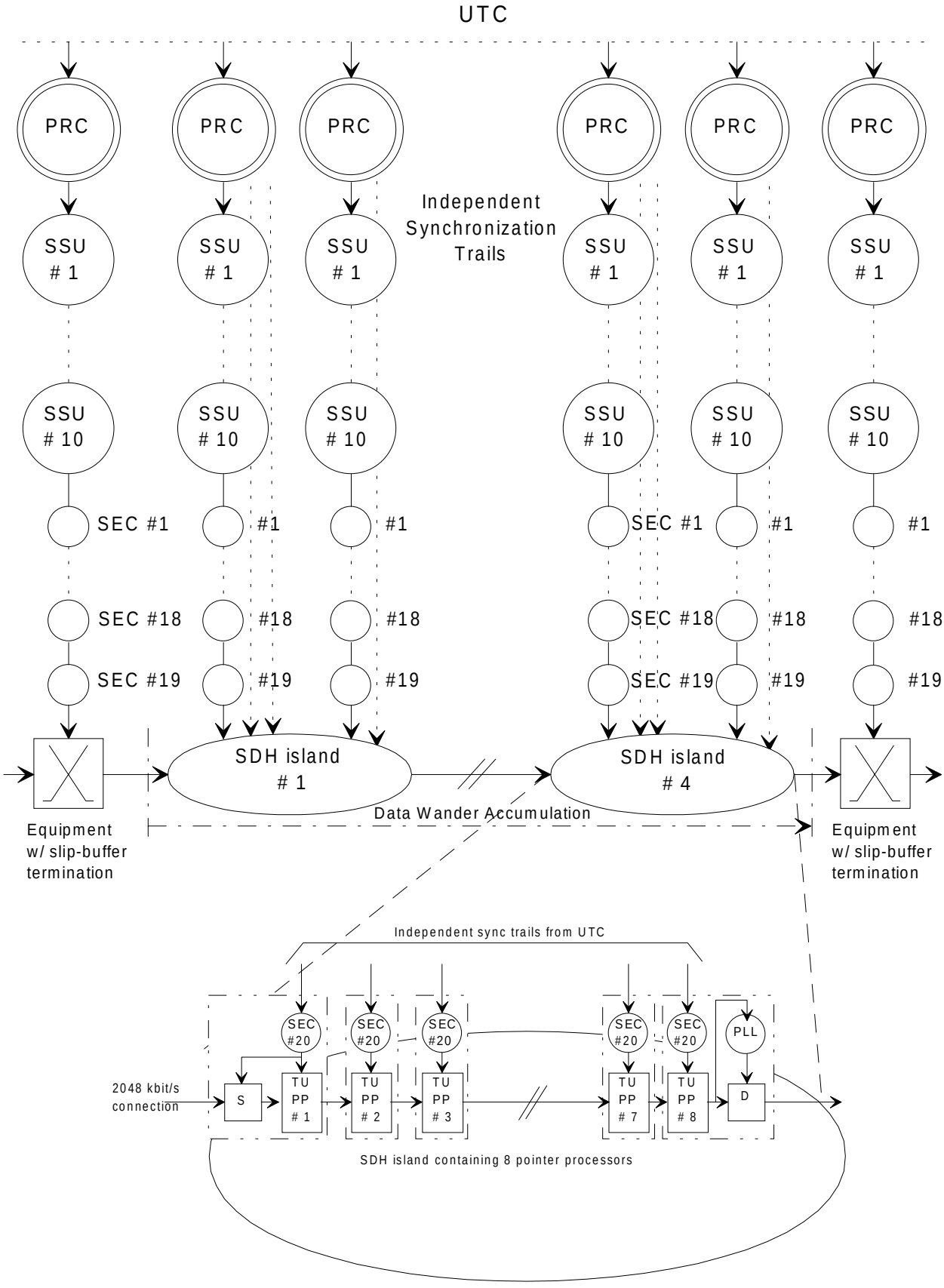


Figure B.1: Network model for data and clock wander accumulation

To determine the differential wander at the input of the receiving slip-buffer terminating equipment, two other factors are of importance, which were not directly included in the simulations, but for which separate allocations have been made in the wander budget (see also clause B.3):

- the mapping wander of 2 Mbit/s signals into VC-12 has to be taken into account;

- the diurnal wander caused by environmental influences on the optical fibres that carry the signals under consideration has to be taken into account.

B.3 Information regarding the simulations

Figure B.2 depicts the model that was used in the simulations to generate the noise on the clock inputs of all SDH equipment along the data path and the transmitting and receiving slip-buffer terminating equipments. The intrinsic noise and the transients are generated separately. The intrinsic noise of 1 PRC and 10 SSUs followed by 20 SECs is based on data from ETS 300 462-4 [3], ETS 300 462-5 [4] and ETS 300 462-6 [5].

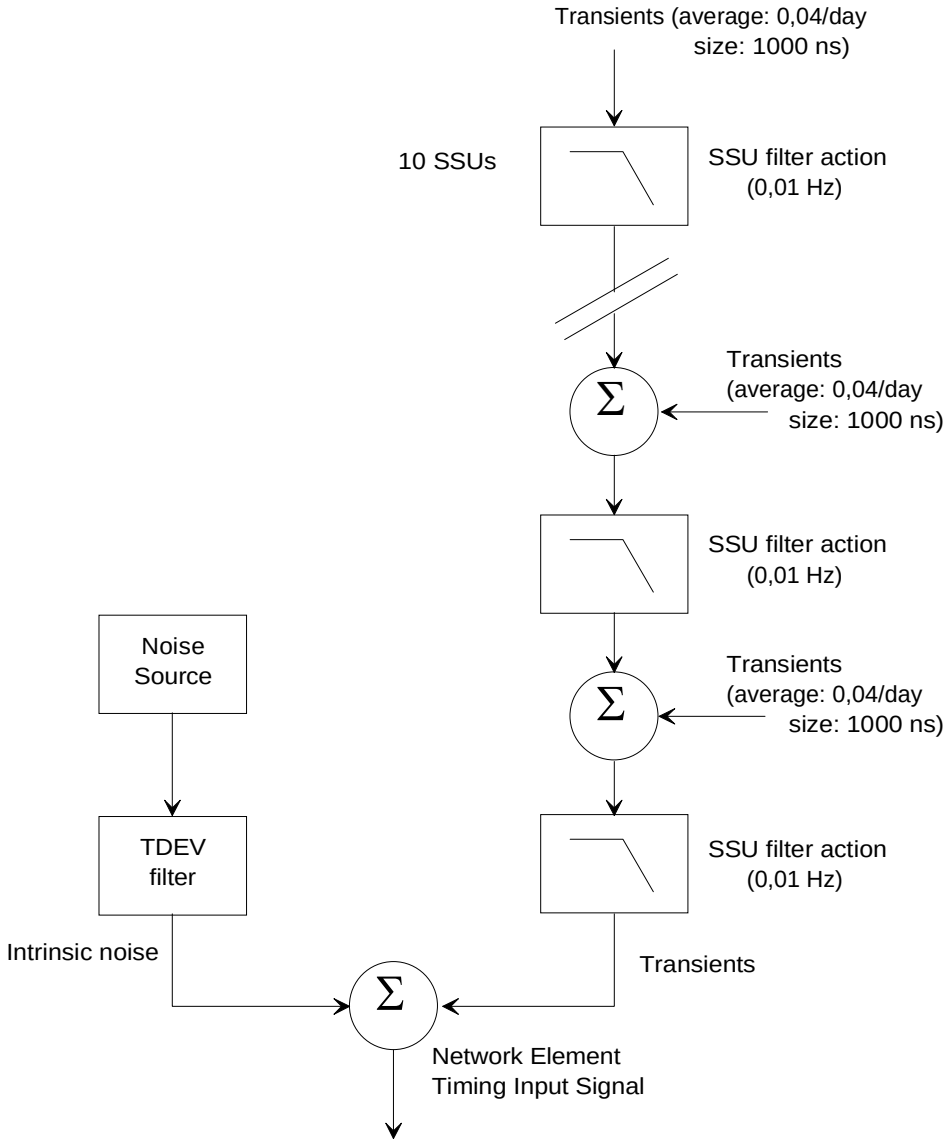


Figure B.2: Clock noise generator in simulation program

For the purpose of the simulations, some more assumptions had to be made to keep the complexity to an acceptable level without affecting the results significantly:

- the elastic stores in the TU-12 pointer processors are taken to be two bytes. This is the minimum elastic store space as prescribed by ITU-T Recommendation G.783 [9];

- the mapping method of the 2 Mbit/s data stream into the VC-12 is taken to be asynchronous;

- the initial buffer fill of the TU-12 pointer processor elastic stores is random with a uniform distribution. To eliminate the effect of initial distribution, the first 50 000 points of each simulation run were discarded;

- the time-increment between subsequent phase points is taken to be 1 s;

- the desynchronizer filters have not been taken into account, as this does not affect the long-term effects that are of importance when evaluating wander and slip performance.

Some factors that were not included in the simulations are:

- the diurnal wander caused by environmental influences on the optical fibres that carry the data signals under consideration has not been taken into account. This effect is separately accounted for, by allocating 1 μs in the wander budget. This number is based on a fibre optical link of 6 000 km length, subject to a temperature change of 2 °C and with a temperature coefficient of 85 ps/km/ °C;

- the mapping wander of 2 Mbit/s signals into VC-12 was not included, but was accounted for, afterwards, by allocating 2 μs in the wander budget to cater for this effect. This number is based on the argument that the VC-12 mapping wander is at most 2 UI for one island. It is assumed that the wander processes are uncorrelated. RMS addition is therefore allowed. For four islands, a wander budget of 4 UI (corresponding to 2 μs at 2 Mbit/s) is allocated;

- the effect of AU-4 pointer processing has entirely been neglected, given the complication of including it in the simulations and since its contribution is not significant;

- the wander that is caused by PDH multiplexing and line equipment that is part of the reference connection was also considered to be a small contributor and was not taken into account in the simulations.

From the above listed allocation, the following budget for the 18 μs can be derived:

Diurnal wander due to environmental effects:	1,0 μs
Mapping wander due to bit-asynchronous 2 Mbit/s mapping:	2,0 μs
Wander caused by clock noise and transients:	15,0 μs
Total:	18,0 μs

Simulations on the network model of figure B.1 show that the differential wander on the input of the receiving slip buffer caused by clock noise is 12,6 μs over 24 hour (averaged MTIE over 40 runs of 800 Ks). The corresponding slip-rate is 0,016 slips/day on average. Thus, the above assumptions and network model lead to a consistent set of specifications.

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