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EUROPEAN TELECOMMUNICATION STANDARD

pr **ETS 300 417-6-1**

August 1997

Source: ETSI TC-TM

Reference: DE/TM-01015-6-1

ICS: 33.020

Key words: Transmission, SDH, synchronization

Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 6-1: Synchronization layer functions

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Foreword

This draft European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI) and is now submitted for the Public Enquiry phase of the ETSI standards approval procedure.

This ETS has been produced in order to provide inter-vendor and inter-operator compatibility of Synchronous Digital Hierarchy (SDH) equipment.

This ETS consists of 8 parts as follows:

Part 1: "Generic processes and performance" (ETS 300 417-1-1 [1]);
Part 2: "SDH and PDH physical section layer functions" (ETS 300 417-2-1 [6]);
Part 3: "STM-N regenerator and multiplex section layer functions" (ETS 300 417-3-1 [7]);
Part 4: "SDH path layer functions" (ETS 300 417-4-1 [8]);
Part 5: "PDH path layer functions" (ETS 300 417-5-1 [9]);
Part 6: "Synchronization layer functions" (ETS 300 417-6-1);
Part 7: "Auxiliary layer functions" (ETS 300 417-7-1);
Part 8: "Compound and major compound functions" (ETS 300 417-8-1).

Proposed transposition dates	
Date of latest announcement of this ETS (doa):	3 months after ETSI publication
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa

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1 Scope

This European Telecommunication Standard (ETS) specifies a library of basic synchronization distribution building blocks, referred to as "atomic functions" and a set of rules by which they are combined in order to describe a digital transmission equipment. The library defined in this ETS forms part of the set of libraries defined in ETS 300 417 series. The library comprises the functional building blocks needed to completely specify the generic functional structure of the European digital transmission hierarchy. Equipment that is compliant with this ETS should be describable as an interconnection of a subset of these functional blocks contained within this ETS. The interconnection of these blocks should obey the combination rules given in ETS 300 417. The generic functionality is described in ETS 300 417-1-1 [1].

This ETS assumes that there are only two types of SSUs, transit and local, as currently defined in ITU-T Recommendation G.812 [18]. However, STC TM3 has approved in September 1996 a new SSU with enhanced characteristics. The inclusion of such an SSU in this ETS is for further study.

2 Normative references

This ETS incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references subsequent amendments to, or revisions of, any of these publications apply to this ETS only when incorporated in it by amendments or revisions. For undated references the latest edition of the publication referred to applies.

[1] ETS 300 417-1-1 (1996): "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 1-1: Generic processes and performance".

[2] ETS 300 147: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Multiplexing structure".

[3] ETS 300 166 (1993): "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s - based plesiochronous or synchronous digital hierarchies".

[4] ITU-T Recommendation G.707 (1996): "Network node interface for the synchronous digital hierarchy (SDH)".

[5] ITU-T Recommendation G.783: "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks".

[6] ETS 300 417-2-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 2-1: Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions".

[7] ETS 300 417-3-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 3-1: Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".

[8] ETS 300 417-4-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 4-1: Synchronous Digital Hierarchy (SDH) path layer functions".

[9] prETS 300 417-5-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 5-1: Plesiochronous Digital Hierarchy (PDH) path layer functions".

[10] ETS 300 462-2: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2: Synchronization network architecture".

[11] prETS 300 462-4: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

[12] ETS 300 462-5: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[13] prETS 300 462-6: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6: Timing characteristics of primary reference clocks".

[14] ITU-T Recommendation G.704 (1995): "Synchronous frame structures used at 1544, 6312, 2048, 8488 and 44 736 kbit/s hierarchical levels".

[15] ETS 300 337 (1996): "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[16] ETS 300 337 (1995): "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the CCITT Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[17] ITU-T Recommendation G.811 (1988): "Timing requirements at the outputs of primary reference clocks suitable for plesiochronous operation of international digital links".

[18] ITU-T Recommendation G.812 (1988.): "Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links".

[19] ITU-T Recommendation G.813 (1996): "Timing characteristics of SDH equipment slave clocks (SEC)".

[20] ETS 300 167: "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".

[21] ETS 300 462-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1: Definitions and terminology for synchronization networks".

3 Definitions, abbreviations and symbols

3.1 Definitions

For the purposes of this ETS, the following definition applies:

timing loop: This is a network condition where a slave clock providing synchronization becomes locked to its own timing signal. It is generally created when the slave clock timing information is looped back to its own input, either directly or via other network equipments. Timing loops should be avoided in networks.

The functional definitions are given in ETS 300 417-1-1 [1].

3.2 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

AI	Adaptation Information
AIS	Alarm Indication Signal
AP	Access Point
CI	Characteristic Information
CK	Timing Information - Clock signal
CLR	Clear
CP	Connection Point
CS	timing information - Clock Source
CSid	Clock Source identifier
DNU	Do Not Use
ES1	STM-1 Electrical Section layer
EXTCMD	External Command
FS	timing information - Frame Start
FSw	Forced Switch
HO	HoldOver mode
ID	IDentifier
INVx	INValid x
LC	Layer Clock
LO	Lock Out
LO	Locked mode
LOS	Loss Of Signal
LSB	Least Significant Bit
LTI	Loss of Timing Information
MA	Maintenance and Adaptation
MI	Management Information
MON	MONitored
MFS	MultiFrame Start
MS	Multiplex Section
MSB	Most Significant Bit
MSw	Manual Switch
MTIE	Maximum Time Interval Error
NE	Network Element
NS	Network Synchronization
NSUPP	Not supported
OSn	STM-n Optical Section layer
P12s	2 048 kbit/s PDH path layer with synchronous 125 μs frame structure according to ETS 300 167 [20]
P31s	34 368 kbit/s PDH path layer with synchronous 125 μs frame structure according to ETS 300 337 [15]
P4s	139 264 kbit/s PDH path layer with synchronous 125 μs frame structure according to ETS 300 337 [15]
PDH	Plesiochronous Digital Hierarchy
PRC	Primary Reference Clock
QL	Quality Level
RI	Remote Information
RSn	STM-n Regenerator Section layer
SASE	Stand Alone Synchronization Equipment
SD	Synchronization Distribution
SDH	Synchronous Digital Hierarchy
SDL	Specification and Description Language
SEC	SDH Equipment Clock
SF	Signal Fail
SQLCH	Squelch
SSF	Server Signal Fail
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
SSUL	Local SSU
SSUT	Transit SSU
STM-N	Synchronous Transport Module, level N

Sk	Sink
So	Source
TCP	Termination Connection Point
TDEV	Time DEViation
TI	Timing Information
TL	Transport Layer
TM	Timing Marker
TT	Trail Termination
TSF	Trail Signal Fail
UNC	UNConnected
VC-n	Virtual Container, level n
WTR	Wait to Restore

3.3 Symbols and diagrammatic conventions

The symbols and diagrammatic conventions are given in ETS 300 417-1-1 [1].

3.4 Introduction

This subclause defines the atomic functions that are part of the 2 synchronization layers, the Synchronization Distribution (SD) layer and the Network Synchronization (NS) layer. It also defines some atomic functions, part of the Transport layer, which are related with synchronization.

These functions describe the synchronization of SDH NEs and how SDH NEs are involved in Network Synchronization.

4 Synchronization principles

4.1 Network synchronization

Synchronization network architecture is specified in ETS 300 462-2 [10].

Synchronization information is transmitted through the network via synchronization network connections. These synchronization network connections can transport different synchronization levels. Each synchronization network connection is provided by one or more synchronization link connections, each supported by a synchronized primary or secondary rate PDH trail or SDH multiplex section trail (see clause 5 of ETS 300 462-2 [10]).

Some of these synchronized primary or secondary rate PDH trail or SDH multiplex section trail signals contain a communication channel, the Synchronization Status Message (SSM) or the Timing Marker (TM)) transporting a quality identifier. This quality level identifier can be used to select the highest synchronization level incoming reference signal from a set of nominated synchronization references available at the network element.

Synchronization network connections are uni-directional and generally point to multipoint. ETS 300 462-2 [10] specifies a master-slave synchronization technique for synchronizing SDH networks (see subclause 4.1 of ETS 300 462-2 [10]). Figures 1 to 4 illustrate the synchronization network connection model.

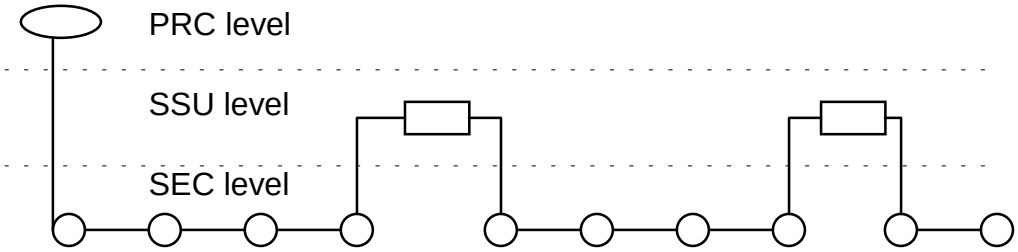

Figure 1: General representation of a synchronization network

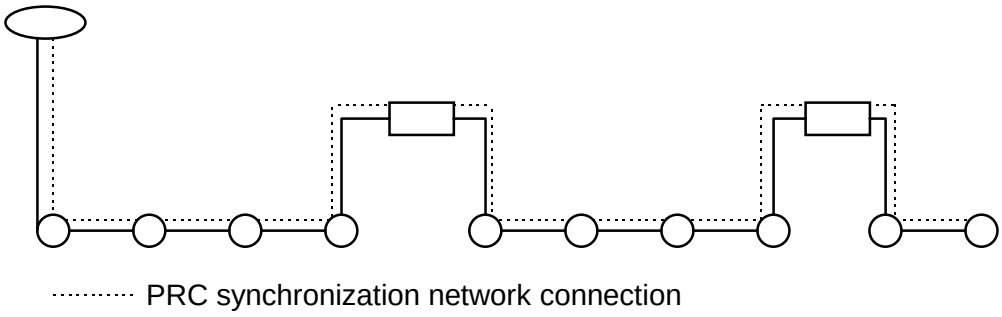

Figure 2: Representation of the PRC network connection

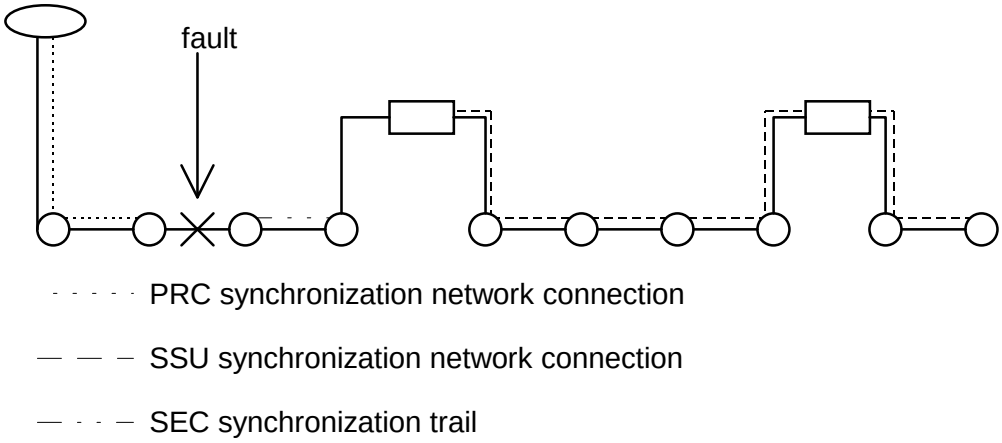

Figure 3: Representation of the synchronization network connection in case of failure

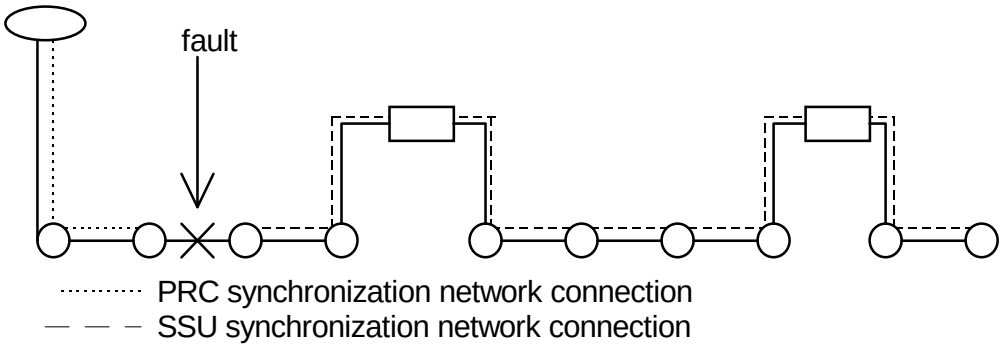

Figure 4: Example of restoration of the synchronization (see figure 7 of ETS 300 462-2 [10])

4.2 Synchronization distribution trails

Synchronization distribution trails transport timing between two adjacent equipments.

From a synchronization view point, adjacent network elements are those network elements that are interconnected via section signals. Between two such adjacent Network Elements (NEs) a uni-directional synchronization distribution trail exists.

A **SD trail** starts at the input of the SD_TT_So function and ends at the output of the SD_TT_Sk function.

A **SD link connection** transports synchronization timing information between two adjacent connection points (CP) of the NS_C function.

A **NS network connection** transports synchronization timing information over a series of synchronization link connection.

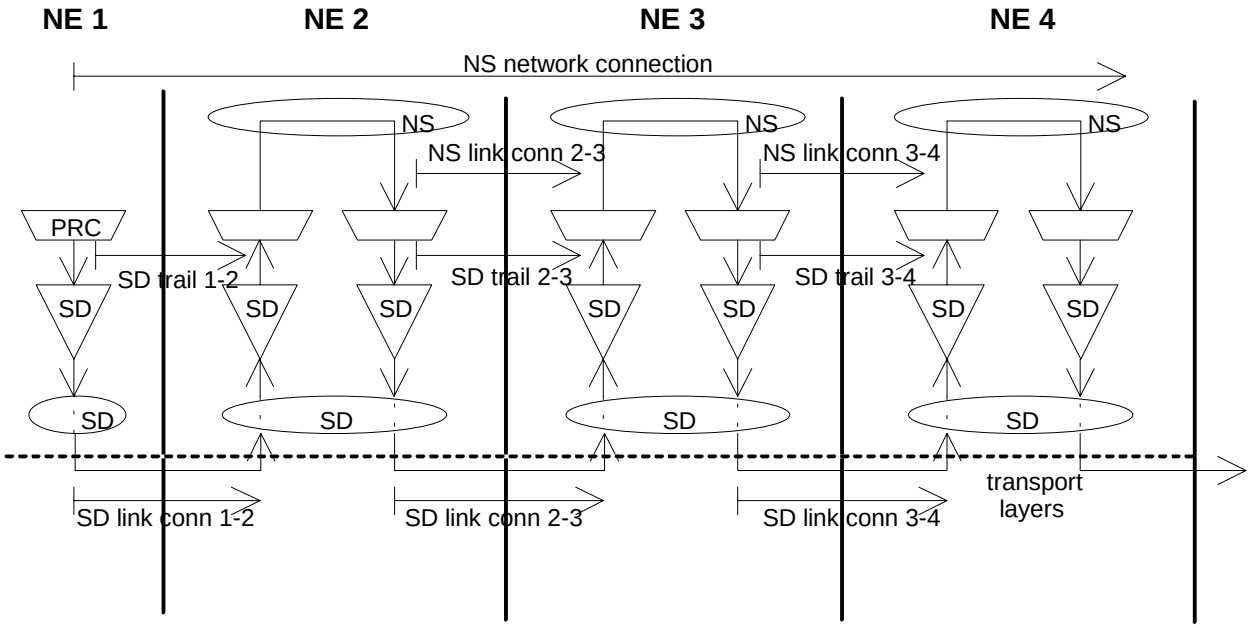

Figure 5: Example of series of synchronization distribution network connection transporting PRC quality timing reference information

4.3 Synchronization interfaces

Synchronization trails can be carried through the network by a number of interfaces. Currently, the following signals are defined for such transport (refer also to figures B.1 to B.4):

- without traffic:

  - 2 048 kHz (T12);
  - 2 048 kbit/s (E12+P12s);

- with traffic:

  - 2 488 320 kbit/s (OS16+RS16+MS16);
  - 622 080 kbit/s (OS4+RS4+MS4);
  - 155 520 kbit/s (OS1 (or ES1)+RS1+MS1);
  - 139 264 kbit/s (E4+P4s);
  - 34 368 kbit/s (E31+P31s);
  - 2 048 kbit/s (E12+P12s).

4.3.1 STM-N

The STM-N transport signals carry (in addition to the payload) reference timing information and an indication of the quality level of the source generating this timing information, via the Synchronization Status Message (SSM) as defined in ETS 300 147 [2].

NOTE: Old equipment may not be able to support SSM via their STM-N interfaces.

4.3.2 2 Mbit/s

The 2 Mbit/s transport signals may carry (in addition to the payload) reference timing information.

The 2 Mbit/s timing reference signals (without payload) carry reference timing information to specific synchronization ports.

Both signals can carry an indication of the quality level of the source generating the timing information via the SSM as specified in ITU-T Recommendation G.704 [14].

NOTE: Old equipment may not be able to support SSM on their 2 Mbit/s interfaces.

4.3.3 2 MHz

Synchronization can be carried through 2 MHz signals to specific synchronization ports (so called station clock ports). This signal does not carry an indication of the quality level of the source generating the timing information.

4.3.4 34 Mbit/s and 140 Mbit/s with 125 μs frame structure

34 Mbit/s and 140 Mbit/s signals with 125 μs frame structure as defined in ETS 300 337 [15] carry a full 4 bit SSM code.

NOTE: For interworking with equipments compliant with the initial edition of ETS 300 337 [15], new equipments should be able to be configured to recognize and generate the Timing Marker which is located in bit 8 of the MA (Maintenance and Adaptation) byte: the timing marker is set to '0' to indicate that the timing source is traceable to a Primary Reference Clock (PRC), and is otherwise set to '1'.

4.4 Quality level

4.4.1 Clock source quality levels

The following clock source quality levels are defined in the synchronization process of SDH network corresponding to 4 levels of synchronization quality (ETS 300 462-2 [10]).

QL-PRC: This synchronization trail transports a timing quality generated by a Primary Reference Clock that is defined in ETS 300 462-6 [13].

QL-SSU T: This synchronization trail transports a timing quality generated by a transit Synchronization Supply Unit (SSU) that is defined in ITU-T Recommendation G.812 [18].

QL-SSU L: This synchronization trail transports a timing quality generated by a local SSU that is defined in ITU-T Recommendation G.812 [18].

QL-SEC: This synchronization trail transports a timing quality generated by a SDH Equipment Clock (SEC) that is defined in ETS 300 462-5 [12].

QL-DNU: This signal should not be used for synchronization.

NOTE: The QL-unknown quality level was defined to characterize the quality of existing network. This QL is no longer supported by the SSM algorithm.

4.4.2 Hierarchy of Quality Levels (QL)

The following table defines the QL hierarchy.

Table 1: Hierarchy of quality levels

Quality Level	Order
QL-PRC	highest
QL-SSU T	|
QL-SSU L	|
QL-SEC	|
QL-DNU	|
QL-INVx, -FAILED, -UNC, -NSUPP	lowest

The quality levels QL-INVx, QL-FAILED, QL- UNC and QL-NSUPP are internal QLs inside the NE and are never generated at an output port.

QL-INVx is generated by the XX/SD_A_Sk function if an unallocated SSM value is received, where x represents the binary value of this SSM.

QL-NSUPP is generated by the XX/SD_A_Sk function when the function is not supporting the SSM (TM) processing.

QL-FAILED is generated by the SD_TT_Sk function when the terminated SD trail is in the signal fail state.

QL-UNC is generated by the SD_C or NS_C function when the output signal is not connected to an input, but instead to the internal unconnected signal generator.

4.4.3 Forcing of quality levels

For synchronization source signals/interfaces not supporting SSM transport/processing, it is possible to force the quality level to a fixed provisioned value. This allows to use these signals/interfaces as synchronization sources in an automatic reference selection process operating in QL-enabled mode.

Forcing of quality levels is used for new equipment operating in QL-enabled mode in order to:

- interwork with old equipment not supporting SSM/TM generation;
- interwork with new equipment operating in QL-disabled mode;
- select interfaces not supporting SSM/TM processing;
- select signals for which SSM/TM is not defined in (2 MHz).

4.5 Synchronization Status Messages (SSM) and Timing Marker (TM) channels

The following signals have a four bit SSM channel defined:

- STM-N (N = 1, 4, 16): bits 5 to 8 of the byte S1 (called SSMB, Synchronization Status Message Byte) of the multiplex section overhead as defined in ITU-T Recommendation G.707 [4].
- 2 Mbit/s octet structured according to ITU-T Recommendation G.704 [14]: bits S_{ax1} to S_{ax4} (x = 4, 5, 6, 7, or 8) of TS0.
- 34 Mbit/s as defined in ETS 300 337 [15]: bit 8 of MA byte with a 4 frame multiframe.
- 140 Mbit/s as defined in ETS 300 337 [15]: bit 8 of MA byte with a 4 frame multiframe.

The following signals may have a one bit TM channel:

- 34 Mbit/s with a 125 μs frame structure as defined in ETS 300 337 [16]: bit 8 of byte MA.

- 140 Mbit/s with a 125 μs frame structure as defined in ETS 300 337 [16]: bit 8 of byte MA.

4.5.1 SSM and TM message sets

Five SSM codes are defined to represent clock source QL as listed below:

- code 0010 (Quality PRC) means that the source of the trail is a PRC clock (ETS 300 462-6 [13], ITU-T Recommendation G.811 [17]);

- code 0100 (Quality SSU-T), means that the source of the trail is a transit SSU clock (ITU-T Recommendation G.812-T [18]);

- code 1000 (Quality SSU-L), means that the source of the trail is a SSU clock (ITU-T Recommendation G.812-L [18]);

- code 1011 (Quality SEC), means that the source of the trail is a SEC clock (ETS 300 462-5 [12], option 1 of ITU-T Recommendation G.813 [19]);

- code 1111 (quality DNU), means that the signal carrying this SSM shall not be used for synchronization because a timing loop situation could result if it is used.

Two TM codes were defined in ETS 300 337 [15] and [16]:

- code 0 (Quality PRC), means that the source of the trail is a PRC clock (ETS 300 462-6 [13], ITU-T Recommendation G.811 [17]);

- code 1 (Quality less_than_PRC), means that the source of the trail is not a PRC clock.

4.5.2 SSM and TM code word generation

The SSM can be viewed as an application specific data communication channel with a limited message set. The message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function. The following table presents the relation between the existing set of QLs and SSM codes.

Table 2: level set and coding in synchronization status message

Quality Level (QL)	SSM usage	SSM coding [MSB..LSB]
QL-PRC	enabled	0010
QL-SSUT	enabled	0100
QL-SSUL	enabled	1000
QL-SEC	enabled	1011
QL-DNU	enabled	1111
-	disabled	1111

The TM can be viewed as an application specific data communication channel with a limited message set. The message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function. The following table presents the relation between the existing set of QLs and TM codes.

Table 3: Quality level set and coding in timing marker

Quality Level (QL)	TM usage	TM coding
QL-PRC	enabled	0
QL-SSUT	enabled	1
QL-SSUL	enabled	1
QL-SEC	enabled	1
QL-DNU	enabled	1
-	disabled	1

At network boundaries, it should be possible to prevent synchronization information passing the interface. This can be achieved by disabling the SSM (TM) usage.

4.5.3 SSM and TM code word interpretation

At the receive side, the received SSM bits are to be validated by a persistency check and then interpreted to determine the QL.

Table 4: Interpretation of synchronization status message codes

SSM code [MSB..LSB]	QL interpretation
0000	QL-INV0
0001	QL-INV1
0010	QL-PRC
0011	QL-INV3
0100	QL-SSUT
0101	QL-INV5
0110	QL-INV6
0111	QL-INV7
1000	QL-SSUL
1001	QL-INV9
1010	QL-INV10
1011	QL-SEC
1100	QL-INV12
1101	QL-INV13
1110	QL-INV14
1111	QL-DNU

Table 5: Interpretation of timing marker codes

TM code	QL interpretation
0	QL-PRC
1	QL-DNU

4.6 Selection process

The process of selecting a synchronization source from the set of physical ports is performed in three steps:

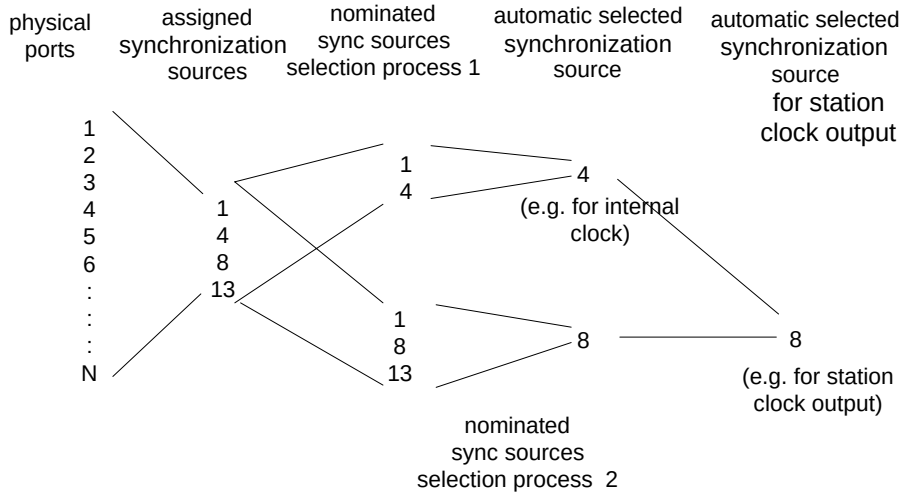

Figure 6: Visualization of the synchronization source selection process(es)

1) *Assignment of a physical port to be a synchronization source*: Select a (limited) set of interface signals (from the total set of interfaces) to act as synchronization sources.
This is performed in the SD_Cfunction by means of adding matrix connections between a group of inputs (connected to the server layer) and outputs (connected to the SD_TT_Sk functions).

2) *Nomination of a synchronization source for an automatic selection process*: Select a (sub)set of the synchronization sources to contribute to a selection process.
This is performed in the NS_C function by means of assigning a priority to the synchronization source (see subclause 4.10).

3) *Automatic Selection Process*. Selects the "best" synchronization source of the set from nominated sources according to the selection algorithm (see subclause 4.12).

NOTE: The specifications in this ETS allow a selection to be made between any set of synchronization interface signals input to a network element, independent of the actual synchronization network architecture deployed in the network. It is the network operator's responsibility to ensure that timing loops are not created.

4.7 Signal fail

Signal fail for a synchronization source is activated in case of defects detected in the server layers. In addition an unconnected synchronization signal has also signal fail active in order to allow correct processing in the QL disabled mode. Inclusion of specific synchronization failures (e.g. exceeded frequency deviation, exceeded wander limits) as signal fail criteria for SSU are for further study.

In order to avoid reactions on short pulses or intermitting signal fail information, the signal fail information is passed through a hold-off and wait to restore processes before it is considered by the selection process.

NOTE 1: The delay of the signal fail information is only performed for the information passed to the selection process. The signal fail information for the main data path to the output of the NS_C function is not delayed.

In QL enabled mode the QL of a synchronization source with active signal fail is set to QL-FAILED. The selection process will react to this QL value instead of the signal fail signal in this mode.

NOTE 2: Due to different persistence times for defect detection and the SSM acceptance process, a defect leading to signal fail could also result in a change of the QL value shortly before signal fail is activated. The implementation has to ensure that the selection process does not select a new synchronization source based on this intermediate QL value.

4.8 Hold-off time

The hold-off time ensures that short activation of signal fail are not passed to the selection process.

In QL-disabled mode signal fail shall be active for the hold-off time before it is passed to the selection process.

In QL-enabled mode a QL value of QL-FAILED shall exist for the hold-off time before it is passed to the selection process. In the mean time the previous QL value is passed to the selection process.

NOTE: Other QL values than QL-FAILED will be passed to the selection process immediately.

Separate hold-off timers are used for each input to a selection process (nominated source).

The hold-off time is fixed in the range of 300 ms to 1 800 ms.

4.9 Wait to restore time

The wait to restore time ensures that a previous failed synchronization source is only again considered as available by the selection process if it is fault free for a certain time.

In QL-disabled mode after deactivation of signal fail, it shall be false for the wait to restore time before signal fail false is passed to the selection process. In the mean time signal fail true is passed to the selection process.

In QL-enabled mode after a change of the quality level from QL-FAILED to any other value, the quality value shall be different from QL-FAILED for the wait to restore time before the new QL value is passed to the selection process. In the mean time the quality level QL-FAILED is passed to the selection process.

Separate wait to restore timers are used for each input to a selection process (nominated source).

The wait to restore time is configurable in the range of 0 to 12 minutes in steps of 1 minute for all inputs of a selection process in common. The default value is 5 minutes.

Each wait to restore timer can be cleared with a separate Clear command. If a wait to restore timer is cleared the new QL value (in QL-enabled mode) or signal fail value (in QL-disabled mode) is immediately passed to the selection process.

4.10 Synchronization source priorities

In order to define a preferred network synchronization flow, priority values are allocated to assigned synchronization sources within a network element.

Different priorities reflect a preference of one synchronization source over the other. Equal synchronization source priorities reflect that no preference exists between the synchronization sources. Within the group of synchronization sources with equal priorities the selection process has a non-revertive behaviour.

A priority of "dis" (disabled) identifies that this assigned synchronization source is not nominated for the selection process.

Table 6: Priority order

Priority value	Order
1	highest
2	|
3	|
:	|
K	|
dis, undef	lowest

NOTE 1: The priority value is not numerical ordered.
The following relation is present: "1" > "2" > "3" > .. > "K" > "undef", "dis".

The priority value "undef" is associated with the unconnected signal of the NS_C function and is not configurable from the outside.

NOTE 2: The assigning of equal priorities to synchronization sources in order to allow for non-revertive operation does not allow for a pre-defined initialization state of known synchronization configuration following failure of a higher priority source.

4.11 External commands

Several external commands are available to the user, (e.g. for maintenance purposes). These commands are independent and have different impact on the selection processes.

4.11.1 External commands per nominated synchronization source

It is possible to temporary remove a timing source as available synchronization source for the selection process.

This is controlled by the lockout commands. Lockout commands are accepted for nominated synchronization sources (synchronization sources that are not disabled) of each selection process.

The lockout status of a disabled synchronization source is "off".

NOTE: A locked out source is still nominated to the selection process and retains its synchronization source priority.

4.11.1.1 Set_Lockout#p command

The Set_Lockout#p command sets the lockout state of input p to "on". This causes this input to be no longer considered available by the selection process.

4.11.1.2 Clear_Lockout#p command

The Clear_Lockout#p command sets the lockout state of input p to "off". This causes this input to be considered available again by the selection process.

4.11.2 External commands per selection process

Only one of the below commands is active at a time.

4.11.2.1 Clear command

A clear (CLR) command clears the forced switch and manual switch commands.

4.11.2.2 Forced switch #p command

A forced switch (FSw) to #p command can be used to override the currently selected synchronization source, assuming the synchronization source #p is enabled and not locked out.

The forced switch pre-empts the manual switch and a subsequent forced switch pre-empts the previous forced switch.

If the source selected by the forced switch command (#p) is disabled or locked out, the forced switch command is automatically rejected.

The forced switch command can be cleared by the "clear" command.

NOTE: A forced switch command to a synchronization source #p which is in the SF state or has a QL of DNU in QL enabled mode, will result in the network element entering holdover.

4.11.2.3 Manual switch #p command

A manual switch (MSw) to #p command selects the synchronization source #p, assuming it is enabled, not locked out, not in signal fail condition, and has a QL better than DNU in QL enabled mode. Furthermore in the QL enabled mode, a manual switch can be performed only to a source which has the highest available QL. As such, these conditions have the effect that manual switching can only be used to override the assigned synchronization source priorities.

A manual switch request pre-empts a previous manual switch request.

If the source selected by the manual switch command (#p) is disabled, locked out, in signal fail, or has a QL of DNU or lower than one of the other source signals, the manual switch command is automatically rejected.

The manual switch command can be cleared by the "clear" command.

4.12 Automatic reference selection process

One or more reference selection processes are operating independently to select the reference signal for the internal clock and, where present, the station clock output(s).

The selection process(es) can work in two distinct modes: QL-enabled, QL-disabled. If multiple selection processes are present in a network element, all processes work in the same mode.

The following is a brief description of the automatic reference selection process. The specific details (SDL diagrams) are defined in annex A.

4.12.1 QL-enabled mode

In QL-enabled mode the following parameters contribute to the selection process:

- Quality Level;
- signal fail via QL-failed;
- priority;
- external commands.

If no overriding external commands are active, the algorithm selects the reference with the highest quality level, which is not experiencing a signal fail condition. If multiple inputs have the same highest quality level, the input with the highest priority is selected. For the case that multiple inputs have the same highest priority and quality level, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

4.12.2 QL-disabled mode

In QL-disabled mode the following parameters contribute to the selection process:

- signal fail;
- priority;
- external commands.

If no overriding external commands are active, the algorithm selects the reference with the highest priority which is not experiencing a signal fail condition. For the case that multiple inputs have the same highest priority, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

4.13 Timing loop prevention

4.13.1 Station clock input used as a source for station clock output

This specification allows the use of the station clock input as a source for the station clock output, either directly or via the SEC. When this functionality is present in a network element, the operator should be aware that this functionality is intended for timing quality monitoring purposes and that its use for other purposes could result in timing loops being created. If a timing loop could be created, the operator should prevent that by a reconfiguration of the synchronization architecture.

4.13.2 Between NEs with SEC type clocks

The master-slave synchronization over several NEs with multiple possible synchronization inputs for protection of synchronization as defined in ETS 300 462-2 [10] could lead to timing loops between NEs. To avoid timing loops a NE should insert a SSM/TM value of DNU in direction of the NE which is used as actual synchronization source for the NE clock (SEC).

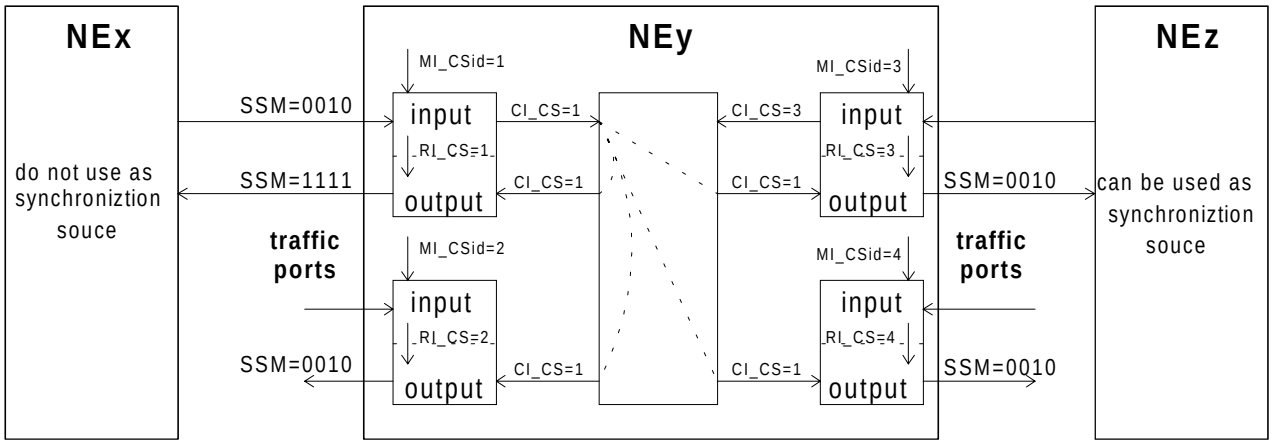

Figure 7: Automatic DNU generation in a NE with SEC timing

The clock source identifier CSid is introduced to support the above feature as shown on figure 7. To each transport and station clock input port a unique CSid is assigned (MI_CSid). This ID is processed in the synchronization layers together with the clock and quality level of the port. The CSid of the selected source for the SEC is distributed to all output ports. If a transport output port receives the same CSid as its associated input port (signalled via RI_CS) via the synchronization distribution layer (SD_CI_CS) the outgoing SSM/TM is set to DNU.

NOTE: The above principle may be extended to generate DNUs on groups, "bundle", of ports, which are known to have the same timing source. A provisional agreement is that processing of DNU generation on all the ports of the "bundle" when any one of them has been selected as the reference source does not require additional information between the atomic functions. Use of identical CS within the "bundle" has been considered but this is left for further study.

4.13.3 Between NEs with a SEC clock and a NE or SASE with a SSU clock and only one link

A NE can be interconnected with a SASE via its (2 MHz and/or 2 Mbit/s) station clock input and output ports. If the SASE is used as the actual synchronization source for the NE clock the mechanism defined in subclause 4.13.2 has to be extended to support automatic DNU insertion also for this case.

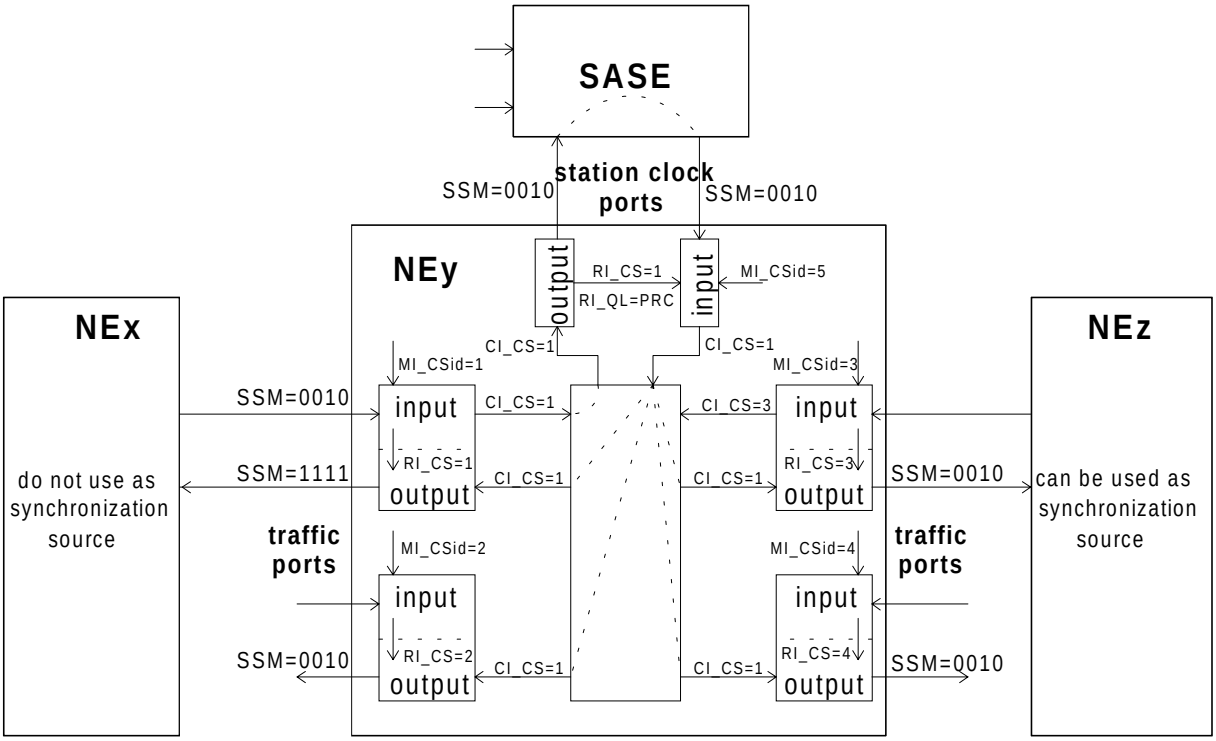

Figure 8: Automatic DNU generation in a NE with SASE timing

If a NE is connected to a SASE, remote information is exchanged between the normally uni-directional station clock input and output ports connected to the same SASE. The remote information transfers the CSid (CI_CS → RI_CS) of the clock signal selected for the station clock output to the station clock input. The station clock input port uses this remote information as CSid for the clock signal to the selection process (RI_CS → CI_CS) instead of its own CSid (MI_CSid) as long as the SASE might use the station clock output of the NE as active source. This will result in DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock (see figure 8).

It is not possible to detect that the SASE has selected the station clock output port of the NE as actual clock source, but several conditions exist that indicate that the station clock output port is not used as clock source by the SASE. If QL/SSM processing is supported by all components (NE, SASE, station clock ports) different SSM values at the output and input station clock ports indicate that the output port is not used as clock source by the SASE (see figure 9). In all other cases a squelched 2 MHz output and a 2 Mbit/s station clock output set to AIS indicate that the output port is not used as clock source by the SASE. If these conditions are detected, the remote CSid is not longer used and the automatic DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock is removed (see figure 9). Their are still conditions in which the SASE does not select the station clock output of the NE as synchronization source, but the automatic DNU insertion is still performed, e.g. if the SASE selects another source with the same QL as the station clock output of the NE (see figure 10).

The user has to enable the above feature by activating the remote indication connection between the station clock ports.

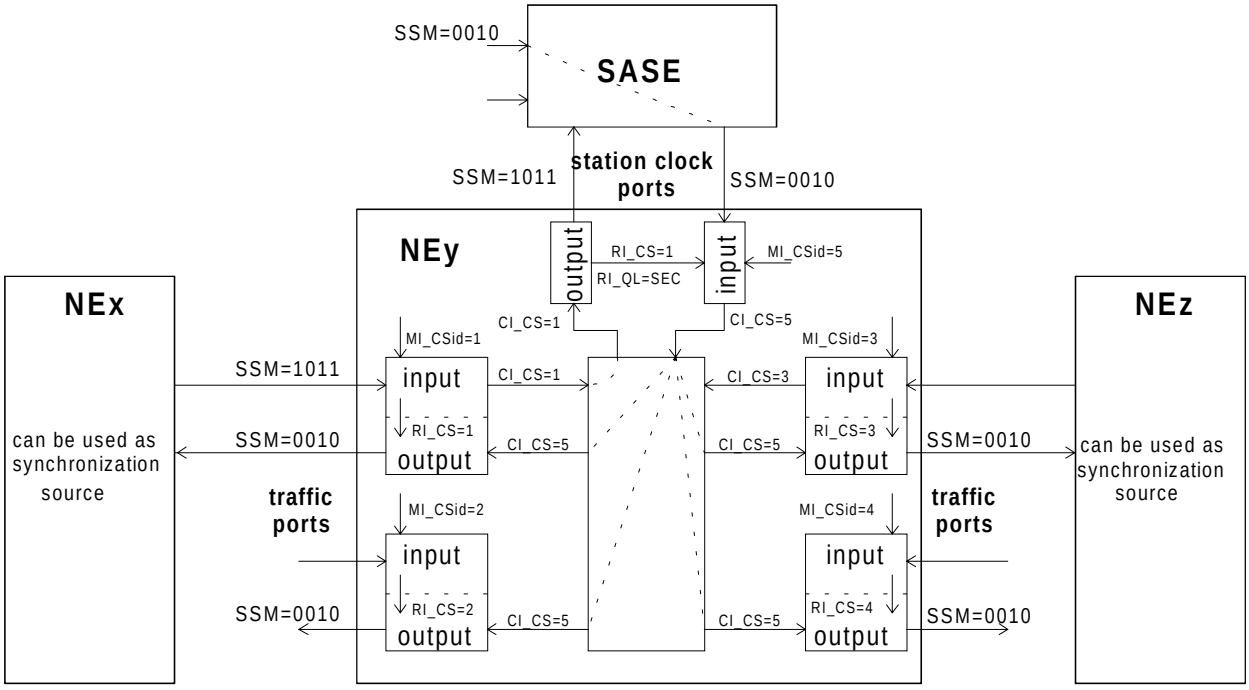

Figure 9: Removal of automatic DNU generation in a NE with SASE timing

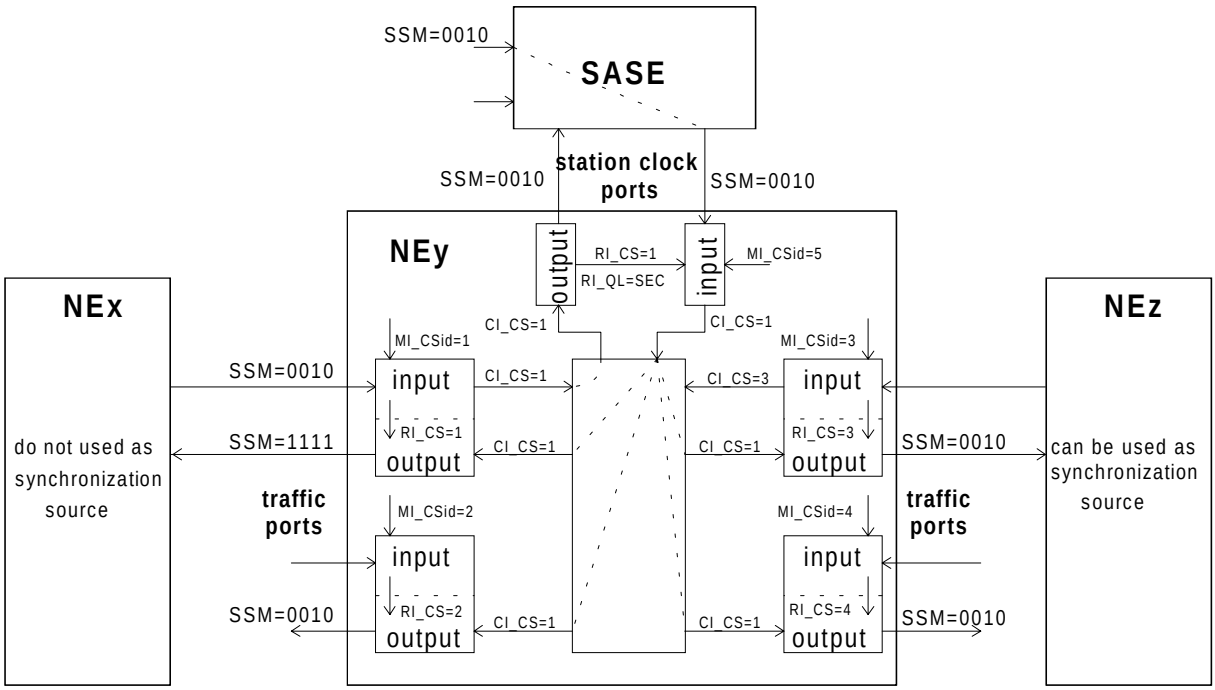

Figure 10: Limitation of automatic DNU generation in a NE with SASE timing

4.13.4 Between NEs with a SEC clock and a NE or SASE with a SSU clock and several links

A generalization of the mechanism described in subclause 4.13.3,applicable when SEC and SSU are interconnected by several links, is for further study.

4.14 Delay times for NEs with SEC

These delay times are caused by the atomic functions which perform the selection of the input synchronization reference. three delays are defined:

- Holdover message delay T_{HM}.

This delay applies when the SEC shall enter holdover because of loss of signal of the input reference and lack of any other available reference. When this event occurs the SEC goes immediately into holdover but changes the output SSM to the holdover code after a delay which has been defined to be between 500 ms and 2 000 ms.

- Non switching message delay T_{NSM}.

This delay applies when the QL of the selected synchronization source changes but no switchover to another source is performed. The outgoing SSM/TM follows this change at the input within a time defined to be less than 200 ms.

- Switching message delay T_{SM}.

This delay applies when a new synchronization source is selected. The output SSM change, if any, is done after a delay that has been defined to be between 180 ms and 500 ms.

A full description of these times is in annex E.

Change of the synchronization direction within a chain of 20 SECs

The above delay times allow the reversal of the synchronization flow in a chain of 20 NEs with SEC timing within 15,6 s. The change of the synchronization direction through 20 SECs requires 39 steps, as shown below:

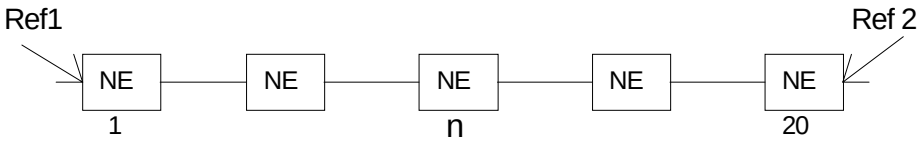

Figure 11: Linear chain of SECs

Step	Action
1	Ref 1 disappears from the first NE of the chain, NE 1 goes into holdover mode and transmits a new SSM. (**T_{HM}** 2 s maximum)
2 to 19	NE n (n = 2,3,..,19) transmits the new SSM without switch of reference to NE n. (**T_{NSM}**200 ms maximum)
20	NE 20 switches to Ref 2. (**T_{SM}** 500 ms maximum)
21 to 39	NE n (n = 19,18,..,1) change to sync received from NE n+1. (**T_{SM}** 500 ms maximum)

This leads to a maximum restoration time of 15,6 s (**T_{HM}** +18 **T_{NSM}** +20 **T_{SM}**).

4.15 Delay times for NEs with SSU or for SASE

For further study.

4.16 Synchronization layer functions

The atomic functions which are involved in the transport of synchronization within the NE are shown in the following figure.

This figure shows two synchronization layers plus the transport layer:

a) The synchronization distribution layer: This layer terminates and adapts the synchronization trails to the network synchronization layer and performs a pre selection of candidate input ports.

b) The network synchronization layer : This layer performs the selection of a timing reference.

c) The transport layer providing the synchronization related SD_CI information.

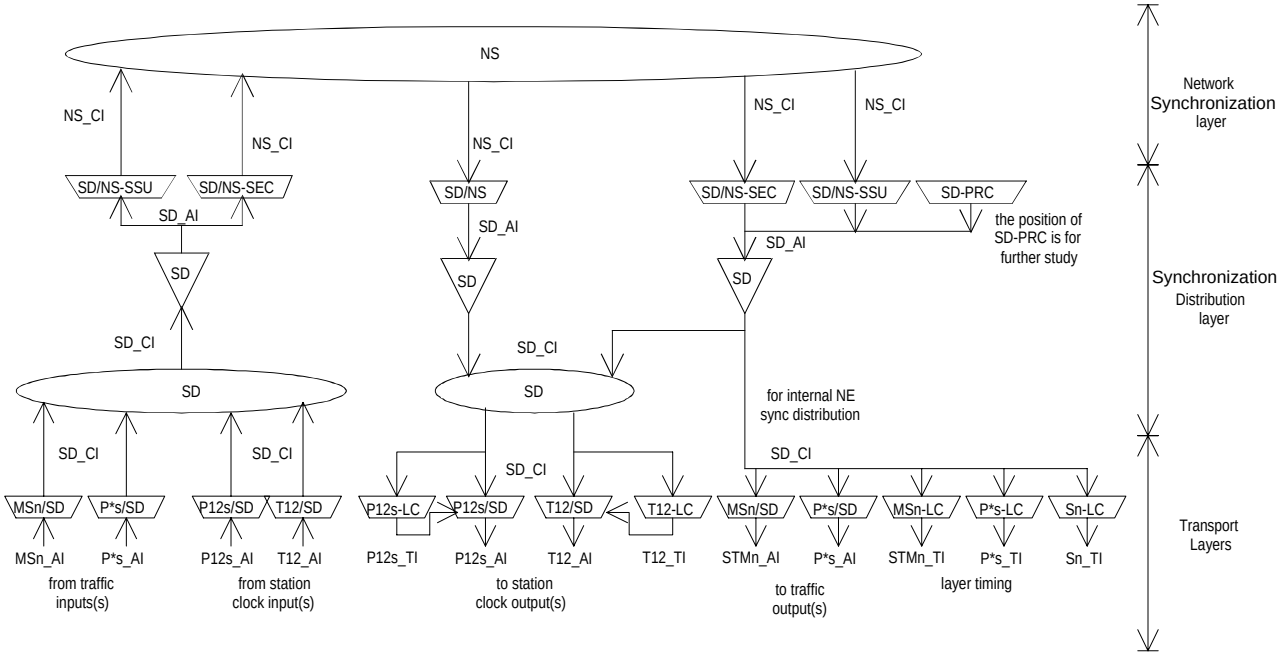

Figure 12: Synchronization Distribution and Network Synchronization layer atomic functions

The relation between the current naming of synchronization signals in ITU-T Recommendation G.783 [5] and in ETS 300 417-1-1 [1] is shown on the following table.

Table 7: Naming of synchronization signals

ITU-T Recommendation G.783 [5] naming	ETS 300 417-1-1 [1] naming
T0	SD_CI signal for internal NE sync distribution
T1	SD_CI signal derived from an STM-N (OSn/RSn/MSn) signal
T2	SD_CI signal derived from a 2 Mbit/s (E12/P12s) traffic carrying signal
T3	SD_CI signal derived from a 2 MHz station clock (T12) input signal
T4	SD_CI signal towards a 2 MHz station clock (T12) output signal
no name	SD_CI signal derived from a 34 Mbit/s synchronous (E31/P31s) signal
no name	SD_CI signal derived from a 140 Mbit/s synchronous (E4/P4s) signal
no name	SD_CI signal towards a 2 Mbit/s station clock (E12/P12s) output signal
no name	SD_CI signal derived from a 2 Mbit/s station clock (E12/P12s) signal

4.17 Overview of the processes performed within the atomic functions

A list of the synchronization atomic functions and a short description of their functionality is given in the table below. For a more detailed description see clauses 5 to 8.

Table 8: Functional overview of atomic functions

Atomic function	Functionality
XX-LC_A_So	Generation of the layer timing
XX/SD_A_Sk	Access to reference clock. SSM(TM) acceptance and extraction of QL; Generate QL-NotSupported if signal does not support SSM; Generation of CS;
XX/SD_A_So	Insertion of QL into SSM(TM); Generate QL-DNU or Squelch to prevent timing loops.
SD_C	Preselection of transport interfaces as possible synchronization sources. Selection of sources for the station clock outputs;
SD_TT_Sk	Report of QL to management. Manual insertion of a fixed QL value.
SD_TT_So	None.
SD/NS-SEC_A_Sk	None.
SD/NS-SSU_A_Sk	for further study.
SD/NS_A_So	Generation of the clock, for the station clock outputs from the selected synchronization reference.
SD/NS-SEC_A_So	generation of holdover, locked and free running modes timings. Generation of the NE clock (SEC type), locked to the selected synchronization reference.
SD/NS-SSU_A_So	Generation of the NE clock (SSU type), locked to the selected synchronization reference. The functionality and the position is for further study.
SD/NS-PRC_A_So	Generation of the NE clock (PRC) type. The functionality and the position is for further study.
NS_C	Selection of synchronization reference sources.

5 Synchronization distribution layer atomic functions

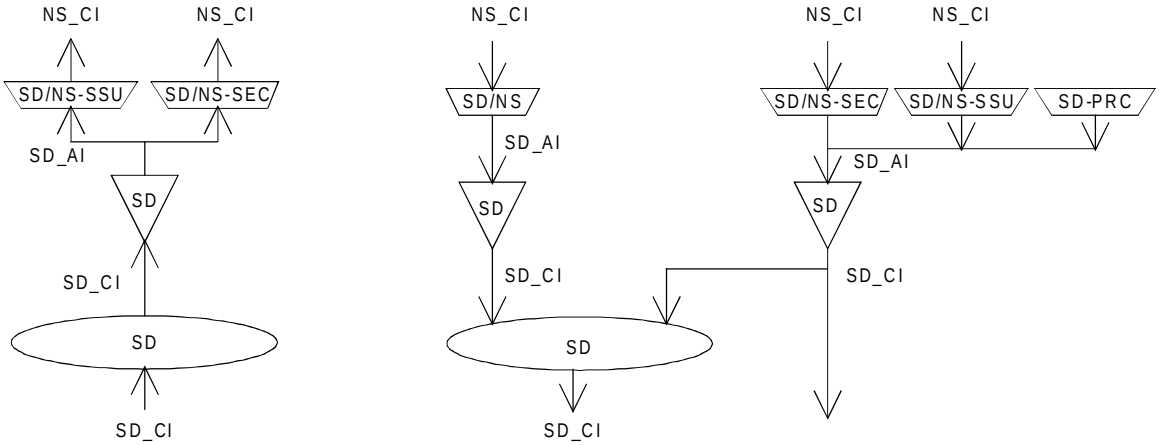

Figure 13: Synchronization distribution layer atomic functions

SD Layer CP

The CI at this point is a clock signal with associated server signal fail, Quality Level and clock source identifier.

SD Layer AP

The AI at this point is a clock signal with associated trail signal fail, Quality Level and clock source identifier.

5.1 SD Connection function (SD_C)

Symbol:

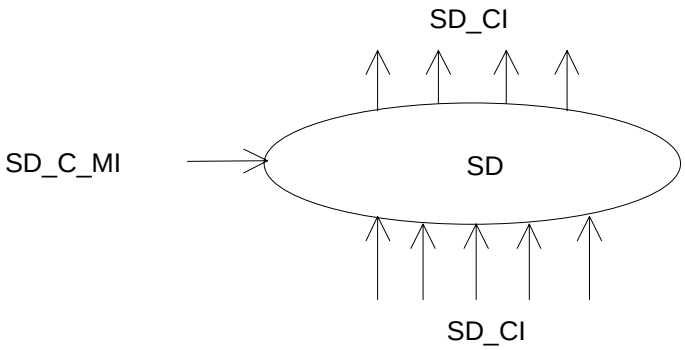

Figure 14: SD_C symbol

Interfaces:

Table 9: SD_C input and output signals

Input(s)	Output(s)
per SD_CI, n x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS per input output connection point SD_C_MI_ConnectionPortIds	per SD_CI, m x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS

Processes:

In the SD_C function SD Layer Characteristic Information is routed between input (termination) connection points ((T)CPs) and output (T)CPs by means of matrix connections.

NOTE 1: Neither the number of input/output signals to the connection function, nor the connectivity is specified in this ETS. That is a property of individual network elements.

Routing: The function shall be able to connect a specific input with a specific output by means of establishing a matrix connection between the specified input and output. It shall be able to remove an established matrix connection.

NOTE 2: Broadcast connections are handled as separate connections to the same input CP.

Unconnected SD signal generation: The function shall generate an unconnected SD signal, specified as: SSF true, CS value None, QL value QL-UNC and undefined clock.

NOTE 3: The unconnected signal is a logical signal defined for the purpose of this formal specification; it is not observable at any of the network elements transport interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected SD signal to the output.

Defect correlations: None.

Performance monitoring: None.

5.2 SD trail termination functions

5.2.1 SD trail termination source function (SD_TT_So)

Symbol:

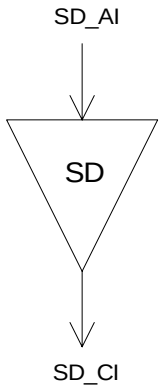

Figure 15: SD_TT_So symbol

Interfaces:

Table 10: SD_TT_So input and output signals

Input(s)	Output(s)
SD_AI_CK	SD_CI_CK
SD_AI_QL	SD_CI_QL
SD_AI_CS	SD_CI_CS
SD_AI_TSF	SD_CI_SSF

Processes: None.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect correlations: None.

Performance monitoring: None.

5.2.2 SD trail termination sink function (SD_TT_Sk)

Symbol:

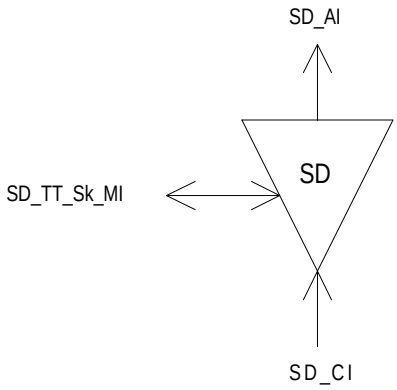

Figure 16: SD_TT_Sk symbol

Interfaces:

Table 11: SD_TT_Sk input and output signals

Input(s)	Output(s)
SD_CI_CK	SD_AI_CK
SD_CI_QL	SD_AI_QL
SD_CI_SSF	SD_AI_TSF
SD_CI_CS	SD_AI_CS
SD_TT_Sk_MI_QLoverwrite	SD_TT_Sk_MI_cSSF
SD_TT_Sk_MI_QLfixedValue	SD_TT_Sk_MI_QL
SD_TT_Sk_MI_QLmode	
SD_TT_Sk_MI_TPmode	
SD_TT_Sk_MI_SSF_Reported	

Processes:

This function terminates a synchronization trail transmitted via one of the synchronization information's transport layers, processes and reports the incoming quality. It can operate in QL-enabled mode and QL-disabled mode.

QL-disabled mode:

In QL disabled mode the function shall report the status of the trail (MI_cSSF).

QL-enabled mode:

In QL-enabled mode the function shall report the status of the trail (MI_cSSF) and the incoming quality level value (CI_QL) via MI_QL.

The function shall support the ability to pass through or overwrite the incoming quality level information.

Pass through:

The quality level output (AI_QL) shall be related to the quality level input (CI_QL) signal as specified in clause 4.

Overwrite:

The quality level output (AI_QL) is a fixed value provisioned via MI_QLfixedValue.

The selection between pass through and overwrite mode shall be controlled via MI_QLoverwrite. The default value of MI_QLoverwrite shall be FALSE. The default for MI_QLfixedValue shall be QL-DNU.

Table 12: Conversion of quality levels

CI_QL	MI_QLoverwrite	CI_SSF	AI_QL
QL-INV0	false	false	QL-INV
QL-INV1	false	false	QL-INV
QL-PRC	false	false	QL-PRC
QL-INV3	false	false	QL-INV
QL-SSUT	false	false	QL-SSUT
QL-INV5	false	false	QL-INV
QL-INV6	false	false	QL-INV
QL-INV7	false	false	QL-INV
QL-SSUL	false	false	QL-SSUL
QL-INV9	false	false	QL-INV
QL-INV10	false	false	QL-INV
QL-SEC	false	false	QL-SEC
QL-INV12	false	false	QL-INV
QL-INV13	false	false	QL-INV
QL-INV14	false	false	QL-INV
QL-DNU	false	false	QL-DNU
QL-NSUPP	false	false	QL-NSUPP
QL-UNC	false	true	QL-FAILED
all	true	false	MI_QLfixedValue
all	x	true	QL-FAILED

Defects: None.

Consequent actions:

aTSF ← CI_SSF

Defect correlations:

cSSF ← MON and CI_SSF and SSF_Reported

Performance monitoring: None.

5.3 SD adaptation functions

5.3.1 SD layer to NS layer SEC quality adaptation source function (SD/NS-SEC-A_So)

Symbol:

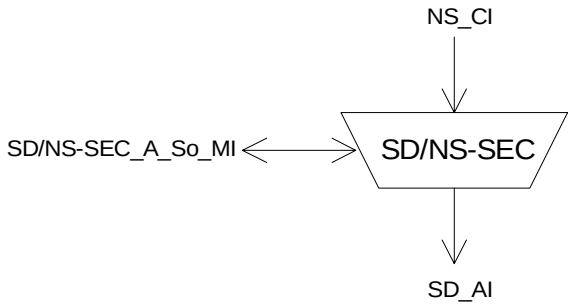

Figure 17: SD/NS-SEC_A_So symbol

Interfaces:

Table 13: SD/NS-SEC_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK	SD_AI_CK
NS_CI_QL	SD_AI_QL
NS_CI_SSF	SD_AI_CS
NS_CI_CS	SD/NS-SEC_A_So_MI_CkMode
SD/NS-SEC_A_So_MI_CkOperation	SD/NS-SEC_A_So_MI_cLTI
SD/NS-SEC_A_So_MI_ QLMode	

Processes:

This function generates a SEC type system clock as defined in ETS 300 462-2 [10] and specified in ETS 300 462-5 [12]. The function shall operate in QL-enabled or QL-disabled mode as selected by MI_QLMode.

The function shall support three types of operation:

- forced free running operation working in the free run mode;
- forced holdover operation, working in the holdover mode;
- normal operation, working in the locked or holdover mode depending on the input signals.

These 3 types of operation are activated by user management input (CkOperation) while modes, defined in ETS 300 462-1 [21], are automatically activated by the status of input signals. Figure 18 shows the relationship between types of operation and modes.

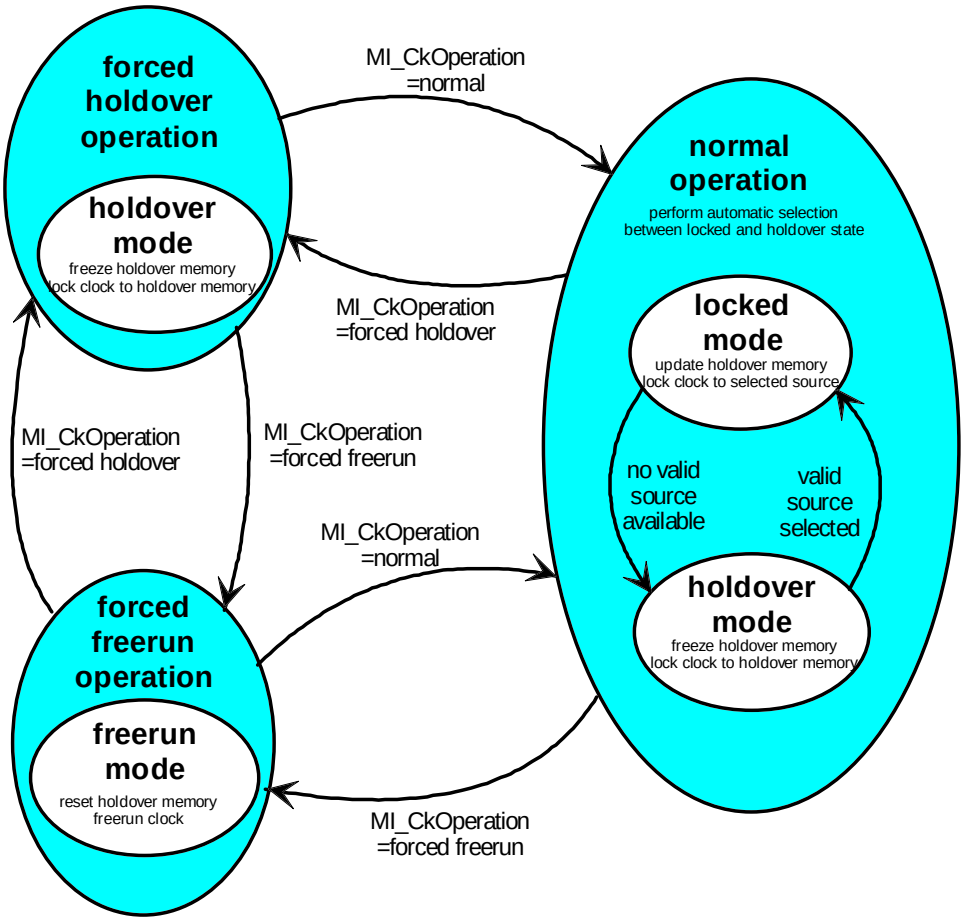

Figure 18: Operational types

Bandwidth, transients, pull in and pull out ranges, noise, input and output jitter for locked mode operation, holdover accuracy and output phase deviation for holdover mode operation, frequency accuracy, transients, noise and output jitter for freerun mode operation shall be as specified in ETS 300 462-5 [12].

Forced Free-running operation:

This type of operation is activated by a management command, the equipment is in free run mode.

- Clock generation:

  The outgoing clock (AI_Ck) is not defined by an incoming reference or stored incoming reference data in the holdover memory. The hold-over memory is reset to a default value.

- QL processing (in QL-enabled mode):

  The outgoing QL of the free running mode is QL-SEC.

- CS processing:

  The outgoing CS of the free running mode is None.

Forced holdover operation:

This type of operation is activated by a management command, the equipment is in holdover mode.

- Clock generation:

  The outgoing clock (AI_Ck) is defined by stored reference data in the holdover memory.

- QL processing (in QL-enabled mode):

  The outgoing QL of the holdover mode is QL-SEC.

- CS processing:

  The outgoing CS of the holdover mode is None.

Normal operation:

This type of operation is activated by a management command.

- Clock generation:

  The normal operation works according two modes, locked and holdover, selected automatically depending on the quality of the incoming reference signal and the selected QLMode:

  - Locked mode:

    In the locked mode the outgoing clock (AI_Ck) is locked to the incoming reference clock (CI_Ck) and the holdover memory is constantly updated with this reference clock.

  - Holdover mode:

    The holdover mode conforms to the holdover mode defined above. The holdover memory is no longer updated by the incoming reference clock.

  - QL-enabled mode:

    The locked mode is selected if the incoming reference is not in the signal fail state and the quality level of the incoming reference is better or equal to QL-SEC.

    The holdover mode is selected without delay when the incoming reference goes into the signal fail state or the quality level of the incoming signal is lower than QL-SEC.

    The holdover mode is left when both the signal fail state and the quality level of the incoming signal is equal or better than QL-SEC.

  - QL-disabled mode:

    The locked mode is selected if the incoming reference is not in the signal fail state.

    The holdover mode is selected when the incoming reference goes into the signal fail state.

    The actual mode is reported to the management (MI_CkMode).

  - QL processing (in QL-enabled mode):

    If the function is in the locked mode the outgoing QL follows the incoming QL.

    In case of a change of the selected synchronization source (change of the incoming CS), the outgoing QL shall be set to the new incoming QL after the settling time t_s, to allow the internal oscillator to adjust to a possible frequency change.

    If the incoming QL changes without a change of the selected synchronization source, the outgoing QL shall follow without settling time.

    If the function is in the holdover mode, the outgoing QL shall be set to QL-SEC as soon as the incoming CS value is "None" or if the incoming QL is too low (NS_CI_QL<"QL-SEC").

    After leaving the holdover mode, the outgoing QL shall be set to the new incoming QL after the settling time t_s.

The settling time t_s shall be in the range of 180 ms to 300 ms.

- CS processing:

  Normally the outgoing CS shall follow the incoming CS immediately.

  If the function is in the holdover mode due to a too low QL value of the selected source (NS_CI_QL<"QL-SEC"), the outgoing CS shall be set to "None".

Defects:

The function shall detect a Loss of Timing Inputs (dLTI) if a unconnected signal is present at its Connection Point (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "None" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS≠"None" for at least Y seconds. The values of X and Y are for further study.

Consequent actions: None.

Defect correlation:

cLTI ← dLTI

Performance monitoring: None.

5.3.2 SD layer to NS layer SEC quality adaptation source function (SD/NS-SEC_A_Sk)

Symbol:

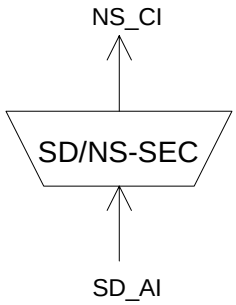

Figure 19: SD/NS-SEC_A_Sk symbol

Interfaces:

Table 14: SD/NS-SEC_A_Sk input and output signals

Input(s)	Output(s)
SD_AI_CK	NS_CI_CK
SD_AI_QL	NS_CI_QL
SD_AI_TSF	NS_CI_SSF
SD_AI_CS	NS_CI_CS

Processes:

This function connects input with output only. Currently no processes are defined within this function.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect Correlation: None.

Performance monitoring: None.

5.3.3 SD layer to NS layer SSU quality adaptation source function (SD/NS-SSU-A_So)

This function is for further study.

5.3.4 SD layer to NS layer SSU quality adaptation sink function (SD/NS-SSU_A_Sk)

This function is for further study.

5.3.5 SD layer to NS layer PRC quality adaptation source function (SD/NS-PRC-A_So)

This function is for further study.

5.3.6 SD layer to NS layer adaptation source function (SD/NS_A_So)

Symbol:

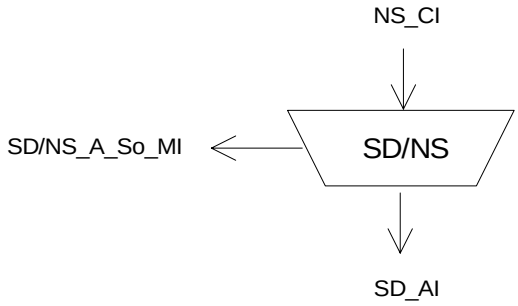

Figure 20: SD/NS_A_So symbol

Interfaces:

Table 15: SD/NS_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS	SD_AI_CK SD_AI_QL SD_AI_CS SD_AI_TSF SD/NS_A_So_MI_cLTI

Processes:

This function produces the station output clock process.

Wander limitation: The wander at the output of this function shall be within the MTIE mask specified in subclause 6.1 figure 2 of ETS 300 462-5 [12].

NOTE: There might be a need for an AIS generator, this is for further study.

Defects:

The function shall detect a Loss of Timing Inputs (dLTI) if a unconnected signal is present at its Connection Point (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "None" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS≠"None" for at least Y seconds. The values of X and Y are for further study.

Consequent actions:

aTSF ← CI_SSF

Defect Correlation:

cLTI ← dLTI

Performance monitoring: None.

6 Network synchronization layer atomic functions

Within this layer the same connection function is used for one or two independent selection processes which may have independent inputs:

- a single selection of an input reference for the NE synchronization distribution;

- a single or no selection of an input reference for the station clock output.

The use of several independent selection processes for this station clock output is for further study.

These two processes shall work in the same QL mode.

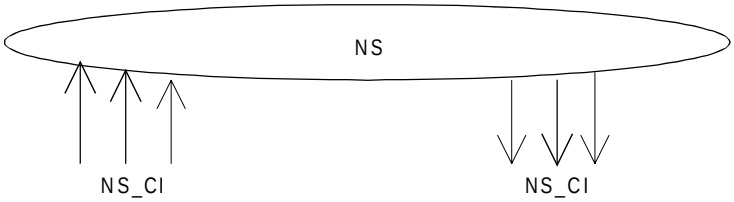

Figure 21: Network Synchronization layer atomic functions

NS Layer CP.

The CI at this point is a clock signal with associated server signal fail, quality level and clock source identifier.

6.1 NS_connection functions (NS_C)

Symbol:

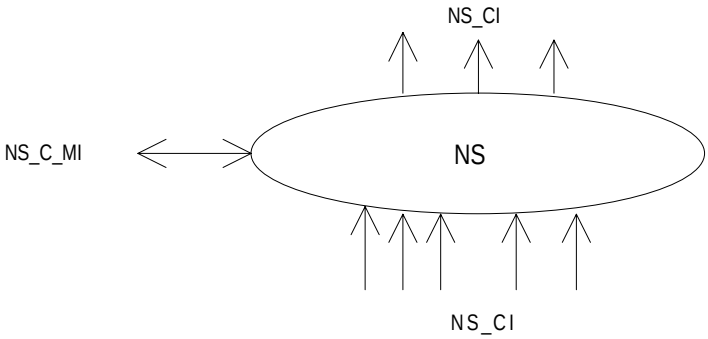

Figure 22: NS_C symbol

Interfaces:

Table 16: NS_C input and output signals

Input(s)	Output(s)
per input: NS_CI_Ck NS_CI_SSF NS_CI QL NS_CI_CS per function: NS_C_MI_QLmode per selector: NS_C_MI_WTR NS_C_MI_EXTCMD per input of a selector NS_C_MI_priority NS_C_MI_CLR_WTR NS_C_MI_Set_lockout NS_C_MI_Clr_Lockout	per output: NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS per selector: NS_C_MI_Selected Input NS_C_MI_Reject_Request per input of a selector: NS_C_MI_State

Processes:

This function performs one or more independent selection processes. Each selection process selects a synchronization source out of the nominated set of synchronization source inputs determined by the selection algorithm.

The function can operate in QL enabled or disabled mode as defined by MI_QLmode.

NOTE 1: The number of input signals to the connection process and the amount of connection processes in the function are not specified in this ETS. That is a property of individual network elements. Examples are presented in annex D.

Automatic reference selection process:

The function shall perform the automatic reference selection process as defined in subclause 4.6 and annex A.

External commands:

The function shall support the use of external commands as defined in subclause 4.11.

Priority:

The function shall support the use of synchronization source priorities as defined in subclause 4.10.

Holdoff time:

The function shall support a holdoff timer per input of a selection process (nominated source) as defined in subclause 4.8.

Wait to restore time:

The function shall support a wait to restore timer per input of a selection process (nominated source) as defined in subclause 4.9.

Via MI_CLR_WTR the WTR timer can be cleared before the WTR time is expired.

Signal fail extension:

For each input to a selection process the signal fail information to the Selector is a combination (OR function) of the incoming signal fail information (CI_SSF) and the signal fail information delayed by the WTR and holdoff process.

SSF[m] = CI_SSF[m] or WTR/HO[CI_SSF[m]]

Status report:

The state of each input to a selection process (available, failed, WTR) shall be reported via MI_State.

The actual selected source of a selection process shall be reported via MI_SelectedInput.

Unconnected NS signal generator:

The function shall generate an unconnected NS signal. The unconnected NS signal has a undefined clock, a quality level of QL-UNC, a CS value of "None" and signal fail true.

NOTE 2: This signal is a logical signal defined for the purpose of this formal specification; it is not observable as such at any of the network elements interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected NS signal to the output.

Defect Correlations: None.

Performance monitoring: For further study.

7 Transport layer to SD layer atomic function

7.1 STM-1 multiplex section adaptation functions

7.1.1 STM-1 multiplex section to sd adaptation source (MS1/SD_A_So)

Symbol:

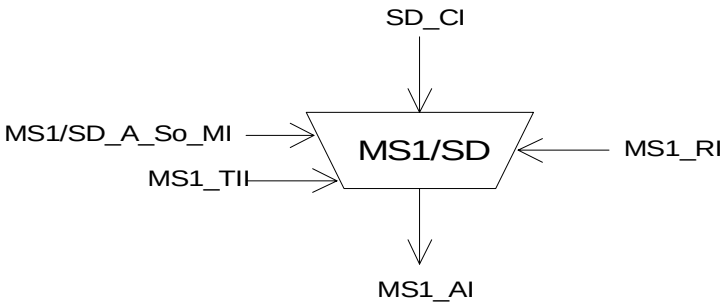

Figure 23: MS1/SD_A_So symbol

Interfaces:

Table 17: MS1/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS1_TI_CK MS1_TI_FS MS1_RI_CS MS1/SD_A_So_MI_SSMdis MS1/SD_A_So_MI_QLmode	MS1_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [2].

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). Table 18 presents the relation between the existing set of QLs and the output SSM.

Table 18: Quality Level set coding into Synchronization Status Message (SSM)

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

```
if (MI_QLmode== dis)
then   S1[5-8] = 1111
else   if (RI_CS == CI_CS) or (SSMdis == true)
                    then   S1[5-8] = 1111
                    else   S1[5-8] = SSM[CI_QL]
               fi
fi
```

Defect Correlations: None.

Performance monitoring: None.

7.1.2 STM-1 multiplex section to SD adaptation sink (MS1/SD_A_Sk)

Symbol:

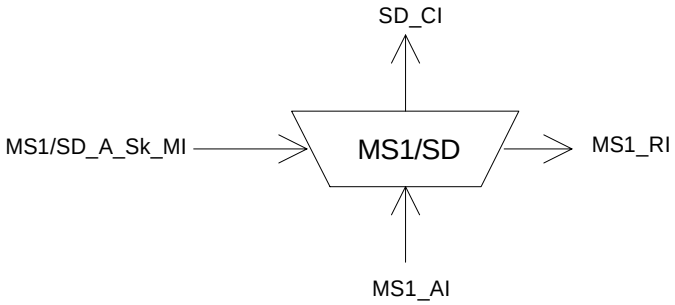

Figure 24: MS1/SD_A_Sk symbol

Interfaces:

Table 19: MS1/SD_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D	SD_CI_CK
MS1_AI_CK	SD_CI_SSF
MS1_AI_FS	SD_CI_CS
MS1_AI_TSF	SD_CI_QL
MS1/SD_A_Sk_MI_SSMsupp	MS1_RI_CS
MS1/SD_A_Sk_MI_CSid	
MS1/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [2]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

```
if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then   CI_QL = QL-NSUPP
else   CI_QL = QL[SSM]
fi
```

Defect Correlations: None.

Performance monitoring: None.

7.2 STM-4 multiplex section adaptation functions

7.2.1 STM-4 multiplex section to SD adaptation source (MS4/SD_A_So)

Symbol:

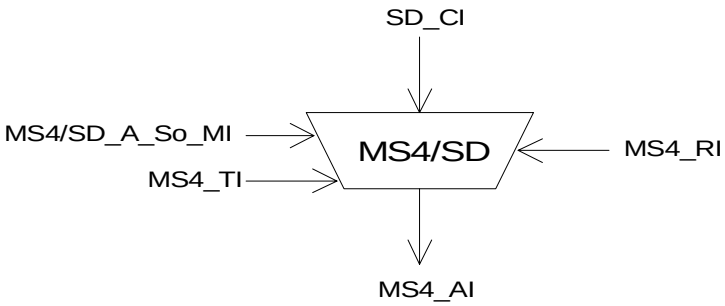

Figure 25: MS4/SD_A_So symbol

Interfaces:

Table 20: MS4/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS4_TI_CK MS4_TI_FS MS4_RI_CS MS4/SD_A_So_MI_SSMdis MS4/SD_A_So_MI_QLmode	MS4_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [2].

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM.

Table 21: Quality Level set coding into Synchronization Status Message

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

```
if (MI_QLmode== dis)
then   S1[5-8] = 1111
else   if (RI_CS == CI_CS) or (SSMdis == true)
                    then   S1[5-8] = 1111
                    else   S1[5-8] = SSM[CI_QL]
               fi
fi
```

Defect Correlations: None.

Performance monitoring: None.

7.2.2 STM-4 multiplex section to SD adaptation sink (MS4/SD_A_Sk)

Symbol:

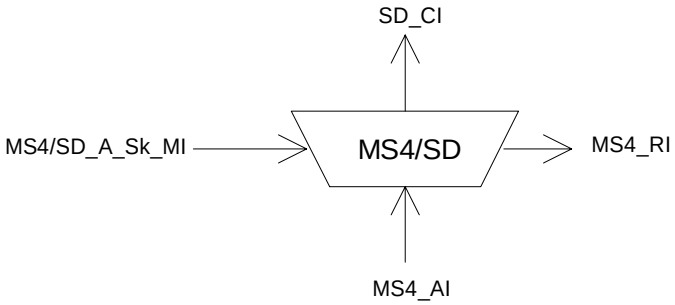

Figure 26: MS4/SD_A_Sk symbol

Interfaces:

Table 22: MS4/SD_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D	SD_CI_CK
MS4_AI_CK	SD_CI_SSF
MS4_AI_FS	SD_CI_CS
MS4_AI_TSF	SD_CI_QL
MS4/SD_A_Sk_MI_SSMsupp	MS4_RI_CS
MS4/SD_A_Sk_MI_CSid	
MS4/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [2]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then CI_QL = QL-NSUPP
else CI_QL = QL[SSM]
fi

Defect Correlations: None.

Performance monitoring: None.

7.3 STM-16 multiplex section adaptation functions

7.3.1 STM-16 multiplex section to SD adaptation source (MS16/SD_A_So)

Symbol:

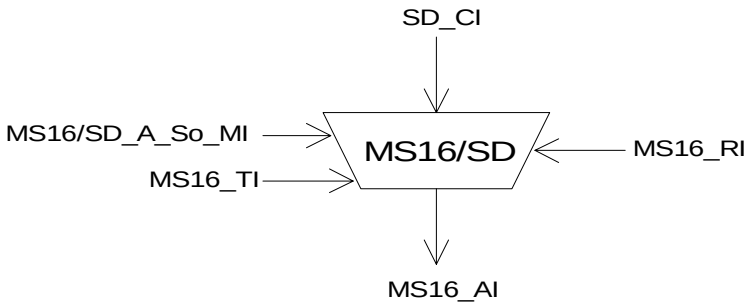

Figure 27: MS16/SD_A_So symbol

Interfaces:

Table 23: MS16/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS16_TI_CK MS16_TI_FS MS16_RI_CS MS16/SD_A_So_MI_SSMdis MS16/SD_A_So_MI_QLmode	MS16_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [2].

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM.

Table 24: Quality Level set coding into Synchronization Status Message

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

```
if (MI_QLmode== dis)
then   S1[5-8] = 1111
else   if (RI_CS == CI_CS) or (SSMdis == true)
                    then   S1[5-8] = 1111
                    else   S1[5-8] = SSM[CI_QL]
               fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.3.2 STM-16 multiplex section to SD adaptation sink (MS16/SD_A_Sk)

Symbol:

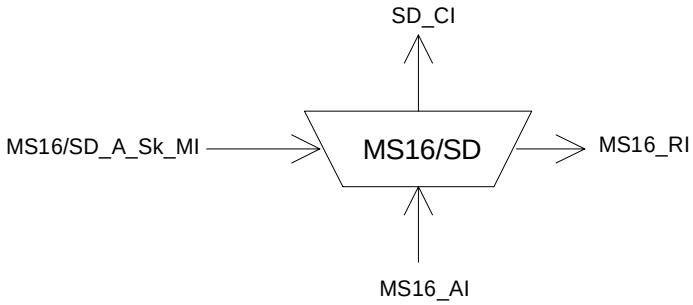

Figure 28: MS16/SD_A_Sk symbol

Interfaces:

Table 25: MS16/SD_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D	SD_CI_CK
MS16_AI_CK	SD_CI_SSF
MS16_AI_FS	SD_CI_CS
MS16_AI_TSF	SD_CI_QL
MS16/SD_A_Sk_MI_SSMsupp	MS16_RI_CS
MS16/SD_A_Sk_MI_CSid	
MS16/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [2]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then CI_QL = QL-NSUPP
else CI_QL = QL[SSM]
fi

Defect correlations: None.

Performance monitoring: None.

7.4 P31s adaptation functions

7.4.1 P31s to SD adaptation source (P31s/SD_A_So)

Symbol:

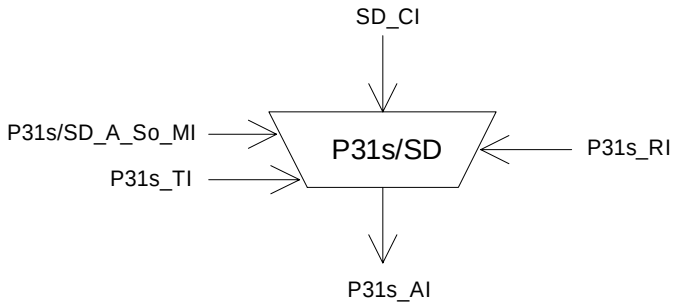

Figure 29: P31s/SD_A_So symbol

Interfaces:

Table 26: P31s/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CSP31s_TI_CK P31s_TI_FS P31s_TI_MFS P31s_RI_CS P31s/SD_A_So_MI_TMmode P31s/SD_A_So_MI_SSMdis P31s/SD_A_So_MI_QLmode	P31s_AI_D

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code (multiframed bit 8 of byte MA), or into the 1 bit TM code, as defined in subclause 4.3.4 of ETS 300 337 [15]. This is controlled by MI_TMmode.

TMmode: For the case TMmode is disabled the function shall generate the SSM code. For the case TMmode is enabled the function shall generate the TM code.

MA[6-7]: If TMmode is disabled, the value of the multiframe indicator bits shall be set as specified by ETS 300 337 [16], 500 µs TU multiframe sequence, and aligned with P31s_TI_MFS. If TMmode is enabled, the multiframe indicator shall not be generated.

					multiframe indicator		
1	2	3	4	5	6	7	8

Figure 30: multiframe indicator bits in byte MA

The SSM or TM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM and TM codes.

NOTE: Setting of these bits is also in P31s/SX_A_So. This is an open issue for the public enquiry.

Table 27: Quality Level set coding into Synchronization Status Message and Timing Marker

Quality Level (CI_QL)	SSM coding [MSB..LSB]	TM coding
QL-PRC	0010	0
QL-SSUT	0100	1
QL-SSUL	1000	1
QL-SEC	1011	1

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern, while the transmitted TM code shall be forced to the "1" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM [TM] shall be forced to the "1111" ["1"] pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM/TM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM [TM] to the "1111" ["1"] pattern.

MA[8], MA[8][1-4]: For the case of TMmode is disabled, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall transport the 4 bit SSM code. For the case of TMmode is enabled, bit 8 of byte MA shall transport the 1 bit TM code.

Defects: None.

Consequent actions:

```
if (MI_TMmode == dis)
        then   if (MI_QLmode == dis)
                then   MA[8][1-4] = 1111
                else   if  (RI_CS == CI_CS) or (SSMdis == true)
                                then   MA[8][1-4] = 1111
                                else   MA[8][1-4] = SSM[CI_QL]
                       fi
        else   if (MI_QLmode == dis)
                then   MA[8] = 1
                else   if  (RI_CS == CI_CS) or (SSMdis == true)
                                then   MA[8] = 1
                                else   MA[8] = TM[CI_QL]
                       fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.4.2 P31s to SD adaptation sink (P31s/SD_A_Sk)

Symbol:

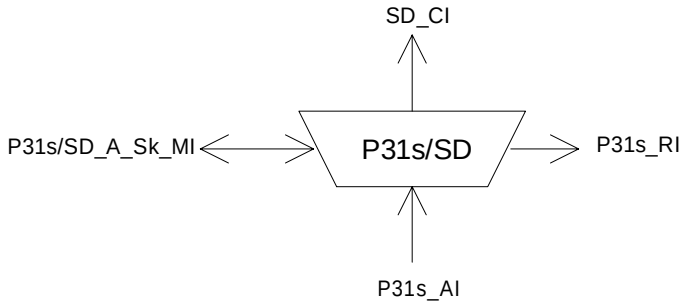

Figure 31: P31s/SD_A_Sk symbol

Interfaces:

Table 28: P31s/SD_A_Sk input and output signals

Input(s)	Output(s)
P31s_AI_D	SD_CI_CK
P31s_AI_CK	SD_CI_SSF
P31s_AI_FS	SD_CI_CS
P31s_AI_TSF	SD_CI_QL
P31s/SD_A_So_MI_TMmode	P31s_RI_CS
P31s/SD_A_So_MI_QLmode	P31s/SD_A_Sk_MI_cLOM
P31s/SD_A_Sk_MI_SSMsupp	
P31s/SD_A_Sk_MI_CSid	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via the multiframed bit 8 of byte MA, or the 1 bit Timing Marker (TM), transmitted via bit 8 of byte MA as defined in ETS 300 337 [15]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

TMmode: For the case TMmode is disabled the function shall interprete bit 8 of byte MA as the SSM code. For the case TMmode is enabled the function shall interprete bit 8 of byte MA as the TM code.

MA[6-7]: In QL-enabled mode and if TMmode is disabled and if SSMsupp is true, the function shall recover the 500 µs (multi)frame start phase performing multi-frame alignment on bits 6 and 7 of byte MA. Out-Of-Multiframe (OOM) shall be assumed once when an error is detected in the MA bit 6 and 7 sequence. Multiframe alignment shall be assumed to be recovered, and the In-Multiframe (IM) state shall be entered, when in four consecutive P31s frames an error free MA sequence is found.

NOTE: Setting of these bits is also in P31s/SX_A_So. This is an open issue for the public enquiry.

MA[8][1-4]: In QL-enabled mode and if TMmode is disabled and SSMsupp is true, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall be recovered and accepted if the same code is present in three consecutive 4 bit multiframes. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

MA[8]: In QL-enabled mode and if TMmode is enabled and SSMsupp is true, bit 8 of byte MA shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[TM] as specified in table 5 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM/TM support: For the case MI_SSMsupp is false, the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects:

If the multiframe alignment process is in the OOM state and the MA[6-7] multiframe is not recovered within X ms, a dLOM defect shall be declared. Once in a dLOM state, this state shall be exited when the multiframe is recovered (multiframe alignment process enter the IM state). X shall be a value in the range 1 ms to 5 (ms). X is not configurable. dLOM shall be cleared when QLmode is disabled or SSMsupp is false or TMmode is enabled.

Consequent actions:

aSSF ← dLOM or AI_TSF

```
if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then   CI_QL = QL-NSUPP
else   if (MI_TMmode == disabled)
              then   CI_QL = QL[SSM]
              else   CI_QL = QL[TM]
              fi
fi
```

Defect correlations:

cLOM ← dLOM and (not AI_TSF)

Performance monitoring: None.

7.5 P4s adaptation functions

7.5.1 P4s to SD adaptation source (P4s/SD_A_So)

Symbol:

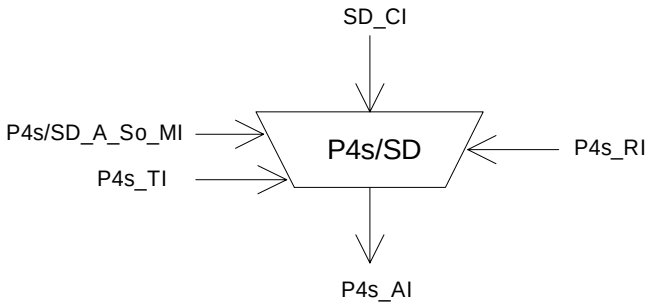

Figure 32: P4s/SD _A_So symbol

Interfaces:

Table 29: P4s/SD _A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS P4s_TI_CK P4s_TI_FS P4s_TI_MFS P4s_RI_CS P4s/SD_A_So_MI_TMmode P4s/SD_A_So_MI_SSMdis P4s/SD_A_So_MI_QLmode	P4s_AI_D

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code (multiframed bit 8 of byte MA), or into the 1 bit TM code, as defined in subclause 4.3.4 of ETS 300 337 [15]. This is controlled by MI_TMmode.

TMmode: For the case TMmode is disabled the function shall generate the SSM code. For the case TMmode is enabled the function shall generate the TM code.

MA[6-7]: If TMmode is disabled, the value of the multiframe indicator bits shall be set as specified by ETS 300 337 [16], 500 µs TU multiframe sequence, and aligned with P4s_TI_MFS. If TMmode is enabled, the multiframe indicator shall not be generated.

Figure 33: Multiframe indicator bits in byte MA

The SSM or TM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM and TM codes.

NOTE: Setting of these bits is also in P31s/SX_A_So. This is an open issue for the public enquiry.

Table 30: Quality Level set coding into Synchronization Status Message and Timing Marker

Quality Level (CI_QL)	SSM coding [MSB..LSB]	TM coding
QL-PRC	0010	0
QL-SSUT	0100	1
QL-SSUL	1000	1
QL-SEC	1011	1

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern, while the transmitted TM code shall be forced to the "1" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM [TM] shall be forced to the "1111" ["1"] pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM/TM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM [TM] to the "1111" ["1"] pattern.

MA[8], MA[8][1-4]: For the case of TMmode is disabled, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall transport the 4 bit SSM code. For the case of TMmode is enabled, bit 8 of byte MA shall transport the 1 bit TM code.

Defects: None.

Consequent actions:

```
if (MI_TMmode == dis)
        then   if (MI_QLmode == dis)
                then   MA[8][1-4] = 1111
                else   if  (RI_CS == CI_CS) or (SSMdis == true)
                                then   MA[8][1-4] = 1111
                                else   MA[8][1-4] = SSM[CI_QL]
                       fi
        else   if (MI_QLmode == dis)
                then   MA[8] = 1
                else   if  (RI_CS == CI_CS) or (SSMdis == true)
                                then   MA[8] = 1
                                else   MA[8] = TM[CI_QL]
                       fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.5.2 P4s to SD adaptation sink (P4s/SD_A_Sk)

Symbol:

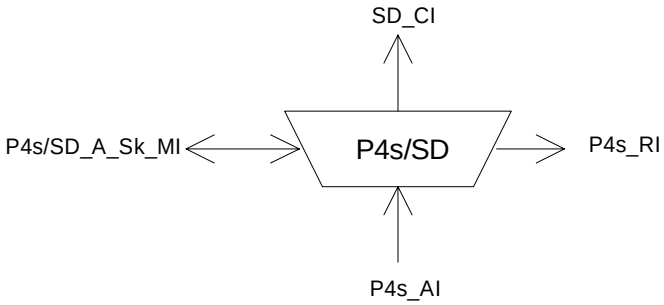

Figure 34: P4s/SD_A_Sk symbol

Interfaces:

Table 31: P4s/SD_A_Sk input and output signals

Input(s)	Output(s)
P4s_AI_D	SD_CI_CK
P4s_AI_CK	SD_CI_SSF
P4s_AI_FS	SD_CI_CS
P4s_AI_TSF	SD_CI_QL
P4s/SD_A_So_MI_TMmode	P4s_RI_CS
P4s/SD_A_So_MI_QLmode	P4s/SD_A_Sk_MI_cLOM
P4s/SD_A_Sk_MI_SSMsupp	
P4s/SD_A_Sk_MI_CSid	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via the multiframed bit 8 of byte MA, or the 1 bit Timing Marker (TM), transmitted via bit 8 of byte MA as defined in ETS 300 337 [15]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

TMmode: For the case TMmode is disabled the function shall interprete bit 8 of byte MA as the SSM code. For the case TMmode is enabled the function shall interprete bit 8 of byte MA as the TM code.

MA[6-7]: In QL-enabled mode and if TMmode is disabled and if SSMsupp is true, the function shall recover the 500 µs (multi)frame start phase performing multi-frame alignment on bits 6 and 7 of byte MA. Out-of-multiframe (OOM) shall be assumed once when an error is detected in the MA bit 6 and 7 sequence. Multiframe alignment shall be assumed to be recovered, and the in-multiframe (IM) state shall be entered, when in four consecutive P4s frames an error free MA sequence is found.

NOTE: Setting of these bits is also in P31s/SX_A_So. This is an open issue for the public enquiry.

MA[8][1-4]: In QL-enabled mode and if TMmode is disabled and SSMsupp is true, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall be recovered and accepted if the same code is present in three consecutive 4 bit multiframes. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

MA[8]: In QL-enabled mode and if TMmode is enabled and SSMsupp is true, bit 8 of byte MA shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[TM] as specified in table 5 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM/TM support: For the case MI_SSMsupp is false, the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects:

If the multiframe alignment process is in the OOM state and the MA[6-7] multiframe is not recovered within X ms, a dLOM defect shall be declared. Once in a dLOM state, this state shall be exited when the multiframe is recovered (multiframe alignment process enter the IM state). X shall be a value in the range 1 to 5 (ms). X is not configurable. dLOM shall be cleared when QLmode is disabled or SSMsupp is false or TMmode is enabled.

Consequent actions:

aSSF ← dLOM or AI_TSF

```
if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then  CI_QL = QL-NSUPP
else  if (MI_TMmode == disabled)
            then  CI_QL = QL[SSM]
            else  CI_QL = QL[TM]
            fi
fi
```

Defect correlations:

cLOM ← dLOM and (not AI_TSF)

Performance monitoring: None.

7.6 P12s layer adaptation functions

7.6.1 P12s layer adaptation source functions

Two types of P12s/SD_A_So functions are defined:

- type 1 for a 2 Mbit/s station clock output: P12s/SD-sc-1_A_So;
- type 2 for a 2 Mbit/s station clock output not supporting SSM messages: P12s/SD-sc-2_A_So.

Other types are for further study.

7.6.1.1 type 1 P12s to SD adaptation source for station clock output supporting SSM (P12s/SD-sc-1_A_So)

Symbol:

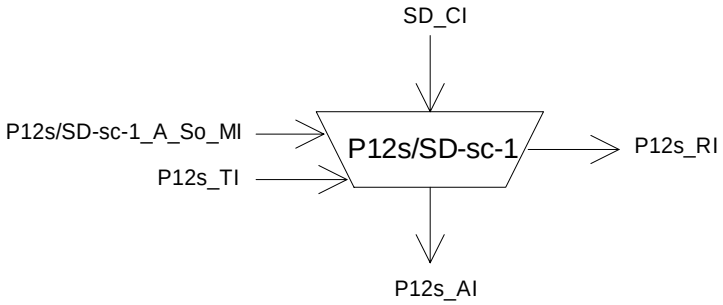

Figure 35: P12s/SD-sc-1_A_So symbol

Interfaces:

Table 32: P12s/SD-sc-1_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	P12s_AI_D
SD_CI_CS	P12s_AI_CK
SD_CI_SSF	P12s_AI_FS
P12s_TI_CK	P12s_AI_MFS
P12s_TI_FS	P12s_AI_AISinsert
P12s_TI_MFS	P12s_RI_CS
P12s/SD-sc-1_A_So_MI_SelSaSSM	P12s_RI_QL
P12s/SD-sc-1_A_So_MI_QLmode	
P12s/SD-sc-1_A_So_MI_Old	
P12s/SD-sc-1_A_So_MI_QLminimum	

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code transmitted in one of the five S_a bits, as defined in ITU-T Recommendation G.704 [14], and an AISinsert control signal.

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM codes.

Table 33: Quality Level set coding into Synchronization Status Message

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011
QL-UNC	1111

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available.

Sax: The 4 bit SSM code shall be inserted in one of the Sa bits (S_{ax}, x = 4 to 8) as selected via MI_SelSaSSM. The four bit SSM code shall be transported in alignment with the CRC-4 submultiframe.

Interworking: For interworking with old equipment not supporting SSM processing AIS insertion can be used instead of SSM insertion to pass synchronization quality information via the interface. For the case MI_Old is true, the function shall force the SSM to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS and the clock quality level received via CI_QL into RI_QL to support timing loop prevention as described under consequent actions (see subclause 4.13).

Defects: None.

Consequent actions:

```
if (MI_QLmode== dis)
then   Sax[1-4] = 1111
            RI_QL = QL-NSUPP
            if (CI_SSF == true)
            then   AI_AISinsert = true
                   RI_CS = none
            else   AI_AISinsert = false
                   RI_CS = CI_CS
            fi
else        if (MI_Old==true)
                   then   Sax[1-4] = 1111
                   RI_QL=QL-NSUPP
                   if(CI_SSF == true) or (CI_QL<MI_QLminimum)
                   then   AI_AISinsert = true
                          RI_CS = none
                   else   AI_AISinsert = false
                          RI_CS = CI_CS
                   fi
            if

else   AI_AISinsert = false
            if (CI_SSF == true)
            then   Sax[1-4] = 1111
                   RI_CS = none
                   RI_QL = QL-DNU
            else   Sax[1-4] = SSM[CI_QL]
                   RI_CS = CI_CS
                   RI_QL = CI_QL
            fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.6.1.2 type 2 P12s to SD adaptation source for station clock output port not supporting SSM (P12s/SD-sc-2_A_So)

Symbol:

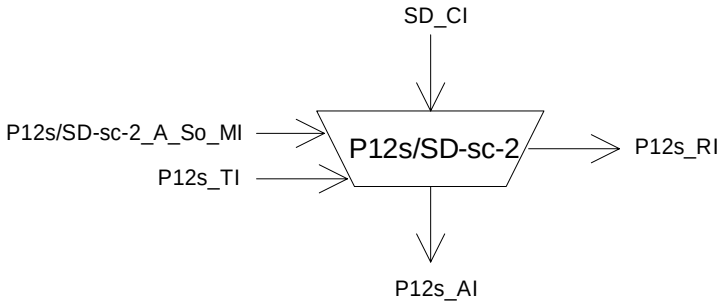

Figure 36: P12s/SD-sc-2_A_So symbol

Interfaces:

Table 34: P12s/SD-sc-2_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	P12s_AI_CK
SD_CI_CS	P12s_AI_FS
SD_CI_SSF	P12s_AI_MFS
P12s_TI_CK	P12s_AI_AISinsert
P12s_TI_FS	P12s_RI_CS
P12s_TI_MFS	P12s_RI_QL
P12s/SD-sc-2_A_So_MI_QLminimum	
P12s/SD-sc-2_A_So_MI_QLmode	

Processes:

This function converts the CI_QL and CI_SSF information into an AISinsert control signal.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) AI_AISinsert shall be activated if CI_SSF is true. For the case of QL-enabled mode, AI_AISinsert shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see also subclause 4.13). RI_QL shall be fixed to QL-NSUPP.

Defects: None.

Consequent actions:

```
RI_QL = QL-NSUPP
if (MI_QLmode == dis)
then   if (CI_SSF == true)
               then   AI_AISinsert = true
                      RI_CS = none
               else   AI_AISinsert = false
                      RI_CS = CI_CS
               fi
else   if (CI_SSF == true) or (CI_QL < MI_QLminimum)
               then   AI_AISinsert = true
                      RI_CS = none
               else   AI_AISinsert = false
                      RI_CS = CI_CS
               fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.6.2 P12s layer adaptation sink functions

Two types of P12s/SD_A_Sk functions are defined:

- type 1 for a 2 Mbit/s traffic input port: P12s/SD-tf_A_Sk;
- type 2 for a 2 Mbit/s station clock input port: P12s/SD-sc_A_Sk.

7.6.2.1 type 1 P12s to SD adaptation sink for traffic input port (P12s/SD-tf_A_Sk)

Symbol:

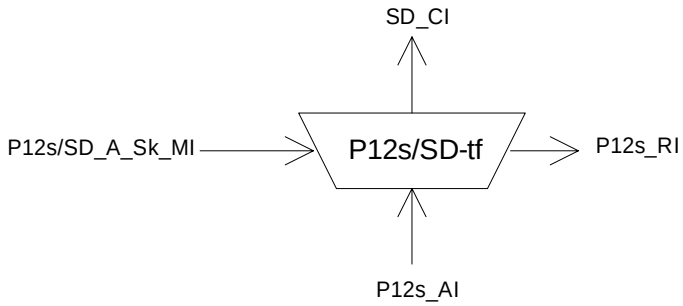

Figure 37: P12s/SD-tf_A_Sk symbol

Interfaces:

Table 35: P12s/SD-tf_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D	SD_CI_CK
P12s_AI_CK	SD_CI_SSF
P12s_AI_FS	SD_CI_CS
P12s_AI_TSF	SD_CI_QL
P12s_AI_MFS	P12s_RI_CS (for further study)
P12s_AI_LOM	
P12s/SD-tf_A_Sk_MI_SSMsupp	
P12s/SD-tf_A_Sk_MI_SelSaSSM	
P12s/SD-tf_A_Sk_MI_QLmode	
P12s/SD-tf_A_Sk_MI_CSid	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via one of the S_a bits as defined in ITU-T Recommendation G.704 [14]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

Sax[1-4]: In QL-enabled mode and if SSMsupp is true, bits Sax[1] to Sax[4] (x = MI_SelSaSSM is a value in the set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS to support timing loop prevention as described in subclause 4.13. RI_CS generation is for further study.

Defects: None.

Consequent actions:

aSSF ← AI_TSF or (AI_ LOM and Qlmode==enabled and SSMsupp==true)

if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then CI_QL = QL-NSUPP
else CI_QL = QL[SSM]
fi

Defect correlations: None

Performance monitoring: None.

7.6.2.2 type 2 P12s to SD adaptation sink for station clock input port (P12s/SD-sc_A_Sk)

Symbol:

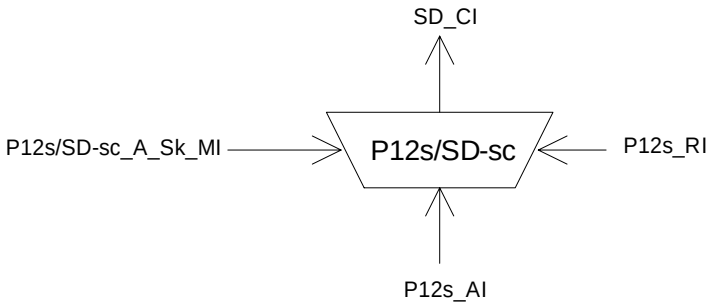

Figure 38: P12s/SD-sc _A_Sk symbol

Interfaces:

Table 36: P12s/SD-sc_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D	SD_CI_CK
P12s_AI_CK	SD_CI_SSF
P12s_AI_FS	SD_CI_CS
P12s_AI_TSF	SD_CI_QL
P12s_AI_MFS	
P12s_AI_LOM	
P12s_RI_CS	
P12s_RI_QL	
P12s/SD-tf_A_Sk_MI_SSMsupp	
P12s/SD-tf_A_Sk_MI_SelSaSSM	
P12s/SD-tf_A_Sk_MI_CSid	
P12s/SD-sc_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit Synchronization Status Message (SSM), transmitted via one of the S_a bits as defined in ITU-T Recommendation G.704 [14]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

Sax: In QL-enabled mode and if SSMsupp is true, bits Sax[1] to Sax[4] (x = MI_SelSaSSM is a value in the set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall process the clock source identifier received via RI_CS to support timing loop prevention (see subclause 4.13). The function shall determine the value of the CI_CS output signal as follows:

```
if (RI_CS == none)
then   CI_CS = MI_CSid
else   if (SSMsupp == true) and (MI_QLMode==enabled)
               then   if (RI_QL == CI_QL) or (RI_QL == QL-NSUPP)
                      then   CI_CS = RI_CS
                      else   CI_CS = MI_CSid
                      fi
               else   CI_CS = RI_CS
               fi
fi
```

Defects: None.

Consequent actions:

aSSF ← AI_TSF or (AI_LOM and Qlmode==enabled and SSMsupp==true)

```
if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then   CI_QL = QL-NSUPP
else   CI_QL = QL[SSM]
fi
```

Defect correlations: None

Performance monitoring: None.

7.7 T12 layer adaptation functions

7.7.1 T12 to SD adaptation source (T12/SD_A_So)

Symbol:

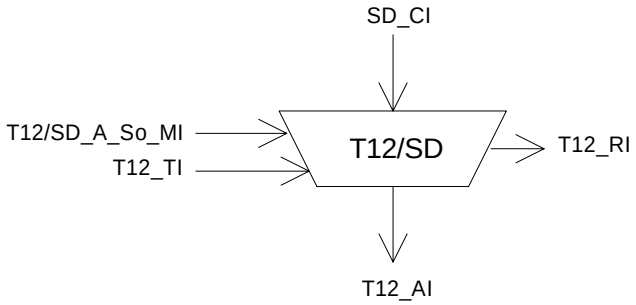

Figure 39: T12/SD_A_So symbol

Interfaces:

Table 37: T12/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF SD_CI_CK T12/SD_A_So_MI_QLminimum T12/SD_A_So_MI_QLmode	T12_AI_CK T12_AI_SQLCH T12_RI_CS T12_RI_QL

Processes:

This function converts the CI_QL and CI_SSF information into an SQLCH control signal.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) AI_SQLCH shall be activated if CI_SSF is true. For the case of QL-enabled mode, AI_SQLCH shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see also subclause 4.13). RI_QL shall be fixed to QL-NSUPP.

Defects: None.

Consequent actions:

```
RI_QL = QL-NSUPP
if (MI_QLmode == dis)
then    if (CI_SSF == true)
                then    AI_SQLCH = true
                        RI_CS = none
                else    AI_SQLCH = false
                        RI_CS = CI_CS
                fi
else    if (CI_SSF == true) or (CI_QL < MI_QLminimum)
                then    AI_SQLCH = true
                        RI_CS = none
                else    AI_SQLCH = false
                        RI_CS = CI_CS
                fi
fi
```

Defect correlations: None.

Performance monitoring: None.

7.7.2 T12 to SD adaptation sink (T12/SD_A_Sk)

Symbol:

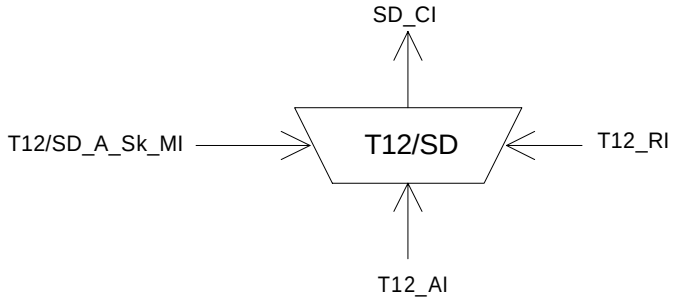

Figure 40: T12/SD_A_Sk symbol

Interfaces:

Table 38: T12/SD_A_Sk input and output signals

Input(s)	Output(s)
T12_AI_CK	SD_CI_CK
T12_AI_TSF	SD_CI_SSF
T12_RI_CS	SD_CI_CS
T12_RI_QL	SD_CI_QL
T12/SD_A_Sk_MI_CSid	

Processes:

This function adapts the 2048 kHz timing information from an external reference to an equipment specific timing characteristic information. This function regenerates the received clock signal and supplies the recovered timing signal to the synchronization distribution layer.

Regeneration: The function shall operate without any errors (shall output a valid clock signal) when any combination of the following signal conditions exist at the input:

- An input electrical amplitude level with any value in the range specified by ETS 300 166 [3];
- Jitter modulation applied to the input signal with any value defined in ETS 300 462-5 [12];
- The input signal frequency has any value in the range 2 048 kHz ± 50 ppm.

SSM support: CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall process the clock source identifier received via RI_CS to support timing loop prevention (see subclause 4.13). The function shall determine the value of the CI_CS output signal as follows:

```
if (RI_CS == none)
then   CI_CS = MI_CSid
else   CI_CS = RI_CS
fi
```

NOTE: The frequency and jitter/wander tolerance is further constrained by the requirements of the client (SD) layer.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect correlations: None

Performance monitoring: None.

8 Equipment clock to transport layers clock adaptation functions

8.1 STM-N layer

8.1.1 STM-1 layer clock adaptation source (MS1-LC_A_So)

Symbol:

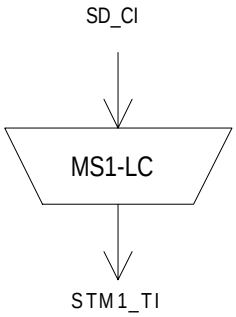

Figure 41: MS1-LC_A_So symbol

Interfaces:

Table 39: MS1-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS_TI_CK MS1_TI_FS

Processes:

This function performs the STM-1 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM1_TI_CK for the STM-1 signal. The STM1_TI_CK frequency shall be 155 520 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-1 output interface as measured over a 60 s interval shall not exceed:

- 0,5 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 500 Hz and 1,3 MHz;

- 0,1 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 65 kHz and 1,3 MHz.

Frame Start signal generation: The function shall generate the frame start reference signal STM1_TI_FS for the STM-1 signal. The STM1_TI_FS signal shall be active once per 19 440 clock cycle.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.1.2 STM-4 layer clock adaptation source (MS4-LC_A_So)

Symbol:

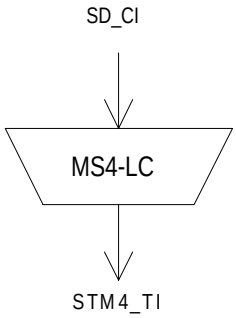

Figure 42: MS4-LC_A_So symbol

Interfaces:

Table 40: MS4-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS4_TI_CK MS4_TI_FS

Processes:

This function performs the STM-4 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM1_TI_CK for the STM-4 signal. The STM4_TI_CK frequency shall be 622 080 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-4 output interface as measured over a 60 s interval shall not exceed:

- 0,5 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 1 000 Hz and 5 MHz;

- 0,1 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 250 kHz and 5 MHz.

Frame Start signal generation: The function shall generate the frame start reference signal STM4_TI_FS for the STM-4 signal. The STM4_TI_FS signal shall be active once per 77 760 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.1.3 STM-16 layer clock adaptation source (MS16-LC_A_So)

Symbol:

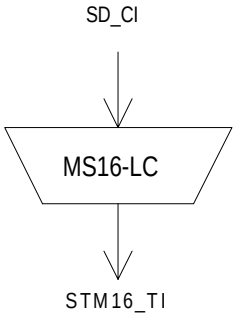

Figure 43: MS16-LC_A_So symbol

Interfaces:

Table 41: MS16-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS16_TI_CK MS16_TI_FS

Processes:

This function performs the STM-16 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM16_TI_CK for the STM-16 signal. The STM16_TI_CK frequency shall be 2 488 320 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-16 output interface as measured over a 60 s interval shall not exceed:

- 0,5 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 5 000 Hz and 20 MHz;

- 0,1 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 1 MHz and 20 MHz.

Frame Start signal generation: The function shall generate the frame start reference signal STM16_TI_FS for the STM-16 signal. The STM16_TI_FS signal shall be active once per 311 040 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2 VC layers

8.2.1 VC-4 layer clock adaptation source (S4-LC_A_So)

Symbol:

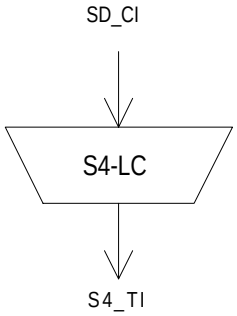

Figure 44: S4-LC_A_So symbol

Interfaces:

Table 42: S4-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S4_TI_CK S4_TI_FS S4_TI_MFS

Processes:

This function performs the VC-4 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S4_TI_CK for the VC-4 signal. The S4_TI_CK frequency shall be 150 336 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For Further study

Frame Start signal generation: The function shall generate the frame start reference signal S4_TI_FS for the VC-4 signal. The S4_TI_FS signal shall be active once per 18 792 clock cycle and the multiframe reference shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2.2 VC-3 layer clock adaptation source (S3-LC_A_So)

Symbol:

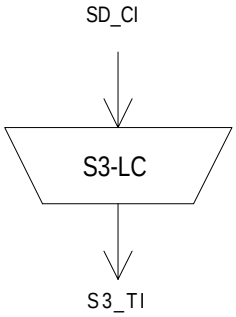

Figure 45: S3-LC_A_So symbol

Interfaces:

Table 43: S3-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S3_TI_CK S3_TI_FS S3_TI_MFS

Processes:

This function performs the VC-3 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S3_TI_CK for the VC-3 signal. The S3_TI_CK frequency shall be 48 960 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For Further study

Frame Start signal generation: The function shall generate the frame start reference signal S3_TI_FS for the VC-3 signal. The S3_TI_FS signal shall be active once per 6 120 clock cycle and the S3_TI_MFS once every four frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2.3 VC-2 layer clock adaptation source (S2-LC_A_So)

Symbol:

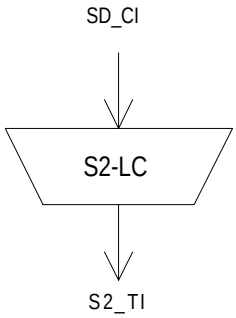

Figure 46: S2-LC_A_So symbol

Interfaces:

Table 44: S2-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S2_TI_CK S2_TI_FS

Processes:

This function performs the VC-2 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S2_TI_CK for the VC-2 signal. The S2_TI_CK frequency shall be 6 848 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the frame start reference signal S2_TI_FS for the VC-2 signal. The S2_TI_FS signal shall be active once per 856 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2.4 VC-12 layer clock adaptation source (S12-LC_A_So)

Symbol:

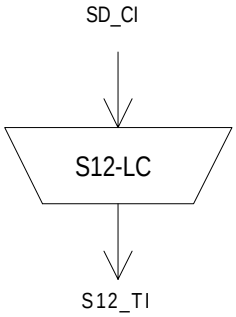

Figure 47: S12-LC_A_So symbol

Interfaces:

Table 45: S12-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S12_TI_CK S12_TI_FS

Processes:

This function performs the VC-12 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S12_TI_CK for the VC-12 signal. The S12_TI_CK frequency shall be 2 240 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the frame start reference signal S12_TI_FS for the VC-12 signal. The S12_TI_FS signal shall be active once per 280 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2.5 VC-11 layer clock adaptation source (S11-LC_A_So)

Symbol:

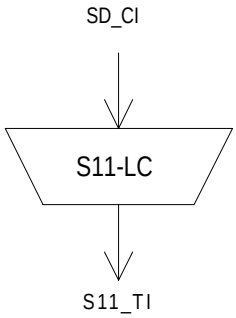

Figure 48: S3-LC_A_So symbol

Interfaces:

Table 46: S3-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S11_TI_CK S11_TI_FS

Processes:

This function performs the VC-11 clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S11_TI_CK for the VC-11 signal. The S11_TI_CK frequency shall be 1 664 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the frame start reference signal S11_TI_FS for the VC-11 signal. The S11_TI_FS signal shall be active once per 208 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.3 Pxx layers

8.3.1 P4s layer clock adaptation source (P4s-LC_A_So)

Symbol:

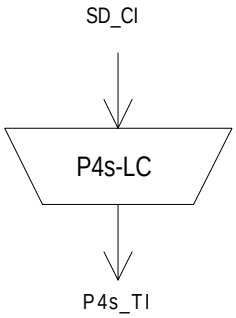

Figure 49: P4s-LC_A_So symbol

Interfaces:

Table 47: P4s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P4s_TI_CK P4s_TI_FS P4s_TI_MFS

Processes:

This function performs the P4s clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P4s_TI_CK for the P4s signal. The P4s_TI_CK frequency shall be 139 264 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the frame start reference signal P4s_TI_FS for the P4s signal. The P4s_TI_FS signal shall be active once per 17 408 clock cycles.P4s_TI_MFS shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.3.2 P31s layer clock adaptation source (P31s-LC_A_So)

Symbol:

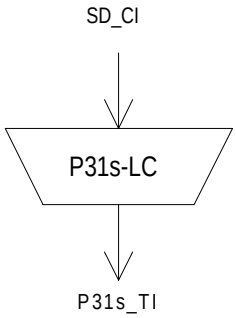

Figure 50: P31s-LC_A_So symbol

Interfaces:

Table 48: P31s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P31s_TI_CK P31s_TI_FS P31s_TI_MFS

Processes:

This function performs the P31s clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P31s_TI_CK for the P31s signal. The P31s_TI_CK frequency shall be 34 368 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the frame start reference signal P31s_TI_FS for the P31s signal. The P31s_TI_FS signal shall be active once per 4 296 clock cycles and P31s_TI_MFS once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.3.3 P12s layer clock adaptation source (P12s-LC_A_So)

Symbol:

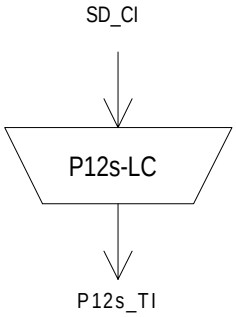

Figure 51: P12s-LC_A_So symbol

Interfaces:

Table 49: P12s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P12s_TI_CK P12s_TI_FS P12s_TI_MFS

Processes:

This function performs the P12s clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P12s_TI_CK for the P12s signal. The P12s_TI_CK frequency shall be 2 048 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence input jitter at the synchronization interface, the intrinsic jitter at the E12 output interface as measured over a 60 s interval shall not exceed 0,05 UI peak-peak when measured through a band-pass filter with corner frequencies at 20 Hz and 100 kHz each with a first order 20 dB/decade roll-off characteristic.

Frame Start signal generation: The function shall generate the frame start reference signal P12s_TI_FS for the P12s signal. The P12s_TI_FS signal shall be active once per 256 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.4 T12 layer

8.4.1 T12 layer clock adaptation source (T12-LC_A_So)

Symbol:

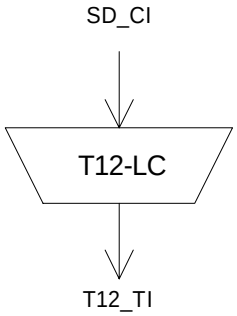

Figure 52: T12-LC_A_So symbol

Interfaces:

Table 50: T12-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	T12_TI_CK

Processes:

This function performs the T12 clock signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions T12/SD_A_So.

Clock generation: The function shall generate the clock reference signal T12_TI_CK for the 2 048 kHz signal. The T12_TI_CK frequency shall be 2 048 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the 2 048 kHz output interface as measured over a 60 s interval shall not exceed 0,05 UI peak-peak when measured through a band-pass filter with corner frequencies at 20 Hz and 100 kHz each with a first order 20 dB/decade roll-off characteristic.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

Annex A (normative): Synchronization selection process

This annex specifies the detailed operation of the automatic synchronization reference selection process located in the NS_C function. Refer to clause 4 for an introduction to this process.

A selection process needs the quality level (NS_CI_QL) and signal fail (NS_CI_SSF) information from each input (i.e. each SD_TT_Sk and SD/NS_A_Sk combination; the pair is henceforth called a "timing source") after it has passed through a holdoff/wait-to-restore process (HO/WtR).

Via the management interface it receives the priority (which includes disabling) of each timing source and its lock-out status. Switch requests (clear, manual, forced) and requests to change the mode of operation between QL-enabled and QL-disabled are also coming in through the management interface.

The output of the selection control process is the actually selected input ("select q") and its QL. The actually selected input is reported towards the management interface. In addition, rejection messages are sent towards the management interface. Figure A.1 shows the interfaces between the selection control process and its environment.

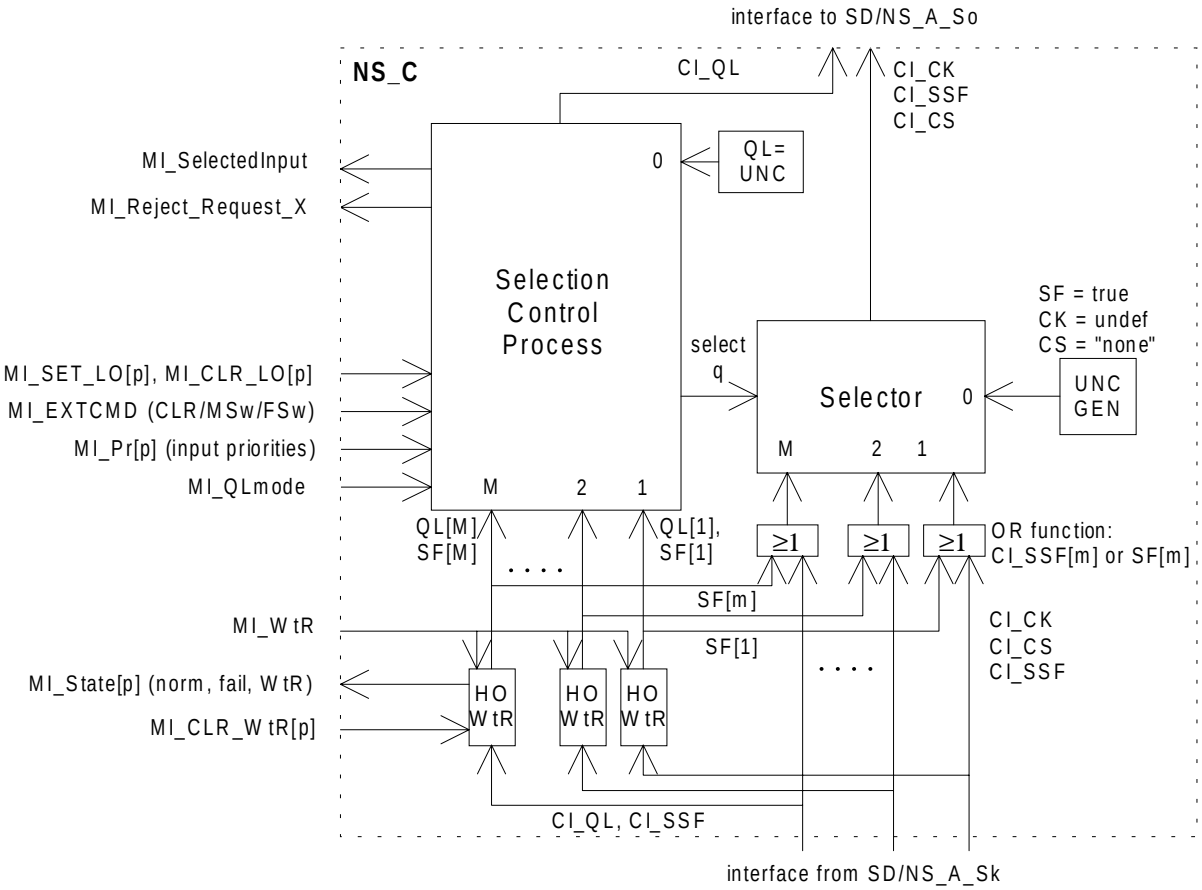

Figure A.1: Environment of selection control process

The selector supports M inputs (1 to M) and one output. In addition, the selector has a M+1th input, the null (0) input connected to an "unconnect" signal generator process.

Unconnect signal - A signal with CI_CK is undefined, CI_SSF is true and CI_CS is "none".

In the SDL diagrams that describe the selection process there are six states which correspond to the two modes of operation (QL-mode enabled (1) and QL-mode disabled (2)) and within each of these modes three "maintenance" states: no request active (A), manual switch active (B) and forced switch active (C). For each of these six states the reaction to all possible input variations are given.

Table A.1: Notational conventions and parameters used in the SDL diagrams

Parameter	**Abbreviation**	**Values (high to low)/Explanation**
Quality Level [input]	QL[p]	PRC, SSU-T, SSU-L, SEC, DNU, INV, FAILED, undef(ined)
Quality Level [0]	QL[0]	UNConnected
Priority [input]	Pr[p]	1, 2, ..., K, dis(abled)
Priority [0]	Pr[0]	undef(ined)
Signal Fail [input]	SF[p]	false, true
Signal Fail [0]	SF[0]	true
Lock Out status [input]	LO[p]	on, off
Lock Out status [0]	LO[0]	off
input	p	1, 2, ..., M
selected input	q	0,1, 2, ..., M
Number of timing sources	M	
Number of different priorities	K	K = M
	:=	assignment symbol
	==	equality test symbol
	<=	less or equal test symbol

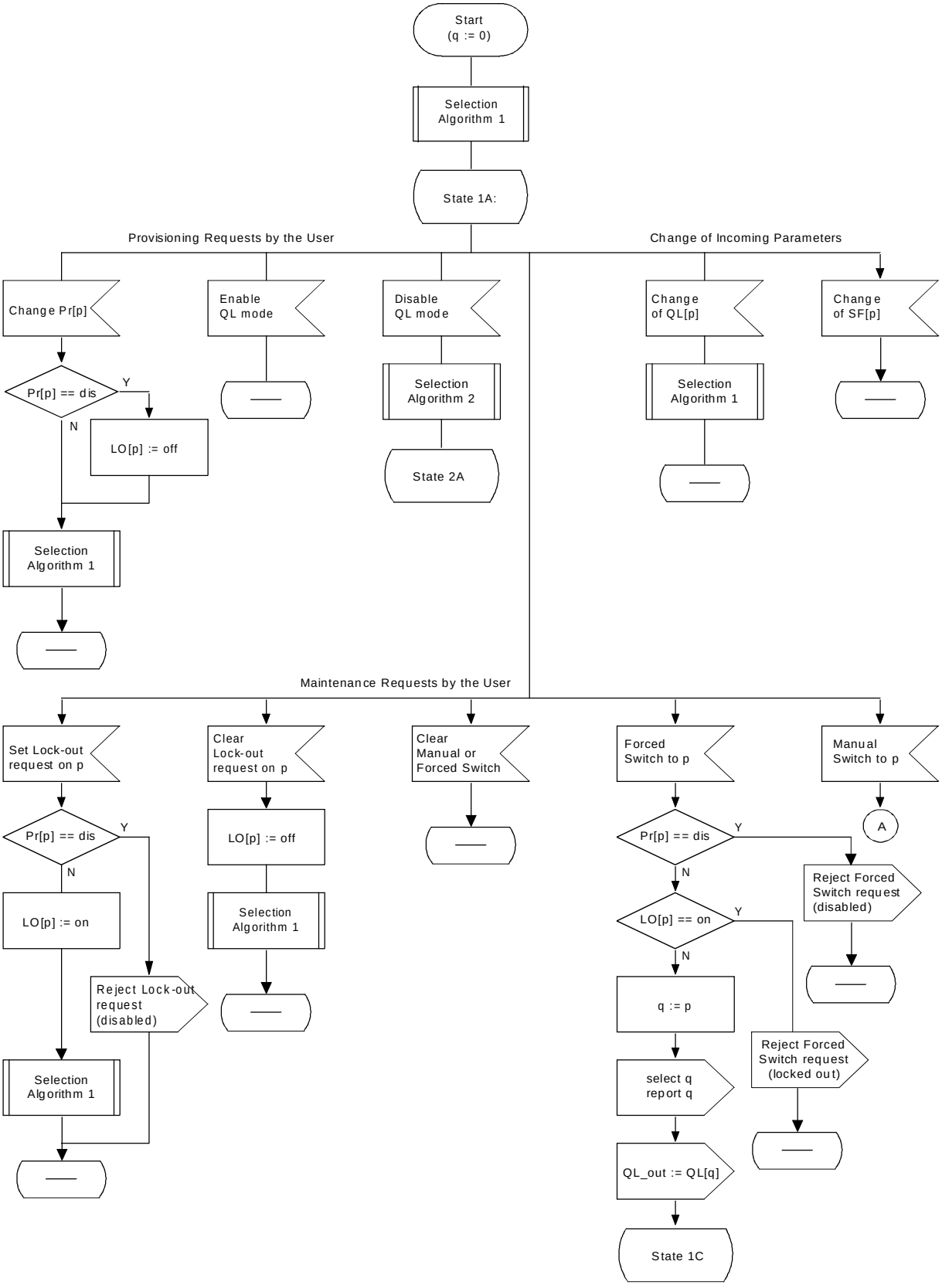

Figure A.2: QL enabled mode, no active switch request (state 1A)

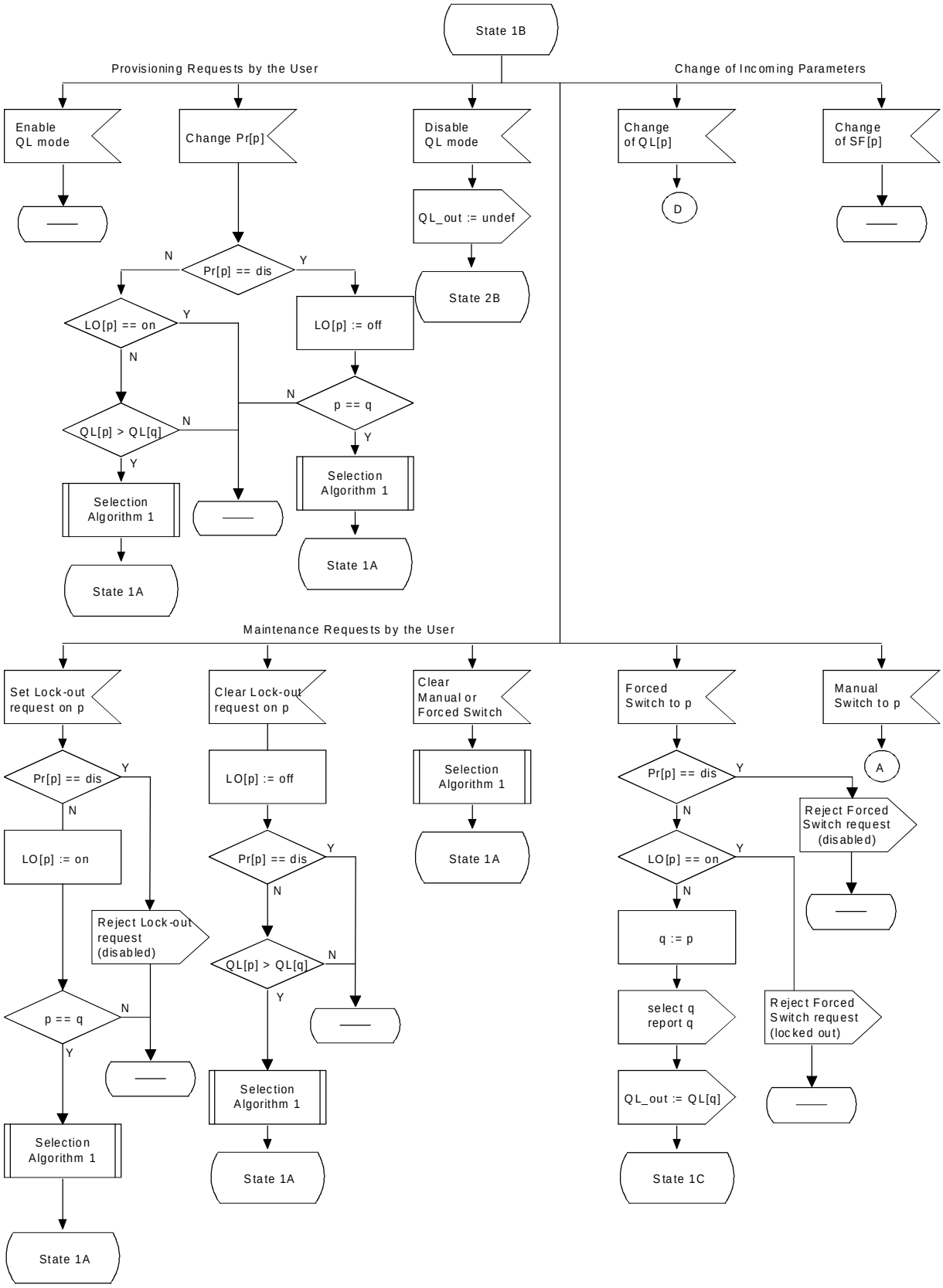

Figure A.3: QL enabled mode, active manual switch request (state 1B)

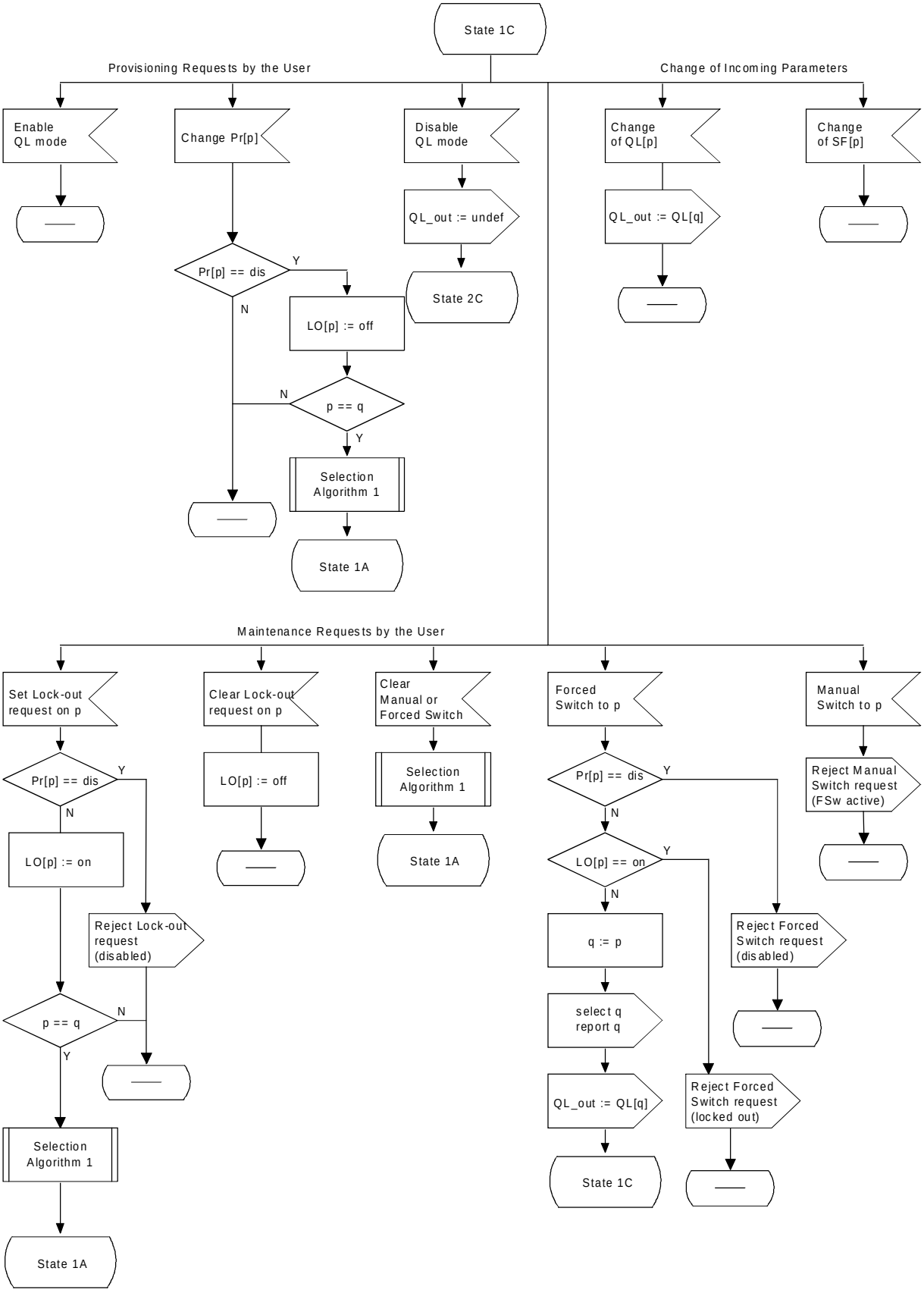

Figure A.4: QL mode enabled, active forced switch (state 1C)

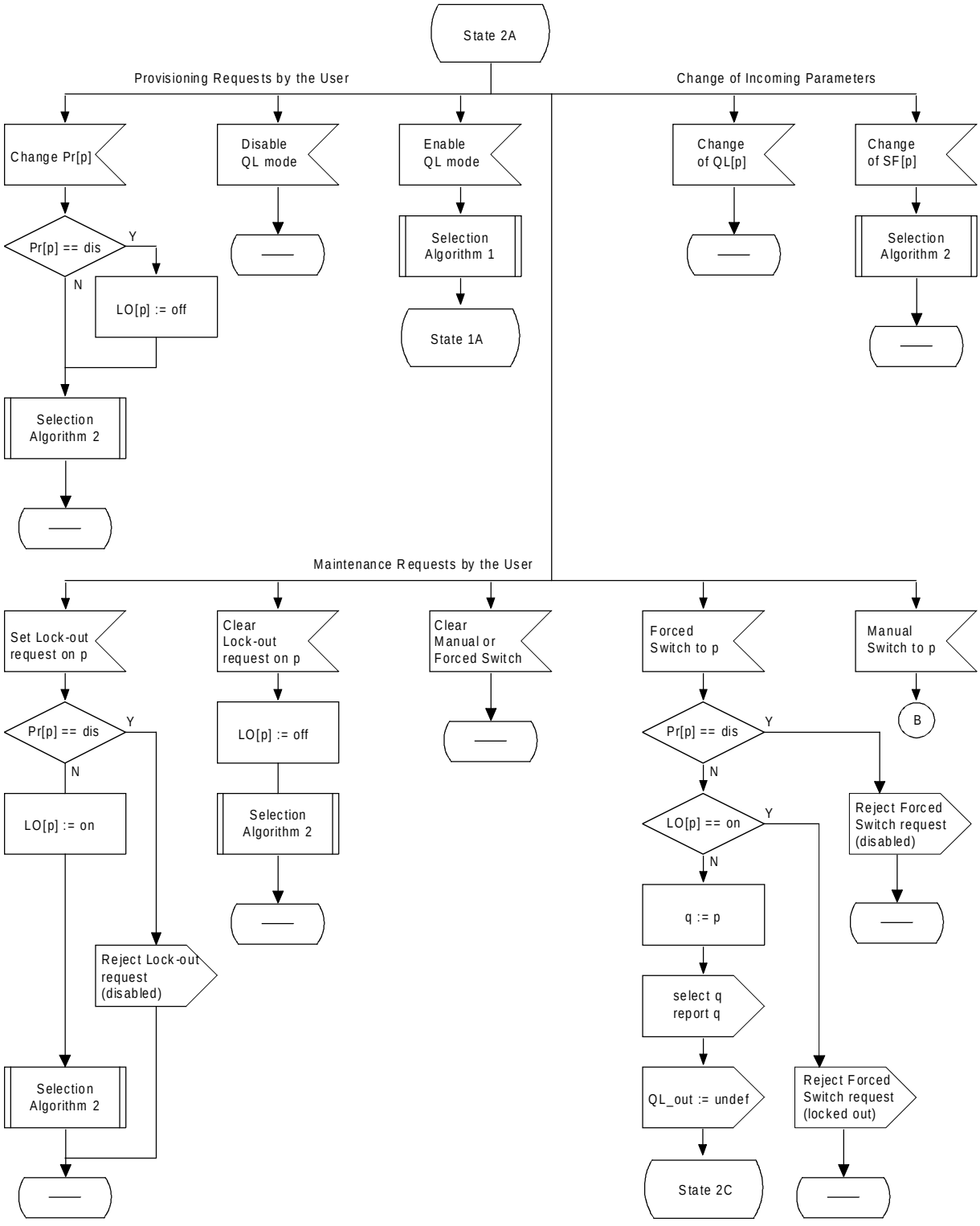

Figure A.5: QL mode disabled, no external switch request active (state 2A)

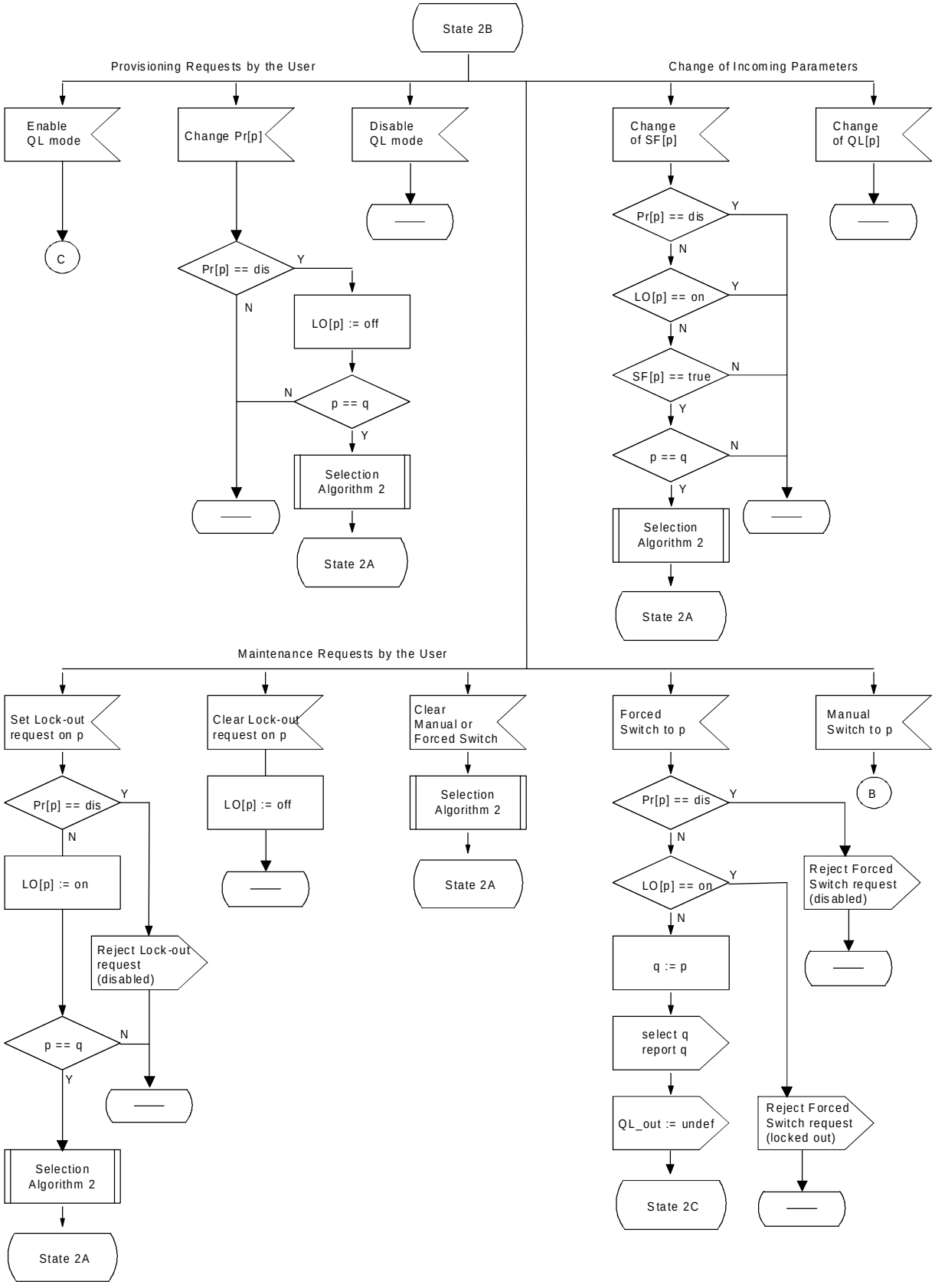

Figure A.6: QL mode disabled, active manual switch request (state 2B)

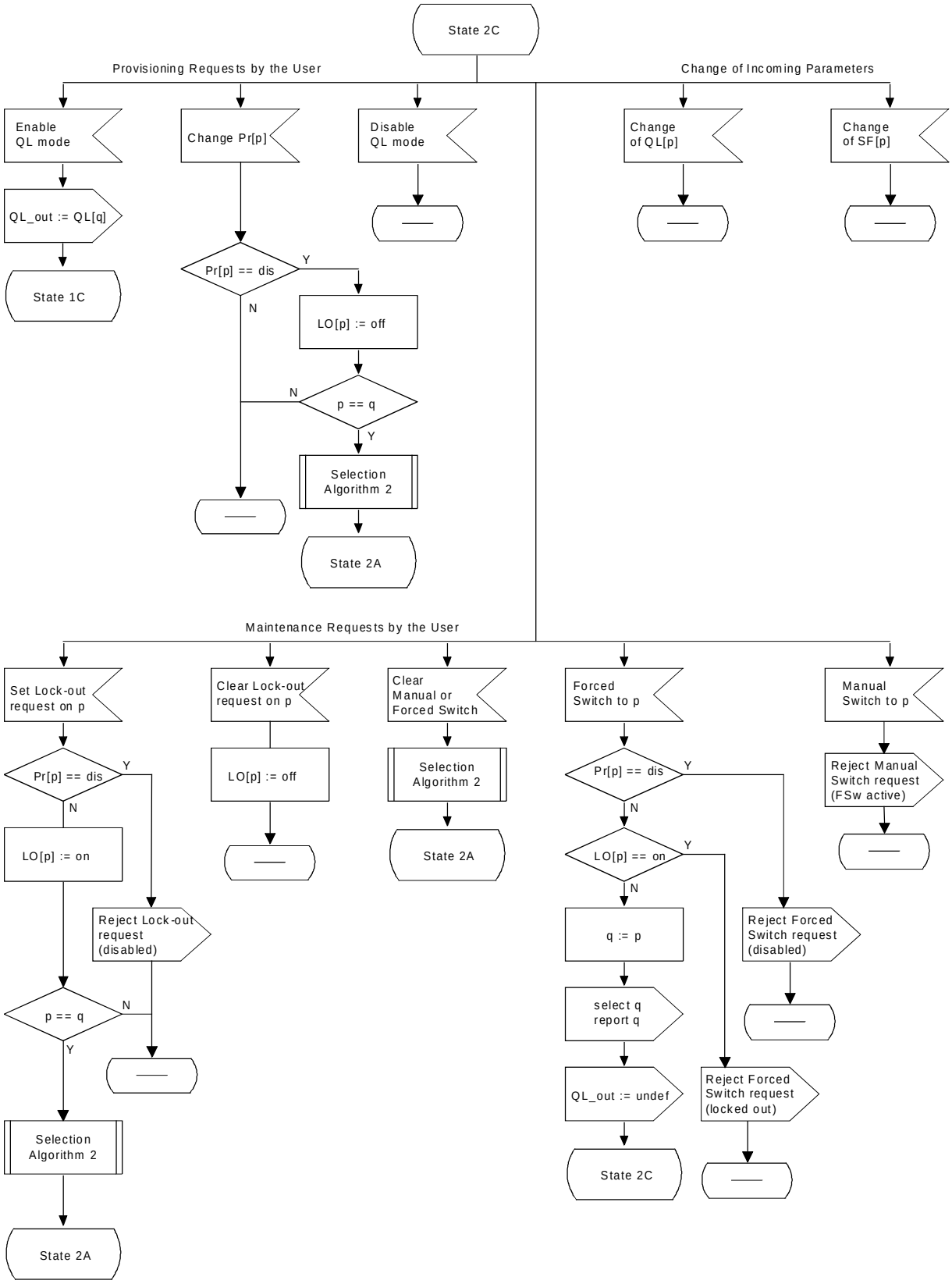

Figure A.7: QL mode disabled, active forced switch request (state 2C)

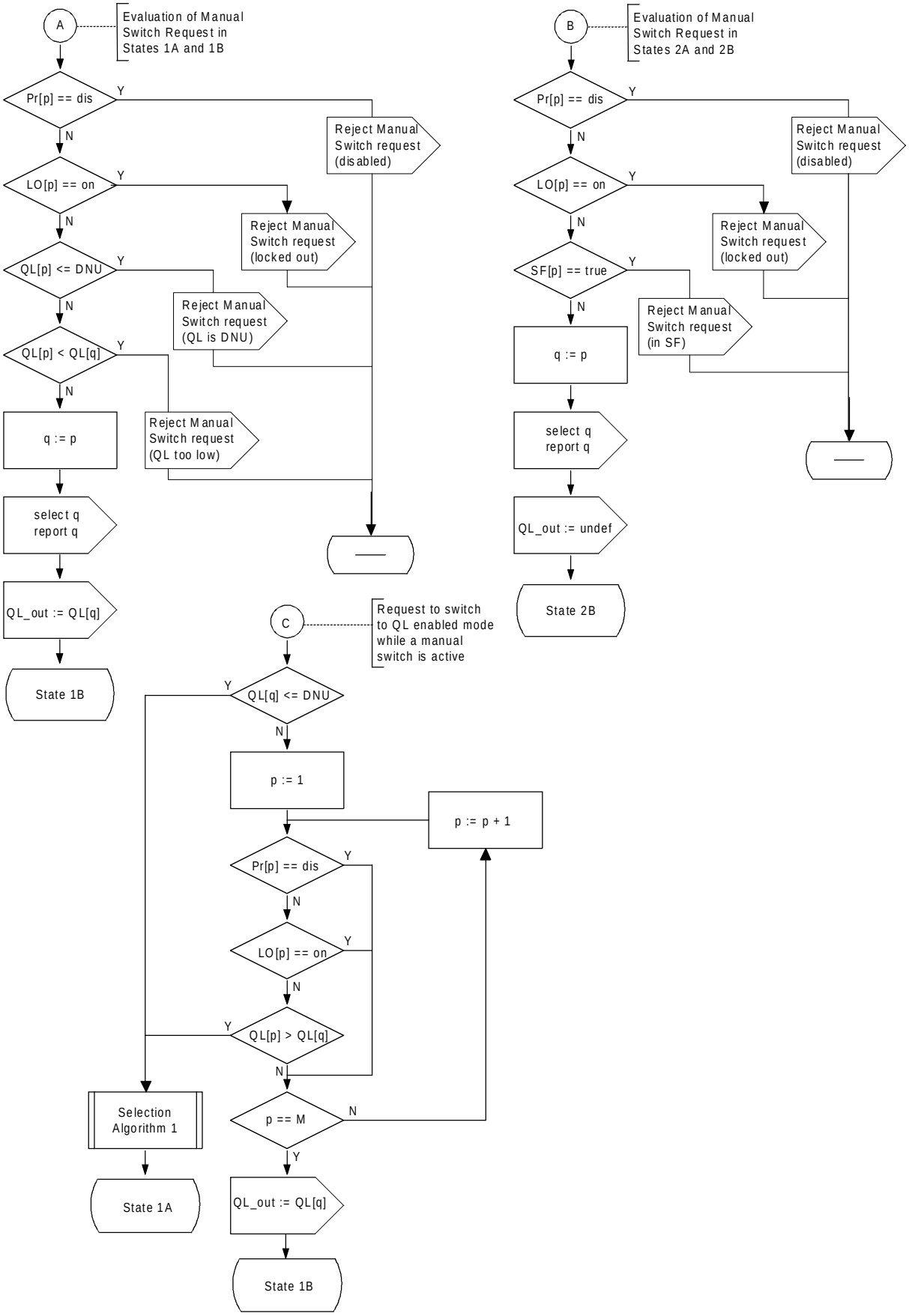

Figure A.8: Continuations of previous states

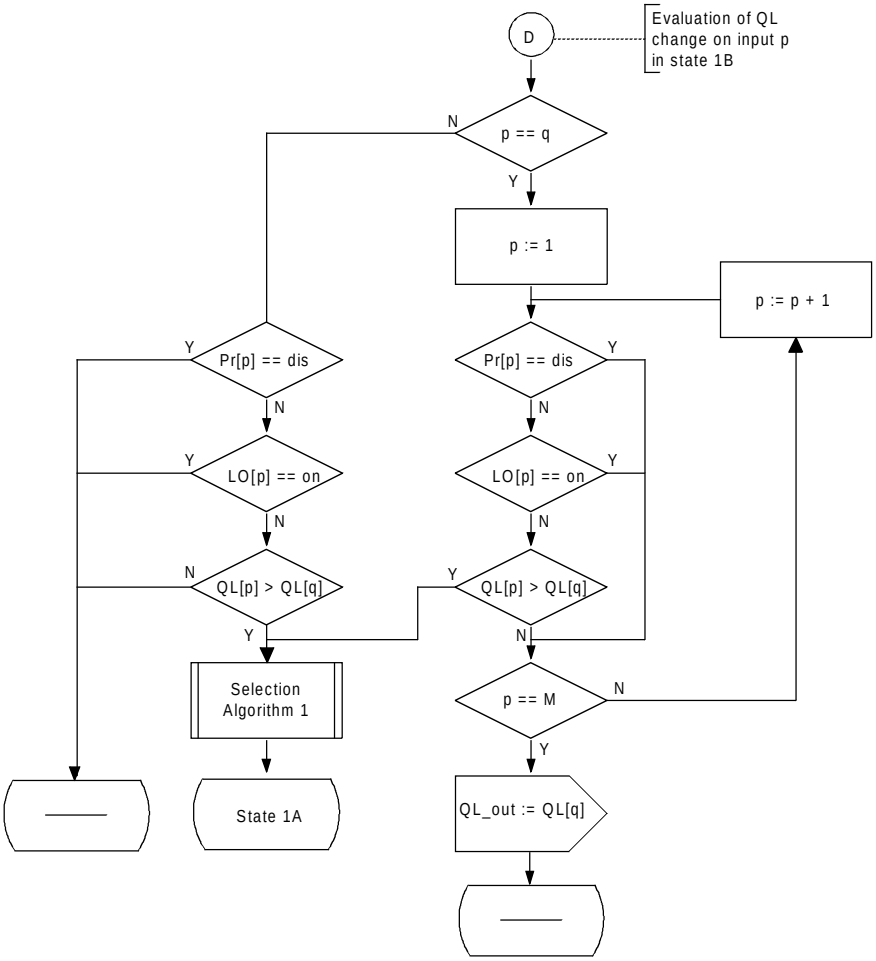

Figure A.9: Continuations of previous states

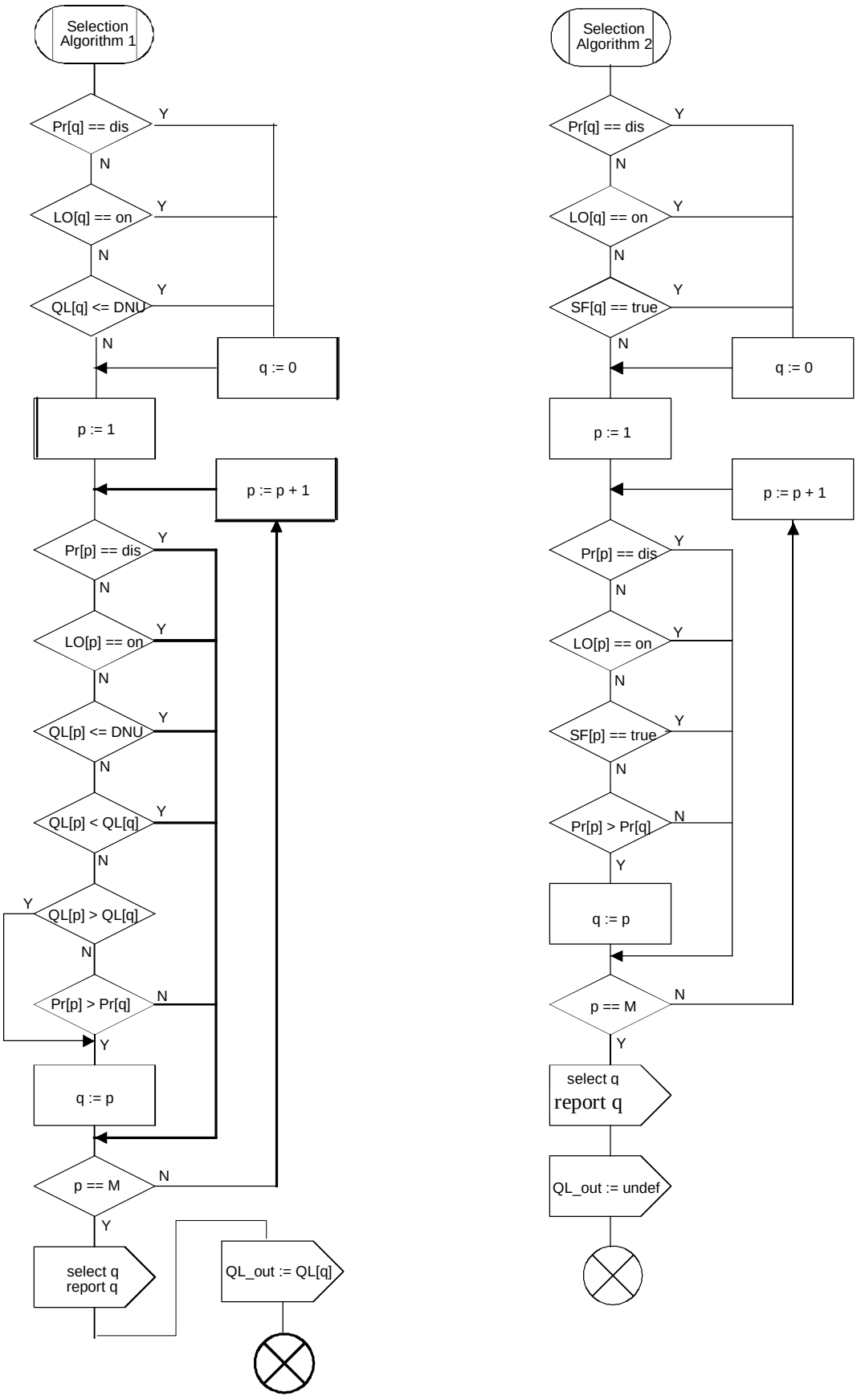

Figure A.10: Synchronization selection algorithms for QL mode enabled (1) and QL mode disabled (2)

Annex B (informative): Transport layer models for synchronization information

This annex shows the interfaces (sink and source) - between NNI and SD_CP - that are able to transport synchronization information using the atomic functions described in different parts of ETS 300 417.

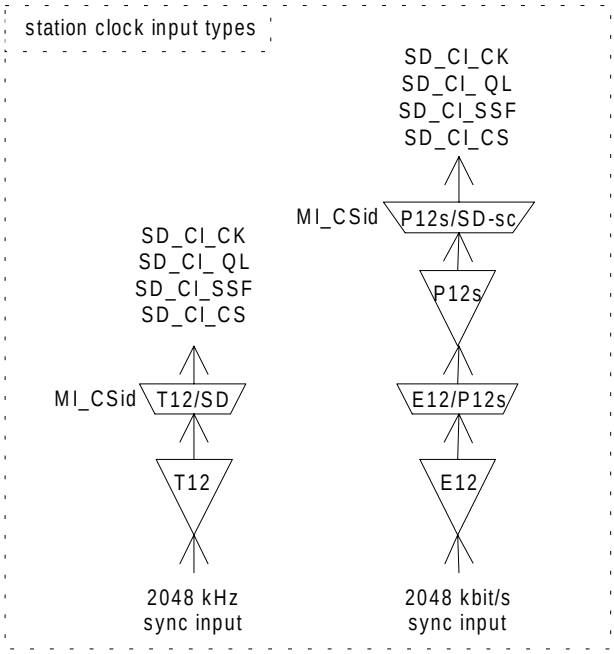

Figure B.1: Synchronization transport port models: station clock inputs

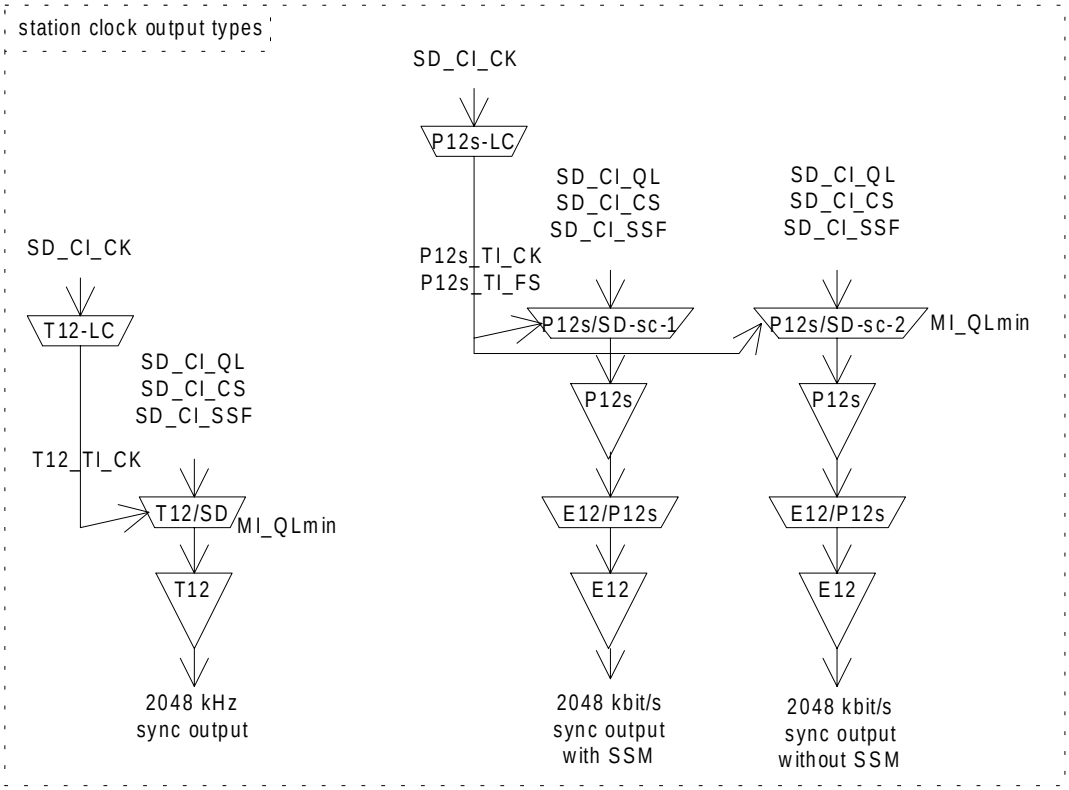

Figure B.2: Synchronization transport port models: station clock outputs

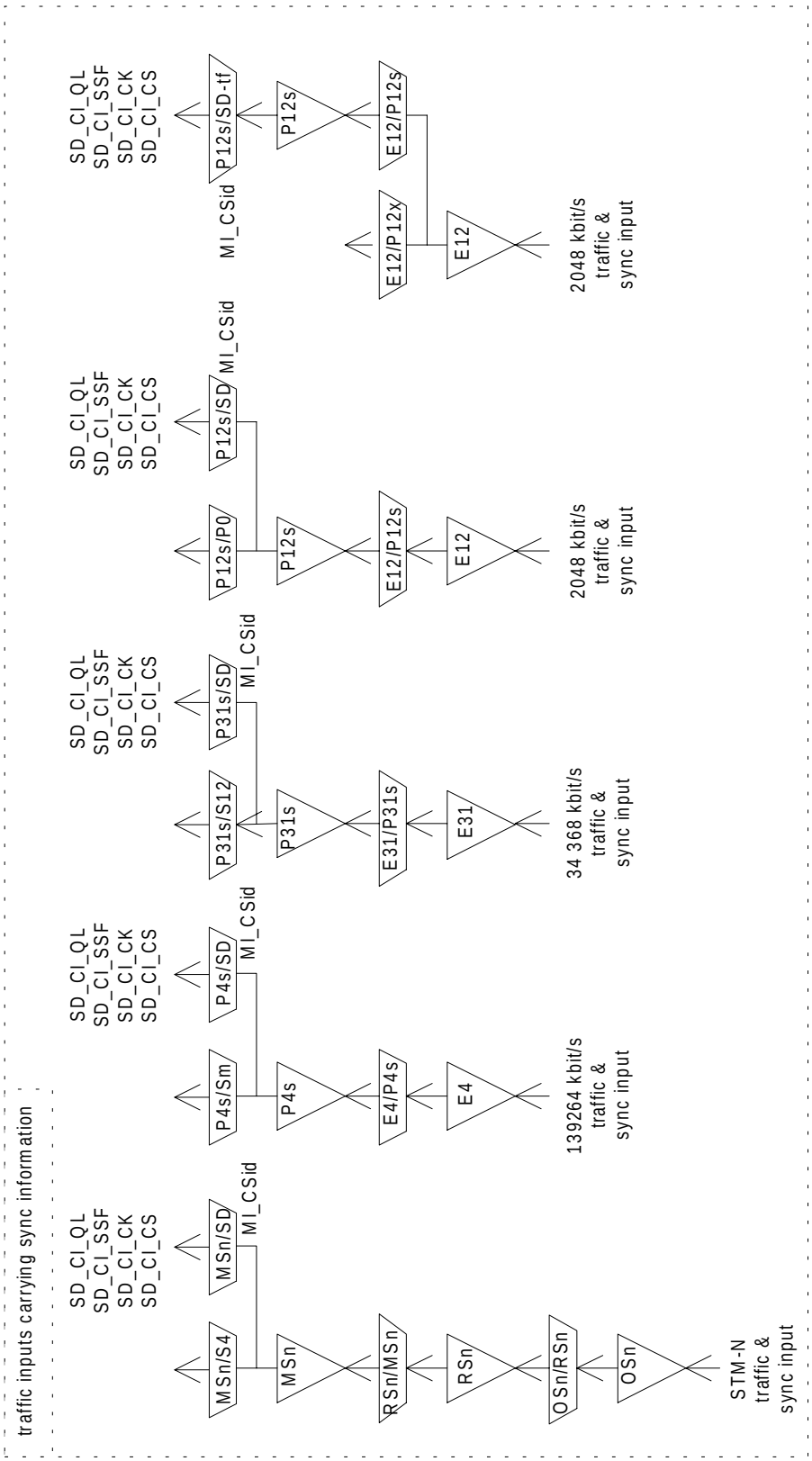

Figure B.3: Synchronization transport port models: traffic (line and tributary) inputs

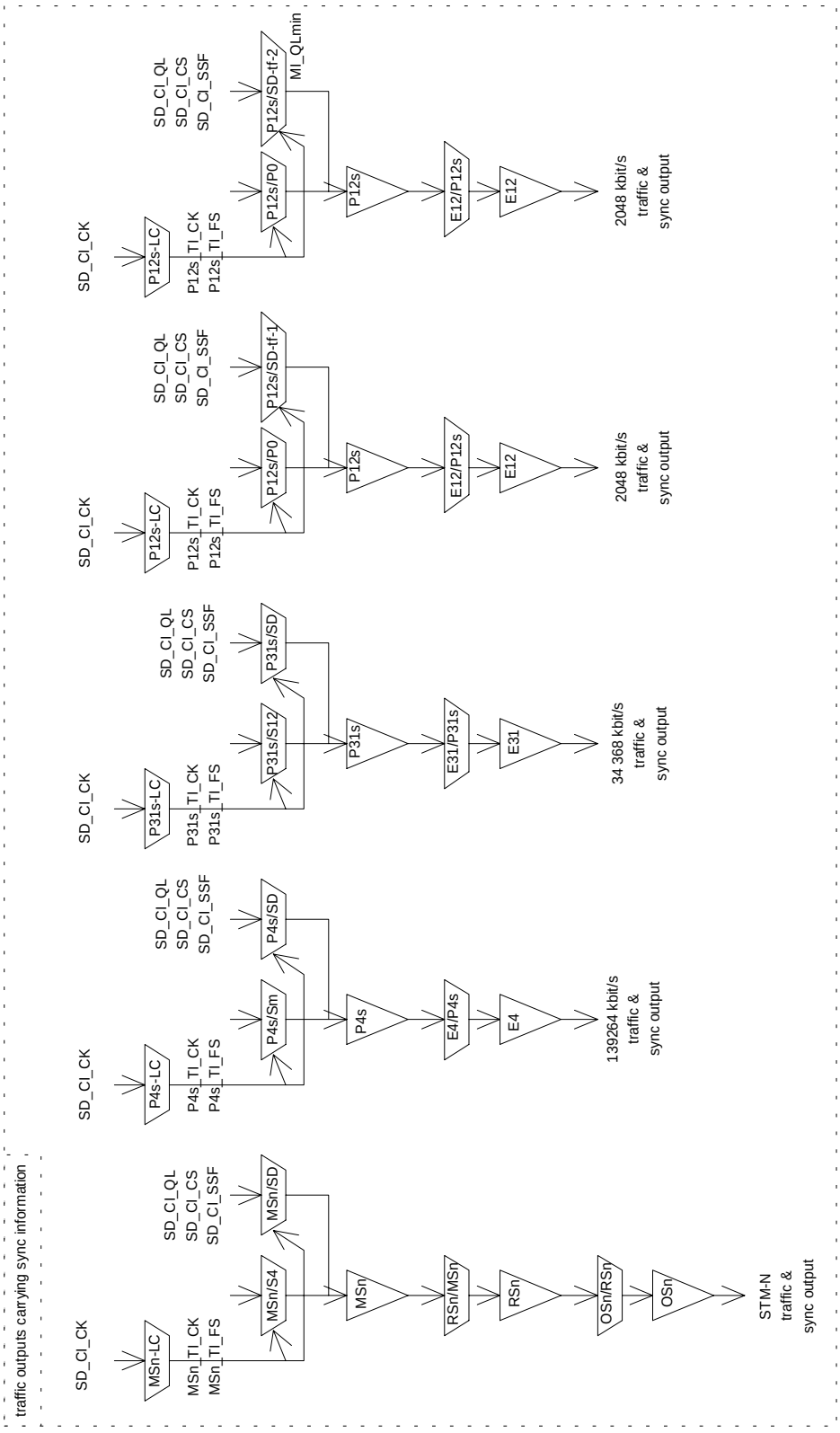

Figure B.4: Synchronization transport port models: traffic (line and tributary) outputs

Annex C (informative): Examples of network synchronization

C.1 Network synchronization structures using SSM

In traditional preselected alternative master slave network synchronization, such as that a slave clock never is slaved to a clock of lower quality than itself.

With the invention of SDH this is no longer always possible.

C.1.1 Vertical link application

A situation as in figure C.1 may arise. Between a PRC and an SSU there are a number of SECs. If the link between the SECs or PRC fails the SSU will receive SEC quality timing. In this case the SSU should have some means other than transmission failures (LOS/AIS) to block the reference from contributing to the timing of the SSU.

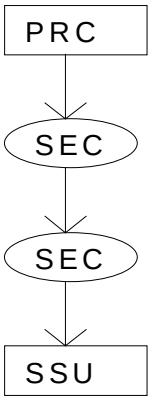

Figure C.1: Vertical distribution

The means in this case is that the quality of the link is less than that of the node itself and the link should not be used for synchronization of the SSU.

C.1.2 Horizontal link application

A situation as in figure C.2 may arise. Two SSUs are synchronized from a PRC. Between the SSUs there is a link with SECs (the existence of SECs on that link is not necessary, only a possibility). SSM may in this case be used on the link with SECs to give both the SSUs a backup connection with the PRC. If the link towards the PRC fails the SEC link will convey the PRC clock to that SSU. It is expected that generation of DNU code by the SSU could prevent timing loop.

NOTE: Care should be taken to the fact that this application of SSM algorithm is still for further study.

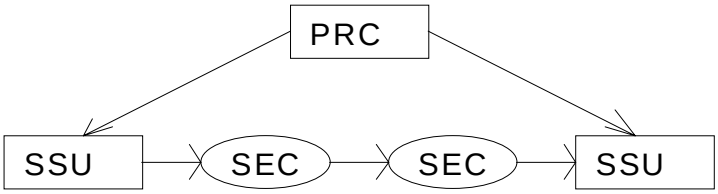

Figure C.2: Horizontal distribution

C.2 Application of SSM in a ring or bus

C.2.1 Introduction

The SSM algorithm is based on a linear structure of maximum 20 connected NEs. Each NE receive timing from two directions. The two NEs at the ends receives timing from the outside environment.

The quality of the NE internal timing is less than that of the timing reference at the ends.

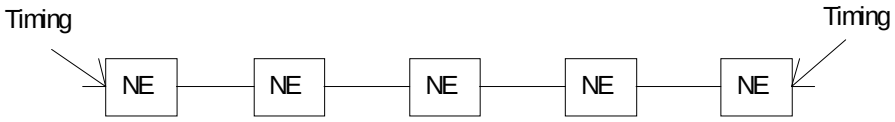

Figure C.3: Linear distribution

The selection algorithm has the capability to produce a synchronization without timing loops in this structure. If the quality of one of the timing at one end is better that the other the whole line is synchronized to that timing reference. If the two timing references at the ends has the same quality, the priority table in the NEs will decide where the border will be between those NEs timed to the left and those timed to the right timing reference. The algorithm will prevent isolated groups of NEs not timed the timing reference regardless of the priority table.

C.2.2 Applications

The SSM algorithm can be used to form to basic topological structures to be used in a network:

- The ring;
- The bus.

Ring application

The ring is obtained by bringing the two ends of the linear structure together and input the same signal with the same quality in both ends.

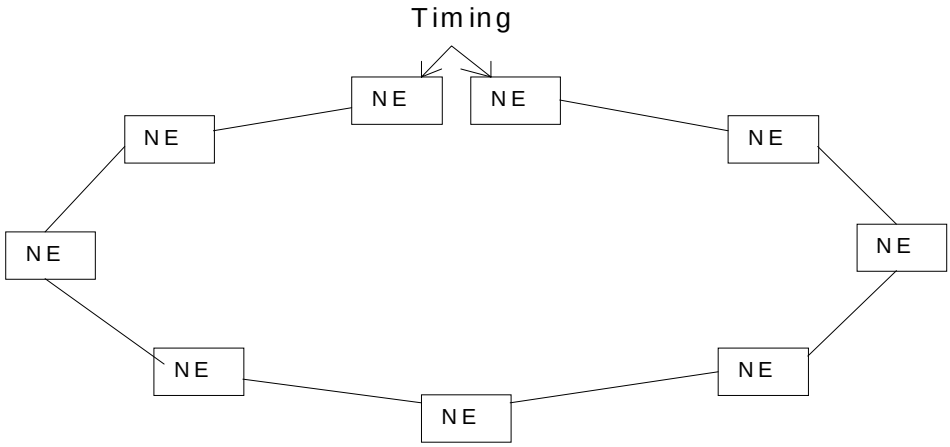

Figure C.4: Linear distribution

Bus application

The bus is obtained by using the linear structure as a link between two nodes. The input signal may then have different quality in the two ends.

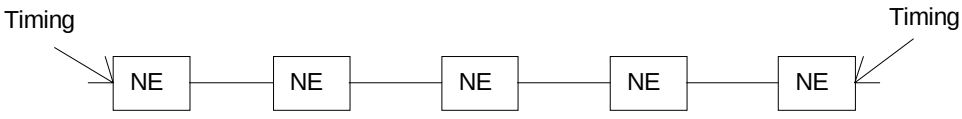

Figure C.5: Linear distribution

Annex D (informative): Examples of synchronization functionality in the NE

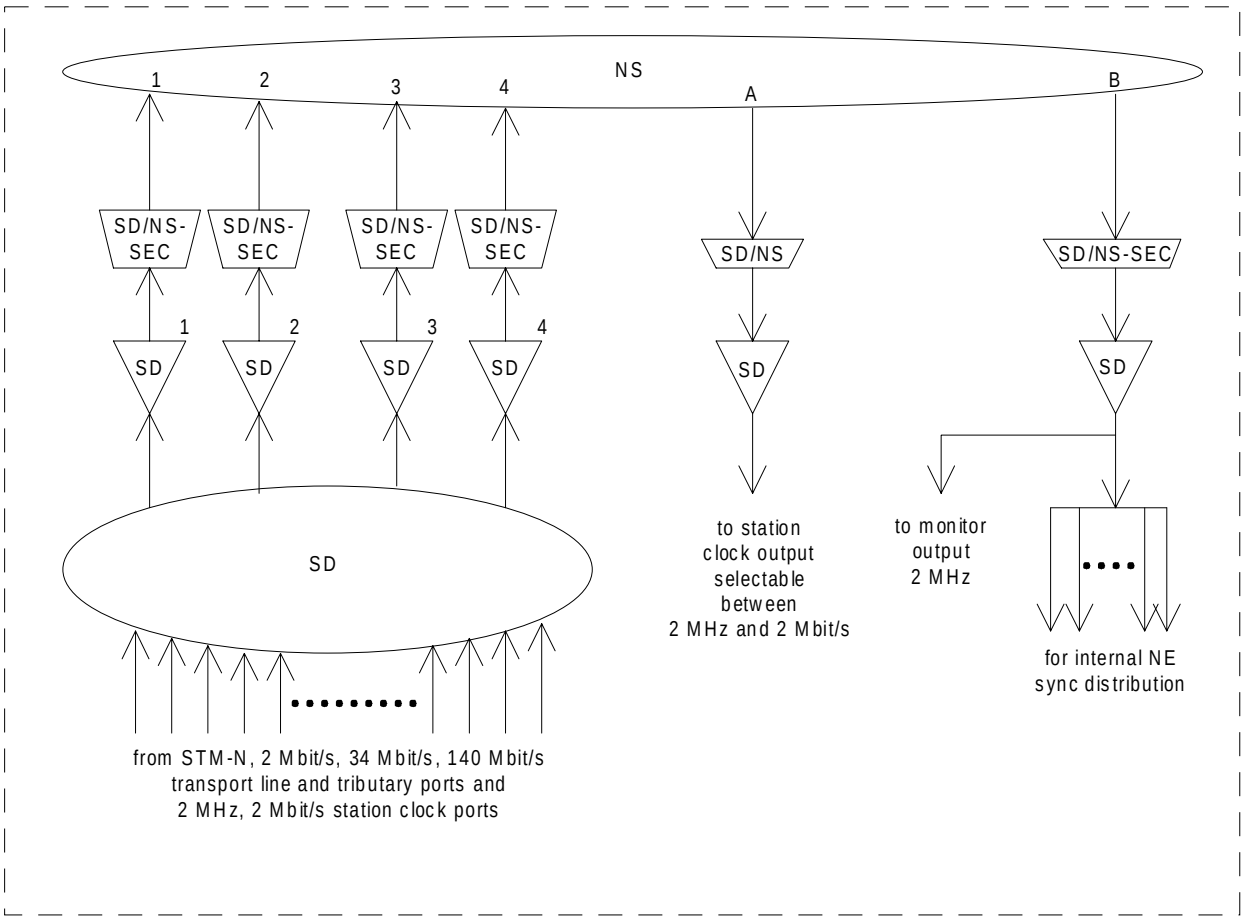

Figure D.1: Example 1 of a Network Element's synchronization distribution layer functional model

Figure D.1 presents an example of the SD layer functionality within a network element providing SEC quality timing. The NE in the example offers four timing ports that can be connected to the transport ports carrying synchronization information, selected from the set of line and tributary transport ports and/or station clock ports within the NE.

Output B of NS_C function may use all four input signals to select the best synchronization reference input signal. Output A should exclude input signals derived from station clock ports. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

NOTE 1: The correct provisioning is a responsibility of the user of the equipment.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criterion it is used as reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the network element. In addition, it is output also via station clock output dedicated for monitoring the internal clock signal.

The signal at output A of NS_C is connected to the station clock output.

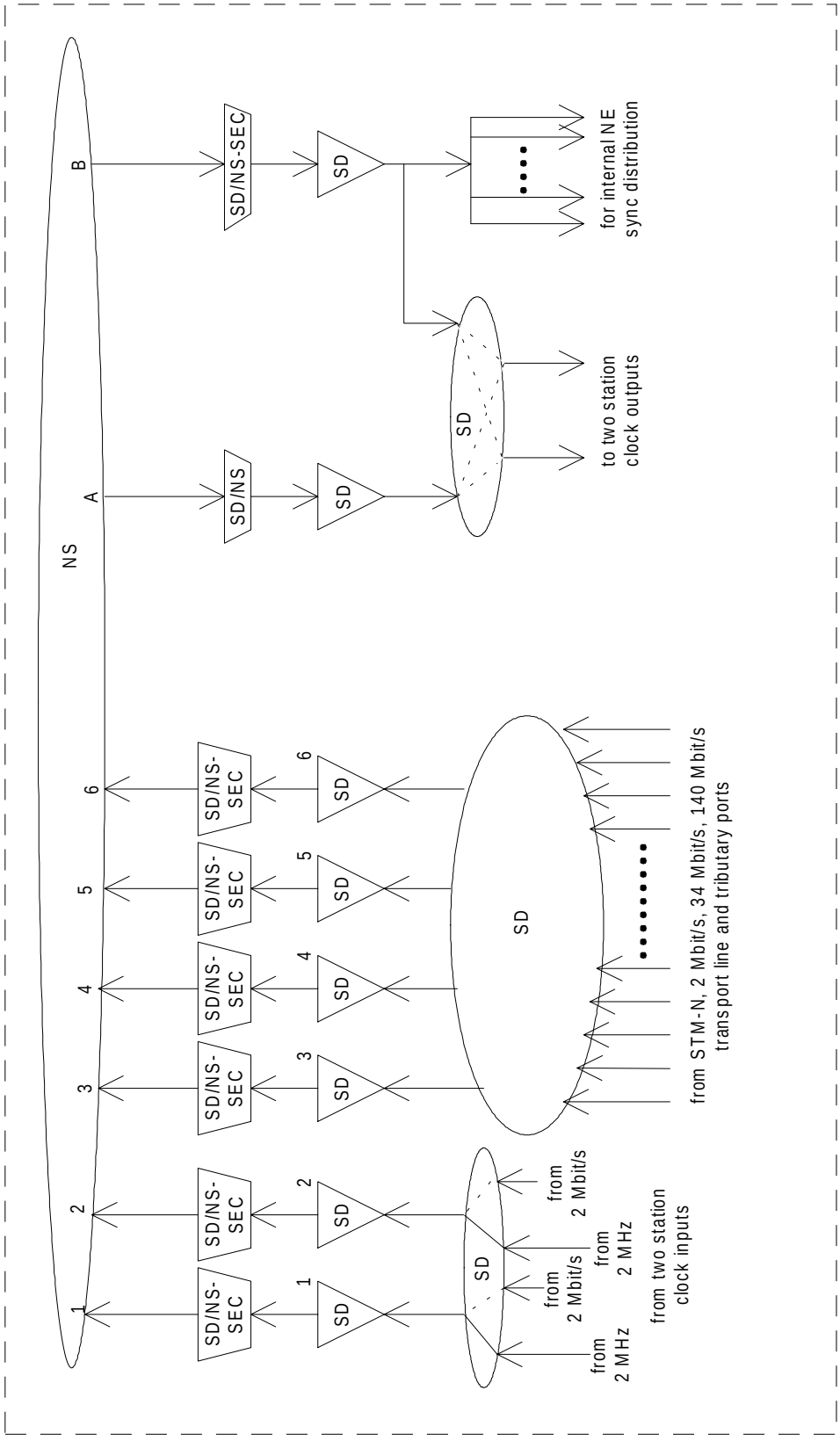

Figure D.2: Example 2 of a Network Element's synchronization distribution layer functional model

Figure D.2 presents a second example of the SD layer functionality within a network element providing SEC quality timing. The NE in the example offers two station clock timing ports each of them being either of the type 2 MHz or 2 Mbit/s. These station clock based synchronization reference input signals can be connected both to a timing port (SD_TT_Sk #1, #2).

The NE offers furthermore four timing ports that can be connected to a number of transport ports carrying synchronization information, selected from the set of line and tributary transport ports within the NE. Signals from timing ports within the range #3 to #6 that are not connected to a transport port will be disconnected in the NS_C function.

Output B of NS_C function may use all six input signals to select the best synchronization reference input signal. Output A should exclude input signals #1 and #2. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criterion it is used as reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the network element. As an option it can be output also via one or both station clock outputs. The latter to support monitoring of the internal clock signal, or to provide a synchronization signal to e.g. a small synchronous network element that is the last in the chain.

The signal at output A of NS_C is connected to the station clock output selector (SD_C). Depending on the application in the network, station clock outputs #1 and #2 can operate as a protection pair both sourced by the same input of SD_C, or as two independent outputs sourced by the same or different input signals (as appropriate for the application).

NOTE 2: Figure D.2 presents two instances of SD_C functions (the first connected to SD_TT_Sk functions #1 and #2 and the second connected to SD_TT_Sk functions #3 to #6) to reflect explicitly the supported connectivity in the network element. The station clock input signals can be connect to timing ports 1, and 2 and not to timing ports 3 to 6. Similarly, the line and tributary input signals can be connected to timing ports 3 to 6, and not to timing ports 1 and 2.

Annex E (informative): Delay time allocation

E.1 Delay and processing times for the synchronization selection process

The following delay and processing times are defined for a SEC using the QL enabled mode for the reference selection process. They are based on a ring configuration with 20 NEs. Delay and processing times for other applications (e.g. SSU) are for further study.

Three delay time values are defined for the synchronization selection process of the SEC. These are the non-switching message delay T_{NSM} , the switching message delay T_{SM} and the holdover message delay T_{HM}. These times are measurable at the interfaces of the NE.

These delay times are caused by internal delay and processing times of the synchronization distribution atomic functions. The hold off time t_h and processing time t_p are part of the reference selection process of the NS_C function. The settling time t_s is part of the SD/NS-SEC_A_So function. For a detailed description see clause 5.

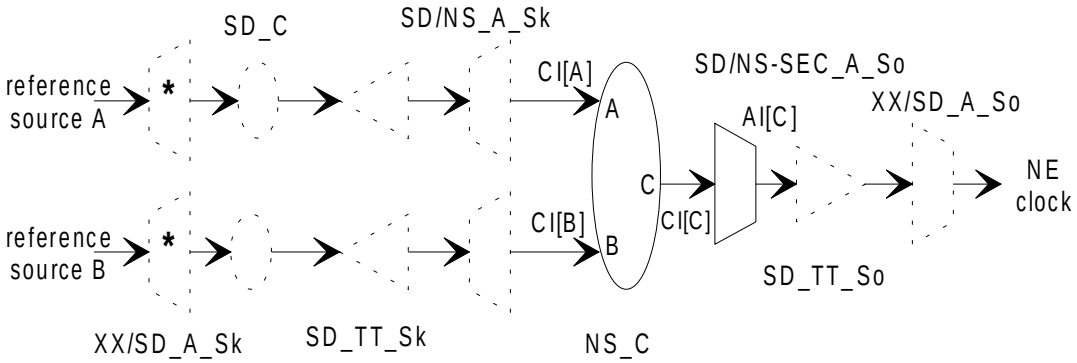

Figure E.1: Example configuration for clock selection

The timing diagrams in the following description are based on a configuration with two clock reference sources as shown in the figure E.1.

The dotted functions in the figure do not contribute to delay and processing times. The persistence check for SSM acceptance in the XX/SD_A_Sk functions is also not considered in the following as it is small compared to the overall time.

E.2 Non switching message delay T_{NSM}

This delay applies when the QL of the selected reference signal changes and the sync source is maintained. T_{NSM} defines the maximum time between the change of the input QL and the change of the output QL.

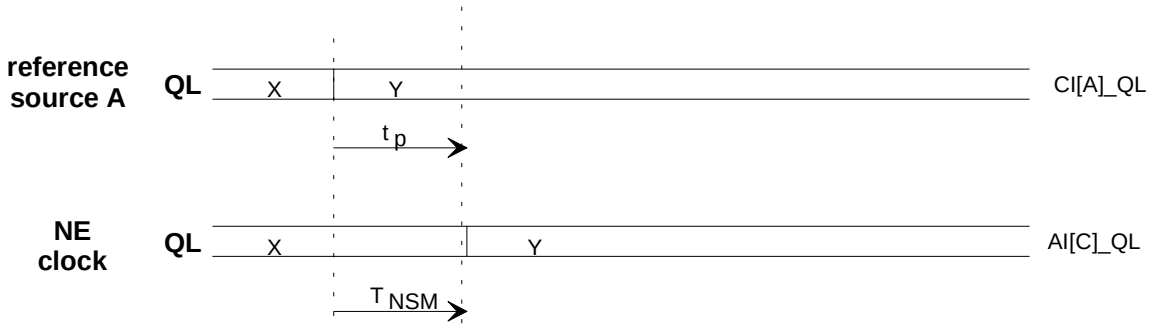

Figure E.2: T_{NSM}

T_{NSM} is due to the processing time t_p of the reference selection process in the NS_C function.

A maximum value of 200 ms is defined for T_{NSM}.

$T_{NSM} = t_p$ = 0 ms to 200 ms.

E.3 Switching message delay T_{SM}

This delay applies if a switch over to another reference source is performed with a different QL value. T_{SM} defines the time between the triggering of the new selection (e.g. change of the QL of a reference, external command, etc.) and the change of the QL at the output.

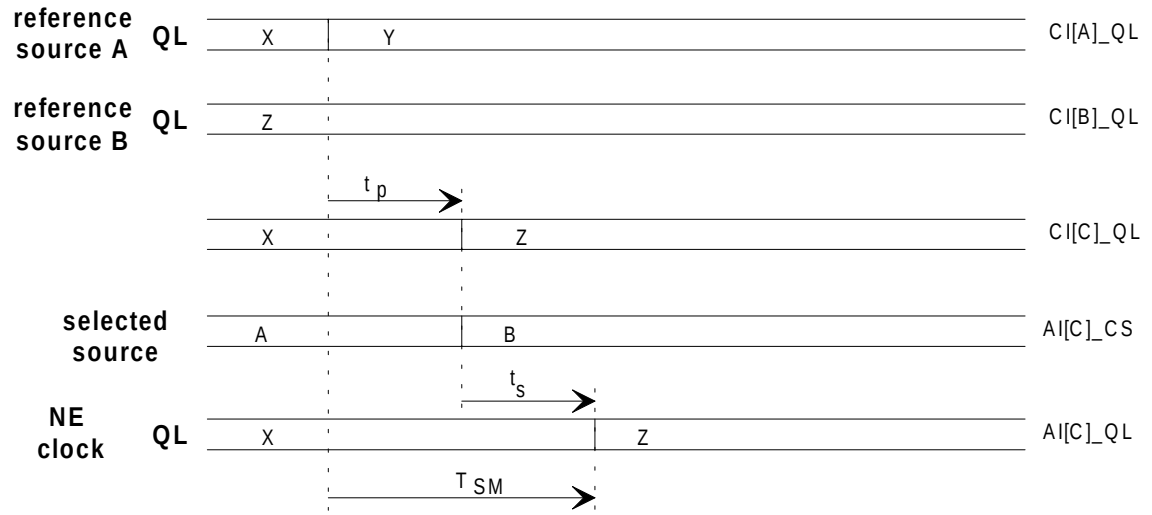

Figure E.3: T_{SM}

T_{SM} is due to the processing time t_p of the selection process in the NS_C function and the settling time t_s of the oscillator in the SD/NS-SEC_A_So function.

A range of 180 ms to 500 ms is defined for T_{SM}.

$T_{SM} = (t_p + t_s)$ = 180 ms to 500 ms.

E.4 Holdover message delay T_{HM}

This delay applies when the SEC should enter a holdover mode due to a failure condition of the selected sync source and the unavailability of any other synchronization source. When this event occurs the SEC goes immediately into holdover mode. The outgoing QL changes to QL_SEC after the time T_{HM}.

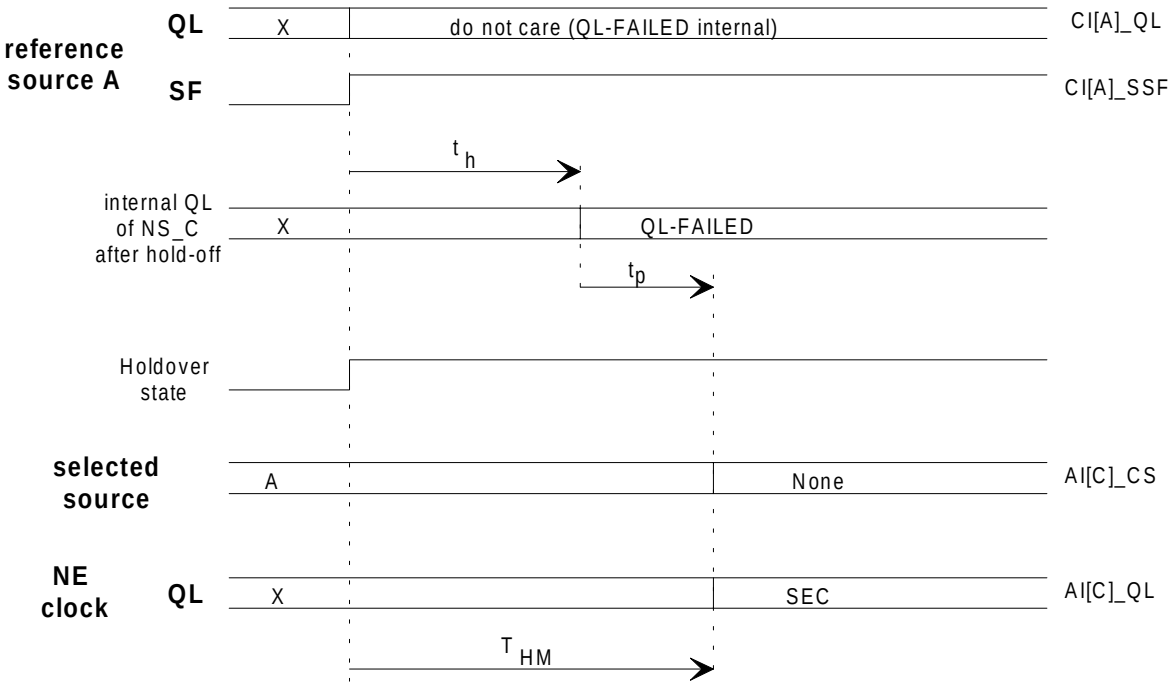

Figure E.4: T_{HM}

NOTE: The internal QL of NS_C after hold-off characterizes a signal located between the WTR bloc and the selection control process box defined in figure A.1

T_{HM} is due to the QL-FAILED (SSF) hold off time t_h and the processing time t_p of the selection process in the NS_C function.

A range of 500 ms to 2 000 ms is defined for T_{HM}.

$T_{HM} = t_h + t_p$ = 500 ms to 2 000 ms

E.5 Wait to restore time T_{WTR}

The wait to restore time applies when a synchronization source signal recovers from a failure condition. This signal comes only available for the selection process after signal fail is cleared at least for the time T_{WTR}.

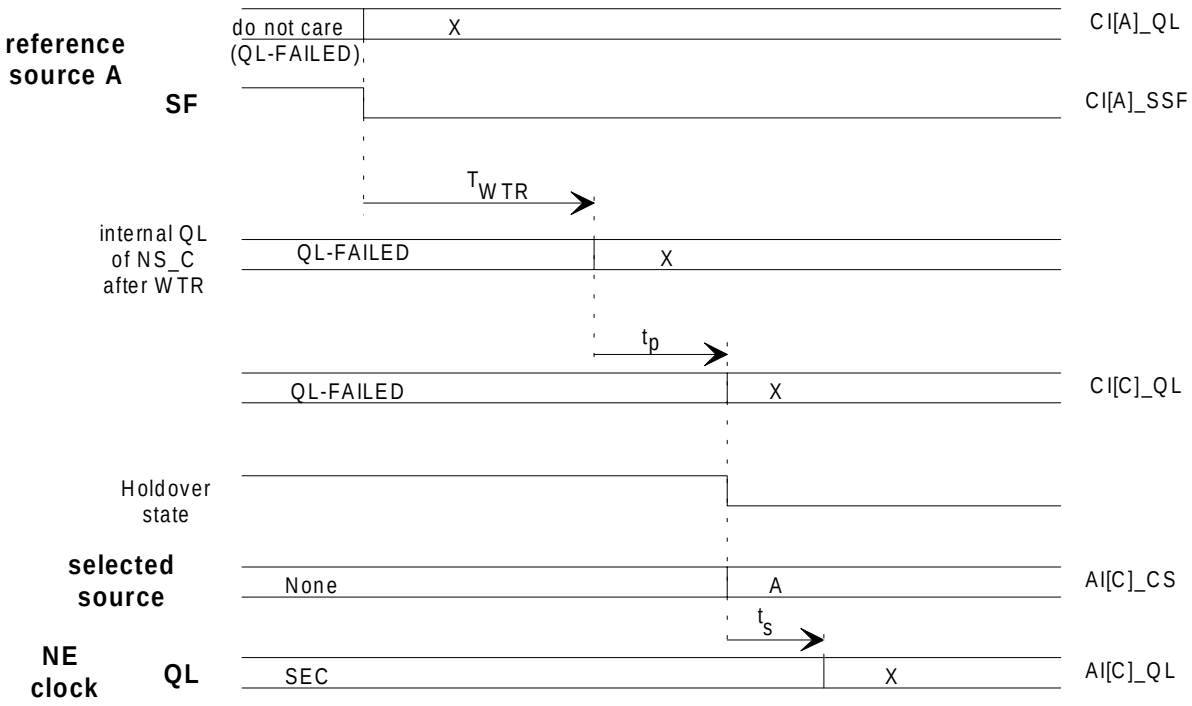

Figure E.5: T_{WTR}

NOTE: The internal QL of NS_C after WTR characterizes a signal located between the WTR bloc and the selection control process box defined in figure A.1

T_{WTR} is implemented in the NS_C function. The definition of WTR is in clause 4.

Annex F (informative): Overview of inputs/outputs to the atomic functions

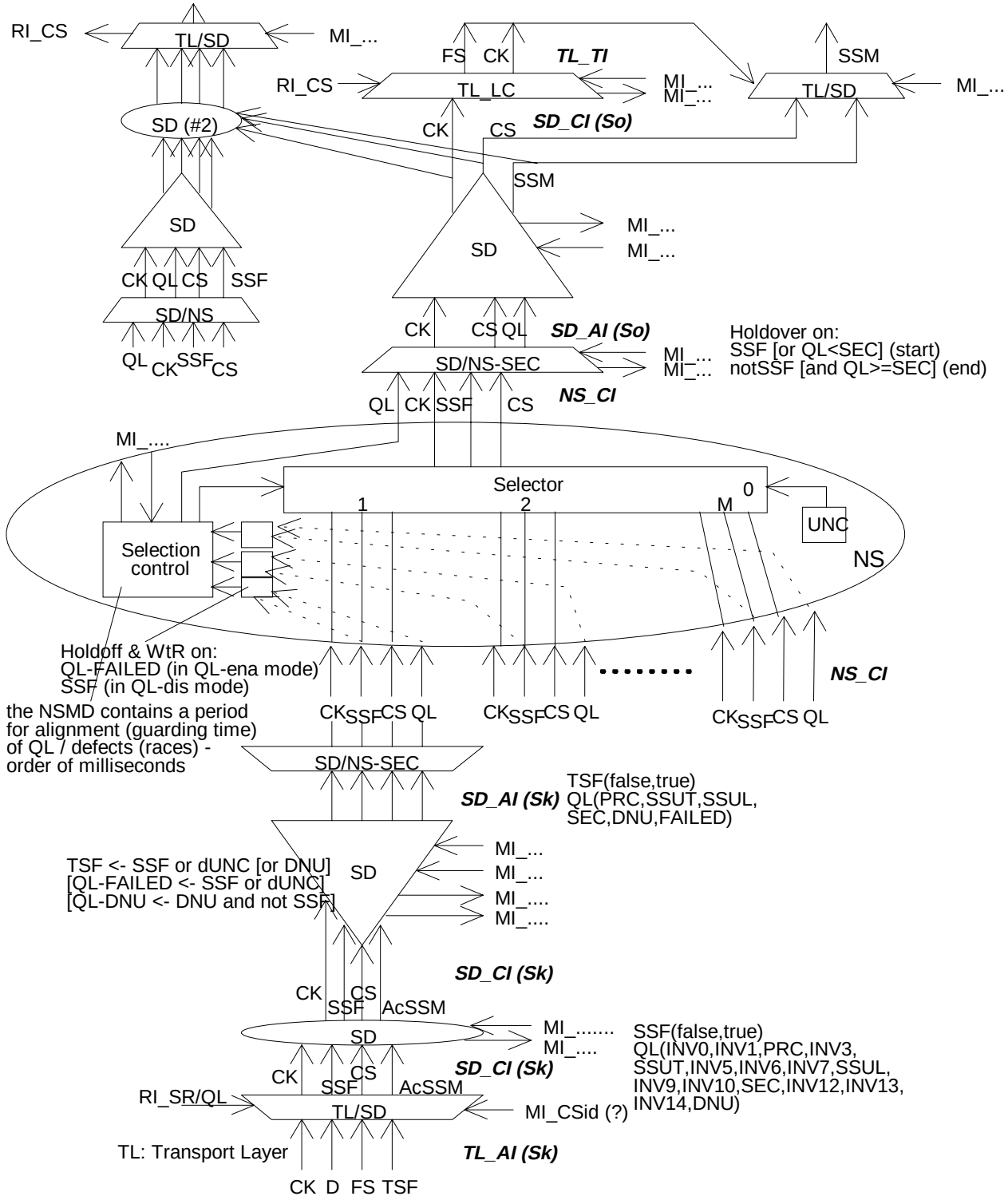

Figure F.1: Interconnection of atomic functions

History

Document history			
August 1997	Public Enquiry	PE 9748:	1997-08-01 to 1997-11-28