EUROPEAN TELECOMMUNICATION STANDARD

DRAFT
pr **ETS 300 417-3-1**
April 1996

Source: ETSI TC-TM

Reference: DE-TM-01015-3-1

ICS: 33.020

Key words: transmission, SDH, interface

Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 3-1: STM-N regenerator and multiplex section layer functions

ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE
Office address: 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
X.400: c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

*

Contents

Blank page

Foreword

This draft European Telecommunications Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI) in order to provide inter-vendor and inter-operator compatibility of SDH equipments, and is now submitted for the Public Enquiry phase of the ETSI standards approval procedure.

This ETS has been produced in order to provide inter-vendor and inter-operator compatibility for Synchronous Digital Hierarchy (SDH) equipment.

This ETS consists of 8 parts as follows:

Part 1: "Generic processes and performance" (ETS 300 417-1-1).
Part 2: "Physical section layer functions" (prETS 300 417-2-1).
Part 3: "STM-N regenerator and multiplex section layer functions" (prETS 300 417-3-1).
Part 4: "SDH path layer functions" (prETS 300 417-4-1).
Part 5: "PDH path layer functions" (prETS 300 417-5-1).
Part 6: "Synchronization distribution layer functions" (prETS 300 417-6-1).
Part 7: "Auxiliary layer functions" (prETS 300 417-7-1).
Part 8: "Compound and major compound functions" (prETS 300 417-8-1).

Proposed transposition dates	
Date of latest announcement of this ETS (doa):	3 months after ETSI publication
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa

Blank page

1 Scope

This European Telecommunications Standard (ETS) specifies a library of basic building blocks and a set of rules by which they are combined in order to describe a digital transmission equipment. The library comprises the functional building blocks needed to completely specify the generic functional structure of the European Digital Transmission Hierarchy. Equipment which is compliant with this standard needs to be describable as an interconnection of a subset of these functional blocks contained within this ETS. The interconnections of these blocks need to obey the combination rules given. The generic functionality is described in ETS 300 417-1-1 [1].

2 Normative references

This ETS incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references subsequent amendments to, or revisions of, any of these publications apply to this ETS only when incorporated in it by amendments or revisions. For undated references the latest edition of the publication referred to applies.

[1] ETS 300 417-1-1 (1996): "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 1-1: Generic processes and performance".

[2] ETS 300 147 (1995): "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH) Multiplexing structure".

[3] ETS 300 166 (1993): "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s - based plesiochronous or synchronous digital hierarchies".

[4] ITU-T Recommendation G.707 (1993): "Synchronous digital hierarchy bit rates".

[5] ITU-T Recommendation G.783 (1994): "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks".

[6] prETS 300 746: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Automatic Protection Switching (APS) protocols and operation".

[7] prETS 300 417-4-1: "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 4-1: SDH path layer functions".

[8] prETS 300 417-6-1: "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 6-1: Synchronization distribution layer functions".

3 Definitions, abbreviations and symbols

3.1 Definitions

The functional definitions are described in ETS 300 417-1-1 [1].

3.2 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

A	Adaptation function
AcTI	Accepted Trace identifier
ADM	Add-Drop Multiplexer
AI	Adapted Information
AIS	Alarm Indication Signal
AP	Access Point
APId	Access Point Identifier
APS	Automatic Protection Switch
AU	Administrative Unit
AU-n	Administrative Unit, level n
AUG	Administrative Unit Group
BER	Bit Error Ratio
BIP	Bit Interleaved Parity
BIP-N	Bit Interleaved Parity, width N
C	Connection function
CI	Characteristic Information
CK	Clock
CM	Connection Matrix
CP	Connection Point
CS	Clock Source
D	Data
DCC	Data Communications Channel
DEC	Decrement
DEG	Degraded
DEGTHR	Degraded Threshold
EBC	Errored Block Count
ECC	Embedded Communications Channel
ECC(x)	Embedded Communications Channel, Layer x
EDC	Error Detection Code
EDCV	Error Detection Code Violation
EMF	Equipment Management Function
EQ	Equipment
ES	Errored Second
ES	Electrical Section
ExTI	Expected Trace Identifier
F_B	Far-end Block
FAS	Frame Alignment Signal
FOP	Failure Of Protocol
FS	Frame Start signal
HO	Higher Order
HOVC	Higher Order Virtual Container
HP	Higher order Path
ID	Identifier
IF	In Frame state
INC	Increment
LC	Link Connection
LO	Lower Order
LOA	Loss Of Alignment; generic for LOF, LOM, LOP
LOF	Loss Of Frame
LOP	Loss Of Pointer
LOS	Loss Of Signal
LOVC	Lower Order Virtual Container
MC	Matrix Connection

MCF	Message Communications Function
MDT	Mean Down Time
mei	maintenance event information
MI	Management Information
MO	Managed Object
MON	Monitored
MP	Management Point
MS	Multiplex Section
MS1	STM-1 Multiplex Section
MS4	STM-4 Multiplex Section
MS16	STM-16 Multiplex Section
MSB	Most Significant Bit
MSOH	Multiplex Section Overhead
MSP	Multiplex Section Protection
MSPG	Multiplex Section Protection Group
N_B	Near-end Block
NC	Network Connection
N.C.	Not Connected
NDF	New Data Flag
NE	Network Element
NNI	Network Node Interface
NMON	Not Monitored
NU	National Use (bits, bytes)
NUx	National Use, bit rate order x
OAM	Operation, Administration and Management
OFS	Out of Frame Second
OOF	Out Of Frame state
OS	Optical Section
OSI(x)	Open Systems Interconnection, Layer x
OW	Order Wire
P	Protection
P_A	Protection Adaptation
P_C	Protection Connection
P_TT	Protection Trail Termination
PDH	Plesiochronous Digital Hierarchy
PJE	Pointer Justification Event
PM	Performance Monitoring
Pn	Plesiochronous signal, Level n
POH	Path Overhead
PRC	Primary Reference Clock
PS	Protection Switching
PSC	Protection Switch Count
PTR	Pointer
QOS	Quality Of Service
RDI	Remote Defect Indicator
REI	Remote Error Indicator
RI	Remote Information
RP	Remote Point
RS	Regenerator Section
RS1	STM-1 Regenerator Section
RS4	STM-4 Regenerator Section
RS16	STM-16 Regenerator Section
RSOH	Regenerator Section Overhead
RxTI	Received Trace identifier
S4	VC-4 path layer
SASE	Stand-Alone Synchronization Equipment
SD	Synchronization Distribution layer, Signal Degrade
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SF	Signal Fail
Sk	Sink
SNC	Sub-Network Connection
SNC/I	Inherently monitored Sub-Network Connection protection

SNC/N	Non-intrusively monitored Sub-Network Connection protection
So	Source
SOH	Section Overhead
SPRING	Shared Protection Ring
SR	Selected Reference
SSD	Server Signal Degrade
SSF	Server Signal Fail
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
STM-N	Synchronous Transport Module, level N
TCP	Termination Connection Point
TIM	Trace Identifier Mismatch
TI	Timing Information
TM	Transmission_Medium, Transmission & Multiplexing
TMN	Telecommunications Management Network
TP	Timing Point
TPmode	Termination Point mode
TS	Time Slot
TSD	Trail Signal Degrade
TSF	Trail Signal Fail
TT	Trail Termination function
TTs	Trail Termination supervisory function
TTI	Trail Trace Identifier
TxTI	Transmitted Trace Identifier
UNEQ	Unequipped
UNI	User Network Interface
USR	User channels
VC	Virtual Container
VC-n	Virtual Container, level n
W	Working

3.3 Symbols and Diagrammatic Conventions

The symbols and diagrammatic conventions are described in ETS 300 417-1-1 [1].

3.4 Introduction

The atomic functions defining the regenerator and multiplex section layers are described below.

4 STM-1 Regenerator Section Layer Functions

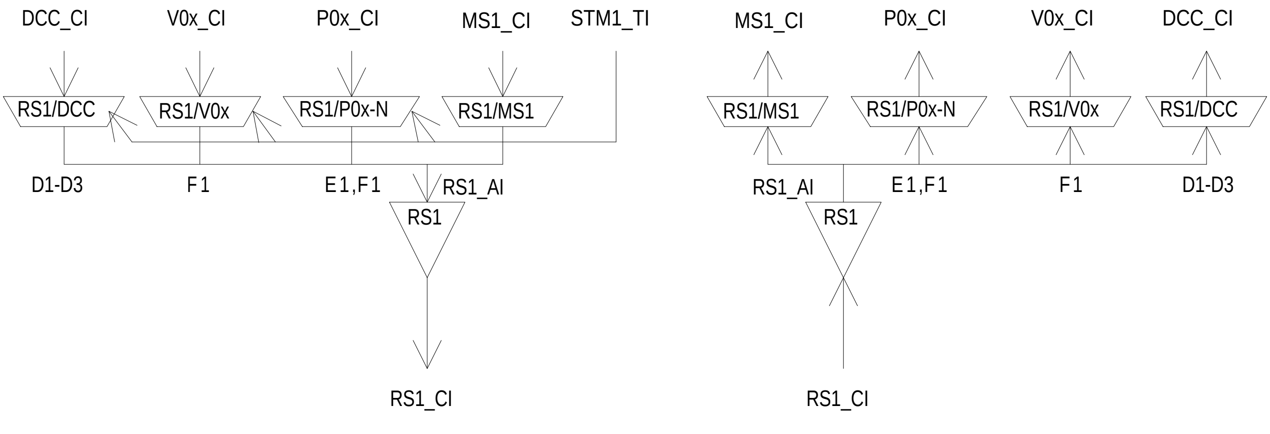


Figure 1: STM-1 Regenerator Section atomic functions

RS1 Layer CP.

The CI at this point is an octet structured, 125 µs framed data stream with co-directional timing. It is the entire STM-1 signal as defined in ETS 300 147 [2]. Figure 2 depicts only bytes handled in the RS1 layer.

NOTE 1: The unmarked bytes [2,6], [3,6], [3,8], [3,9] in rows 2,3 (figure 2) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The unmarked bytes [2,2], [2,3], [2,5], [3,2], [3,3], [3,5] in rows 2,3 (figure 2) are reserved for media specific usage (e.g. radio sections). In optical and electrical section applications they are undefined.

NOTE 3: The bytes for National Use (NU) in rows 1,2 (figure 2) are reserved for operator specific usage. Their processing is not within the province of this ETS. If NU bytes [1,8] and [1,9] are unused, care should be taken in selecting the binary content of the bytes which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of “1”s or “0”s do not occur.

	1	2	3	4	5	6	7	8	9	10 270
1	A1	A1	A1	A2	A2	A2	J0	NU	NU	
2	B1			E1			F1	NU	NU	
3	D1			D2			D3			
4										
5										
6										MS1_CI
7										
8										
9										

Figure 2: RS1_CI_D signal

RS1 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing and represents the combination of adapted information from the MS1 layer (2403 bytes per frame), the management communication DCC layer (3 bytes per frame if supported), the OW layer (1 byte per frame if supported) and the user channel F1 (1 byte per frame if supported). The location of these four components in the frame is defined in ETS 300 147 [2] and depicted in figure 3.

NOTE 4: Bytes E1, F1 and D1-D3 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

	1	2	3	4	5	6	7	8	9	10 270
1								NU	NU	
2				E1			F1	NU	NU	
3	D1			D2			D3			
4										
5										
6										MS1_CI
7										
8										
9										

Figure 3: RS1_AI_D signal

4.1 STM-1 Regenerator Section Connection functions

For further study.

4.2 STM-1 Regenerator Section Trail Termination functions

4.2.1 STM-1 Regenerator Section Trail Termination Source RS1_TT_So

Symbol:

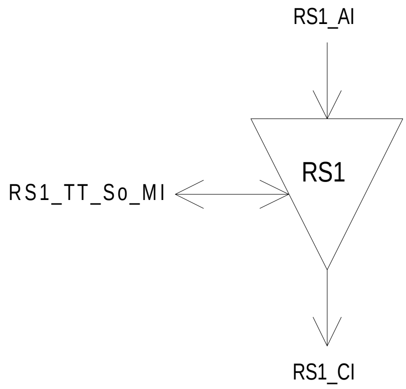


Figure 4: RS1_TT_So symbol

Interfaces:

Table 1: RS1_TT_So input and output signals

Input(s)	Output(s)

Processes:

The function builds the STM-1 signal by adding the frame alignment information, bytes A1A2, the STM Section Trace Identifier (STI) byte J0, computing the parity and inserting the B1 byte.

J0: In this byte the function shall insert the Transmitted Trail Trace Identifier TxTI. Its format is described in ETS 300 417-1-1 [1], subclause 7.1.

B1: The function shall calculate a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 shall be calculated over all bits of the previous STM-1 frame after scrambling and is placed in byte position B1 of the current STM-1 frame before scrambling (figure 5).

A1A2: The function shall insert the STM-1 frame alignment signal A1A1A1A2A2A2 into the regenerator section overhead as defined in ETS 300 147 [2].

Scrambler: This function provides scrambling of the RS1_CI. The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate. The generating polynomial shall be $1+X^6+X^7$. The scrambler shall be reset to '1111 1111' on the most significant bit (MSB) of the byte (1,10) following the last byte of the STM-1 SOH in the first row. This bit and all subsequent bits to be scrambled shall be modulo 2 added to the output of the X^7 position of the scrambler. The scrambler shall run continuously throughout the remaining STM-1 frame.

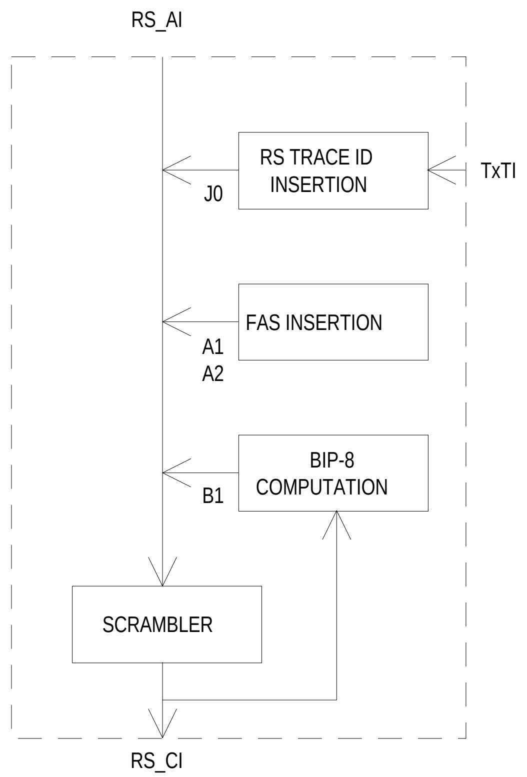


Figure 5: Some processes within RS1_TT_So

NOTE: The insertion of the frame alignment signal (A1A2) and the scrambling of the signal would be OS1/RS1_A_So processes according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-1 signal causes a violation of this process allocation, hence the frame alignment insertion and scrambling processes are located in the RS1_TT_So function.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

4.2.2 STM-1 Regenerator Section Trail Termination Sink RS1_TT_Sk

Symbol:

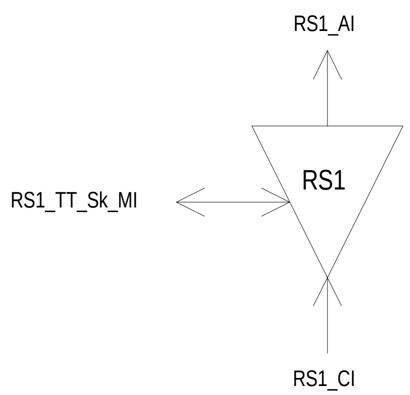


Figure 6: RS1_TT_Sk symbol

Interfaces:

Table 2: RS1_TT_Sk input and output signals

Input(s)	Output(s)

Processes:

This function monitors the STM-1 signal for RS errors, and recovers the RS trail termination status. It extracts the payload independent overhead bytes (J0, B1) from the RS1 layer Characteristic Information:

Descrambling: The function shall descramble the incoming STM-1 signal. The operation of the descrambler shall be functionally identical to that of a scrambler in OS1/RS1_A_So.

NOTE 1: The descrambling of the signal would be an OS/RS_A_Sk or ES/RS_A_Sk process according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-N signal causes a violation of this process allocation, hence the descrambling process is located in the RS1_TT_Sk function.

B1: Even bit parity is computed for each bit n of every byte of the preceding scrambled STM-1 frame and compared with bit n of B1 recovered from the current frame (n=1 to 8 inclusive) (figure 7). A difference between the computed and recovered B1 values is taken as evidence of one or more errors (nN_B) in the computation block.

J0: The Received Trail Trace Identifier RxTI shall be recovered from the J0 byte and shall be made available as AcTI for network management purposes. The application and acceptance and mismatch detection process shall be performed as specified in ETS 300 417-1-1 [1], subclauses 7.1, and 8.2.1.3.

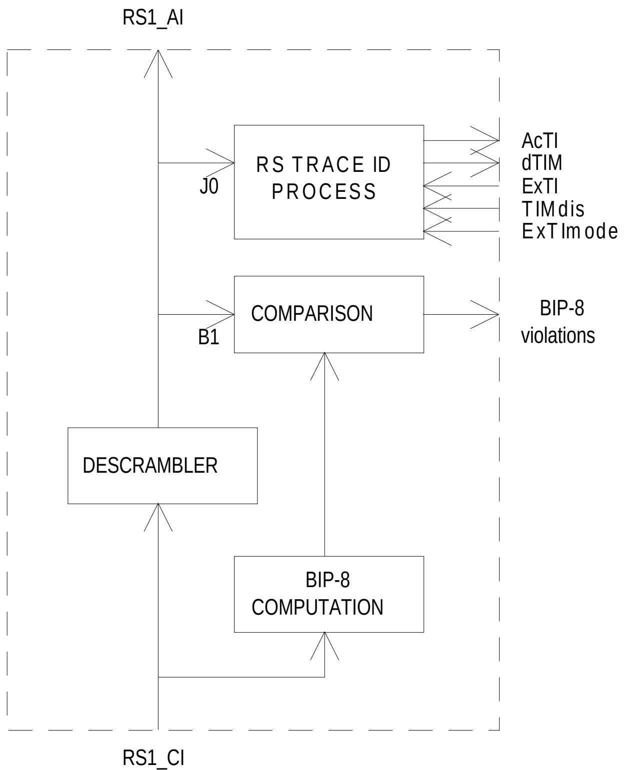


Figure 7: Some processes within RS1_TT_Sk

Defects:

The function shall detect for dTIM defect according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

Consequent Actions:

aAIS ← CI_SSF or dTIM

aTSF ← CI_SSF or dTIM

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 μs; on clearing of aAIS the function shall output normal data within 250 μs.

NOTE 2: The term "CI_SSF" has been added to the conditions for aAIS while the descrambler function has been moved from the e.g. OS1/RS1_A_Sk to this function. Consequently, an all-ONEs (AIS) pattern inserted in the mentioned adaptation function would be descrambled in this function. A "refreshment" of all-ONEs is required.

Defect Correlations:

cTIM ← MON and dTIM

Performance Monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← AI_TSF or dEQ

pN_EBC ← Σ nN_B

4.3 STM-1 Regenerator Section Adaptation functions

4.3.1 STM-1 Regenerator Section to Multiplex Section Adaptation Source RS1/MS1_A_So

Symbol:

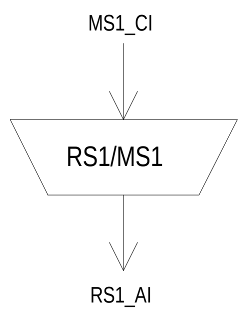


Figure 8: RS1/MS1_A_So symbol

Interfaces:

Table 3: RS1/MS1_A_So input and output signals

Input(s)	Output(s)

Processes:

The function multiplexes the MS1_CI data (2 403 bytes/frame) into the STM-1 byte locations defined in ETS 300 147 [2] and depicted in figure 2.

NOTE 1: There might be cases in which the network element knows that the timing reference for a particular STM-1 interface can not be maintained within ± 4.6 ppm. For such cases MS-AIS can be generated. This is network element specific and outside the scope of this ETS.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output all ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs. The frequency of the all ONEs signal shall be within 155 520 kHz ± 20 ppm.

NOTE 2: if CI_SSF is not connected (when RS1/MS1_A_So is connected to a MS1_TT_So), SSF is assumed to be false.

Defect Correlations: None.

Performance Monitoring: None.

4.3.2 STM-1 Regenerator Section to Multiplex Section Adaptation Sink RS1/MS1_A_Sk

Symbol:

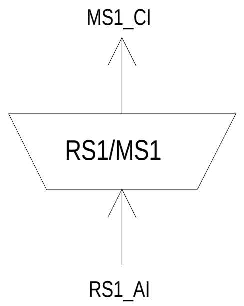


Figure 9: RS1/MS1_A_Sk symbol

Interfaces:

Table 4: RS1/MS1_A_Sk input and output signals

Input(s)	Output(s)

Processes:

The function separates MS1_CI data from RS1_AI as depicted in figure 2.

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

4.3.3 STM-1 Regenerator Section to DCC Adaptation Source RS1/DCC_A_So

Symbol:

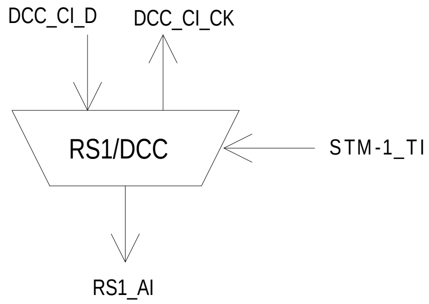


Figure 10: RS1/DCC_A_So symbol

Interfaces:

Table 5: RS1/DCC_A_So input and output signals

Input(s)	Output(s)

Processes:

The function multiplexes the DCC CI data (192 kbit/s) into the byte locations D1, D2 and D3 as defined in ETS 300 147 [2] and depicted in figure 3 [1].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

4.3.4 STM-1 Regenerator Section to DCC Adaptation Sink RS1/DCC_A_Sk

Symbol:

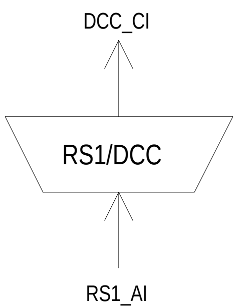


Figure 11: RS1/DCC_A_Sk symbol

---

1 DCC transmission can be “disabled” when the matrix connection in the connected DCC_C function is removed.

Interfaces:

Table 6: RS1/DCC_A_Sk input and output signals

Input(s)	Output(s)

Processes:

The function separates DCC data from RS Overhead as defined in ETS 300 147 [2] and depicted in figure 3 [2].

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

4.3.5 STM-1 Regenerator Section to P0x Adaptation Source RS1/P0x_A_So/N

Symbol:

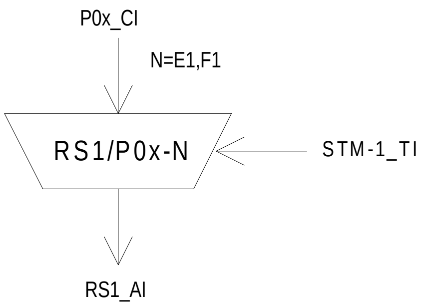


Figure 12: RS1/P0x_A_So symbol

Interfaces:

Table 7: RS1/P0x_A_So input and output signals

Input(s)	Output(s)

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire or user channel information stream into the RS1_AI using slip buffering. It takes P0x_CI, a 64 kbit/s signal as defined in ETS 300 166 [3], as an octet structured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the RSOH byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 3.

---

2 DCC processing can be "disabled" when the matrix connection in the connected DCC_C function is removed.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-1 clock, frame position (STM1_TI), and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification (slip) action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification (slip) action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

64 kbit/s timeslot: The adaptation source function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

4.3.6 STM-1 Regenerator Section to P0x Adaptation Sink RS1/P0x_A_Sk/N

Symbol:

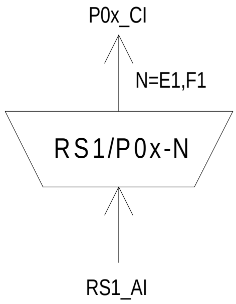


Figure 13: RS1/P0x_A_Sk symbol

Interfaces:

Table 8: RS1/P0x_A_Sk input and output signals

Input(s)	Output(s)
RS1_AI_D RS1_AI_CK RS1_AI_FS RS1_AI_TSF	P0x_CI_D P0x_CI_CK P0x_CI_FS

Processes:

The function separates P0x data from RS Overhead byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 3.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-1 signal generated at the remote node containing RS1/P0x_A_So). The residual jitter (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 20 ppm, this smoothing process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the RS1_AI (for example due to a frequency step of the server STM-1 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

64 kbit/s timeslot: The adaptation sink function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

4.3.7 STM-1 Regenerator Section toV0x Adaptation Source RS1/V0x_A_So

Symbol:

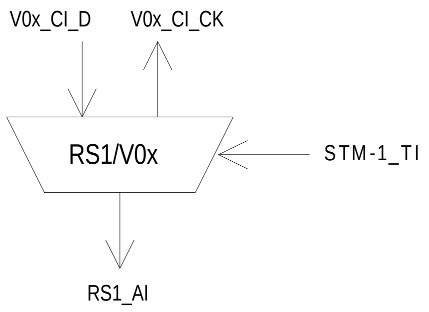


Figure 14: RS1/V0x_A_So symbol

Interfaces:

Table 9: RS1/V0x_A_So input and output signals

Input(s)	Output(s)
V0x_CI_D STM1_TI_CK STM1_TI_FS	RS1_AI_D V0x_CI_CK

Processes: None.

This function multiplexes the V0x_CI data (64 kbit/s) into the byte location F1 as defined in ETS 300 147 [2] and depicted in figure 3.

The user channel byte F1 shall be added to the 125 µs frame.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

4.3.8 STM-1 Regenerator Section to V0x Adaptation Sink RS1/V0x_A_Sk

Symbol:

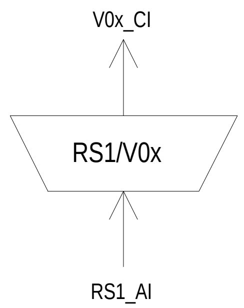


Figure 15: RS1/V0x_A_Sk symbol

Interfaces:

Table 10: RS1/V0x_A_Sk input and output signals

Input(s)	Output(s)
RS1_AI_D RS1_AI_CK RS1_AI_FS RS1_AI_TSF	V0x_CI_D V0x_CI_CK V0x_CI_SSF

Processes:

This function separates user channel data from RS Overhead (byte F1) as defined in ETS 300 147 [2] and depicted in figure 3.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± TBD ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

5 STM-1 Multiplex Section layer functions

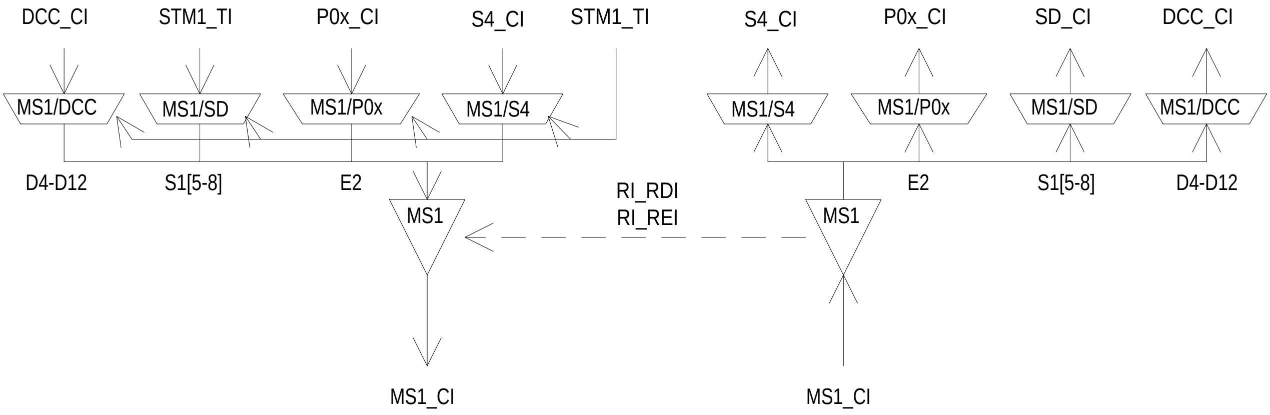


Figure 16: STM-1 Multiplex Section atomic functions

MS1 Layer CP.

The CI at this point is octet structured and 125 µs framed with co-directional timing. Its format is characterised as the MS1_AI with an additional MS Trail Termination overhead in the three B2 bytes, byte M1, and bits 6-8 of the K2 byte in the frame locations defined in ETS 300 147 [2] and depicted in figure 17.

NOTE 1: The unmarked bytes in rows 5,6,7,8,9 (figure 17) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The bytes for National Use (NU) in row 9 (figure 17) are reserved for operator specific usage. Their processing is not within the province of this ETS.

	1	2	3	4	5	6	7	8	9	10 270
1										
2										
3										
4	**H1**	**'Y'**	**'Y'**	**H2**	**'1'**	**'1'**	**H3**	**H3**	**H3**	
5	**B2**	**B2**	**B2**	**K1**			**K2**			**AU4 payload capacity**
6	**D4**			**D5**			**D6**			**(261 X 9 bytes)**
7	**D7**			**D8**			**D9**			
8	**D10**			**D11**			**D12**			
9	**S1**					**M1**	**E2**	**NU**	**NU**	

Figure 17: MS1_CI_D

MS1 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing. It represents the combination of information adapted from the VC-4 layer (150 336 kbit/s), the management communications DCC layer (576 kbit/s), the OW layer (64 kbit/s if supported), the AU-4 pointer (3 bytes per frame), the APS signalling channel (13 [3] or 16 [4] bits per frame if supported), and the Synchronisation Status Message channel (4 bits per frame if supported). The location of these five components in the frame is defined in ETS 300 147 [2] and depicted in figure 18.

NOTE 3: Bytes E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

---

3 13 bits APS channel for the case of linear MS protection
4 16 bits APS channel for the case of MS SPRING protection

	1	2	3	4	5	6	7	8	9	10	....	270
1												
2												
3												
4	H1	'Y'	'Y'	H2	'1'	'1'	H3	H3	H3	H3+1	H3+1	H3+1
5				K1			K2			AU4 payload capacity		
6	D4			D5			D6			(261 X 9 bytes)		
7	D7			D8			D9					
8	D10			D11			D12					
9	S1						E2	NU	NU			

Figure 18: MS1_AI_D

NOTE 4: The allocation of definitions and associated processing of unused MS OH bytes might change due to their future application.

Figure 19 shows the MS trail protection specific sublayer atomic functions (MS1/MS1P_A, MS1P_C, MS1P_TT) within the MS1 layer. Note that the DCC (D4-D12), OW (E2), and SSM (S1[5-8]) signals can be accessible before (unprotected) and after (protected) the MS1P_C function. The choice is outside the scope of this ETS.

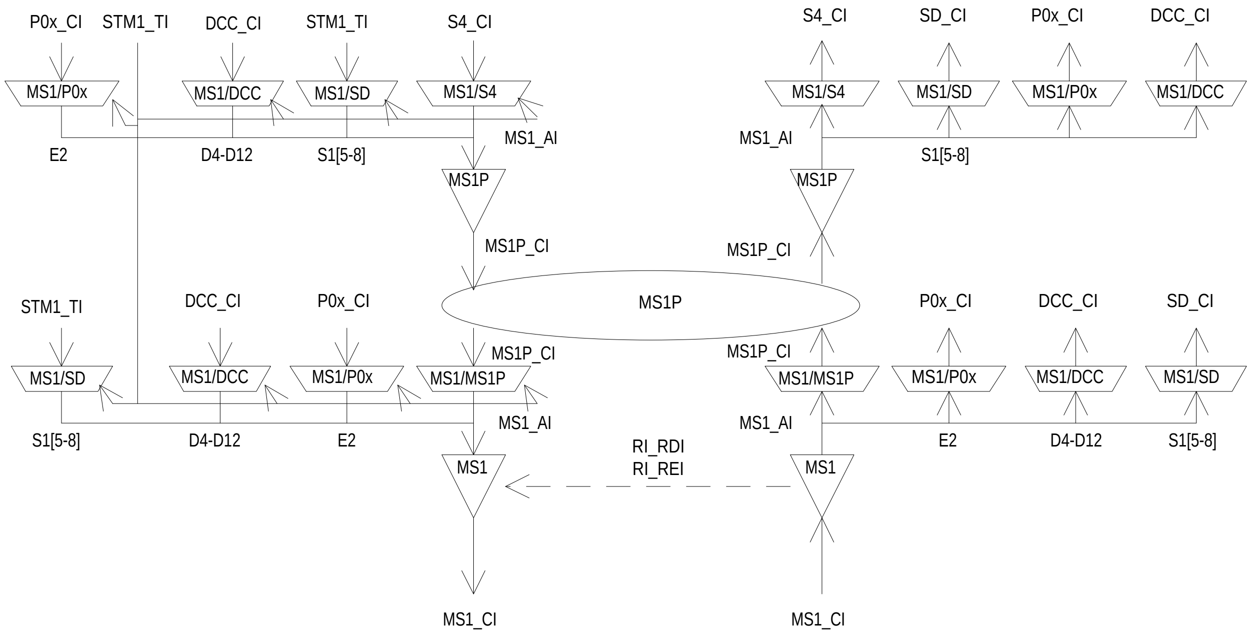


Figure 19: STM-1 Multiplex Section Linear Trail Protection Functions

MS1P Sublayer CP.

The CI at this point is octet structured and 125 μs framed with co-directional timing. Its format is equivalent to the MS1_AI and depicted in figure 20.

NOTE 5: Bytes S1, E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element or are unprotected (see above).

	1	2	3	4	5	6	7	8	9	10 270
1										AU4 payload capacity (261 X 9 bytes)
2										
3										
4	H1	'Y'	'Y'	H2	'1'	'1'	H3	H3	H3	
5				K1			K2*			
6	D4			D5			D6			
7	D7			D8			D9			
8	D10			D11			D12			
9	S1						E2	NU	NU	

NOTE 6: K2* represents bits 1 to 5 of K2

Figure 20: MS1P_CI_D

5.1 STM-1 Multiplex Section Connection functions

For further study.

5.2 STM-1 Multiplex Section Trail Termination functions

5.2.1 STM-1 Multiplex Section Trail Termination Source MS1_TT_So

Symbol:

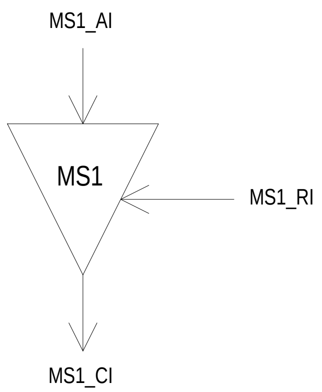


Figure 21: MS1_TT_So symbol

Interfaces:

Table 11: MS1_TT_So input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_RI_REI MS1_RI_RDI	MS1_CI_D MS1_CI_CK MS1_CI_FS

Processes:

This function adds error monitoring capabilities and remote maintenance information signals to the MS1_AI.

M1: The function shall set the REI (Remote Error Indication) to "0000 0001" if one or more errors were detected by the BIP-24 process in MS1_TT_Sk (communicated via MS1_RI_REI), and shall set REI to ”0000 0000” otherwise.

NOTE: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8]: These bits represents the defect status of the associated MS1_TT_Sk. The RDI indication shall be set to "110" on activation of MS1_RI_RDI within 250 µs, determined by the associated MS1_TT_Sk function, and set to "000" within 250 µs on the clearing of MS1_RI_RDI.

B2: The function shall calculate a Bit Interleaved Parity 24 (BIP-24) code using even parity. The BIP-24 shall be calculated over all bits, except those in the RSOH bytes, of the previous STM-1 frame and placed in three B2 bytes of the current STM-1 frame [5].

Defects: None.

Consequent Actions:

On declaration of RI_RDI the function shall output RDI (pattern '110' in bit 6,7, and 8 of byte K2) within 250 µs; on clearing of RI_RDI the function shall output normal data within 250 µs.

Defect Correlations: None.

Performance Monitoring: None.

5.2.2 STM-1 Multiplex Section Trail Termination Sink MS1_TT_Sk

Symbol:

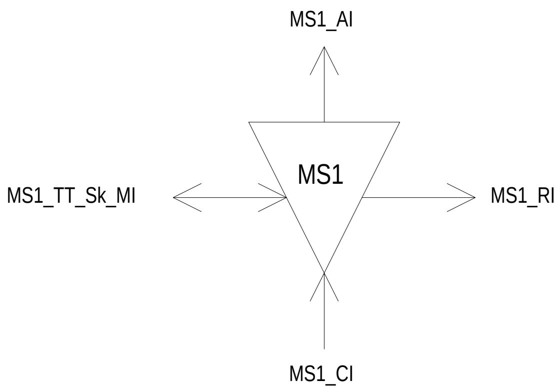


Figure 22: MS1_TT_Sk symbol

---

5 The BIP-24 procedure is described in ETS 300 147.

Interfaces:

Table 12: MS1_TT_Sk input and output signals

Input(s)	Output(s)
MS1_CI_D	MS1_AI_D
MS1_CI_CK	MS1_AI_CK
MS1_CI_FS	MS1_AI_FS
MS1_CI_SSF	MS1_CI_TSF
MS1_TT_Sk_DEGTHR	MS1_TT_Sk_MI_cAIS
MS1_TT_Sk_DEGM	MS1_TT_Sk_MI_cDEG
MS1_TT_Sk_1second	MS1_TT_Sk_MI_cRDI
MS1_TT_Sk_MI_TPmode	MS1_TT_Sk_MI_cSSF
MS1_TT_Sk_MI_SSF_Reported	MS1_TT_Sk_MI_pN_EBC
MS1_TT_Sk_MI_AIS_Reported	MS1_TT_Sk_MI_pF_EBC
MS1_TT_Sk_MI_RDI_Reported	MS1_TT_Sk_MI_pN_DS
	MS1_TT_Sk_MI_pF_DS
	MS1_RI_REI
	MS1_RI_RDI

Processes:

This function monitors error performance of associated MS1 including the far end receiver.

B2: The BIP-24 shall be calculated over all bits, except of those in the RSOH bytes, of the previous STM-1 frame and compared with the three error monitoring bytes B2 recovered from the MSOH of the current STM-1 frame. A difference between the computed and recovered B2 values is taken as evidence of one or more errors (nN_B) in the computation block.

M1: The REI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The REI (nF_B) is used to monitor the error performance of the other direction of transmission. The application process is described in ETS 300 417-1-1 [1], subclause 7.4.2 (REI).

The function shall interpret the code, for interworking with old equipment generating a code that represents the number of BIP-24 violations, as shown in table 13.

Table 13

M1[2-8] code, bits 234 5678	code interpretation
000 0000	0 errored blocks
000 0001	1 errored block
000 0010	1 errored block
000 0011	1 errored block
⋮	⋮
001 1000	1 errored block
001 1001	0 errored blocks
001 1010	0 errored blocks
⋮	⋮
111 1111	0 errored blocks

NOTE 1: bit 1 of byte M1 is ignored.

NOTE 2: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8] - RDI: The RDI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The RDI provides information as to the status of the remote receiver. A "110" indicates a Remote Defect Indication state, while other patterns indicate the normal state. The application process is described in ETS 300 417-1-1 [1], subclauses 7.4.11 and 8.2.

K2[6-8] - AIS: The MS-AIS information carried in these bits shall be extracted.

Defects:

The function shall detect for dDEG and dRDI defects according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

dAIS: If at least ***x*** consecutive frames contain the '111' pattern in bits 6, 7 and 8 of the K2 byte a dAIS defect shall be detected. dAIS shall be cleared if in at least ***x*** consecutive frames any pattern other then the '111' is detected in bits 6, 7 and 8 of byte K2. The ***x*** is in range 3 to 5.

Consequent Actions:

aAIS ← dAIS

aRDI ← dAIS

aTSF ← dAIS

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

Defect Correlations:

cAIS ← MON and dAIS and (not CI_SSF) and AIS_Reported

cDEG ← MON and dDEG

cRDI ← MON and dRDI and RDI_Reported

cSSF ← MON and dAIS and SSF_Reported

Performance monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← aTSF or dEQ

pF_DS ← dRDI

pN_EBC ← Σ nN_B

pF_EBC ← Σ nF_B

5.3 STM-1 Multiplex Section Adaptation functions

5.3.1 STM-1 Multiplex Section to S4 Layer Adaptation Source MS1/S4_A_So

Symbol:

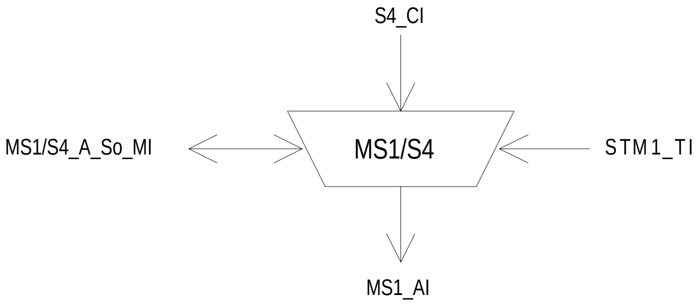


Figure 23: MS1/S4_A_So symbol

Interfaces:

Table 14: MS1/S4_A_So input and output signals

Input(s)	Output(s)
S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF STM1_TI_CK STM1_TI_FS	MS1_AI_D MS1_AI_CK MS1_AI_FS MS1/S4_A_So_MI_pPJE+ MS1/S4_A_So_MI_pPJE-

Processes:

This function provides frequency justification and bitrate adaptation for a VC-4 signal, represented by a nominally (261*9*64) = 150 336 kbit/s information stream and the related frame phase with a frequency accuracy within ± 4.6 ppm, to be multiplexed into a STM-1 signal.

The frame phase of the VC-4 is coded in the related AU-4 pointer. Frequency justification, if required, is performed by pointer adjustments. The accuracy of this coding process is specified below. Refer to prETS 300 417-4-1 [7], annex A.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (buffer) process. The data and frame start signals shall be written into the buffer under control of the associated input clock. The data and frame start signals shall be read out of the buffer under control of the STM-1 clock, frame position, and justification decision.

The justification decisions determine the phase error introduced by the MS1/S4_A_So function. The amount of this phase error can be measured at the physical interfaces by monitoring the AU-4 pointer actions. An example is given in prETS 300 417-4-1 [7], annex A.2.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of 24 data bits shall be cancelled once and no data written at the three positions H3+1. Upon a negative justification action, an extra 24 data bits shall be read out once into the three positions H3.

NOTE 1: A requirement for maximum introduced phase error cannot be defined until a reference path is defined from which the requirements for network elements can be deduced. Such a requirement would also limit excessive phase error caused by pointer processors under fixed frequency offset conditions.

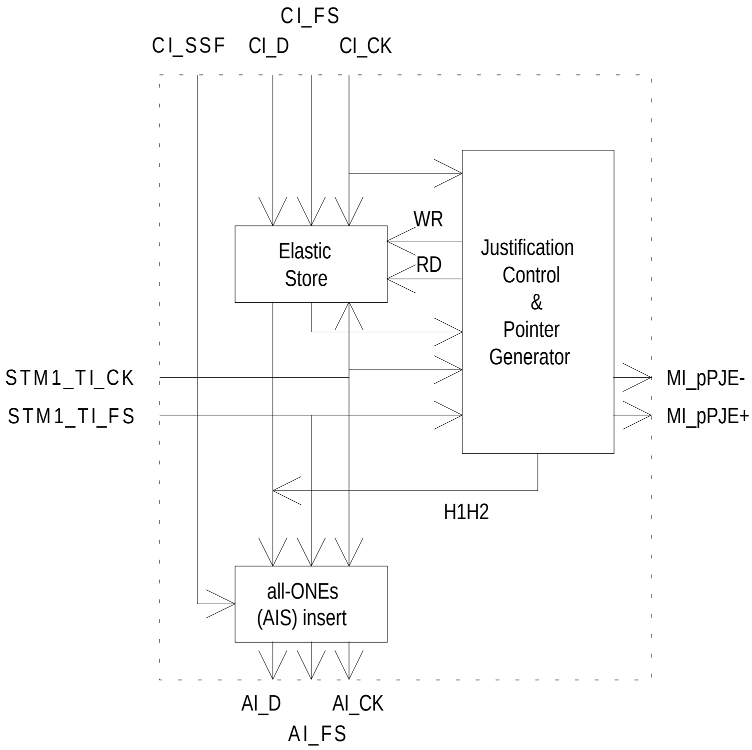


Figure 24: Main processes within MS1/S4_A_So

Buffer size: For further study.

Behaviour at recovery from defect condition: The incoming frequency (S4_CI_CK) of a passing through VC-4 may exceed its limits during a STM1dLOS condition. As a consequence, the buffer (elastic store) fill is not reliable any more. Due to all-ONEs (AIS) insertion after the pointer generator this reliability is not important for the operation of the network element. However, it shall be prevented to generate excessive pointer adjustments when recovering from the defect condition.

NOTE 2: The definition of excessive pointer adjustments is for further study.

The AU-4 pointer is carried in 2 bytes of payload specific OH in each STM-1 frame. The AU-4 pointer is aligned in the STM-1 payload in fixed position relative to the STM-1 frame. The AU-4 pointer points to the begin of the VC-4 frame within the STM-1. The format of the AU-4 pointer and its location in the frame are defined in ETS 300 147 [2].

H1H2 - *Pointer generation:* The function shall generate the AU-4 pointer as is described in ETS 300 417-1-1 [1], annex A: Pointer Generation. It shall insert the pointer in the appropriate H1, H2 positions with the SS field set to 10 to indicate AU-4.

YY1*1* - *Fixed stuff insertion:* The function shall insert fixed stuff codes Y = 1001ss11 in bytes [4,2],[4,3] and code '1' = 11111111 in bytes [4,5],[4,6]. Bits ss are undefined.

Defects: None

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 3: if CI_SSF is not connected (when MS1/S4_A_So is connected to a S4_TT_So), CI_SSF is assumed to be false.

Defect Correlations: None

Performance Monitoring:

Every second the number of generated pointer increments within that second shall be counted as the pPJE+. Every second the number of generated pointer decrements within that second shall be counted as the pPJE-.

NOTE 4: This is applicable for a passing through VC-4 only. A locally generated VC-4 may have a fixed frame phase; pointer justifications will not occur.

5.3.2 STM-1 Multiplex Section to S4 Layer Adaptation Sink MS1/S4_A_Sk

Symbol:

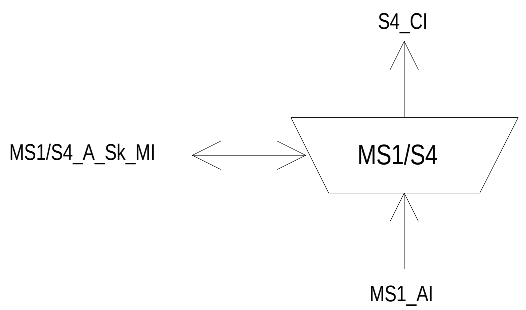


Figure 25: MS1/S4_A_Sk symbol

Interfaces:

Table 15: MS1/S4_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_AI_TSF MS1/S4_A_Sk_MI_AIS_Reported	S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF MS1/S4_A_Sk_MI_cAIS MS1/S4_A_Sk_MI_cLOP

Processes:

This function recovers the VC-4 data with frame phase information from the STM-1 as defined in ETS 300 147 [2].

H1H2 - *AU-4 pointer interpretation:* The function shall perform AU-4 pointer interpretation according to annex B of ETS 300 417-1-1 [1] to recover the VC-4 frame phase within the STM-1. The process shall maintain its current phase on detection of an invalid pointer and searches in parallel for a new phase.

YY1*1*: An AU-4 pointer consists of 2 bytes, [4,1] and [4,4]. The bytes [4,2],[4,3], [4,5],[4,6] contain fixed stuff, of a specified value, ignored by the AU-4 pointer interpreter.

Defects:

dAIS: The dAIS defect shall be detected if the pointer interpreter is in the AIS_state (refer to ETS 300 417-1-1 [1], annex B). The dAIS defect shall be cleared if the pointer interpreter is not in the AIS_state.

dLOP: The dLOP defect shall be detected if the pointer interpreter is in the LOP_state (refer to ETS 300 417-1-1 [1], annex B). The dLOP defect shall be cleared if the pointer interpreter is not in the LOP_state.

Consequent Actions:

aAIS ← dAIS or dLOP

aSSF ← dAIS or dLOP

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output the recovered data within 250 µs.

Defect Correlations:

cAIS ← dAIS and (not AI_TSF) and AIS_Reported

cLOP ← dLOP

Performance Monitors: None.

5.3.3 STM-1 Multiplex Section to DCC Adaptation Source MS1/DCC_A_So

Symbol:

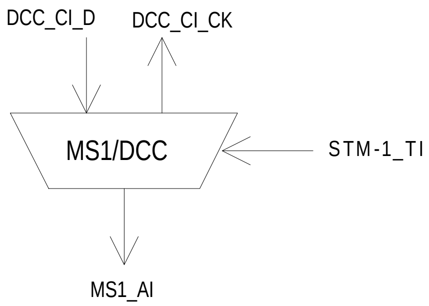


Figure 26: MS1/DCC_A_So symbol

Interfaces:

Table 16: MS1/DCC_A_So input and output signals

Input(s)	Output(s)
DCC_CI_D STM1_TI_CK STM1_TI_FS	MS1_AI_D DCC_CI_CK

Processes:

The function multiplexes the DCC CI data (576 kbit/s) into the byte locations D4 to D12 as defined in ETS 300 147 [2] and depicted in figure 18 [6].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

---

6 DCC transmission can be "disabled" when the matrix connection in the connected DCC_C function is removed.

Performance Monitoring: None.

5.3.4 STM-1 Multiplex Section to DCC Adaptation Sink MS1/DCC_A_Sk

Symbol:

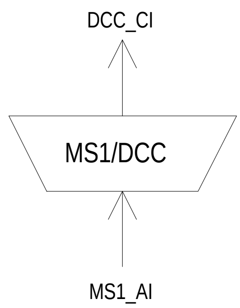


Figure 27: MS1/DCC_A_Sk symbol

Interfaces:

Table 17: MS1/DCC_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_AI_TSF	DCC_CI_D DCC_CI_CK DCC_CI_SSF

Processes:

The function separates DCC data from MS Overhead as defined in ETS 300 147 [2] and depicted in figure 18 [7].

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

---

[7] DCC processing can be “disabled” when the matrix connection in the connected DCC_C function is removed.

5.3.5 STM-1 Multiplex Section to P0x Adaptation Source MS1/P0x_A_So

Symbol:

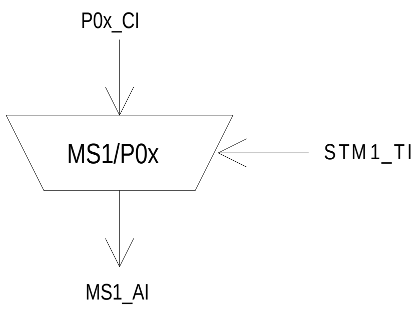


Figure 28: MS1/P0x_A_So symbol

Interfaces:

Table 18: MS1/P0x_A_So input and output signals

Input(s)	Output(s)
P0x_CI_D P0x_CI_CK P0x_CI_FS STM1_TI_CK STM1_TI_FS	MS1_AI_D

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire information stream into the MS1_AI using slip buffering. It takes P0x_CI, defined in ETS 300 166 [3] as an unstructured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the MSOH byte E2 as defined in ETS 300 147 [2] and depicted in figure 18.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-1 clock, frame position, and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification (slip) action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification (slip) action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

5.3.6 STM-1 Multiplex Section to P0x Adaptation Sink MS1/P0x_A_Sk

Symbol:

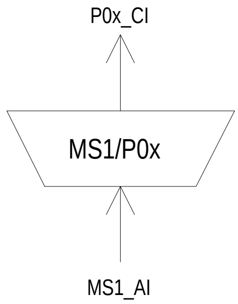


Figure 29: MS1/P0x_A_Sk symbol

Interfaces:

Table 19: MS1/P0x_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_AI_TSF	P0x_CI_D P0x_CI_CK P0x_CI_FS

Processes:

The function separates P0x data from MS Overhead byte E2 as defined in ETS 300 147 [2] and depicted in figure 18.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-1 signal generated at the remote node containing MS1/P0x_A_So). The residual jitter (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 4.6 ppm, this justification process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the MS1_AI (for example due to a frequency step of the server MS1 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

5.3.7 STM-1 Multiplex Section to Synchronisation Distribution Source MS1/SD_A_So

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

5.3.8 STM-1 Multiplex Section to Synchronisation Distribution Sink MS1/SD_A_Sk

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

5.4 STM-1 Multiplex Section Layer Monitoring Functions

For further study.

5.5 STM-1 Multiplex Section Linear Trail Protection Functions

5.5.1 STM-1 Multiplex Section Linear Trail Protection Connection Functions

5.5.1.1 STM-1 Multiplex Section 1+1 Linear Trail Protection Connection MS1P1+1_C

Symbol:

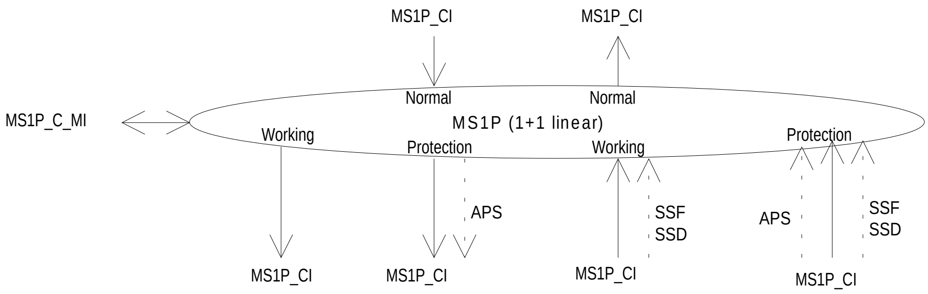


Figure 30: MS1P1+1_C symbol

Interfaces:

Table 20: MS1P1+1_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF MS1P_CI_SSD MS1P_C_MI_SFpriority MS1P_C_MI_SDpriority for connection points N and E: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS per function: MS1P_CI_APS MS1P_C_MI_SWtype MS1P_C_MI_OPERtype MS1P_C_MI_WTRTime MS1P_C_MI_HOTime MS1P_C_MI_EXTCMD	for connection points W and P: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS for connection points N and E: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF Note: protection status reporting signals are for further study. per function: MS1P_CI_APS MS1P_C_MI_cFOP MS1P_C_MI_pPSC

Processes:

The function performs the STM-1 linear multiplex section protection process for 1+1 protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 48 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #1 reference point can be the signal received via either the associated working #1 section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output connected to the normal #1 input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 21

Architecture:	1 + 1
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1+1 switching, revertive operation) LO, FSw-#1, MSw-#1, CLR, EXER-#1 (1+1 switching, non-revertive operation) LO or FSw, FSw-#i, MSw, MSw-#i, CLR, EXER-#i

Defects: None.

Consequent Actions: None.

Defect Correlations:

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

5.5.1.2 STM-1 Multiplex Section 1:n Linear Trail Protection Connection MS1P1:n_C

Symbol:

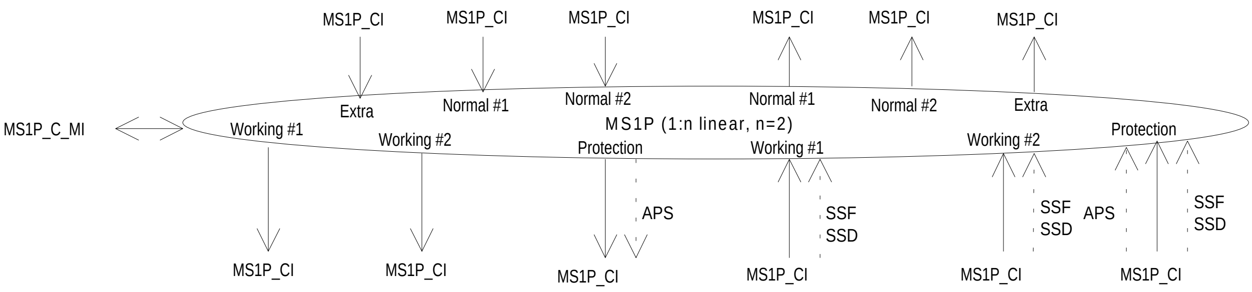


Figure 31: MS1P1:n_C symbol

Interfaces:

Table 22: MS1P1:n_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF MS1P_CI_SSD MS1P_C_MI_SFpriority MS1P_C_MI_SDpriority for connection points N and E: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS per function: MS1P_CI_APS MS1P_C_MI_SWtype MS1P_C_MI_OPERtype MS1P_C_MI_EXTRAtraffic MS1P_C_MI_WTRTime MS1P_C_MI_HOTime MS1P_C_MI_EXTCMD	for connection points W and P: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS for connection points N and E: MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF Note: protection status reporting signals are for further study. per function: MS1P_CI_APS MS1P_C_MI_cFOP MS1P_C_MI_pPSC

Processes:

The function performs the STM-1 linear multiplex section protection process for 1:n protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 47 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #i reference point can be the signal received via either the associated working #i section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output is unsourced (no input connected), connected to the extra traffic input, or connected to any normal input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 23

Architecture:	1:n (n ≤ 14)
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1:n switching, revertive operation) LO, FSw-#i, MSw-#i, CLR, EXER

Defects: None.

Consequent Actions:

For the case where neither the extra traffic nor a normal signal input is to be connected to the protection section output, the null signal shall be connected to the protection output. The null signal is either one of the normal signals, an all-ONEs, or a test signal.

For the case of a protection switch, the extra traffic output (if applicable) is disconnected from the protection input, set to all-ONEs (AIS) and aSSF is activated.

Defect Correlations:

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

5.5.2 STM-1 Multiplex Section Linear Trail Protection Trail Termination Functions

5.5.2.1 Multiplex Section Protection Trail Termination Source MS1P_TT_So

Symbol:

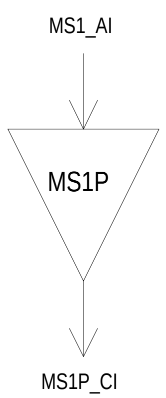


Figure 32: MS1P_TT_So symbol

Interfaces:

Table 24: MS1P_TT_So input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS	MS1P_CI_D MS1P_CI_CK MS1P_CI_FS

Processes:

No information processing is required in the MS1P_TT_So, the MS1_AI at its output being identical to the MS1P_CI at its input.

Defects: None.

Consequent Actions: None

Defect Correlations: None.

Performance Monitoring: None.

5.5.2.2 Multiplex Section Protection Trail Termination Sink MS1P_TT_Sk

Symbol:

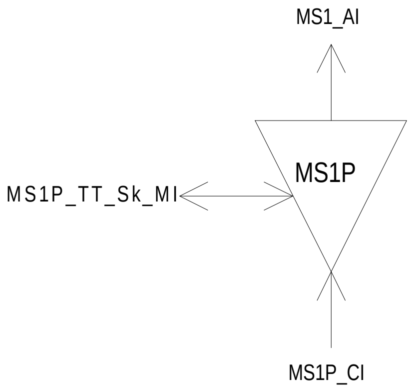


Figure 33: MS1P_TT_Sk symbol

Interfaces:

Table 25: MS1P_TT_Sk input and output signals

Input(s)	Output(s)
MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF MS1P_TT_Sk_MI_SSF_Reported	MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_AI_TSF MS1P_TT_Sk_MI_cSSF

Processes:

The MS1P_TT_Sk function reports, as part of the MS1 layer, the state of the protected MS1 trail. In case all connections are unavailable the MS1P_TT_Sk reports the signal fail condition of the protected trail.

Defects: None.

Consequent Actions:

aTSF ← CI_SSF

Defect Correlations:

cSSF ← CI_SSF and SSF_Reported

Performance Monitoring: None.

5.5.3 STM-1 Multiplex Section Linear Trail Protection Adaptation Functions

5.5.3.1 STM-1 Multiplex Section to STM-1 Multiplex Section Protection Layer Adaptation Source MS1/MS1P_A_So

Symbol:

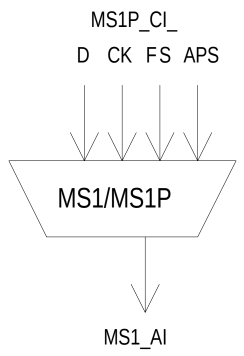


Figure 34: MS1/MS1P_A_So symbol

Interfaces:

Table 26: MS1/MS1P_A_So input and output signals

Input(s)	Output(s)
MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_APS	MS1_AI_D MS1_AI_CK MS1_AI_FS

Processes:

The function shall multiplex the MS1 APS signal and MS1 data signal onto the MS1 access point.

Defects: None.

Consequent actions: None.

Defect Correlations: None.

Performance Monitoring: None.

5.5.3.2 STM-1 Multiplex Section to STM-1 Multiplex Section Protection Layer Adaptation Sink MS1/MS1P_A_Sk

Symbol:

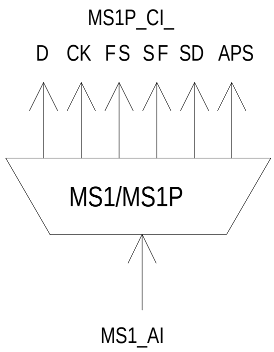


Figure 35: MS1/MS1P_A_Sk symbol

Interfaces:

Table 27: MS1/MS1P_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D MS1_AI_CK MS1_AI_FS MS1_AI_TSF MS1_AI_TSD	MS1P_CI_D MS1P_CI_CK MS1P_CI_FS MS1P_CI_SSF MS1P_CI_SSD MS1P_CI_APS (for Protection signal only)

Processes:

The function shall extract and output the MS1P_CI_D signal from the MS1_AI_D signal.

K1[1-8]K2[1-5]: The function shall extract the 13 APS bits K1[1-8] and K2[1-5] from the MS1_AI_D signal. A new value shall be accepted when the value is identical for three consecutive frames. This value shall be output via MS1P_CI_APS. This process is required only for the protection section.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

aSSD ← AI_TSD

Defect Correlations: None.

Performance Monitoring: None.

6 STM-4 Regenerator Section Layer Functions

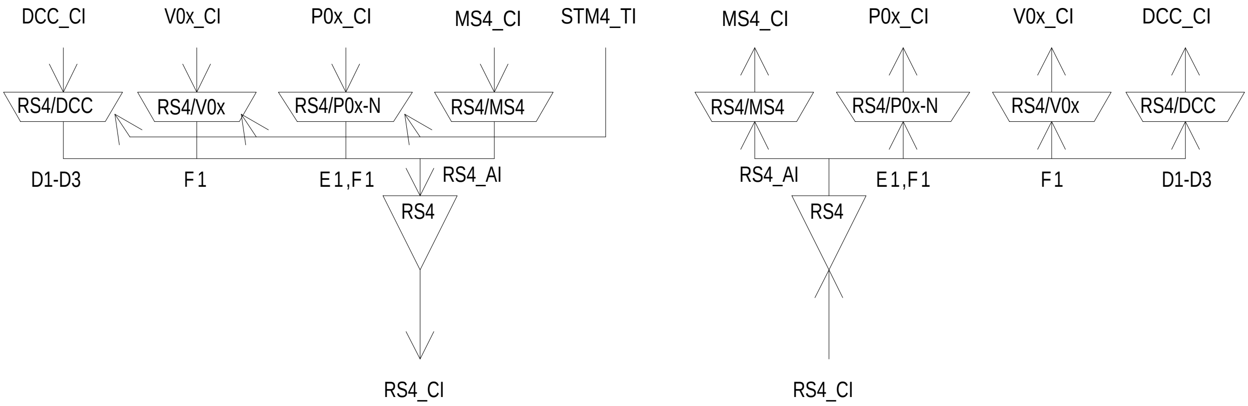


Figure 36: STM-4 Regenerator Section atomic functions

RS4 Layer CP.

The CI at this point is an octet structured, 125 µs framed data stream with co-directional timing. It is the entire STM-4 signal as defined in ETS 300 147 [2]. Figure 37 depicts only bytes handled in the RS4 layer.

NOTE 1: The unmarked bytes [2,2] to [2,12], [2,14] to [2,24], [3,2] to [3,12], [3,14] to [3,24], and [3,26] to [3,36] in rows 2,3 (figure 37) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The bytes for National Use (NU) in rows 1,2 (figure 37) are reserved for operator specific usage. Their processing is not within the province of this ETS. If NU bytes [1,29] to [1,36] are unused, care should be taken in selecting the binary content of the bytes which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of “1”s or “0”s do not occur.

NOTE 3: The bytes Z0 [1,26] to [1,28] are reserved for future international standardisation. Currently, they are undefined Care should be taken in selecting the binary content of these bytes which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of “1”s or “0”s do not occur.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	1080
1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	J0	Z0	Z0	Z0	NU	NU	NU	NU	NU	NU	NU	NU		
2	B1												E1												F1	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU		
3	D1												D2												D3													
4																																						
5																																						
6																											MS4_CI											
7																																						
8																																						
9																																						

Figure 37: RS4_CI_D signal

RS4 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing and represents the combination of adapted information from the MS4 layer (9612 bytes per frame), the management communication DCC layer (3 bytes per frame if supported), the OW layer (1 byte per frame if supported) and the user channel F1 (1 byte per frame if supported). The location of these four components in the frame is defined in ETS 300 147 [2] and depicted in figure 38.

NOTE 4: Bytes E1, F1 and D1-D3 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

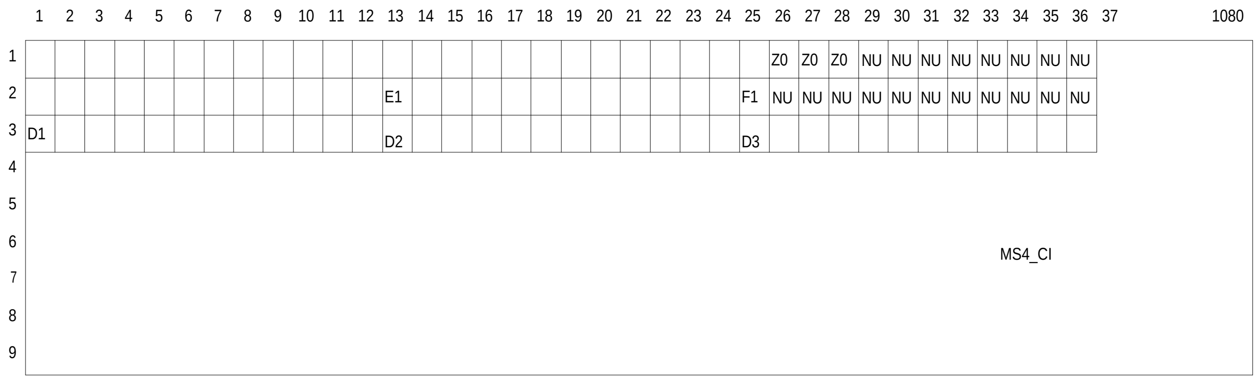


Figure 38: RS4_AI_D signal

6.1 STM-4 Regenerator Section Connection functions

For further study.

6.2 STM-4 Regenerator Section Trail Termination functions

6.2.1 STM-4 Regenerator Section Trail Termination Source RS4_TT_So

Symbol:

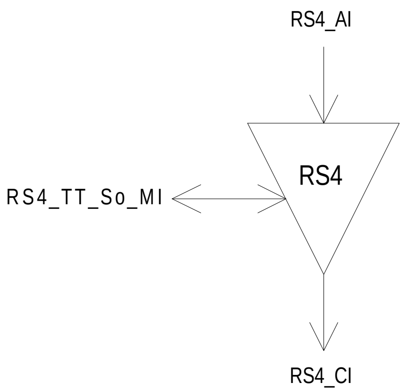


Figure 39: RS4_TT_So symbol

Interfaces:

Table 28: RS4_TT_So input and output signals

Input(s)	Output(s)
RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_TT_So_MI_TxTI	RS4_CI_D RS4_CI_CK RS4_CI_FS

Processes:

The function builds the STM-4 signal by adding the frame alignment information, bytes A1A2, the STM Section Trace Identifier (STI) byte J0, computing the parity and inserting the B1 byte.

J0: In this byte the function shall insert the Transmitted Trail Trace Identifier TxTI. Its format is described in ETS 300 417-1-1 [1], subclause 7.1.

B1: The function shall calculate a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 shall be calculated over all bits of the previous STM-4 frame after scrambling and is placed in byte position B1 of the current STM-4 frame before scrambling (figure 40).

A1A2: The function shall insert the STM-4 frame alignment signal A1...A1A2...A2 into the regenerator section overhead as defined in ETS 300 147 [2] and depicted in figure 37.

Scrambler: This function provides scrambling of the RS4_CI. The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate. The generating polynomial shall be $1+X^6+X^7$. The scrambler shall be reset to '1111 1111' on the most significant bit (MSB) of the byte (1,37) following the last byte of the STM-4 SOH in the first row. This bit and all subsequent bits to be scrambled shall be modulo 2 added to the output of the X^7 position of the scrambler. The scrambler shall run continuously throughout the remaining STM-4 frame.

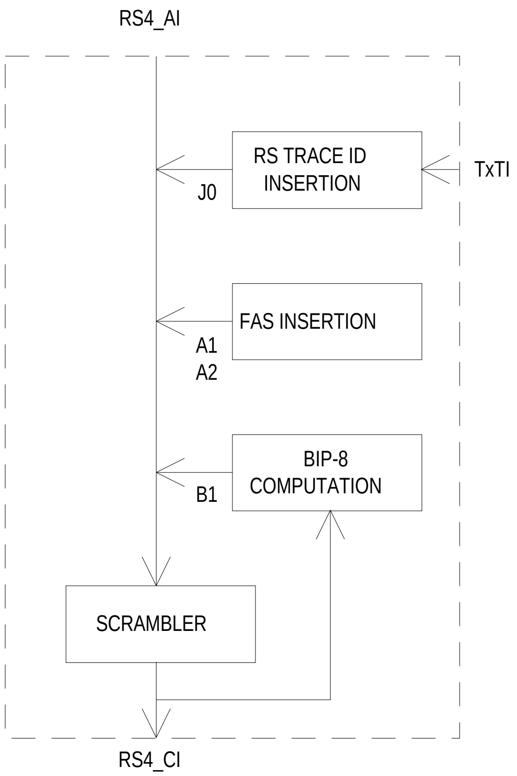


Figure 40: Some processes within RS4_TT_So

NOTE: The insertion of the frame alignment signal (A1A2) and the scrambling of the signal would be OS4/RS4_A_So processes according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-4 signal causes a violation of this process allocation, hence the frame alignment insertion and scrambling processes are located in the RS4_TT_So function.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

6.2.2 STM-4 Regenerator Section Trail Termination Sink RS4_TT_Sk

Symbol:

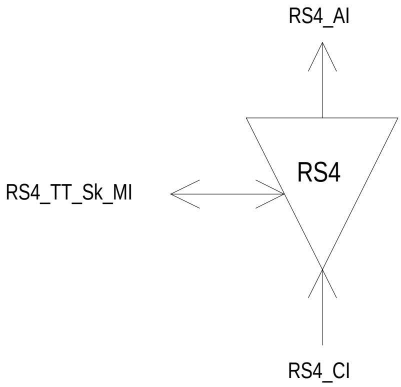


Figure 41: RS4_TT_Sk symbol

Interfaces:

Table 29: RS4_TT_Sk input and output signals

Input(s)	Output(s)
RS4_CI_D RS4_CI_CK RS4_CI_FS RS4_CI_SSF RS4_TT_Sk_MI_ExTI RS4_TT_Sk_MI_TPmode RS4_TT_Sk_MI_TIMdis RS4_TT_Sk_MI_ExTImode RS4_TT_Sk_MI_1second	RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_AI_TSF RS4_TT_Sk_MI_AcTI RS4_TT_Sk_MI_cTIM RS4_TT_Sk_MI_pN_EBC RS4_TT_Sk_MI_pN_DS

Processes:

This function monitors the STM-4 signal for RS errors, and recovers the RS trail termination status. It extracts the payload independent overhead bytes (J0, B1) from the RS4 layer Characteristic Information:

Descrambling: The function shall descramble the incoming STM-4 signal. The operation of the descrambler shall be functionally identical to that of a scrambler in OS4/RS4_A_So.

NOTE 1: The descrambling of the signal would be an OS/RS_A_Sk or ES/RS_A_Sk process according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-4 signal causes a violation of this process allocation, hence the descrambling process is located in the RS4_TT_Sk function.

B1: Even bit parity is computed for each bit n of every byte of the preceding scrambled STM-4 frame and compared with bit n of B1 recovered from the current frame (n=1 to 8 inclusive) (figure 42). A difference between the computed and recovered B1 values is taken as evidence of one or more errors (nN_B) in the computation block.

J0: The Received Trail Trace Identifier RxTI shall be recovered from the J0 byte and shall be made available as AcTI for network management purposes. The application and acceptance and mismatch detection process shall be performed as specified in ETS 300 417-1-1 [1], subclauses 7.1, and 8.2.1.3.

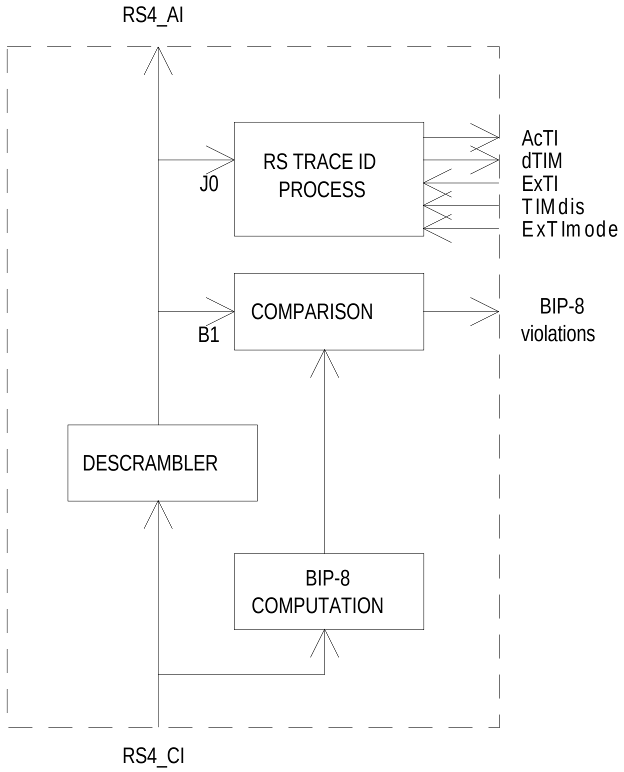


Figure 42: Some processes within RS4_TT_Sk

Defects:

The function shall detect for dTIM defects according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

Consequent Actions:

aAIS ← CI_SSF or dTIM

aTSF ← CI_SSF or dTIM

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 2: The term “CI_SSF” has been added to the conditions for aAIS while the descrambler function has been moved from the e.g. OS4/RS4_A_Sk to this function. Consequently, an all-ONEs (AIS) pattern inserted in the mentioned adaptation function would be descrambled in this function. A “refreshment” of all-ONEs is required.

Defect Correlations:

cTIM ← MON and dTIM

Performance Monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← aTSF or dEQ

pN_EBC ← Σ nN_B

6.3 STM-4 Regenerator Section Adaptation functions

6.3.1 STM-4 Regenerator Section to Multiplex Section Adaptation Source RS4/MS4_A_So

Symbol:

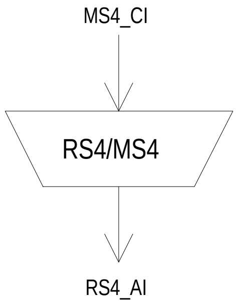


Figure 43: RS4/MS4_A_So symbol

Interfaces:

Table 30: RS4/MS4_A_So input and output signals

Input(s)	Output(s)
MS4_CI_D MS4_CI_CK MS4_CI_FS MS4_CI_SSF	RS4_AI_D RS4_AI_CK RS4_AI_FS

Processes:

The function multiplexes the MS4_CI data (9 612 bytes/frame) into the STM-4 byte locations defined in ETS 300 147 [2] and depicted in figure 37.

NOTE 1: There might be cases in which the network element knows that the timing reference for a particular STM-4 interface can not be maintained within ± 4.6 ppm. For such cases MS-AIS can be generated. This is network element specific and outside the scope of this ETS.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output all ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs. The frequency of the all ONEs signal shall be within 622,080 kHz ± 20 ppm.

NOTE 2: if CI_SSF is not connected (when RS4/MS4_A_So is connected to a MS4_TT_So), SSF is assumed to be false.

Defect Correlations: None.

Performance Monitoring: None.

6.3.2 STM-4 Regenerator Section to Multiplex Section Adaptation Sink RS4/MS4_A_Sk

Symbol:

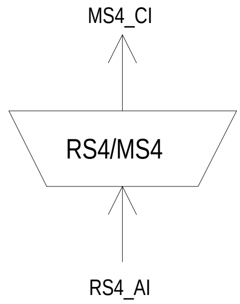


Figure 44: RS4/MS4_A_Sk symbol

Interfaces:

Table 31: RS4/MS4_A_Sk input and output signals

Input(s)	Output(s)
RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_AI_TSF	MS4_CI_D MS4_CI_CK MS4_CI_FS MS4_CI_SSF

Processes:

The function separates MS4_CI data from RS4_AI as depicted in figure 37.

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

6.3.3 STM-4 Regenerator Section to DCC Adaptation Source RS4/DCC_A_So

Symbol:

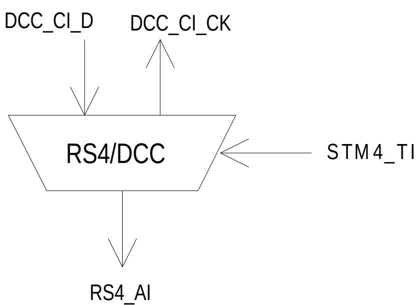


Figure 45: RS4/DCC_A_So symbol

Interfaces:

Table 32: RS4/DCC_A_So input and output signals

Input(s)	Output(s)
DCC_CI_D STM4_TI_CK STM4_TI_FS	RS4_AI_D DCC_CI_CK

Processes:

The function multiplexes the DCC CI data (192 kbit/s) into the byte locations D1, D2 and D3 as defined in ETS 300 147 [2] and depicted in figure 38 [8].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

6.3.4 STM-4 Regenerator Section to DCC Adaptation Sink RS4/DCC_A_Sk

Symbol:

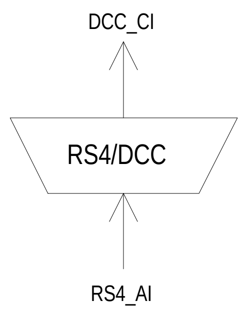


Figure 46: RS4/DCC_A_Sk symbol

Interfaces:

Table 33: RS4/DCC_A_Sk input and output signals

Input(s)	Output(s)
RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_AI_TSF	DCC_CI_D DCC_CI_CK DCC_CI_SSF

Processes:

The function separates DCC data from RS Overhead as defined in ETS 300 147 [2] and depicted in figure 38 [9].

Defects: None.

---

8 DCC transmission can be “disabled” when the matrix connection in the connected DCC_C function is removed.
9 DCC processing can be “disabled” when the matrix connection in the connected DCC_C function is removed.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

6.3.5 STM-4 Regenerator Section to P0x Adaptation Source RS4/P0x_A_So/N

Symbol:

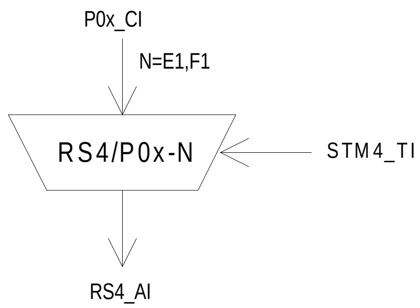


Figure 47: RS4/P0x_A_So symbol

Interfaces:

Table 34: RS4/P0x_A_So input and output signals

Input(s)	Output(s)
P0x_CI_D P0x_CI_CK P0x_CI_FS STM4_TI_CK STM4_TI_FS	RS4_AI_D

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire or user channel information stream into the RS4_AI using slip buffering. It takes P0x_CI, defined in ETS 300 166 [3] as an octet structured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the RSOH byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 38.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-4 clock, frame position (STM4_TI), and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

64 kbit/s timeslot: The adaptation source function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

6.3.6 STM-4 Regenerator Section to P0x Adaptation Sink RS4/P0x_A_Sk/N

Symbol:

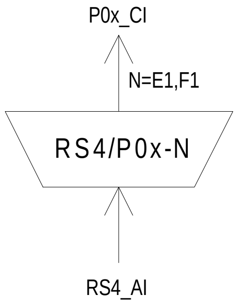


Figure 48: RS4/P0x_A_Sk symbol

Interfaces:

Table 35: RS4/P0x_A_Sk input and output signals

Input(s)	Output(s)
RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_AI_TSF	P0x_CI_Sk_D P0x_CI_Sk_CK P0x_CI_FS P0x_CI_SSF

Processes:

The function separates P0x data from RS Overhead byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 38.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-4 signal generated at the remote node containing RS4/P0x_A_So). The residual jitter caused by pointer adjustments and octet slips (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 20 ppm, this smoothing process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the RS4_AI (for example due to a frequency step of the server STM-4 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

64 kbit/s timeslot: The adaptation sink function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

6.3.7 STM-4 Regenerator Section to V0x Adaptation Source RS4/V0x_A_So

Symbol:

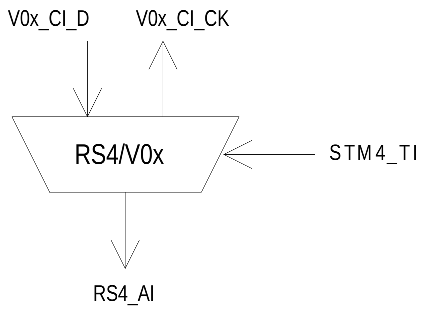


Figure 49: RS4/V0x_A_So symbol

Interfaces:

Table 36: RS4/V0x_A_So input and output signals

Input(s)	Output(s)
V0x_CI_D STM4_TI_CK STM4_TI_FS	RS4_AI_D V0x_CI_CK

Processes: None.

This function multiplexes the V0x_CI data (64 kbit/s) into the byte location F1 as defined in ETS 300 147 [2] and depicted in figure 38.

The user channel byte F1 shall be added to the 125 µs frame.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

6.3.8 STM-4 Regenerator Section to V0x Adaptation Sink RS4/V0x_A_Sk

Symbol:

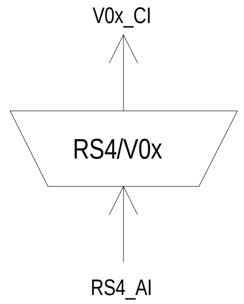


Figure 50: RS4/V0x_A_Sk symbol

Interfaces:

Table 37: RS4/V0x_A_Sk input and output signals

Input(s)	Output(s)
RS4_AI_D RS4_AI_CK RS4_AI_FS RS4_AI_TSF	V0x_CI_D V0x_CI_CK V0x_CI_SSF

Processes:

This function separates user channel data from RS Overhead (byte F1) as defined in ETS 300 147 [2] and depicted in figure 38.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± TBD ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

7 STM-4 Multiplex Section layer functions

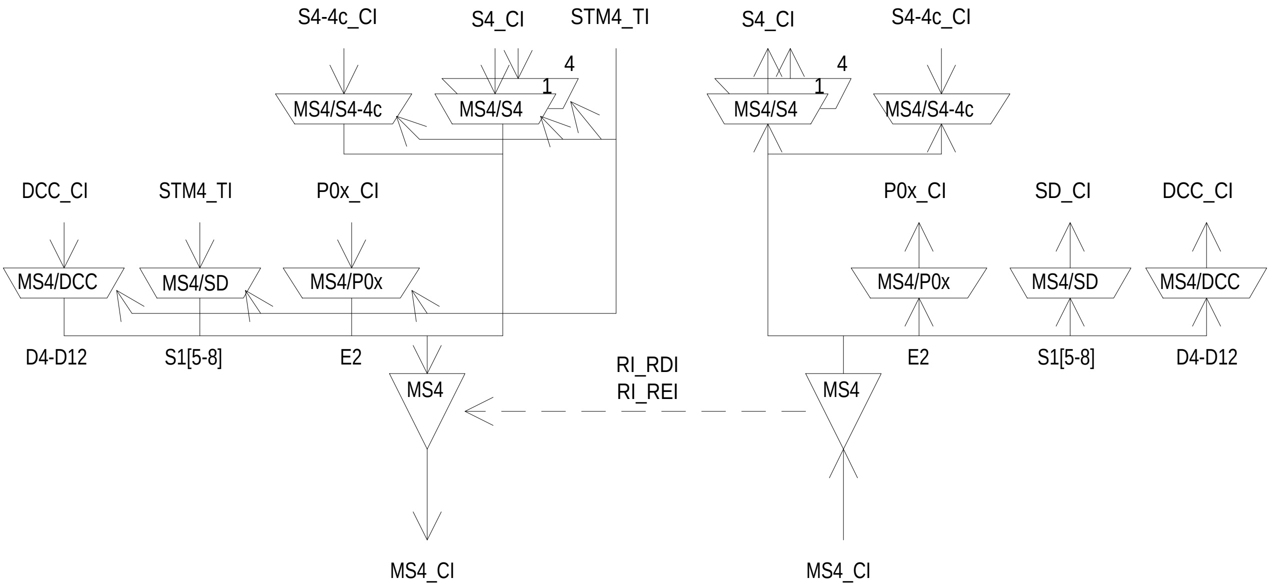


Figure 51: STM-4 Multiplex Section atomic functions

MS4 Layer CP.

The CI at this point is octet structured and 125 µs framed with co-directional timing. Its format is characterised as the MS4_AI with an additional MS Trail Termination overhead in the twelve B2 bytes, byte M1, and bits 6-8 of the K2 byte in the frame locations defined in ETS 300 147 [2] and depicted in figure 52.

NOTE 1: The unmarked bytes in rows 5,6,7,8,9 (figure 52) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The bytes for National Use (NU) in row 9 (figure 52) are reserved for operator specific usage. Their processing is not within the province of this ETS.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37 – 1080
1																																					
2																																					
3																																					
4	H1	H1	H1	H1	Y	Y	Y	Y	Y	Y	Y	Y	H2	H2	H2	H2	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	STM-4 payload (4 x 261 x 9 bytes)
5	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	K1												K2												
6	D4												D5												D6												
7	D7												D8												D9												
8	D10												D11												D12												
9	S1														M1										E2	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	

Figure 52: MS4_CI_D

MS4 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing. It represents the combination of information adapted from the VC-4 layer (150 336 kbit/s), the management communications DCC layer (576 kbit/s), the OW layer (64 kbit/s if supported), the AU-4 pointer (3 bytes per frame), the APS signalling channel (13 [10] or 16 [11] bits per frame if supported), and the Synchronisation Status Message channel (4 bits per frame if supported). The location of these five components in the frame is defined in ETS 300 147 [2] and depicted in figure 53.

NOTE 3: Bytes E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

The composition of the payload transported by an STM-4 will be determined by the client layer application. Typical compositions of the payload include:

- one VC-4-4c of 601 344 kbit/s;
- four VC-4s of 150 336 kbit/s.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37-48	49	1080
1																																							
2																																							
3																																							
4	H1	H1	H1	H1	Y	Y	Y	Y	Y	Y	Y	Y	H2	H2	H2	H2	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3+1		
5													K1												K2													STM-4 payload (4 x 261 x 9 bytes)	
6	D4												D5												D6														
7	D7												D8												D9														
8	D10												D11												D12														
9	S1																								E2	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU			

Figure 53: MS4_AI_D

Figure 54 shows the MS trail protection specific sublayer atomic functions (MS4/MS4P_A, MS4P_C, MS4P_TT) within the MS4 layer. Note that the DCC (D4-D12), OW (E2) , and SSM (S1[5-8]) signals can be accessible before (unprotected) and after (protected) the MS4P_C function. The choice is outside the scope of this ETS.

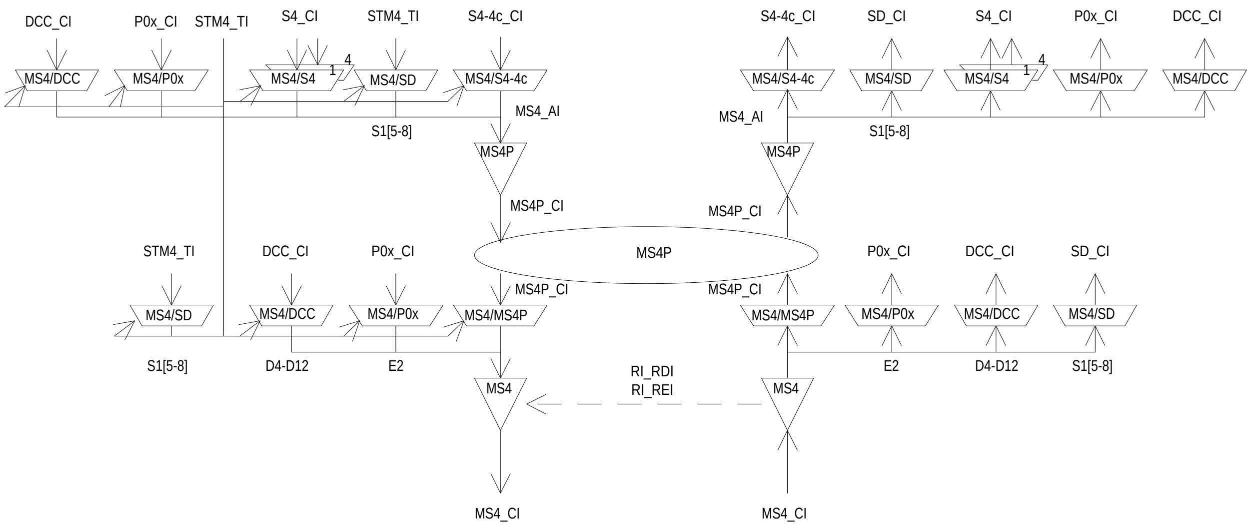


Figure 54: STM-4 Multiplex Section Linear Trail Protection Functions

10 13 bits APS channel for the case of linear MS protection
11 16 bits APS channel for the case of MS SPRING protection

MS4P Sublayer CP.

The CI at this point is octet structured and 125 µs framed with co-directional timing. Its format is equivalent to the MS4_AI and depicted in figure 55.

NOTE 4: Bytes S1, E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element or are unprotected (see above).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37 1080
1																																					
2																																					
3																																					
4	H1	H1	H1	H1	Y	Y	Y	Y	Y	Y	Y	Y	H2	H2	H2	H2	'1'	'1'	'1'	'1'	'1'	'1'	'1'	'1'	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	STM-4 payload (4 x 261 x 9 bytes)
5													K1												K2												
6	D4												D5												D6												
7	D7												D8												D9												
8	D10												D11												D12												
9	S1																								E2	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	

Figure 55: MS4P_CI_D

7.1 STM-4 Multiplex Section Connection functions

For further study.

7.2 STM-4 Multiplex Section Trail Termination functions

7.2.1 STM-4 Multiplex Section Trail Termination Source MS4_TT_So

Symbol:

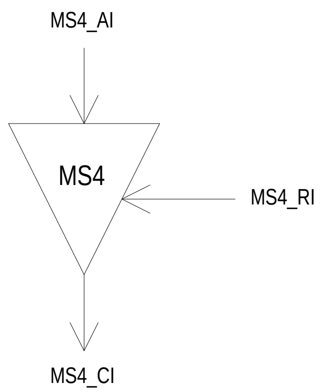


Figure 56: MS4_TT_So symbol

Interfaces:

Table 38: MS4_TT_So input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_RI_REI MS4_RI_RDI	MS4_CI_D MS4_CI_CK MS4_CI_FS

Processes:

This function adds error monitoring capabilities and remote maintenance information signals to the MS4_AI.

M1: The function shall set the REI (Remote Error Indication) to one of the codes in table 39 if one or more errored blocks were detected by the BIP-96 process in MS4_TT_Sk (communicated via MS4_RI_REI), and shall set REI to ”0000 0000” otherwise.

Table 39: M1 code generation

Number of errored blocks	M1code, bits 1234 5678
0 errored blocks	0000 0000
1 errored block	0000 0001
2 errored blocks	0000 0010
3 errored blocks	0000 0011
4 errored blocks	0000 0100

NOTE 1: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8]: These bits represents the defect status of the associated MS4_TT_Sk. The RDI indication shall be set to "110" on activation of MS4_RI_RDI within 250 µs, determined by the associated MS4_TT_Sk function, and passed through transparently (except for incoming codes "111" and "110") within 250 µs on the MS4_RI_RDI removal. If MS4_RI_RDI is inactive an incoming codes "111" or "110" shall be replaced by code "000".

NOTE 2: K2[6-8] can not be set to "000" on clearing of RI_RDI; MS SPRING APS extends into those bits. The bits must be passed transparently in this case. With linear MS protection or without protection it must be guaranteed that neither code "111" nor "110" will be output.

B2: The function shall calculate a Bit Interleaved Parity 96 (BIP-96) code using even parity. The BIP-96 shall be calculated over all bits, except those in the RSOH bytes, of the previous STM-4 frame and placed in twelve B2 bytes of the current STM-4 frame [12].

Defects: None.

Consequent Actions:

On declaration of RI_RDI the function shall output RDI (pattern '110' in bit 6,7, and 8 of byte K2) within 250 µs; on clearing of RI_RDI the function shall output normal data within 250 µs.

Defect Correlations: None.

Performance Monitoring: None.

---

12 The BIP-96 procedure is described in ETS 300 147.

7.2.2 STM-4 Multiplex Section Trail Termination Sink MS4_TT_Sk

Symbol:

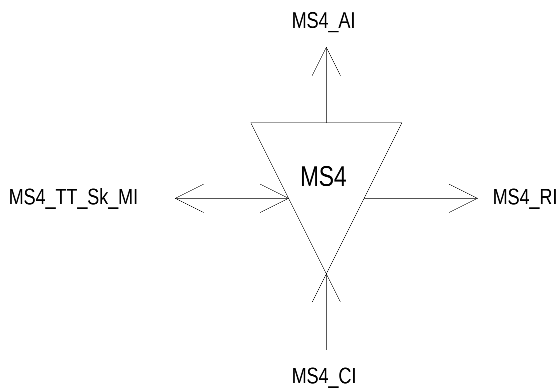


Figure 57: MS4_TT_Sk symbol

Interfaces:

Table 40: MS4_TT_Sk input and output signals

Input(s)	Output(s)
MS4_CI_D MS4_CI_CK MS4_CI_FS MS4_CI_SSF MS4_TT_Sk_DEGTHR MS4_TT_Sk_DEGM MS4_TT_Sk_1second MS4_TT_Sk_MI_TPmode MS4_TT_Sk_MI_SSF_Reported MS4_TT_Sk_MI_AIS_Reported MS4_TT_Sk_MI_RDI_Reported	MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_CI_TSF MS4_TT_Sk_MI_cAIS MS4_TT_Sk_MI_cDEG MS4_TT_Sk_MI_cRDI MS4_TT_Sk_MI_cSSF MS4_TT_Sk_MI_pN_EBC MS4_TT_Sk_MI_pF_EBC MS4_TT_Sk_MI_pN_DS MS4_TT_Sk_MI_pF_DS MS4_RI_REI MS4_RI_RDI

Processes:

This function monitors error performance of associated MS4 including the far end receiver.

B2: The BIP-96 is organised as four times BIP-24 as specified in ITU-T Recommendation G.707 [4]. It shall be calculated over all bits, except of those in the RSOH bytes, of the previous STM-4 frame and compared with the four times BIP-24 value (bytes B2) recovered from the MSOH of the current STM-4 frame. For each BIP-24 a difference between the computed BIP-24 and recovered BIP-24 value in the B2 bytes shall be taken as evidence of one or more errors in the computation BIP-24 block. The number of errored blocks (nN_B) in the BIP-96 shall be calculated by adding the total number of BIP-24 errored blocks.

M1: The REI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The REI is used to monitor the error performance of the other direction of transmission. The application process is described in ETS 300 417-1-1 [1], subclause 7.4.2 (REI).

The function shall interprete the code, to allow interworking with old equipment generating a code that represents the number of BIP-96 violations.

Table 41

M1[2-8] code, bits 234 5678	**code interpretation (nF_B)**
000 0000	0 errored blocks
000 0001	1 errored block
000 0010	2 errored blocks
000 0011	3 errored blocks
000 0100	4 errored blocks
000 0101	4 errored blocks
⋮	⋮
110 0000	4 errored blocks
110 0001	0 errored blocks
110 0010	0 errored blocks
⋮	⋮
111 1111	0 errored blocks

NOTE 1: bit 1 of byte M1 is ignored.

NOTE 2: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8] - RDI: The RDI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The RDI provides information as to the status of the remote receiver. A "110" indicates a Remote Defect Indication state, while other patterns indicate the normal state. The application process is described in ETS 300 417-1-1 [1], subclauses 7.4.11 and 8.2.

K2[6-8] - AIS: The MS-AIS information carried in these bits shall be extracted.

Defects:

The function shall detect for dDEG and dRDI defects according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

dAIS: If at least ***x*** consecutive frames contain the '111' pattern in bits 6, 7 and 8 of the K2 byte a dAIS defect shall be detected. dAIS shall be cleared if in at least ***x*** consecutive frames any pattern other then the '111' is detected in bits 6, 7 and 8 of byte K2. The ***x*** shall be in range 3 to 5.

Consequent Actions:

aAIS ← dAIS

aRDI ← dAIS

aTSF ← dAIS

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

Defect Correlations:

cAIS ← MON and dAIS and (not CI_SSF) and AIS_Reported

cDEG ← MON and dDEG

cRDI ← MON and dRDI and RDI_Reported

cSSF ← MON and dAIS and SSF_Reported

Performance monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← aTSF or dEQ

pF_DS ← dRDI

pN_EBC ← Σ nN_B

pF_EBC ← Σ nF_B

7.3 STM-4 Multiplex Section Adaptation functions

7.3.1 STM-4 Multiplex Section to S4 Layer Adaptation Source MS4/S4_A_So/N

Symbol:

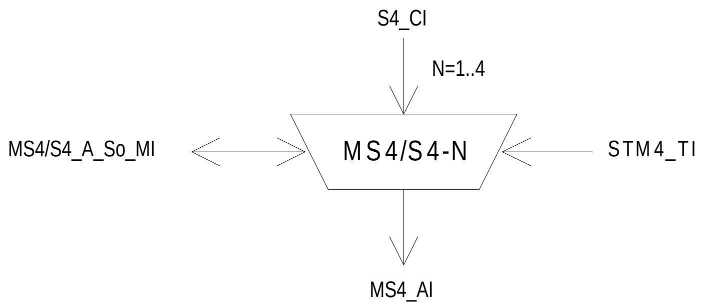


Figure 58: MS4/S4_A_So symbol

Interfaces:

Table 42: MS4/S4_A_So input and output signals

Input(s)	Output(s)
S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF STM4_TI_CK STM4_TI_FS MS4/S4_A_So_MI_Active	MS4_AI_D MS4_AI_CK MS4_AI_FS MS4/S4_A_So_MI_pPJE+ MS4/S4_A_So_MI_pPJE-

Processes:

This function provides frequency justification and bitrate adaptation for a VC-4 signal, represented by a nominally (261*9*64) = 150 336 kbit/s information stream and the related frame phase with a frequency accuracy within ± 4.6 ppm, to be multiplexed into a STM-4 signal at the AU tributary location indicated by MI_AUnum. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

The frame phase of the VC-4 is coded in the related AU-4 pointer. Frequency justification, if required, is performed by pointer adjustments. The accuracy of this coding process is specified below. Refer to prETS 300 417-4-1 [7], annex A.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (buffer) process. The data and frame start signals shall be written into the buffer under control of the associated input clock. The data and frame start signals shall be read out of the buffer under control of the STM-4 clock, frame position, and justification decision.

The justification decisions determine the phase error introduced by the MS4/S4_A_So function. The amount of this phase error can be measured at the physical interfaces by monitoring the AU-4 pointer actions. An example is given in prETS 300 417-4-1 [7], annex A.2.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of 24 data bits shall be cancelled once and no data written at the three positions H3+1. Upon a negative justification action, an extra 24 data bits shall be read out once into the three positions H3.

NOTE 1: A requirement for maximum introduced phase error cannot be defined until a reference path is defined from which the requirements for network elements can be deduced. Such a requirement would also limit excessive phase error caused by pointer processors under fixed frequency offset conditions.

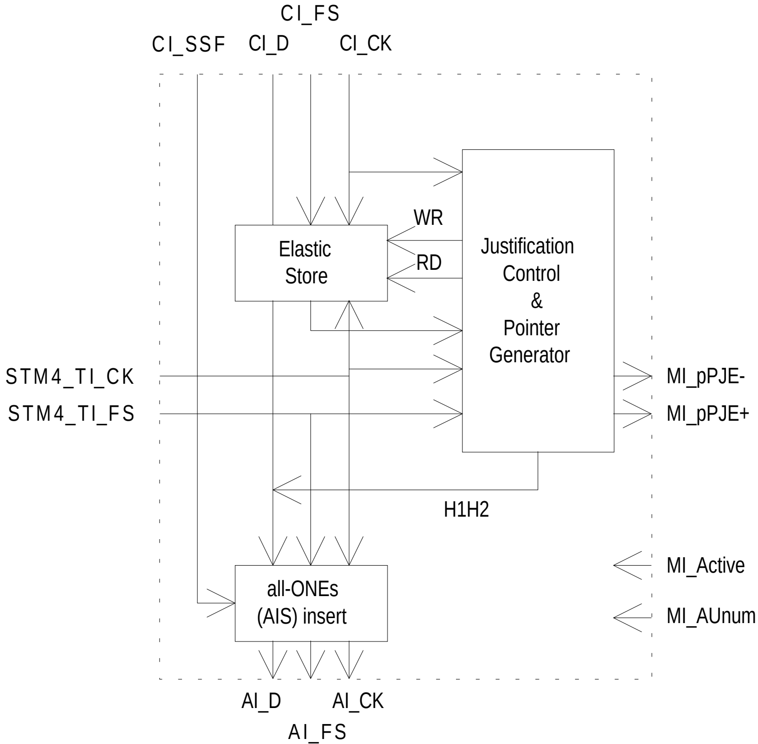


Figure 59: main processes within MS4/S4_A_So

Buffer size: For further study.

Behaviour at recovery from defect condition: The incoming frequency (S4_CI_CK) of a passing through VC-4 may exceed its limits during a STM4dLOS condition. As a consequence, the buffer (elastic store) fill is not reliable any more. Due to all-ONEs (AIS) insertion after the pointer generator this reliability is not important for the operation of the network element. However, it shall be prevent to generate excessive pointer adjustments when recovering from the defect condition.

NOTE 2: The definition of excessive pointer adjustments is for further study.

The AU-4 pointer is carried in 2 bytes of payload specific OH in each STM-4 frame. The AU-4 pointer is aligned in the STM-4 payload in fixed position relative to the STM-4 frame. The AU-4 pointer points to the begin of the VC-4 frame within the STM-4. The format of the AU-4 pointer and its location in the frame are defined in ETS 300 147 [2].

H1H2 - *Pointer generation:* The function shall generate the AU-4 pointer as is described in ETS 300 417-1-1 [1], annex A: Pointer Generation. It shall insert the pointer in the appropriate H1, H2 positions with the SS field set to 10 to indicate AU-4.

YY1*1* - *Fixed stuff insertion:* The function shall insert fixed stuff codes Y = 1001ss11 in bytes [4,4+AUnum] and [4,8+AUnum] and code '1' = 11111111 in bytes [4,16+AUnum] and [4,20+AUnum]. Bits ss are undefined.

AU-4 timeslot: The adaptation source function has access to a specific AU-4 of the MS4 access point. The AU-4 is defined by the parameter N (N=1..4).

Figure 51 shows that more than one adaptation source function exists in the MS4 layer that can be connected to one MS4 access point. For such case, a subset of these adaptation source functions is allowed to be activated together, but only one adaptation source function may have access to a specific AU timeslot. Access to the same AU timeslot by other adaptation source functions must be denied.

Activation: The function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 3: if CI_SSF is not connected (when MS4/S4_A_So is connected to a S4_TT_So), CI_SSF is assumed to be false.

Defect Correlations: None

Performance Monitoring:

Every second the number of generated pointer increments within that second shall be counted as the pPJE+. Every second the number of generated pointer decrements within that second shall be counted as the pPJE-.

NOTE 4: This is applicable for a passing through VC-4 only. A locally generated VC-4 may have a fixed frame phase; pointer justifications will not occur.

7.3.2 STM-4 Multiplex Section to S4 Layer Adaptation Sink MS4/S4_A_Sk/N

Symbol:

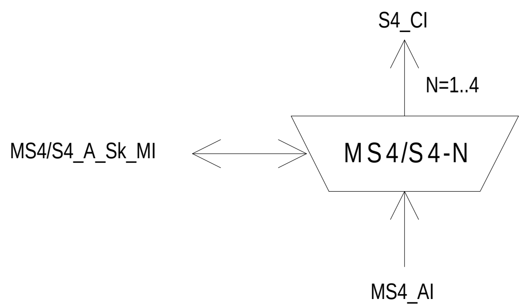


Figure 60: MS4/S4_A_Sk symbol

Interfaces:

Table 43: MS4/S4_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF MS4/S4_A_Sk_MI_Active MS4/S4_A_Sk_MI_AIS_Reported	S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF MS4/S4_A_Sk_MI_cAIS MS4/S4_A_Sk_MI_cLOP

Processes:

This function recovers the VC-4 data with frame phase information from the STM-4 as defined in ETS 300 147 [2]. The VC-4 is extracted from the AU tributary location indicated by MI_AUnum. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

H1H2 - *AU-4 pointer interpretation:* The function shall perform AU-4 pointer interpretation according to annex B of ETS 300 417-1-1 [1] to recover the VC-4 frame phase within the STM-4. The process shall maintain its current phase on detection of an invalid pointer and searches in parallel for a new phase.

YY1*1*: An AU-4 pointer consists of 2 bytes, [4,AUnum] and [4,12+AUnum]. The bytes [4,4+AUnum], [4,8+AUnum], [4,16+AUnum], and [4,20+AUnum] contain fixed stuff, of a specified value, ignored by the AU-4 pointer interpreter.

AU-4 timeslot: The adaptation sink function has access to a specific AU-4 of the MS4 access point. The AU-4 is defined by the parameter N (N=1..4).

Figure 51 shows that more than one adaptation sink function exists in this MS4 layer that can be connected to one MS4 access point. In contradiction with the source direction, adaptation sink functions may be activated all together. Faults (e.g. cLOP) may be detected and reported. To prevent this an adaptation sink function can be deactivated.

Activation: The function shall perform the operation specified above when it is activated (MI_Active is true). Otherwise, it shall transmit the all-ONEs signal at its output (CI_D) and not report its status via its management point.

Defects:

dAIS: The dAIS defect shall be detected if the pointer interpreter is in the AIS_state (refer to ETS 300 417-1-1 [1], annex B). The dAIS defect shall be cleared if the pointer interpreter is not in the AIS_state.

dLOP: The dLOP defect shall be detected if the pointer interpreter is in the LOP_state (refer to ETS 300 417-1-1 [1], annex B). The dLOP defect shall be cleared if the pointer interpreter is not in the LOP_state.

Consequent Actions:

aAIS ← dAIS or dLOP

aSSF ← dAIS or dLOP

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output the recovered data within 250 µs.

Defect Correlations:

cAIS ← dAIS and (not AI_TSF) and AIS_Reported

cLOP ← dLOP

Performance Monitoring: None.

7.3.3 STM-4 Multiplex Section to S4-4c Layer Adaptation Source MS4/S4-4c_A_So

Symbol:

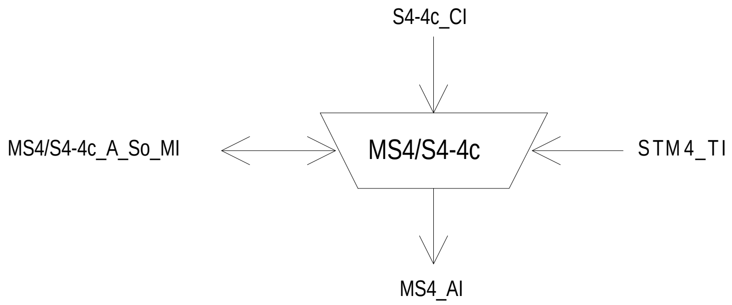


Figure 61: MS4/S4-4c_A_So symbol

Interfaces:

Table 44: MS4/S4-4c_A_So input and output signals

Input(s)	Output(s)
S4-4c_CI_D S4-4c_CI_CK S4-4c_CI_FS S4-4c_CI_SSF STM4_TI_CK STM4_TI_FS MS4/S4-4c_A_So_MI_Active	MS4_AI_D MS4_AI_CK MS4_AI_FS MS4/S4-4c_A_So_MI_pPJE+ MS4/S4-4c_A_So_MI_pPJE-

Processes:

This function provides frequency justification and bitrate adaptation for a VC-4-4c signal, represented by a nominally (4 x 261*9*64) = 601 344 kbit/s information stream and the related frame phase with a frequency accuracy within ± 4.6 ppm, to be multiplexed into a STM-4 signal. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

The frame phase of the VC-4-4c is coded in the related AU-4-4c pointer. Frequency justification, if required, is performed by pointer adjustments. The accuracy of this coding process is specified below. Refer to prETS 300 417-4-1 [7], annex A.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (buffer) process. The data and frame start signals shall be written into the buffer under control of the associated input clock. The data and frame start signals shall be read out of the buffer under control of the STM-4 clock, frame position, and justification decision.

The justification decisions determine the phase error introduced by the MS4/S4-4c_A_So function. The amount of this phase error can be measured at the physical interfaces by monitoring the AU-4-4c pointer actions. An example is given in prETS 300 417-4-1 [7], annex A.2.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of 96 data bits shall be cancelled once and no data written at the twelve positions H3+1. Upon a negative justification action, an extra 96 data bits shall be read out once into the twelve positions H3.

NOTE 1: A requirement for maximum introduced phase error cannot be defined until a reference path is defined from which the requirements for network elements can be deduced. Such a requirement would also limit excessive phase error caused by pointer processors under fixed frequency offset conditions.

Buffer size: For further study.

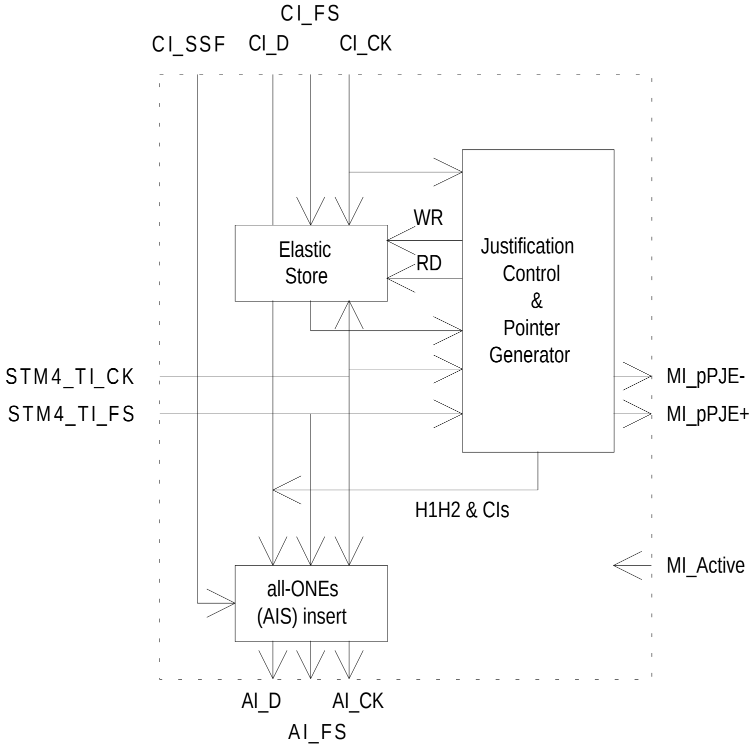


Figure 62: main processes within MS4/S4-4c_A_So

Behaviour at recovery from defect condition: The incoming frequency (S4-4c_CI_CK) of a passing through VC-4-4c may exceed its limits during a STM4dLOS condition. As a consequence, the buffer (elastic store) fill is not reliable any more. Due to all-ONEs (AIS) insertion after the pointer generator this reliability is not important for the operation of the network element. However, it shall be prevent to generate excessive pointer adjustments when recovering from the defect condition.

NOTE 2: The definition of excessive pointer adjustments is for further study.

The AU-4-4c pointer is carried in 2+6 bytes of payload specific OH in each STM-4 frame. The AU-4-4c pointer is aligned in the STM-4 payload in fixed position relative to the STM-4 frame. The AU-4-4c pointer points to the begin of the VC-4-4c frame within the STM-4. The format of the AU-4-4c pointer and its location in the frame are defined in ETS 300 147 [2].

H1H2 - *Pointer generation:* The function shall generate the AU-4-4c pointer as is described in ETS 300 417-1-1 [1], annex A: Pointer Generation. It shall insert the pointer in the H1 [4,1], H2 [4,13] positions with the SS field set to 10 to indicate AU-3/AU-4/AU-4-4c. It shall insert the concatenation indicator in the other pointer locations H1 [4,2] to [4,4], H2 [4,14] to [4,16]. The concatenation indicator is defined as 1001ss11 11111111, with ss being undefined bits.

YY1*1* - *Fixed stuff insertion:* The function shall insert fixed stuff codes Y = 1001ss11 in bytes [4,5] to [4,12] and code '1' = 11111111 in bytes [4,17] to [4,24]. Bits ss are undefined.

Figure 51 shows that more than one adaptation source function exists in the MS4 layer that can be connected to one MS4 access point. For such case, a subset of these adaptation source functions is allowed to be activated together, but only one adaptation source function may have access to a specific AU timeslot. Access to the same AU timeslot by other adaptation source functions must be denied.

Activation: The function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 3: if CI_SSF is not connected (when MS4/S4-4c_A_So is connected to a S4-4c_TT_So), CI_SSF is assumed to be false.

Defect Correlations: None

Performance Monitoring:

Every second the number of generated pointer increments within that second shall be counted as the pPJE+. Every second the number of generated pointer decrements within that second shall be counted as the pPJE-.

NOTE 4: This is applicable for a passing through VC-4-4c only. A locally generated VC-4-4c may have a fixed frame phase; pointer justifications will not occur.

7.3.4 STM-4 Multiplex Section to S4-4c Layer Adaptation Sink MS4/S4-4c_A_Sk

Symbol:

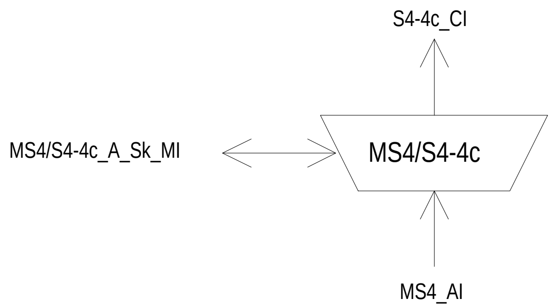


Figure 63: MS4/S4-4c_A_Sk symbol

Interfaces:

Table 45: MS4/S4-4c_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF MS4/S4-4c_A_Sk_MI_Active MS4/S4-4c_A_Sk_MI_AIS_Reported	S4-4c_CI_D S4-4c_CI_CK S4-4c_CI_FS S4-4c_CI_SSF MS4/S4-4c_A_Sk_MI_cAIS MS4/S4-4c_A_Sk_MI_cLOP

Processes:

This function recovers the VC-4-4c data with frame phase information from the STM-4 as defined in ETS 300 147 [2]. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

H1H2 - *AU-4-4c pointer interpretation:* The function shall perform AU-4-4c pointer interpretation according to annex B of ETS 300 417-1-1 [1] to recover the VC-4-4c frame phase within the STM-4. The process shall maintain its current phase on detection of an invalid pointer and searches in parallel for a new phase.

YY1*1*: An AU-4-4c pointer consists of 2 bytes, [4,1] and [4,13]. There will be 3 concatenation indicators, each 2 bytes long, in [4,2]/[4,14], [4,3]/[4,15], and [4,4]/[4,16]. The bytes [4,5] to [4,12] and [4,17] to [4,24] contain fixed stuff, of a specified value, ignored by the AU-4-4c pointer interpreter.

Figure 51 shows that more than one adaptation sink function exists in this MS4 layer that can be connected to one MS4 access point. In contradiction with the source direction, adaptation sink functions may be activated all together. Faults (e.g. cLOP) may be detected and reported. To prevent this an adaptation sink function can be deactivated.

Activation: The function shall perform the operation specified above when it is activated (MI_Active is true). Otherwise, it shall transmit the all-ONEs signal at its output (CI_D) and not report its status via its management point.

Defects:

dAIS: The dAIS defect shall be detected if the pointer interpreter is in the AISX_state (refer to ETS 300 417-1-1 [1], annex B). The dAIS defect shall be cleared if the pointer interpreter is not in the AISX_state.

dLOP: The dLOP defect shall be detected if the pointer interpreter is in the LOPX_state (refer to ETS 300 417-1-1 [1], annex B). The dLOP defect shall be cleared if the pointer interpreter is not in the LOPX_state.

Consequent Actions:

aAIS ← dAIS or dLOP

aSSF ← dAIS or dLOP

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output the recovered data within 250 µs.

Defect Correlations:

cAIS ← dAIS and (not aTSF) and AIS_Reported

cLOP ← dLOP

Performance Monitoring: None.

7.3.5 STM-4 Multiplex Section to DCC Adaptation Source MS4/DCC_A_So

Symbol:

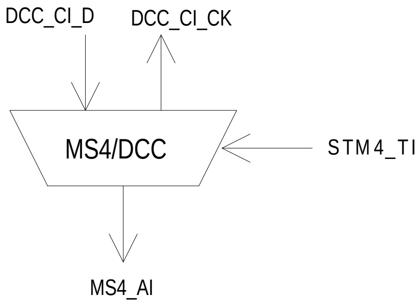


Figure 64: MS4/DCC_A_So symbol

Interfaces:

Table 46: MS4/DCC_A_So input and output signals

Input(s)	Output(s)
DCC_CI_D STM4_TI_CK STM4_TI_FS	MS4_AI_D DCC_CI_CK

Processes:

The function multiplexes the DCC CI data (576 kbit/s) into the byte locations D4 to D12 as defined in ETS 300 147 [2] and depicted in figure 53 [13].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

7.3.6 STM-4 Multiplex Section to DCC Adaptation Sink MS4/DCC_A_Sk

Symbol:

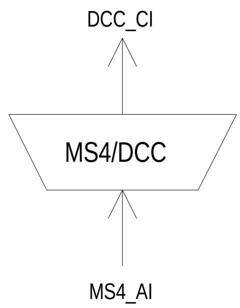


Figure 65: MS4/DCC_A_Sk symbol

---

13 DCC transmission can be "disabled" when the matrix connection in the connected DCC_C function is removed.

Interfaces:

Table 47: MS4/DCC_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF	DCC_CI_D DCC_CI_CK DCC_CI_SSF

Processes:

The function separates DCC data from MS Overhead as defined in ETS 300 147 [2] and depicted in figure 53 [14].

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

7.3.7 STM-4 Multiplex Section to P0x Adaptation Source MS4/P0x_A_So

Symbol:

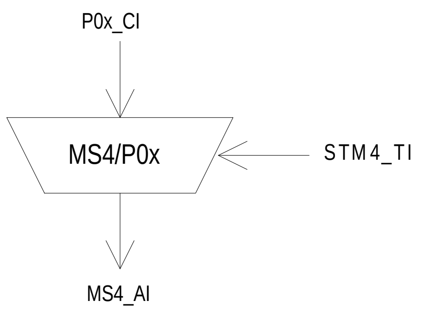


Figure 66: MS4/P0x_A_So symbol

Interfaces:

Table 48: MS4/P0x_A_So input and output signals

Input(s)	Output(s)
P0x_CI_D P0x_CI_CK P0x_CI_FS STM4_TI_CK STM4_TI_FS	MS4/P0x_AI_So_D

---

14 DCC processing can be “disabled” when the matrix connection in the connected DCC_C function is removed.

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire information stream into the MS4_AI using slip buffering. It takes P0x_CI, defined in ETS 300 166 [3] as an unstructured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the MSOH byte E2 as defined in ETS 300 147 [2] and depicted in figure 53.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-4 clock, frame position, and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification (slip) action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification (slip) action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

7.3.8 STM-4 Multiplex Section to P0x Adaptation Sink MS4/P0x_A_Sk

Symbol:

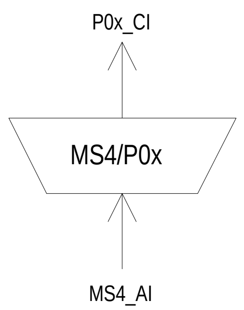


Figure 67: MS4/P0x_A_Sk symbol

Interfaces:

Table 49: MS4/P0x_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF	P0x_CI_Sk_D P0x_CI_Sk_CK P0x_CI_FS

Processes:

The function separates P0x data from MS Overhead byte E2 as defined in ETS 300 147 [2] and depicted in figure 53.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-4 signal generated at the remote node containing MS4/P0x_A_So). The residual jitter caused by pointer adjustments and octet slips (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 4.6 ppm, this justification process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the MS4_AI (for example due to a frequency step of the server STM-4 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

7.3.9 STM-4 Multiplex Section to Synchronisation Distribution Source MS4/SD_A_So

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

7.3.10 STM-4 Multiplex Section to Synchronisation Distribution Sink MS4/SD_A_Sk

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

7.4 STM-4 Multiplex Section Layer Monitoring Functions

For further study.

7.5 STM-4 Multiplex Section Linear Trail Protection Functions

7.5.1 STM-4 Multiplex Section Linear Trail Protection Connection Functions

7.5.1.1 STM-4 Multiplex Section 1+1 Linear Trail Protection Connection MS4P1+1_C

Symbol:

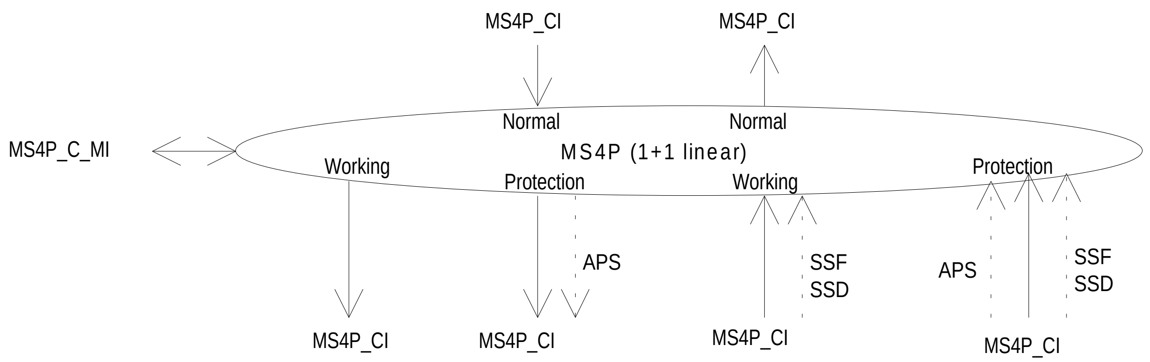


Figure 68: MS4P1+1_C symbol

Interfaces:

Table 50: MS4P1+1_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF MS4P_CI_SSD MS4P_C_MI_SFpriority MS4P_C_MI_SDpriority for connection points N and E: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS per function: MS4P_CI_APS MS4P_C_MI_SWtype MS4P_C_MI_OPERtype MS4P_C_MI_WTRTime MS4P_C_MI_HOTime MS4P_C_MI_EXTCMD	for connection points W and P: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF for connection points N and E: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF Note: protection status reporting signals are for further study. per function: MS4P_CI_APS MS4P_C_MI_cFOP MS4P_C_MI_pPSC

Processes:

The function performs the STM-4 linear multiplex section protection process for 1+1 protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 48 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #1 reference point can be the signal received via either the associated working #1 section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output is connected to the normal #1 input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 51

Architecture:	1 + 1
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1+1 switching, revertive operation) LO, FSw-#1, MSw-#1, CLR, EXER-#1 (1+1 switching, non-revertive operation) LO or FSw, FSw-#i, MSw, MSw-#i, CLR, EXER-#1

Defects: None.

Consequent Actions: None.

Defect Correlations:

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

7.5.1.2 STM-4 Multiplex Section 1:n Linear Trail Protection Connection MS4P1:n_C

Symbol:

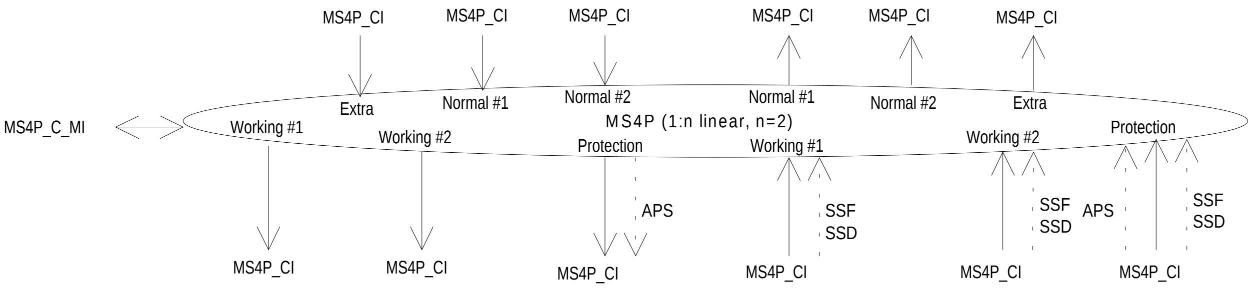


Figure 69: MS4P1:n_C symbol(s)

Interfaces:

Table 52: MS4P1:n_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF MS4P_CI_SSD MS4P_MI_SFpriority MS4P_MI_SDpriority for connection points N and E: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS per function: MS4P_CI_APS MS4P_C_MI_SWtype MS4P_C_MI_OPERtype MS4P_C_MI_EXTRAtraffic MS4P_C_MI_WTRTime MS4P_C_MI_HOTime MS4P_C_MI_EXTCMD	for connection points W and P: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF for connection points N and E: MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF Note: protection status reporting signals are for further study. per function: MS4P_CI_APS MS4P_C_MI_cFOP MS4P_C_MI_pPSC

Processes:

The function performs the STM-4 linear multiplex section protection process for 1:n protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 47 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #i reference point can be the signal received via either the associated working #i section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output is unsourced (no input connected), connected to the extra traffic input, or connected to any normal input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 53

Architecture:	1:n (n ≤ 14)
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1:n switching, revertive operation) LO, FSw-#i, MSw-#i, CLR, EXER

Defects: None.

Consequent Actions:

For the case where neither the extra traffic nor a normal signal input is to be connected to the protection section output, the null signal shall be connected to the protection output. The null signal is either one of the normal signals, an all-ONEs, or a test signal.

For the case of a protection switch, the extra traffic output (if applicable) is disconnected from the protection input, set to all-ONEs (AIS) and aSSF is activated.

Defect Correlations:

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

7.5.2 STM-4 Multiplex Section Linear Trail Protection Trail Termination Functions

7.5.2.1 Multiplex Section Protection Trail Termination Source MS4P_TT_So

Symbol:

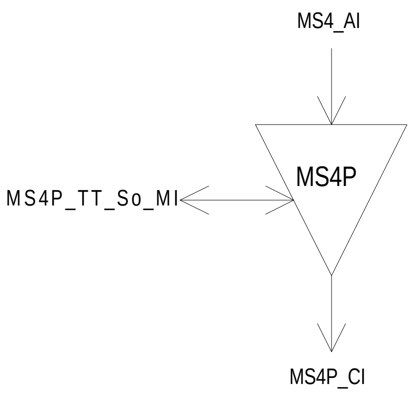


Figure 70: MS4P_TT_So symbol

Interfaces:

Table 54: MS4P_TT_So input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS	MS4P_CI_D MS4P_CI_CK MS4P_CI_FS

Processes:

No information processing is required in the MS4P_TT_So, the MS4_AI at its output being identical to the MS4P_CI at its input.

Defects: None.

Consequent Actions: None

Defect Correlations: None.

Performance Monitoring: None.

7.5.2.2 Multiplex Section Protection Trail Termination Sink MS4P_TT_Sk

Symbol:

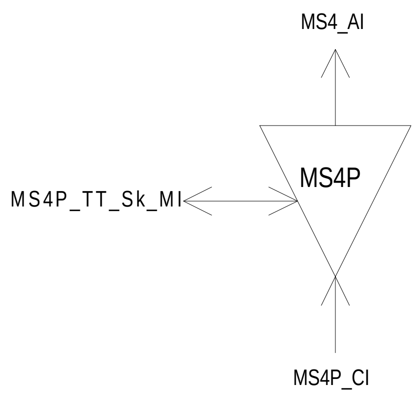


Figure 71: MS4P_TT_Sk symbol

Interfaces:

Table 55: MS4P_TT_Sk input and output signals

Input(s)	Output(s)
MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF MS4P_TT_Sk_MI_SSF_Reported	MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF MS4P_TT_Sk_MI_cSSF

Processes:

The MS4P_TT_Sk function reports, as part of the MS4 layer, the state of the protected MS4 trail. In case all connections are unavailable the MS4P_TT_Sk reports the signal fail condition of the protected trail.

Defects: None.

Consequent Actions:

aTSF ← CI_SSF

Defect Correlations: None.

cSSF ← CI_SSF and SSF_Reported

Performance Monitoring: None.

7.5.3 STM-4 Multiplex Section Linear Trail Protection Adaptation Functions

7.5.3.1 STM-4 Multiplex Section to STM-4 Multiplex Section Protection Layer Adaptation Source MS4/MS4P_A_So

Symbol:

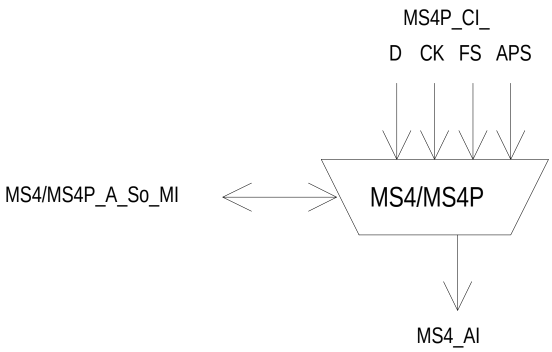


Figure 72: MS4/MS4P_A_So symbol

Interfaces:

Table 56: MS4/MS4P_A_So input and output signals

Input(s)	Output(s)
MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_APS	MS4_AI_D MS4_AI_CK MS4_AI_FS

Processes:

The function shall multiplex the MS4 APS signal and MS4 data signal onto the MS4 access point.

Defects: None.

Consequent actions: None.

Defect Correlations: None.

Performance Monitoring: None.

7.5.3.2 STM-4 Multiplex Section to STM-4 Multiplex Section Protection Layer Adaptation Sink MS4/MS4P_A_Sk

Symbol:

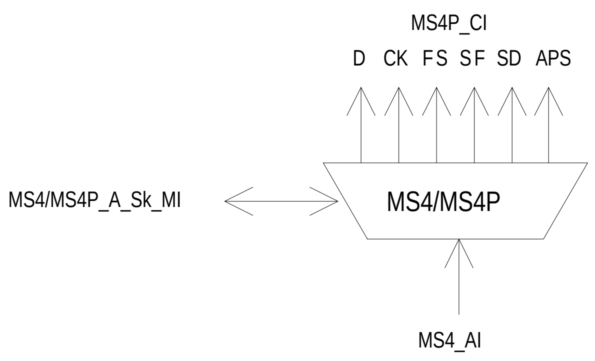


Figure 73: MS4/MS4P_A_Sk symbol

Interfaces:

Table 57: MS4/MS4P_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D MS4_AI_CK MS4_AI_FS MS4_AI_TSF MS4_AI_TSD	MS4P_CI_D MS4P_CI_CK MS4P_CI_FS MS4P_CI_SSF MS4P_CI_SSD MS4P_CI_APS (for Protection signal only)

Processes:

The function shall extract and output the MS4P_CI_D signal from the MS4_AI_D signal.

K1[1-8]K2[1-5]: The function shall extract the 13 APS bits K1[1-8] and K2[1-5] from the MS4_AI_D signal. A new value shall be accepted when the value is identical for three consecutive frames. This value shall be output via MS4P_CI_APS. This process is required only for the protection section.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

aSSD ← AI_TSD

Defect Correlations: None.

Performance Monitoring: None.

8 STM-16 Regenerator Section Layer Functions

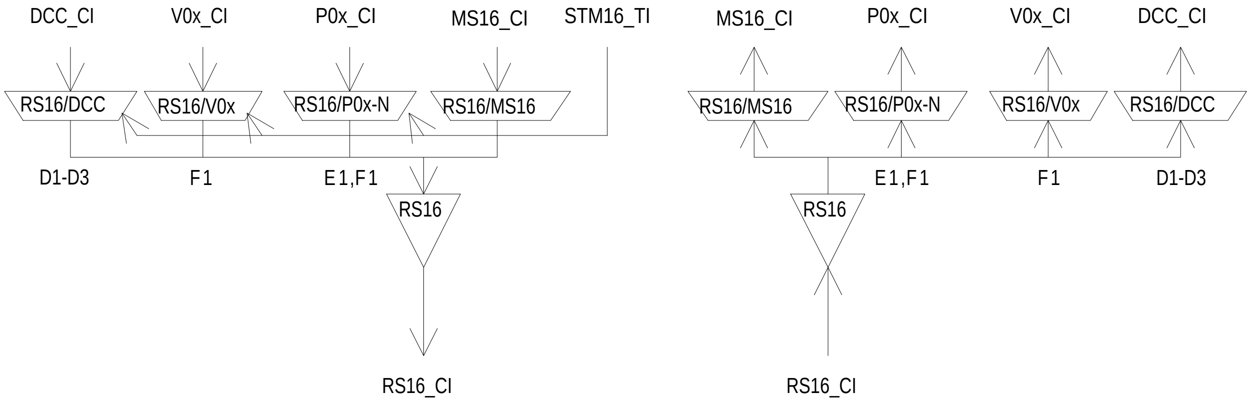


Figure 74: STM-16 Regenerator Section atomic functions

RS16 Layer CP.

The CI at this point is an octet structured, 125 µs framed data stream with co-directional timing. It is the entire STM-16 signal as defined in ETS 300 147 [2]. The figure 75 depicts only bytes handled in the RS16 layer.

NOTE 1: The unmarked bytes [2,2] to [2,48], [2,50] to [2,96], [3,2] to [3,48], [3,50] to [3,96], and [3,98] to [3,144] in rows 2,3 (figure 75) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The bytes for National Use (NU) in rows 1,2 (figure 75) are reserved for operator specific usage. Their processing is not within the province of this ETS. If NU bytes [1,113] to [1,144] are unused, care should be taken in selecting the binary content of the bytes which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of “1”s or “0”s do not occur.

NOTE 3: The bytes Z0 [1,98] to [1,112] are reserved for future international standardisation. Currently, they are undefined. Care should be taken in selecting the binary content of these bytes which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of “1”s or “0”s do not occur.

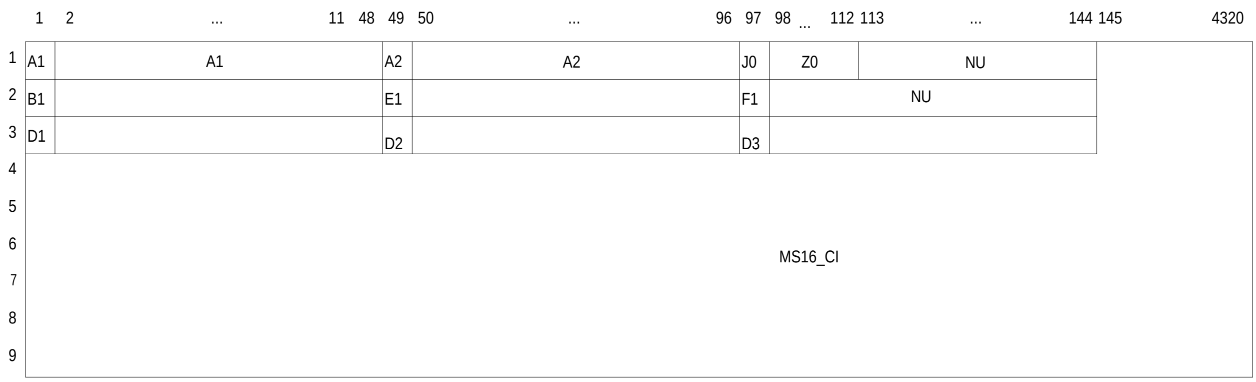


Figure 75: RS16_CI_D signal

RS16 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing and represents the combination of adapted information from the MS16 layer (38 448 bytes per frame), the management communication DCC layer (3 bytes per frame if supported), the OW layer (1 byte per frame if supported) and the user channel F1 (1 byte per frame if supported). The location of these four components in the frame is defined in ETS 300 147 [2] and depicted in figure 76.

NOTE 4: Bytes E1, F1 and D1-D3 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

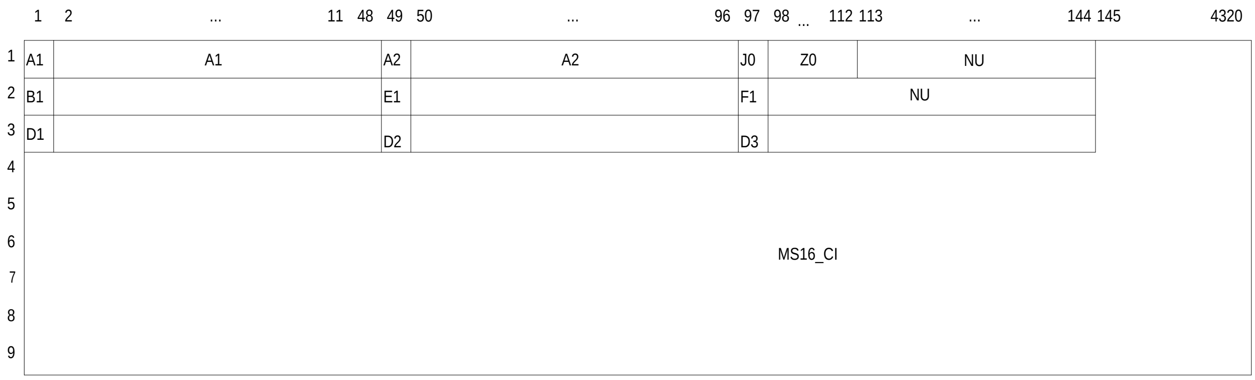


Figure 76: RS16_AI_D signal

8.1 STM-16 Regenerator Section Connection functions

For further study.

8.2 STM-16 Regenerator Section Trail Termination functions

8.2.1 STM-16 Regenerator Section Trail Termination Source RS16_TT_So

Symbol:

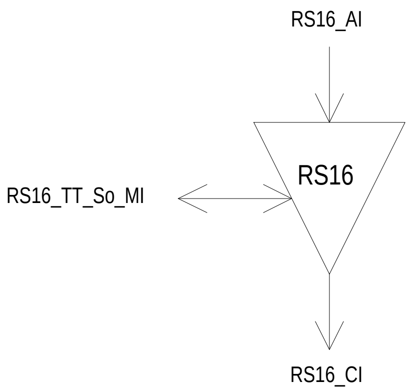


Figure 77: RS16_TT_So symbol

Interfaces:

Table 58: RS16_TT_So input and output signals

Input(s)	Output(s)
RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_TT_So_MI_TxTI	RS16_CI_D RS16_CI_CK RS16_CI_FS

Processes:

The function builds the STM-16 signal by adding the frame alignment information, bytes A1A2, the STM Section Trace Identifier (STI) byte J0, computing the parity and inserting the B1 byte.

J0: In this byte the function shall insert the Transmitted Trail Trace Identifier TxTI. Its format is described in ETS 300 417-1-1 [1], subclause 7.1.

B1: The function shall calculate a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 shall be calculated over all bits of the previous STM-16 frame after scrambling and is placed in byte position B1 of the current STM-16 frame before scrambling (figure 78).

A1A2: The function shall insert the STM-16 frame alignment signal A1...A1A2...A2 into the regenerator section overhead as defined in ETS 300 147 [2] and depicted in figure 75.

Scrambler: This function provides scrambling of the RS16_CI. The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate. The generating polynomial shall be $1+X^6+X^7$. The scrambler shall be reset to '1111 1111' on the most significant bit (MSB) of the byte (1,145) following the last byte of the STM-16 SOH in the first row. This bit and all subsequent bits to be scrambled shall be modulo 2 added to the output of the X^7 position of the scrambler. The scrambler shall run continuously throughout the remaining STM-16 frame.

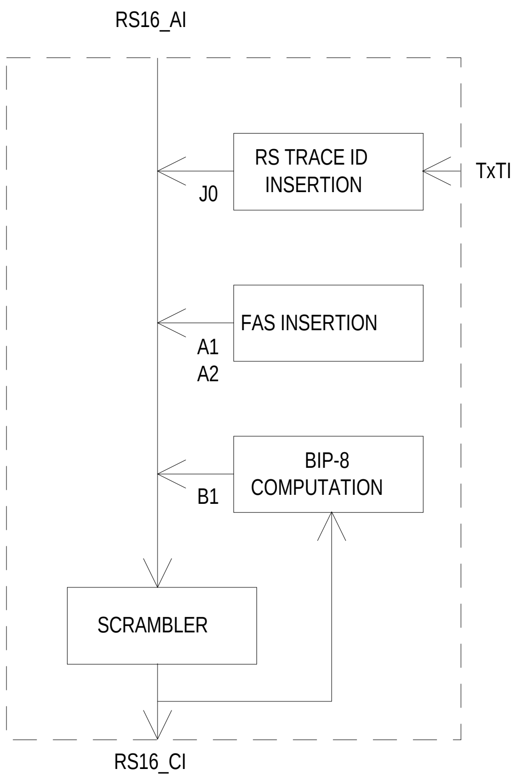


Figure 78: Some processes within RS16_TT_So

NOTE: The insertion of the frame alignment signal (A1A2) and the scrambling of the signal would be OS16/RS16_A_So processes according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-16 signal causes a violation of this process allocation, hence the frame alignment insertion and scrambling processes are located in the RS16_TT_So function.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

8.2.2 STM-16 Regenerator Section Trail Termination Sink RS16_TT_Sk

Symbol:

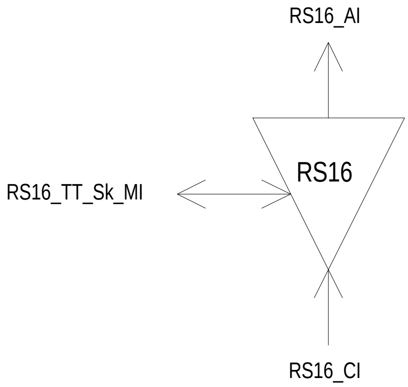


Figure 79: RS16_TT_Sk symbol

Interfaces:

Table 59: RS16_TT_Sk input and output signals

Input(s)	Output(s)
RS16_CI_D RS16_CI_CK RS16_CI_FS RS16_CI_SSF RS16_TT_Sk_MI_ExTI RS16_TT_Sk_MI_TPmode RS16_TT_Sk_MI_TIMdis RS16_TT_Sk_MI_ExTImode RS16_TT_Sk_MI_1second	RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_AI_TSF RS16_TT_Sk_MI_AcTI RS16_TT_Sk_MI_cTIM RS16_TT_Sk_MI_pN_EBC RS16_TT_Sk_MI_pN_DS

Processes:

This function monitors the STM-16 signal for RS errors, and recovers the RS trail termination status. It extracts the payload independent overhead bytes (J0, B1) from the RS16 layer Characteristic Information:

Descrambling: The function shall descramble the incoming STM-16 signal. The operation of the descrambler shall be functionally identical to that of a scrambler in OS16/RS16_A_So.

NOTE 1: The descrambling of the signal would be an OS16/RS16_A_Sk process according to ETS 300 417-1-1 [1]. The (historical) definition of the STM-16 signal causes a violation of this process allocation, hence the descrambling process is located in the RS16_TT_Sk function.

B1: Even bit parity is computed for each bit n of every byte of the preceding scrambled STM-16 frame and compared with bit n of B1 recovered from the current frame (n=1 to 8 inclusive) (figure 80). A difference between the computed and recovered B1 values is taken as evidence of one or more errors (nN_B) in the computation block.

J0: The Received Trail Trace Identifier RxTI shall be recovered from the J0 byte and shall be made available as AcTI for network management purposes. The application and acceptance and mismatch detection process shall be performed as specified in ETS 300 417-1-1 [1], subclauses 7.1, and 8.2.1.3.

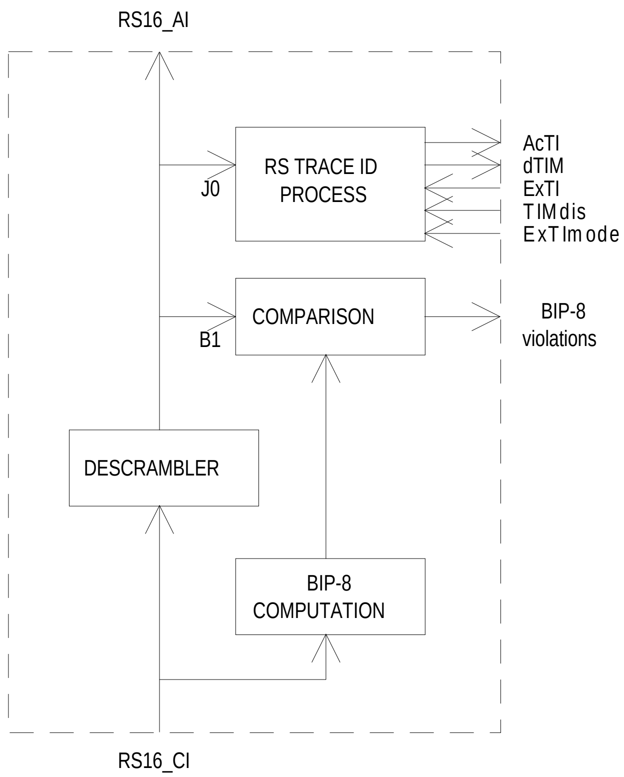


Figure 80: Some processes within RS16_TT_Sk

Defects:

The function shall detect for dTIM defects according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

Consequent Actions:

aAIS ← CI_SSF or dTIM

aTSF ← CI_SSF or dTIM

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 2: The term “CI_SSF” has been added to the conditions for aAIS while the descrambler function has been moved from the e.g. OS16/RS16_A_Sk to this function. Consequently, an all-ONEs (AIS) pattern inserted in the mentioned adaptation function would be descrambled in this function. A “refreshment” of all-ONEs is required.

Defect Correlations:

cTIM ← MON and dTIM

Performance Monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← aTSF or dEQ

pN_EBC ← Σ nN_B

8.3 STM-16 Regenerator Section Adaptation functions

8.3.1 STM-16 Regenerator Section to Multiplex Section Adaptation Source RS16/MS16_A_So

Symbol:

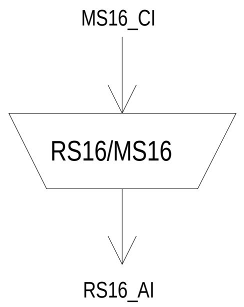


Figure 81: RS16/MS16_A_So symbol

Interfaces:

Table 60: RS16/MS16_A_So input and output signals

Input(s)	Output(s)
MS16_CI_D MS16_CI_CK STM16_CI_FS STM16_CI_SSF	RS16_AI_D RS16_AI_CK RS16_AI_FS

Processes:

The function multiplexes the MS16_CI data (38 448 bytes/frame) into the STM-16 byte locations defined in ETS 300 147 [2] and depicted in figure 75.

NOTE 1: There might be cases in which the network element knows that the timing reference for a particular STM-16 interface can not be maintained within ± 4.6 ppm. For such cases MS-AIS can be generated. This is network element specific and outside the scope of this ETS.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs. The frequency of the all ONEs signal shall be within 2 488,320 kHz ± 20 ppm.

NOTE 2: if CI_SSF is not connected (when RS16/MS16_A_So is connected to a MS16_TT_So), SSF is assumed to be false.

Defect Correlations: None.

Performance Monitoring: None.

8.3.2 STM-16 Regenerator Section to Multiplex Section Adaptation Sink RS16/MS16_A_Sk

Symbol:

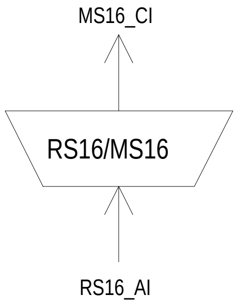


Figure 82: RS16/MS16_A_Sk symbol

Interfaces:

Table 61: RS16/MS16_A_Sk input and output signals

Input(s)	Output(s)
RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_AI_TSF	MS16_CI_D MS16_CI_CK MS16_CI_FS MS16_CI_SSF

Processes:

The function separates MS16_CI data from RS16_AI as depicted in figure 75.

Defects: None.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

8.3.3 STM-16 Regenerator Section to DCC Adaptation Source RS16/DCC_A_So

Symbol:

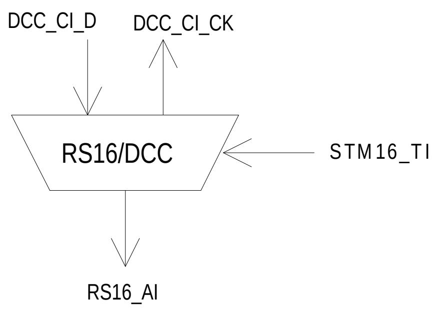


Figure 83: RS16/DCC_A_So symbol

Interfaces:

Table 62: RS16/DCC_A_So input and output signals

Input(s)	Output(s)
DCC_CI_D STM16_TI_CK STM16_TI_FS	RS16_AI_D DCC_CI_CK

Processes:

The function multiplexes the DCC CI data (192 kbit/s) into the byte locations D1, D2 and D3 as defined in ETS 300 147 [2] and depicted in figure 76 [15].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

8.3.4 STM-16 Regenerator Section to DCC Adaptation Sink RS16/DCC_A_Sk

Symbol:

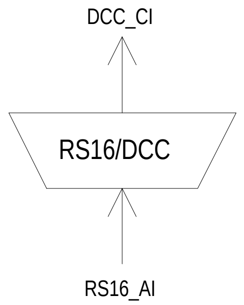


Figure 84: RS16/DCC_A_Sk symbol

Interfaces:

Table 63: RS16/DCC_A_Sk input and output signals

Input(s)	Output(s)
RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_AI_TSF	DCC_CI_D DCC_CI_CK DCC_CI_SSF

Processes:

The function separates DCC data from RS Overhead as defined in ETS 300 147 [2] and depicted in figure 76 [16].

Defects: None.

---

15 DCC transmission can be “disabled” when the matrix connection in the connected DCC_C function is removed.
16 DCC transmission can be “disabled” when the matrix connection in the connected DCC_C function is removed.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

8.3.5 STM-16 Regenerator Section to P0x Adaptation Source RS16/P0x_A_So/N

Symbol:

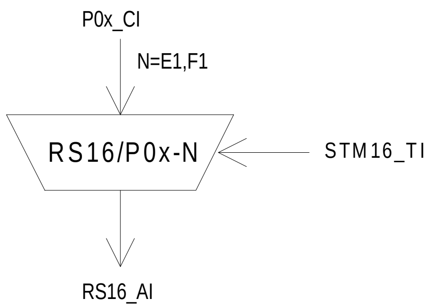


Figure 85: RS16/P0x_A_So symbol

Interfaces:

Table 64: RS16/P0x_A_So input and output signals

Input(s)	Output(s)
P0x_CI_D P0x_CI_CK P0x_CI_FS MS16_TI_CK MS16_TI_FS	RS16_AI_D

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire or user channel information stream into the RS16_AI using slip buffering. It takes P0x_CI, defined in ETS 300 166 [3] as an octet structured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the RSOH byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 76.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-16 clock, frame position (STM16_TI), and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

64 kbit/s timeslot: The adaptation source function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

8.3.6 STM-16 Regenerator Section to P0x Adaptation Sink RS16/P0x_A_Sk/N

Symbol:

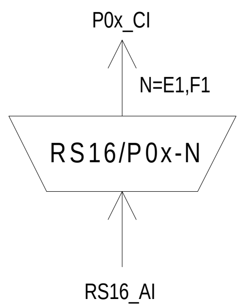


Figure 86: RS16/P0x_A_Sk symbol

Interfaces:

Table 65: RS16/P0x_A_Sk input and output signals

Input(s)	Output(s)
RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_AI_TSF	P0x_CI_Sk_D P0x_CI_Sk_CK P0x_CI_FS P0x_CI_SSF

Processes:

The function separates P0x data from RS Overhead byte E1 or F1 as defined in ETS 300 147 [2] and depicted in figure 76.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-16 signal generated at the remote node containing RS16/P0x_A_So). The residual jitter caused by pointer adjustments and octet slips (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 20 ppm, this smoothing process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the RS16_AI (for example due to a frequency step of the server STM-16 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

64 kbit/s timeslot: The adaptation sink function has access to a specific 64 kbit/s of the RS access point. The specific 64 kbit/s is defined by the parameter N (N = E1, F1).

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

8.3.7 STM-16 Regenerator Section to V0x Adaptation Source RS16/V0x_A_So

Symbol:

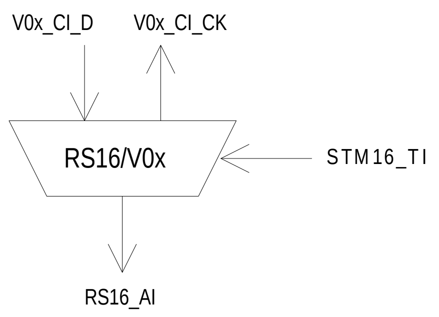


Figure 87: RS16/V0x_A_So symbol

Interfaces:

Table 66: RS16/V0x_A_So input and output signals

Input(s)	Output(s)
V0x_CI_D STM16_TI_CK STM16_TI_FS	RS16_AI_D V0x_CI_CK

Processes: None.

This function multiplexes the V0x_CI data (64 kbit/s) into the byte location F1 as defined in ETS 300 147 [2] and depicted in figure 76.

The user channel byte F1 shall be added to the 125 µs frame.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

8.3.8 STM-16 Regenerator Section to V0x Adaptation Sink RS16/V0x_A_Sk

Symbol:

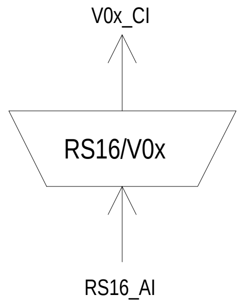


Figure 88: RS16/V0x_A_Sk symbol

Interfaces:

Table 67: RS16/V0x_A_Sk input and output signals

Input(s)	Output(s)
RS16_AI_D RS16_AI_CK RS16_AI_FS RS16_AI_TSF	V0x_CI_D V0x_CI_CK V0x_CI_SSF

Processes:

This function separates user channel data from RS Overhead (byte F1) as defined in ETS 300 147 [2] and depicted in figure 76.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± TBD ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

9 STM-16 Multiplex Section layer functions

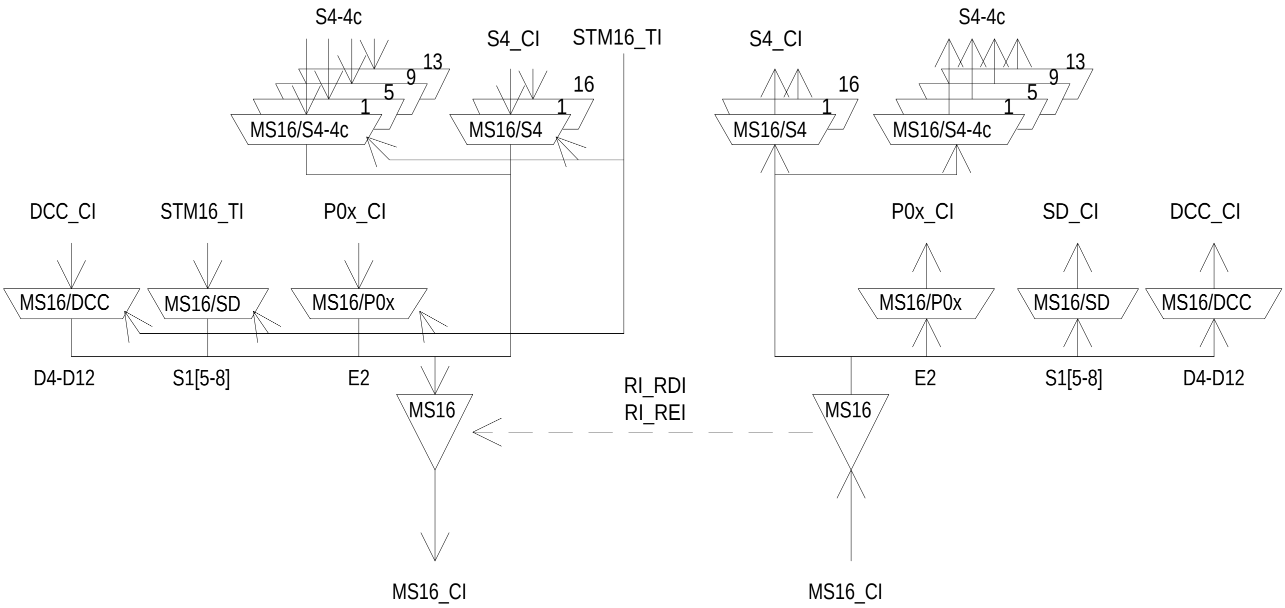


Figure 89: STM-16 Multiplex Section atomic functions

MS16 Layer CP.

The CI at this point is octet structured and 125 µs framed with co-directional timing. Its format is characterised as the MS16_AI with an additional MS Trail Termination overhead in the forty eight B2 bytes, byte M1, and bits 6-8 of the K2 byte in the frame locations defined in ETS 300 147 [2] and depicted in figure 90.

NOTE 1: The unmarked bytes in rows 5,6,7,8,9 (figure 90) are reserved for future international standardisation. Currently, they are undefined.

NOTE 2: The bytes for National Use (NU) in row 9 (figure 90) are reserved for operator specific usage. Their processing is not within the province of this ETS.

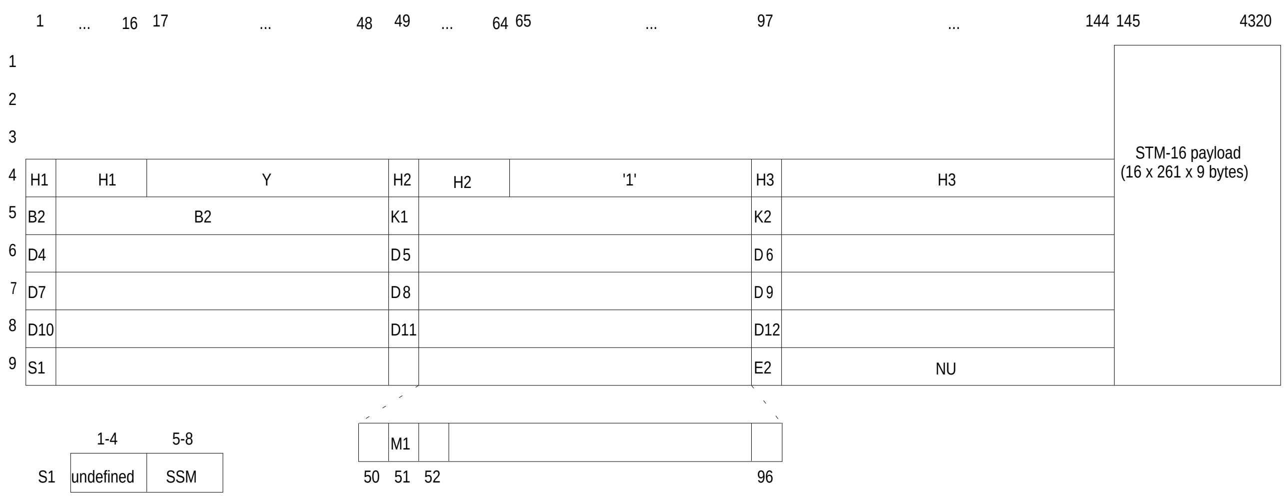


Figure 90: MS16_CI_D

MS16 Layer AP.

The AI at this point is octet structured and 125 µs framed with co-directional timing. It represents the combination of information adapted from the VC-4 layer (150 336 kbit/s), the management communications DCC layer (576 kbit/s), the OW layer (64 kbit/s if supported), the AU-4 pointer (3 bytes per frame), the APS signalling channel (13 [17] or 16 [18] bits per frame if supported), and the Synchronisation Status Message channel (4 bits per frame if supported). The location of these five components in the frame is defined in ETS 300 147 [2] and depicted in figure 91.

NOTE 3: Bytes E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element.

The composition of the payload transported by an STM-16 will be determined by the client layer application. Typical compositions of the payload include:

- four VC-4-4c of 601 344 kbit/s;
- sixteen VC-4s of 150 336 kbit/s;
- eight [two] working VC-4s [VC-4-4c's] and eight [two] protection VC-4s [VC-4-4c's] (in MS16 SPRING application).

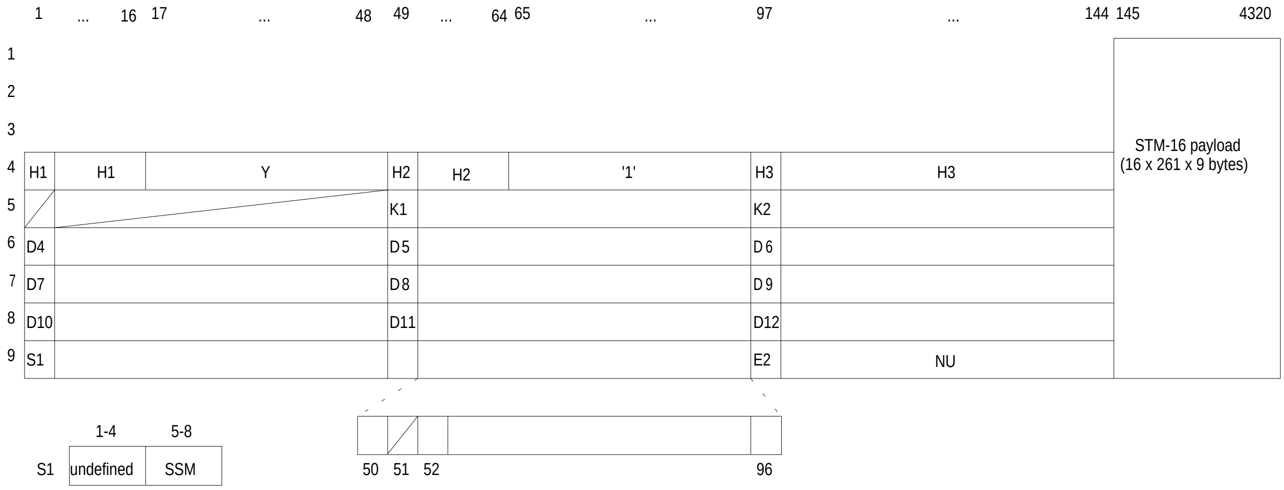


Figure 91: MS16_AI_D

17 13 bits APS channel for the case of linear MS protection
18 16 bits APS channel for the case of MS SPRING protection

Figure 92 shows the MS trail protection specific sublayer atomic functions (MS16/MS16P_A, MS16P_C, MS16P_TT) within the MS16 layer. Note that the DCC (D4-D12), OW (E2) , and SSM (S1[5-8]) signals can be accessible before (unprotected) and after (protected) the MS16P_C function. The choice is outside the scope of this ETS.

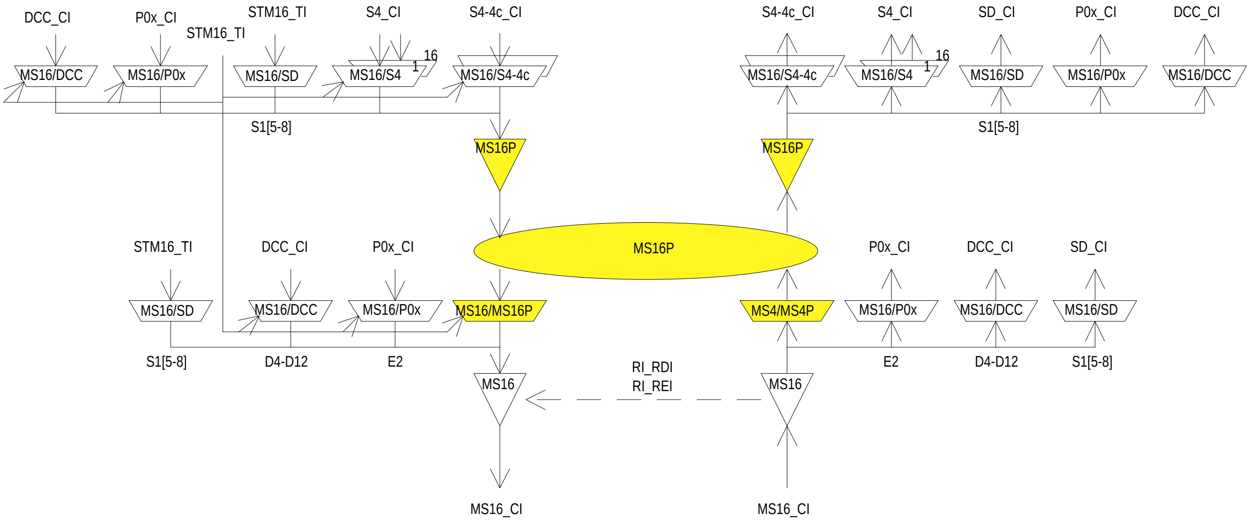


Figure 92: STM-16 Multiplex Section Linear Trail Protection Functions

MS16P Sublayer CP.

The CI at this point is octet structured and 125 µs framed with co-directional timing. Its format is equivalent to the MS4_AI and depicted in figure 93.

NOTE 4: Bytes S1, E2 and D4-D12 will be undefined when the adaptation functions sourcing these bytes are not present in the network element or are unprotected (see above).

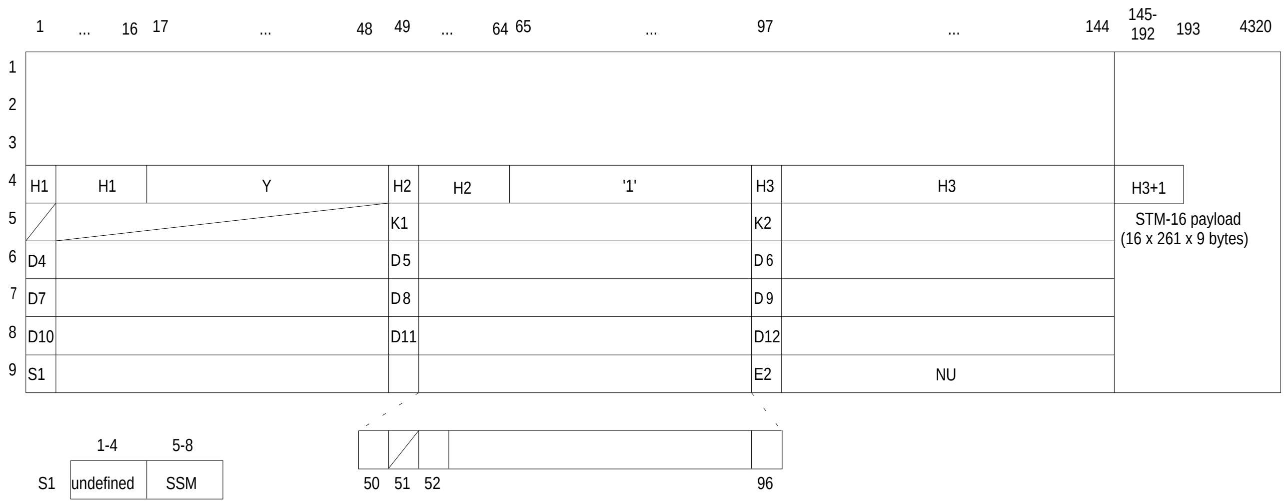


Figure 93: MS16P_CI_D

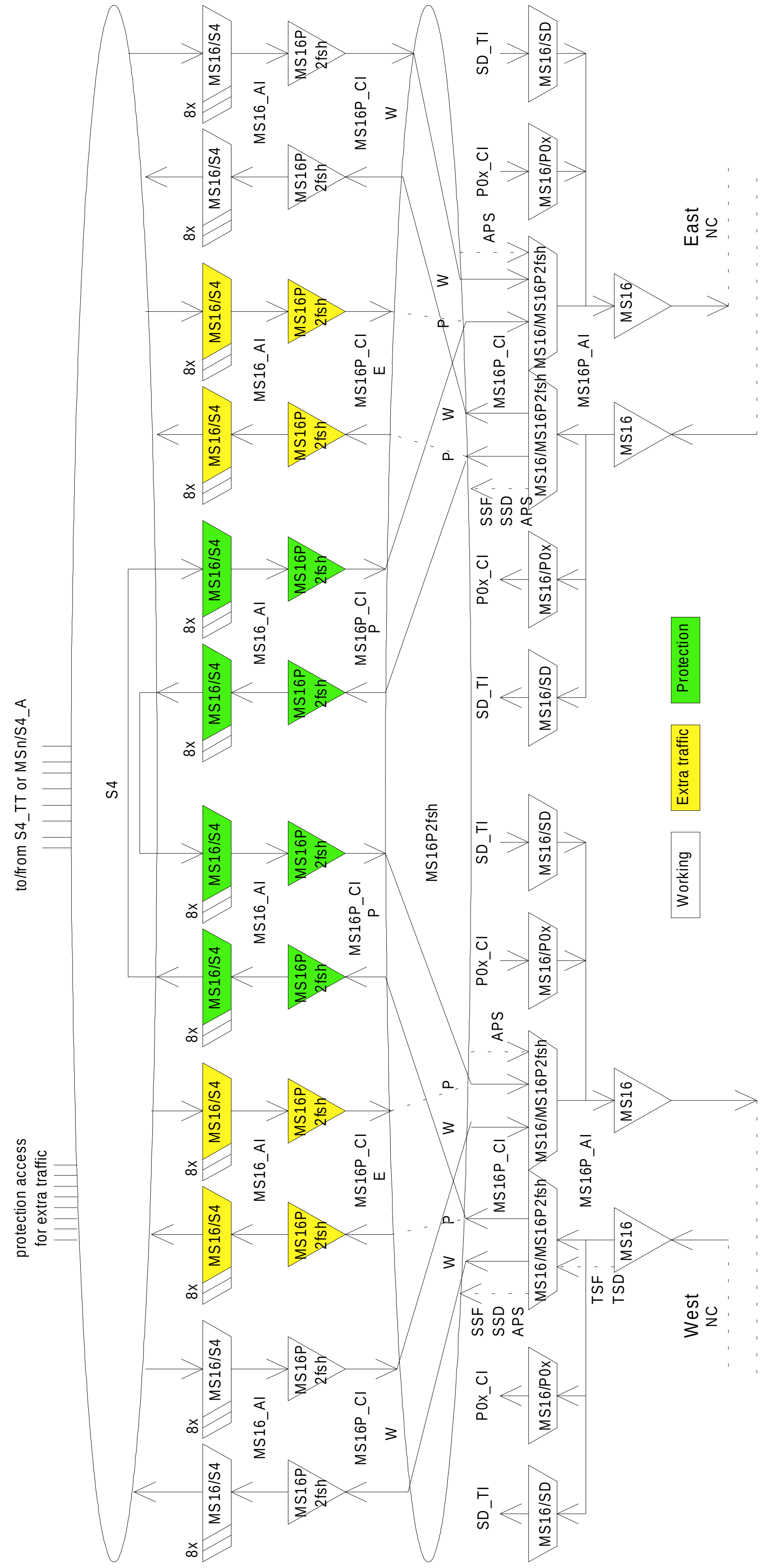


Figure 94: STM-16 Multiplex Section 2 fibre Shared Protection Ring model (working: AU-4 #1 to AU-4 #8, protection: AU-4 #9 to AU-4 #16) [see next page]

9.1 STM-16 Multiplex Section Connection functions

For further study.

9.2 STM-16 Multiplex Section Trail Termination functions

9.2.1 STM-16 Multiplex Section Trail Termination Source MS16_TT_So

Symbol:

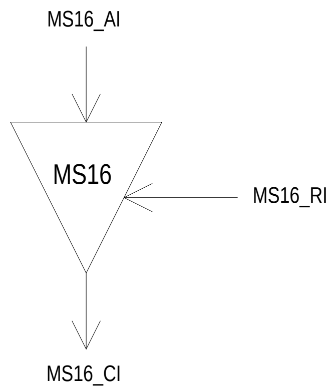


Figure 95: MS16_TT_So symbol

Interfaces:

Table 68: MS16_TT_So input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_RI_REI MS16_RI_RDI	MS16_CI_D MS16_CI_CK MS16_CI_FS

Processes:

This function adds error monitoring capabilities and remote maintenance information signals to the MS16_AI.

M1: The function shall set the REI (Remote Error Indication) to one of the codes in table 69 if one or more errored blocks were detected by the BIP-384 process in MS16_TT_Sk (communicated via MS16_RI_REI), and shall set REI to ”0000 0000” otherwise.

Table 69: M1 code generation

Number of errored blocks	M1code, bits 1234 5678
0 errored blocks	0000 0000
1 errored block	0000 0001
2 errored blocks	0000 0010
3 errored blocks	0000 0011
4 errored blocks	0000 0100
⋮	⋮
16 errored blocks	0001 0000

NOTE 1: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8]: These bits represents the defect status of the associated MS16_TT_Sk. The RDI indication shall be set to "110" on activation of MS16_RI_RDI within 250 µs, determined by the associated MS16_TT_Sk function, and passed through transparently (except for incoming codes "111" and "110") within 250 µs on the MS16_RI_RDI removal. If MS16_RI_RDI is inactive an incoming code "111" or "110" shall be replaced by code "000".

NOTE 2: K2[6-8] can not be set to "000" on clearing of RI_RDI; MS SPRING APS extends into those bits. The bits must be passed transparently in this case. With linear MS protection or without protection it must be guaranteed that neither code "111" nor "110" will be output.

B2: The function shall calculate a Bit Interleaved Parity 384 (BIP-384) code using even parity. The BIP-384 shall be calculated over all bits, except those in the RSOH bytes, of the previous STM-16 frame and placed in forty-eight B2 bytes of the current STM-16 frame [19].

Defects: None.

Consequent Actions:

On declaration of RI_RDI the function shall output RDI (pattern '110' in bit 6,7, and 8 of byte K2) within 250 µs; on clearing of RI_RDI the function shall output normal data within 250 µs.

Defect Correlations: None.

Performance Monitoring: None.

9.2.2 STM-16 Multiplex Section Trail Termination Sink MS16_TT_Sk

Symbol:

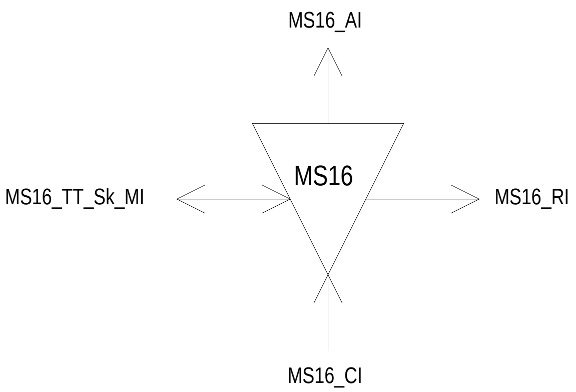


Figure 96: MS16_TT_Sk symbol

[19] The BIP-384 procedure is described in ETS 300 147.

Interfaces:

Table 70: MS16_TT_Sk input and output signals

Input(s)	Output(s)
MS16_CI_D MS16_CI_CK MS16_CI_FS MS16_CI_SSF MS16_TT_Sk_DEGTHR MS16_TT_Sk_DEGM MS16_TT_Sk_1second MS16_TT_Sk_MI_TPmode MS16_TT_Sk_MI_SSF_Reported MS16_TT_Sk_MI_AIS_Reported MS16_TT_Sk_MI_RDI_Reported	MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_CI_TSF MS16_TT_Sk_MI_cAIS MS16_TT_Sk_MI_cDEG MS16_TT_Sk_MI_cRDI MS16_TT_Sk_MI_cSSF MS16_TT_Sk_MI_pN_EBC MS16_TT_Sk_MI_pF_EBC MS16_TT_Sk_MI_pN_DS MS16_TT_Sk_MI_pF_DS MS16_RI_REI MS16_RI_RDI

Processes:

This function monitors error performance of associated MS16 including the far end receiver.

B2: The BIP-384 is organised as sixteen times BIP-24 as specified in Recommendation G.707 [4]. It shall be calculated over all bits, except of those in the RSOH bytes, of the previous STM-16 frame and compared with the sixteen times BIP-24 value (bytes B2) recovered from the MSOH of the current STM-16 frame. For each BIP-24 a difference between the computed BIP-24 and recovered BIP-24 value in the B2 bytes shall be taken as evidence of one or more errors in the computation BIP-24 block. The number of errored blocks (nN_B) in the BIP-384 shall be calculated by adding the total number of BIP-24 errored blocks.

M1: The REI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The REI is used to monitor the error performance of the other direction of transmission. The application process is described in ETS 300 417-1-1 [1], subclause 7.4.2 (REI).

The function shall interpret the code as follows.

Table 71

M1[2-8] code, bits 1234 5678	code interpretation (nF_B)
0000 0000	0 errored blocks
0000 0001	1 errored block
0000 0010	2 errored blocks
0000 0011	3 errored blocks
0000 0100	4 errored blocks
⋮	⋮
0001 0000	16 errored blocks
0001 0001	0 errored blocks
0001 0010	0 errored blocks
⋮	⋮
1111 1111	0 errored blocks

NOTE: The definition of the M1 byte is currently under study in ITU-T SG13 and SG15.

K2[6-8] - RDI: The RDI information carried in these bits shall be extracted to enable single ended maintenance of a bi-directional trail (section). The RDI provides information as to the status of the remote receiver. A "110" indicates a Remote Defect Indication state, while other patterns indicate the normal state. The application process is described in ETS 300 417-1-1 [1], subclauses 7.4.11 and 8.2.

K2[6-8] - AIS: The MS-AIS information carried in these bits shall be extracted.

Defects:

The function shall detect for dDEG and dRDI defects according the specification in ETS 300 417-1-1 [1], subclause 8.2.1.

dAIS: If at least ***x*** consecutive frames contain the '111' pattern in bits 6, 7 and 8 of the K2 byte a dAIS defect shall be detected. dAIS shall be cleared if in at least ***x*** consecutive frames any pattern other then the '111' is detected in bits 6, 7 and 8 of byte K2. The ***x*** shall be in range 3 to 5.

Consequent Actions:

aAIS ← dAIS

aRDI ← dAIS

aTSF ← dAIS

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

Defect Correlations:

cAIS ← MON and dAIS and (not CI_SSF) and AIS_Reported

cDEG ← MON and dDEG

cRDI ← MON and dRDI and RDI_Reported

cSSF ← MON and dAIS and SSF_Reported

Performance monitoring:

The performance monitoring process shall be performed as specified in ETS 300 417-1-1 [1], subclause 8.2.4 through 8.2.7.

pN_DS ← aTSF or dEQ

pF_DS ← dRDI

pN_EBC ← Σ nN_B

pF_EBC ← Σ nF_B

9.3 STM-16 Multiplex Section Adaptation functions

9.3.1 STM-16 Multiplex Section to S4 Layer Adaptation Source MS16/S4_A_So/N

Symbol:

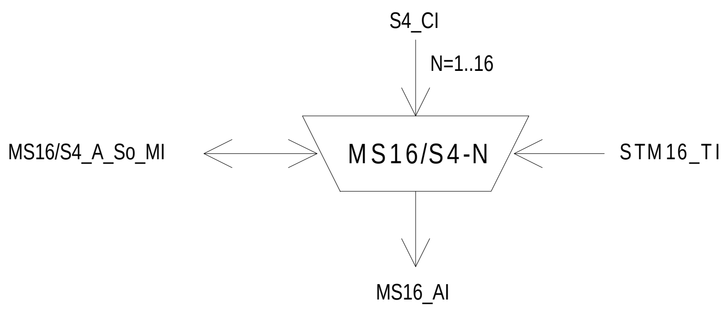


Figure 97: MS16/S4_A_So symbol

Interfaces:

Table 72: MS16/S4_A_So input and output signals

Input(s)	Output(s)
S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF STM16_TI_CK STM16_TI_FS MS16/S4_A_So_MI_Active	MS16_AI_D MS16_AI_CK MS16_AI_FS MS16/S4_A_So_MI_pPJE+ MS16/S4_A_So_MI_pPJE-

Processes:

This function provides frequency justification and bitrate adaptation for a VC-4 signal, represented by a nominally (261*9*64) = 150 336 kbit/s information stream and the related frame phase with a frequency accuracy within ± 4.6 ppm, to be multiplexed into a STM-16 signal at the AU tributary location indicated by MI_AUnum. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

The frame phase of the VC-4 is coded in the related AU-4 pointer. Frequency justification, if required, is performed by pointer adjustments. The accuracy of this coding process is specified below. Refer to prETS 300 417-4-1 [7], annex A.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (buffer) process. The data and frame start signals shall be written into the buffer under control of the associated input clock. The data and frame start signals shall be read out of the buffer under control of the STM-16 clock, frame position, and justification decision.

The justification decisions determine the phase error introduced by the MS16/S4_A_So function. The amount of this phase error can be measured at the physical interfaces by monitoring the AU-4 pointer actions. An example is given in prETS 300 417-4-1 [7], annex A.2.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of 24 data bits shall be cancelled once and no data written at the three positions H3+1. Upon a negative justification action, an extra 24 data bits shall be read out once into the three positions H3.

NOTE 1: A requirement for maximum introduced phase error cannot be defined until a reference path is defined from which the requirements for network elements can be deduced. Such a requirement would also limit excessive phase error caused by pointer processors under fixed frequency offset conditions.

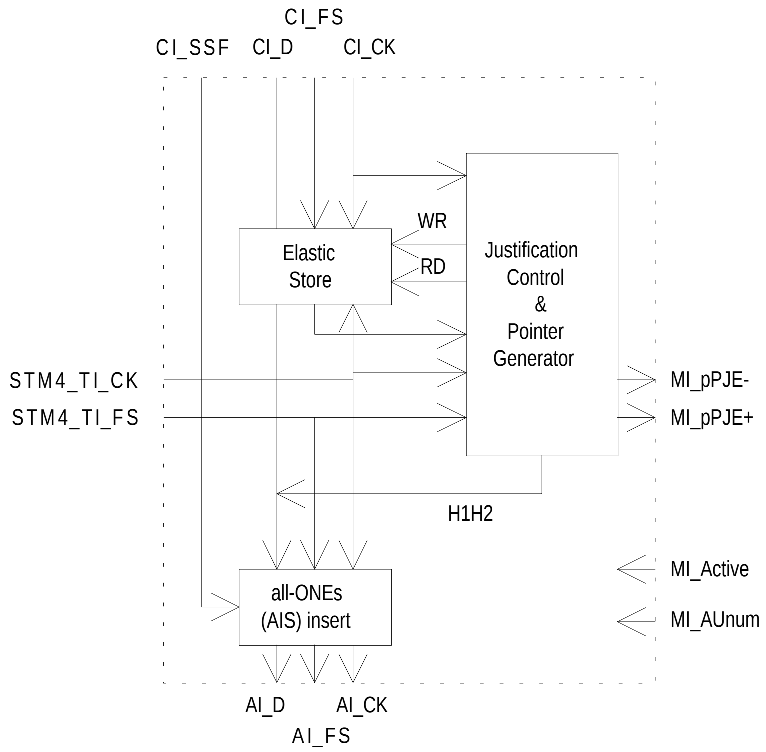


Figure 98: main processes within MS16/S4_A_So

Buffer size: For further study.

Behaviour at recovery from defect condition: The incoming frequency (S4_CI_CK) of a passing through VC-4 may exceed its limits during a STM16dLOS condition. As a consequence, the buffer (elastic store) fill is not reliable any more. Due to all-ONEs (AIS) insertion after the pointer generator this reliability is not important for the operation of the network element. However, it shall be prevent to generate excessive pointer adjustments when recovering from the defect condition.

NOTE 2: The definition of excessive pointer adjustments is for further study.

The AU-4 pointer is carried in 2 bytes of payload specific OH in each STM-16 frame. The AU-4 pointer is aligned in the STM-16 payload in fixed position relative to the STM-16 frame. The AU-4 pointer points to the begin of the VC-4 frame within the STM-16. The format of the AU-4 pointer and its location in the frame are defined in ETS 300 147 [2].

H1H2 - *Pointer generation:* The function shall generate the AU-4 pointer as is described in ETS 300 417-1-1 [1], annex A: Pointer Generation. It shall insert the pointer in the appropriate H1, H2 positions with the SS field set to 10 to indicate AU-4.

YY1*1* - *Fixed stuff insertion:* The function shall insert fixed stuff codes Y = 1001ss11 in bytes [4,16+AUnum] and [4,32+AUnum] and code '1' = 11111111 in bytes [4,64+AUnum] and [4,80+AUnum]. Bits ss are undefined.

AU-4 timeslot: The adaptation source function has access to a specific AU-4 of the MS16 access point. The AU-4 is defined by the parameter N (N=1..16).

Figure 89 shows that more than one adaptation source function exists in the MS16 layer that can be connected to one MS16 access point. For such case, a subset of these adaptation source functions is allowed to be activated together, but only one adaptation source function may have access to a specific AU timeslot. Access to the same AU timeslot by other adaptation source functions must be denied.

Activation: The function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 3: if CI_SSF is not connected (when MS16/S4_A_So is connected to a S4_TT_So), CI_SSF is assumed to be false.

Defect Correlations: None

Performance Monitoring:

Every second the number of generated pointer increments within that second shall be counted as the pPJE+. Every second the number of generated pointer decrements within that second shall be counted as the pPJE-.

NOTE 4: This is applicable for a passing through VC-4 only. A locally generated VC-4 will have a fixed frame phase; pointer justifications will not occur.

9.3.2 STM-16 Multiplex Section to S4 Layer Adaptation Sink MS16/S4_A_Sk/N

Symbol:

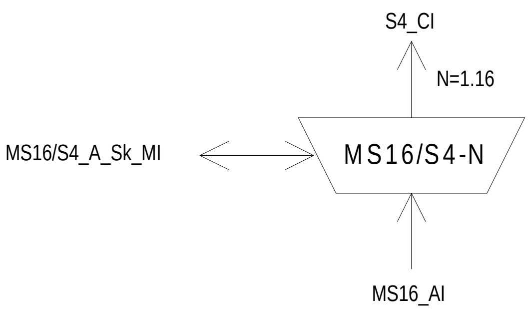


Figure 99: MS16/S4_A_Sk symbol

Interfaces:

Table 73: MS16/S4_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16/S4_A_Sk_MI_Active MS16/S4_A_Sk_MI_AUnum MS16/S4_A_Sk_MI_AIS_Reported	S4_CI_D S4_CI_CK S4_CI_FS S4_CI_SSF MS16/S4_A_Sk_MI_cAIS MS16/S4_A_Sk_MI_cLOP

Processes:

This function recovers the VC-4 data with frame phase information from the STM-16 as defined in ETS 300 147 [2]. The VC-4 is extracted from the AU tributary location indicated by MI_AUnum. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

H1H2 - *AU-4 pointer interpretation:* The function shall perform AU-4 pointer interpretation according to annex B of ETS 300 417-1-1 [1] to recover the VC-4 frame phase within the STM-16. The process shall maintain its current phase on detection of an invalid pointer and searches in parallel for a new phase.

YY1*1*: An AU-4 pointer consists of 2 bytes, [4,AUnum] and [4,48+AUnum]. The bytes [4,16+AUnum], [4,32+AUnum], [4,64+AUnum], and [4,80+AUnum] contain fixed stuff, of a specified value, ignored by the AU-4 pointer interpreter.

AU-4 timeslot: The adaptation sink function has access to a specific AU-4 of the MS16 access point. The AU-4 is defined by the parameter N (N=1..16).

Figure 89 shows that more than one adaptation sink function exists in this MS16 layer that can be connected to one MS16 access point. In contradiction with the source direction, adaptation sink functions may be activated all together. Faults (e.g. cLOP) may be detected and reported. To prevent this an adaptation sink function can be deactivated.

Activation: The function shall perform the operation specified above when it is activated (MI_Active is true). Otherwise, it shall transmit the all-ONEs signal at its output (CI_D) and not report its status via its management point.

Defects:

dAIS: The dAIS defect shall be detected if the pointer interpreter is in the AIS_state (refer to ETS 300 417-1-1 [1], annex B). The dAIS defect shall be cleared if the pointer interpreter is not in the AIS_state.

dLOP: The dLOP defect shall be detected if the pointer interpreter is in the LOP_state (refer to ETS 300 417-1-1 [1], annex B). The dLOP defect shall be cleared if the pointer interpreter is not in the LOP_state.

Consequent Actions:

aAIS ← dAIS or dLOP

aSSF ← dAIS or dLOP

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output the recovered data within 250 µs.

Defect Correlations:

cAIS ← dAIS and (not AI_TSF) and AIS_Reported

cLOP ← dLOP

Performance Monitoring: None.

9.3.3 STM-16 Multiplex Section to S4-4c Layer Adaptation Source MS16/S4-4c_A_So/N

Symbol:

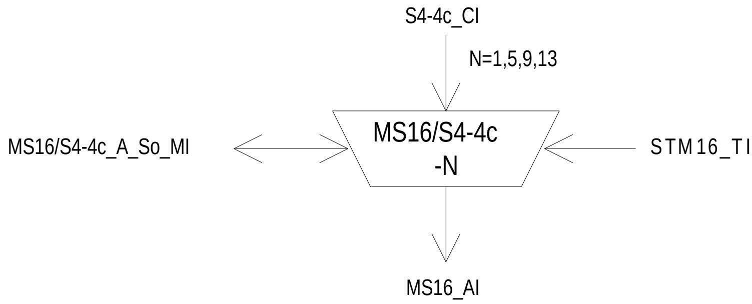


Figure 100: MS4/S4-4c_A_So symbol

Interfaces:

Table 74: MS16/S4-4c_A_So input and output signals

Input(s)	Output(s)
S4-4c_CI_D S4-4c_CI_CK S4-4c_CI_FS S4-4c_CI_SSF STM16_TI_CK STM16_TI_FS MS16/S4-4c_A_So_MI_Active	MS16_AI_D MS16_AI_CK MS16_AI_FS MS16/S4-4c_A_So_MI_pPJE+ MS16/S4-4c_A_So_MI_pPJE-

Processes:

This function provides frequency justification and bitrate adaptation for a VC-4-4c signal, represented by a nominally (4 x 261*9*64) = 601 344 kbit/s information stream and the related frame phase with a frequency accuracy within $\pm$ 4.6 ppm, to be multiplexed into a STM-16 signal. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

The frame phase of the VC-4-4c is coded in the related AU-4-4c pointer. Frequency justification, if required, is performed by pointer adjustments. The accuracy of this coding process is specified below. Refer to prETS 300 417-4-1 [7], annex A.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (buffer) process. The data and frame start signals shall be written into the buffer under control of the associated input clock. The data and frame start signals shall be read out of the buffer under control of the STM-16 clock, frame position, and justification decision.

The justification decisions determine the phase error introduced by the MS16/S4-4c_A_So function. The amount of this phase error can be measured at the physical interfaces by monitoring the AU-4-4c pointer actions. An example is given in prETS 300 417-4-1 [7], annex A.2.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification action, the reading of 96 data bits shall be cancelled once and no data written at the twelve positions H3+1. Upon a negative justification action, an extra 96 data bits shall be read out once into the twelve positions H3.

NOTE 1: A requirement for maximum introduced phase error cannot be defined until a reference path is defined from which the requirements for network elements can be deduced. Such a requirement would also limit excessive phase error caused by pointer processors under fixed frequency offset conditions.

Buffer size: For further study.

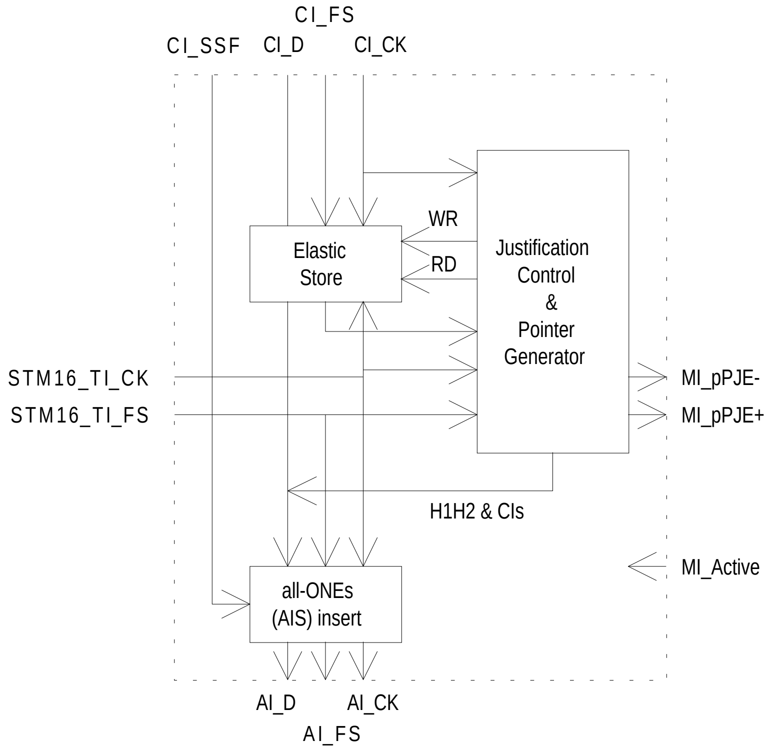


Figure 101: main processes within MS16/S4-4c_A_So

Behaviour at recovery from defect condition: The incoming frequency (S4-4c_CI_CK) of a passing through VC-4-4c may exceed its limits during a STM16dLOS condition. As a consequence, the buffer (elastic store) fill is not reliable any more. Due to all-ONEs (AIS) insertion after the pointer generator this reliability is not important for the operation of the network element. However, it shall be prevent to generate excessive pointer adjustments when recovering from the defect condition.

NOTE 2: The definition of excessive pointer adjustments is for further study.

The AU-4-4c pointer is carried in 2+6 bytes of payload specific OH in each STM-16 frame. The AU-4-4c pointer is aligned in the STM-16 payload in fixed position relative to the STM-16 frame. The AU-4-4c pointer points to the begin of the VC-4-4c frame within the STM-16. The format of the AU-4-4c pointer and its location in the frame are defined in ETS 300 147 [2].

H1H2 - *Pointer generation:* The function shall generate the AU-4-4c pointer as is described in ETS 300 417-1-1 [1], annex A: Pointer Generation. It shall insert the pointer in the H1 [4,1], H2 [4,13] positions with the SS field set to 10 to indicate AU-3/AU-4/AU-4-4c. It shall insert the concatenation indicator in the other pointer locations H1 [4,2] to [4,4], H2 [4,14] to [4,16]. The concatenation indicator is defined as 1001ss11 11111111, with ss being undefined bits.

YY1*1* - *Fixed stuff insertion:* The function shall insert fixed stuff codes Y = 1001ss11 in bytes [4,5] to [4,12] and code '1' = 11111111 in bytes [4,17] to [4,24]. Bits ss are undefined.

AU-4-4c timeslots: The adaptation source function has access to a specific AU-4-4c of the MS16 access point. The AU-4-4c is defined by the parameter N (N=1,5,9,13).

Figure 89 shows that more than one adaptation source function exists in the MS16 layer that can be connected to one MS16 access point. For such case, a subset of these adaptation source functions is allowed to be activated together, but only one adaptation source function may have access to a specific AU timeslot. Access to the same AU timeslot by other adaptation source functions must be denied.

Activation: The function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

Defects: None.

Consequent Actions:

aAIS ← CI_SSF

On declaration of aAIS the function shall output an all-ONEs signal within 250 µs; on clearing of aAIS the function shall output normal data within 250 µs.

NOTE 3: if CI_SSF is not connected (when MS16/S4-4c_A_So is connected to a S4-4c_TT_So), CI_SSF is assumed to be false.

Defect Correlations: None

Performance Monitoring:

Every second the number of generated pointer increments within that second shall be counted as the pPJE+. Every second the number of generated pointer decrements within that second shall be counted as the pPJE-.

NOTE 4: This is applicable for a passing through VC-4-4c only. A locally generated VC-4-4c may have a fixed frame phase; pointer justifications will not occur.

9.3.4 STM-16 Multiplex Section to S4-4c Layer Adaptation Sink MS16/S4-4c_A_Sk/N

Symbol:

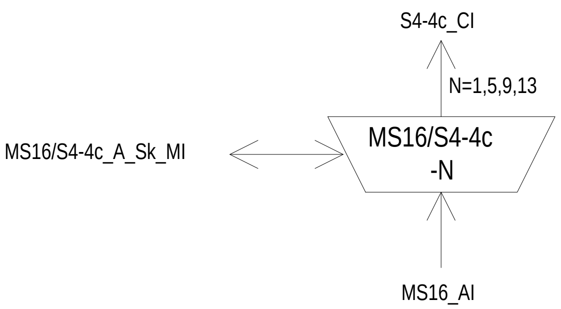


Figure 102: MS16/S4-4c_A_Sk symbol

Interfaces:

Table 75: MS16/S4-4c_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16/S4-4c_A_Sk_MI_Active MS16/S4-4c_A_Sk_MI_AIS_Reported	S4-4c_CI_D S4-4c_CI_CK S4-4c_CI_FS S4-4c_CI_SSF MS16/S4-4c_A_Sk_MI_cAIS MS16/S4-4c_A_Sk_MI_cLOP

Processes:

This function recovers the VC-4-4c data with frame phase information from the STM-16 as defined in ETS 300 147 [2]. The function can be activated/deactivated when multiple payload adaptation functions are connected to the access point.

H1H2 - *AU-4-4c pointer interpretation:* The function shall perform AU-4-4c pointer interpretation according to annex B of ETS 300 417-1-1 [1] to recover the VC-4-4c frame phase within the STM-16. The process shall maintain its current phase on detection of an invalid pointer and searches in parallel for a new phase.

YY1*1*: An AU-4-4c pointer consists of 2 bytes, [4,1] and [4,13]. There will be 3 concatenation indicators, each 2 bytes long, in [4,2]/[4,14], [4,3]/[4,15], and [4,4]/[4,16]. The bytes [4,5] to [4,12] and [4,17] to [4,24] contain fixed stuff, of a specified value, ignored by the AU-4-4c pointer interpreter.

Figure 89 shows that more than one adaptation sink function exists in this MS16 layer that can be connected to one MS16 access point. In contradiction with the source direction, adaptation sink functions may be activated all together. Faults (e.g. cLOP) may be detected and reported. To prevent this an adaptation sink function can be deactivated.

AU-4-4c timeslots: The adaptation source function has access to a specific AU-4-4c of the MS16 access point. The AU-4-4c is defined by the parameter N (N=1,5,9,13).

Activation: The function shall perform the operation specified above when it is activated (MI_Active is true). Otherwise, it shall transmit the all-ONEs signal at its output (CI_D) and not report its status via its management point.

Defects:

dAIS: The dAIS defect shall be detected if the pointer interpreter is in the AISX_state (refer to ETS 300 417-1-1 [1], annex B). The dAIS defect shall be cleared if the pointer interpreter is not in the AISX_state.

dLOP: The dLOP defect shall be detected if the pointer interpreter is in the LOPX_state (refer to ETS 300 417-1-1 [1], annex B). The dLOP defect shall be cleared if the pointer interpreter is not in the LOPX_state.

Consequent Actions:

aAIS ← dAIS or dLOP

aSSF ← dAIS or dLOP

On declaration of aAIS the function shall output an all-ONEs (AIS) signal within 250 µs; on clearing of aAIS the function shall output the recovered data within 250 µs.

Defect Correlations:

cAIS ← dAIS and (not aTSF) and AIS_Reported

cLOP ← dLOP

Performance Monitoring: None.

9.3.5 STM-16 Multiplex Section to DCC Adaptation Source MS16/DCC_A_So

Symbol:

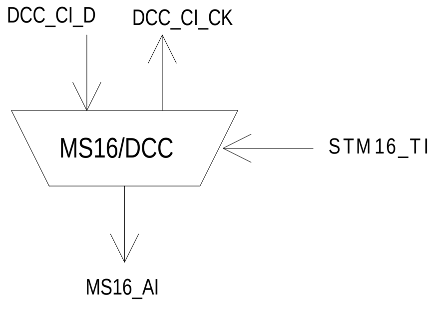


Figure 103: MS16/DCC_A_So symbol

Interfaces:

Table 76: MS16/DCC_A_So input and output signals

Input(s)	Output(s)
DCC_CI_D STM16_TI_CK STM16_TI_FS	MS16_AI_D DCC_CI_CK

Processes:

The function multiplexes the DCC CI data (576 kbit/s) into the byte locations D4 to D12 as defined in ETS 300 147 [2] and depicted in figure 91 [20].

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

9.3.6 STM-16 Multiplex Section to DCC Adaptation Sink MS16/DCC_A_Sk

Symbol:

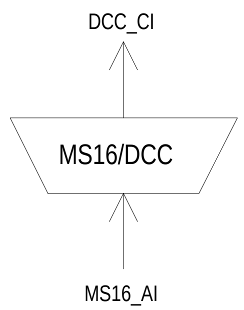


Figure 104: MS16/DCC_A_Sk symbol

Interfaces:

Table 77: MS16/DCC_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF	DCC_CI_D DCC_CI_CK DCC_CI_SSF

Processes:

The function separates DCC data from MS Overhead as defined in ETS 300 147 [2] and depicted in figure 91 [21].

Defects: None.

---

20 DCC transmission can be “disabled” when the matrix connection in the connected DCC_C function is removed.
21 DCC processing can be “disabled” when the matrix connection in the connected DCC_C function is removed.

Consequent Actions:

aSSF ← AI_TSF

Defect Correlations: None.

Performance Monitoring: None.

9.3.7 STM-16 Multiplex Section to P0x Adaptation Source MS16/P0x_A_So

Symbol:

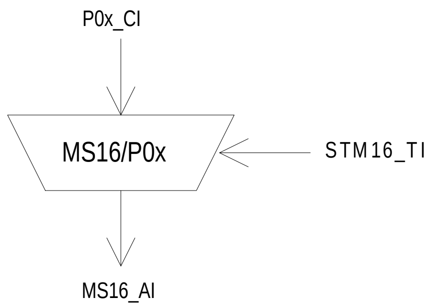


Figure 105: MS16/P0x_A_So symbol

Interfaces:

Table 78: MS16/P0x_A_So input and output signals

Input(s)	Output(s)
P0x_CI_D P0x_CI_CK P0x_CI_FS STM16_TI_CK STM16_TI_FS	MS16/P0x_AI_So_D

Processes:

This function provides the multiplexing of a 64 kbit/s orderwire information stream into the MS16_AI using slip buffering. It takes P0x_CI, defined in ETS 300 166 [3] as an unstructured bit-stream with a rate of 64 kbit/s ± 100 ppm, present at its input and inserts it into the MSOH byte E2 as defined in ETS 300 147 [2] and depicted in figure 91.

Frequency justification and bitrate adaptation: The function shall provide for an elastic store (slip buffer) process. The data signal shall be written into the store under control of the associated input clock. The data shall be read out of the store under control of the STM-16 clock, frame position, and justification decisions.

Each justification decision results in a corresponding negative/positive justification action. Upon a positive justification (slip) action, the reading of one 64 kbit/s octet (8 bits) shall be cancelled once. Upon a negative justification (slip) action, the same 64 kbit/s octet (8 bits) shall be read out a second time.

Buffer size: The elastic store (slip buffer) size shall be at least 2 octets.

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

Performance Monitoring: None.

9.3.8 STM-16 Multiplex Section to P0x Adaptation Sink MS16/P0x_A_Sk

Symbol:

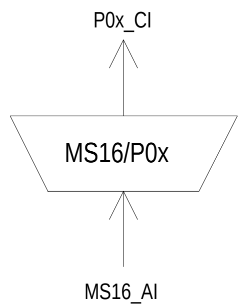


Figure 106: MS16/P0x_A_Sk symbol

Interfaces:

Table 79: MS16/P0x_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF	P0x_CI_Sk_D P0x_CI_Sk_CK P0x_CI_FS

Processes:

The function separates P0x data from MS Overhead byte E2 as defined in ETS 300 147 [2] and depicted in figure 91.

Smoothing and jitter limiting process: The function shall provide for a clock smoothing and elastic store (buffer) process. The data signal shall be written into the buffer under control of the associated (gapped) input clock. The data signal shall be read out of the buffer under control of a smoothed (equally spaced) 64 kHz clock (the rate is determined by the STM-16 signal generated at the remote node containing MS16/P0x_A_So). The residual jitter caused by pointer adjustments and octet slips (measured at the 64 kbit/s interface) shall be within the limits specified in TBD.

Buffer size: In the presence of jitter as specified by TBD and a frequency within the range 64 kbit/s ± 4.6 ppm, this justification process shall not introduce any errors.

Following a step in frequency of the P0x signal transported by the MS16_AI (for example due to a frequency step of the server STM-16 signal, or removal of all-ONEs (AIS) signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors.

The value of X is for further study; a value of 1 second has been proposed.

Defects: None.

Consequent Actions:

aAIS ← AI_TSF

On declaration of aAIS the function shall output an all-ONEs (AIS) signal - complying to the frequency limits for this signal (a bit rate in range 64 kbit/s ± 100 ppm) - within 1 ms; on clearing of aAIS the function shall output normal data within 1 ms.

Defect Correlations: None.

Performance Monitoring: None.

9.3.9 STM-16 Multiplex Section to Synchronisation Distribution Source MS16/SD_A_So

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

9.3.10 STM-16 Multiplex Section to Synchronisation Distribution Sink MS16/SD_A_Sk

The specification of this function will be addressed under work program prETS 300 417-6-1 [8].

9.4 STM-16 Multiplex Section Layer Monitoring Functions

For further study.

9.5 STM-16 Multiplex Section Linear Trail Protection Functions

9.5.1 STM-16 Multiplex Section Linear Trail Protection Connection Functions

9.5.1.1 STM-16 Multiplex Section 1+1 Linear Trail Protection Connection MS16P1+1_C

Symbol:

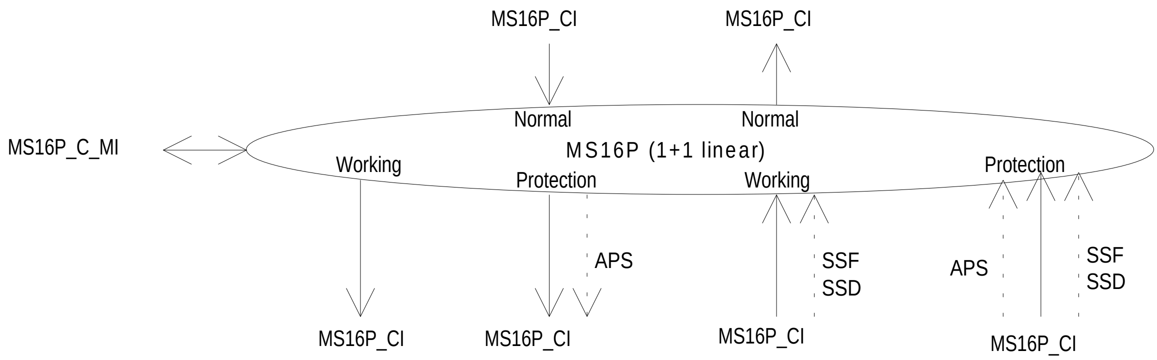


Figure 107: MS16P1+1_C symbol

Interfaces:

Table 80: MS16P1+1_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF MS16P_CI_SSD MS16P_C_MI_SFpriority MS16P_C_MI_SDpriority for connection points N and E: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS per function: MS16P_CI_APS MS16P_C_MI_SWtype MS16P_C_MI_OPERtype MS16P_C_MI_WTRTime MS16P_C_MI_HOTime MS16P_C_MI_EXTCMD	for connection points W and P: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF for connection points N and E: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF Note: protection status reporting signals are for further study. per function: MS16P_CI_APS MS16P_C_MI_cFOP MS16P_C_MI_pPSC

Processes:

The function performs the STM-16 linear multiplex section protection process for 1+1 protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 48 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #1 reference point can be the signal received via either the associated working #1 section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output is unsourced (no input connected) or connected to any normal input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 81

Architecture:	1 + 1
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1+1 switching, revertive operation) LO, FSw-#1, MSw-#1, CLR, EXER-#1 (1+1 switching, non-revertive operation) LO or FSw, FSw-#i, MSw, MSw-#i, CLR, EXER-#1

Defects: None.

Consequent Actions: None.

Defect Correlations: None.

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

9.5.1.2 STM-16 Multiplex Section 1:n Linear Trail Protection Connection MS16P1:n_C

Symbol:

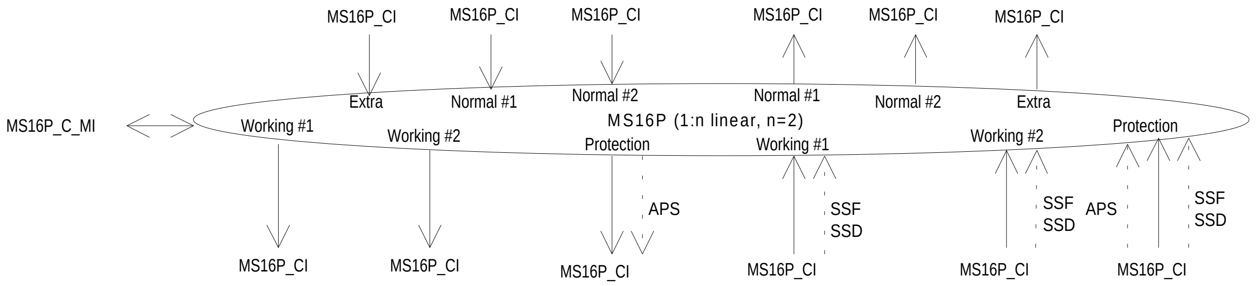


Figure 108: MS16P1:n_C symbol(s)

Interfaces:

Table 82: MS16P1:n_C input and output signals

Input(s)	Output(s)
for connection points W and P: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF MS16P_CI_SSD MS16P_MI_SFpriority MS16P_MI_SDpriority for connection points N and E: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS per function: MS16P_CI_APS MS16P_C_MI_SWtype MS16P_C_MI_OPERtype MS16P_C_MI_EXTRAtraffic MS16P_C_MI_WTRTime MS16P_C_MI_HOTime MS16P_C_MI_EXTCMD	for connection points W and P: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF for connection points N and E: MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF Note: protection status reporting signals are for further study. per function: MS16P_CI_APS MS16P_C_MI_cFOP MS16P_C_MI_pPSC

Processes:

The function performs the STM-16 linear multiplex section protection process for 1:n protection architectures; refer to ETS 300 417-1-1 [1], subclause 9.2. It performs the bridge and selector functionality as presented in figure 47 of ETS 300 417-1-1 [1]. In the sink direction, the signal output at the normal #i reference point can be the signal received via either the associated working #i section or the protection section; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal. In the source direction, the working outputs are connected to the associated normal inputs. The protection output is unsourced (no input connected), connected to the extra traffic input, or connected to any normal input.

Provided no protection switching action is activated/required the following changes to (the configuration of) a connection shall be possible without disturbing the CI passing the connection:

- change between switching types;
- change between operation types;
- change of WTR time.

MS Protection Operation: The MS trail protection process shall operate as specified in annex A, according the following characteristics.

Table 83

Architecture:	1:n (n ≤ 14)
Switching type:	single-ended or dual-ended
Operation type:	revertive or non-revertive
APS channel:	13 bits, K1[1-8] and K2[1-5]
Wait-To-Restore time:	in the order of 5-12 minutes
Switch, Hold-off time:	≤ 50 ms, not applicable
Signal switch conditions:	SF, SD
External commands:	(1:n switching, revertive operation) LO, FSw-#i, MSw-#i, CLR, EXER

Defects: None.

Consequent Actions:

For the case where neither the extra traffic nor a normal signal input is to be connected to the protection section output, the null signal shall be connected to the protection output. The null signal is either one of the normal signals, an all-ONEs, or a test signal.

For the case of a protection switch, the extra traffic output (if applicable) is disconnected from the protection input, set to all-ONEs (AIS) and aSSF is activated.

Defect Correlations:

cFOP ← {refer to annex A}

Performance Monitoring:

cPSC ← {refer to annex A}

9.5.2 STM-16 Multiplex Section Linear Trail Protection Trail Termination Functions

9.5.2.1 Multiplex Section Protection Trail Termination Source MS16P_TT_So

Symbol:

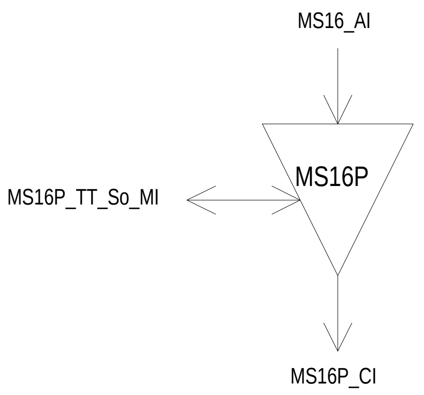


Figure 109: MS16P_TT_So symbol

Interfaces:

Table 84: MS16P_TT_So input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS	MS16P_CI_D MS16P_CI_CK MS16P_CI_FS

Processes:

No information processing is required in the MS16P_TT_So, the MS16_AI at its output being identical to the MS16P_CI at its input.

Defects: None.

Consequent Actions: None

Defect Correlations: None.

Performance Monitoring: None.

9.5.2.2 Multiplex Section Protection Trail Termination Sink MS16P_TT_Sk

Symbol:

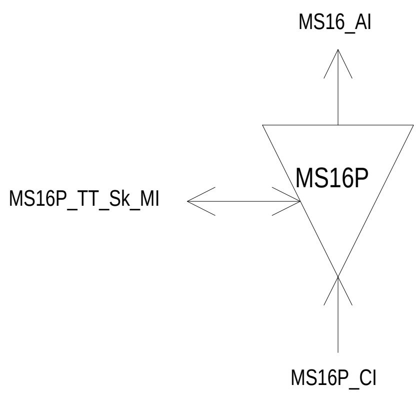


Figure 110: MS16P_TT_Sk symbol

Interfaces:

Table 85: MS16P_TT_Sk input and output signals

Input(s)	Output(s)
MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF MS16P_TT_Sk_MI_SSF_Reported	MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16P_TT_Sk_MI_cSSF

Processes:

The MS16P_TT_Sk function reports, as part of the MS16 layer, the state of the protected MS16 trail. In case all connections are unavailable the MS16P_TT_Sk reports the signal fail condition of the protected trail.

Defects: None.

Consequent Actions:

aTSF ← CI_SSF

Defect Correlations: None.

cSSF ← CI_SSF and SSF_Reported

Performance Monitoring: None.

9.5.3 STM-16 Multiplex Section Linear Trail Protection Adaptation Functions

9.5.3.1 STM-16 Multiplex Section to STM-16 Multiplex Section Protection Layer Adaptation Source MS16/MS16P_A_So

Symbol:

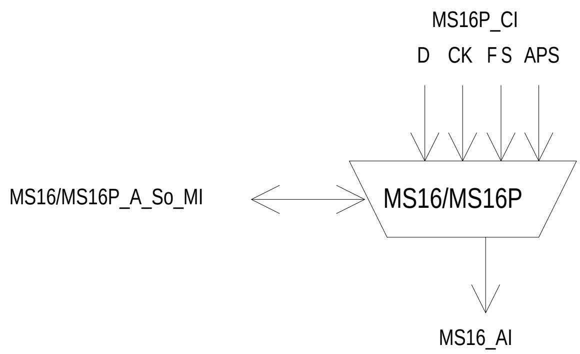


Figure 111: MS16/MS16P_A_So symbol

Interfaces:

Table 86: MS16/MS16P_A_So input and output signals

Input(s)	Output(s)
MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_APS	MS16_AI_D MS16_AI_CK MS16_AI_FS

Processes:

The function shall multiplex the MS16 APS signal and MS16 data signal onto the MS16 access point.

Defects: None.

Consequent actions: None.

Defect Correlations: None.

Performance Monitoring: None.

9.5.3.2 STM-16 Multiplex Section to STM-16 Multiplex Section Protection Layer Adaptation Sink MS16/MS16P_A_Sk

Symbol:

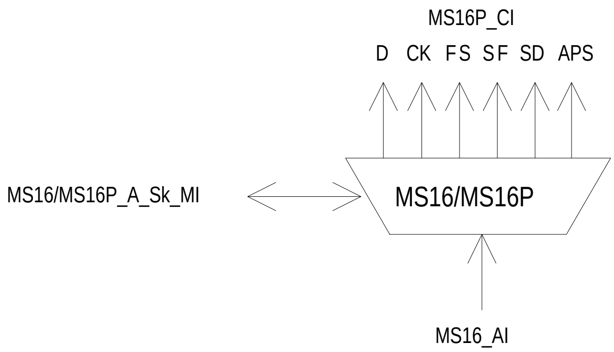


Figure 112: MS16/MS16P_A_Sk symbol

Interfaces:

Table 87: MS16/MS16P_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16_AI_TSD	MS16P_CI_D MS16P_CI_CK MS16P_CI_FS MS16P_CI_SSF MS16P_CI_SSD MS16P_CI_APS (for Protection signal only)

Processes:

The function shall extract and output the MS16P_CI_D signal from the MS16_AI_D signal.

K1[1-8]K2[1-5]: The function shall extract the 13 APS bits K1[1-8] and K2[1-5] from the MS16_AI_D signal. A new value shall be accepted when the value is identical for three consecutive frames. This value shall be output via MS16P_CI_APS. This process is required only for the protection section.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

aSSD ← AI_TSD

Defect Correlations: None.

Performance Monitoring: None.

9.6 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Functions

Figure 113 specifies the 2 fibre STM-16 MS SPRING protection sublayer atomic functions and the 2 fibre MS SPRING protection functional model.

For the characteristics of this protection scheme, see Annex E. The protection protocol and operation is specified in prETS 300 746 [6].

9.6.1 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Connection MS16P2fsh_C

Symbol:

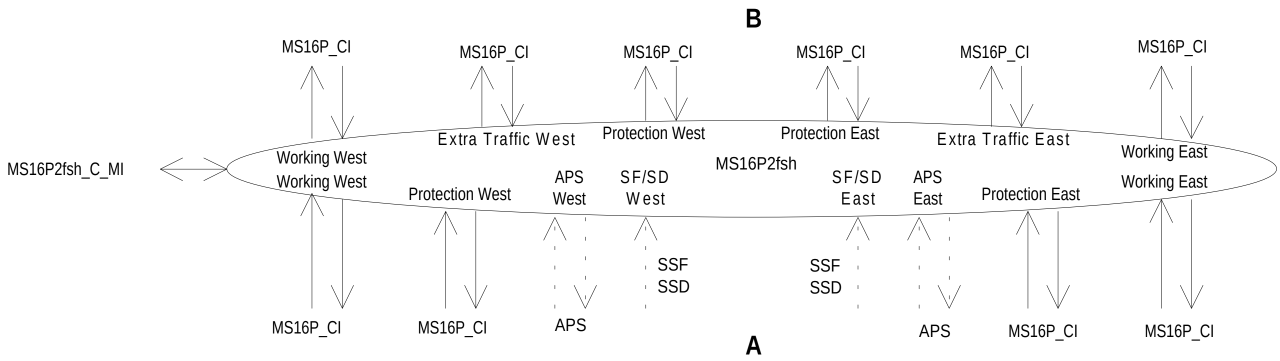


Figure 113: MS16P2fsh_C symbol

Interfaces:

Table 88: MS16P2fsh_C input and output signals

Input(s)	Output(s)
for connection points A West and A East: MS16P2fsh_CI_Dw MS16P2fsh_CI_Dp MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_SSF MS16P2fsh_CI_SSD MS16P2fsh_CI_APS for connection points B West and B East: MS16P2fsh_CI_Dw MS16P2fsh_CI_Dp MS16P2fsh_CI_De MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_MI_EXTRAtraffic MS16P2fsh_C_MI_WTRTime MS16P2fsh_C_MI_EXTCMD MS16P2fsh_C_MI_RingNodeID MS16P2fsh_C_MI_RingMap	for connection points A West and A East: MS16P2fsh_CI_Dw MS16P2fsh_CI_Dp MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_APS for connection points B West and B East: MS16P2fsh_CI_Dw MS16P2fsh_CI_CKw MS16P2fsh_CI_FSw MS16P2fsh_CI_SSFw MS16P2fsh_CI_Dp MS16P2fsh_CI_CKp MS16P2fsh_CI_FSp MS16P2fsh_CI_SSFp MS16P2fsh_CI_De MS16P2fsh_CI_CKe MS16P2fsh_CI_FSe MS16P2fsh_CI_SSFe Note: protection status reporting signals are for further study.

Processes:

The function is able to route (bridge and select) the Working and Protection group signals between its connection points (inputs/outputs) as specified in prETS 300 746 [6], multiplex section 2 fibre shared protection ring operation.

NOTE 1: The functional model is a maximum model; the extra traffic related inputs and outputs may not be present in an actual equipment.

Possible Matrix Connections that can be supported are:

Ww_A ↔ Ww_B
Pw_A ↔ Pw_B
Pw_A ↔ Ew_B
Pw_A ↔ We_B

We_A ↔ We_B
Pe_A ↔ Pe_B
Pe_A ↔ Ee_B
Pe_A ↔ Ww_B

Pw_A [TSx] ← all-ONEs (AIS)
Pw_A [TSx] ← unequipped HOVC

Pe_A [TSx] ← all-ONEs (AIS)
Pe_A [TSx] ← unequipped HOVC

APSw ↔ APSe (APS pass through)
APSw sourced
APSe sourced

legend: Xy_Z - X = Working, Protection, Extra traffic
y = west, east
Z = A, B
TSx - AU-4 TimeSlot #x (x = 1..16)

Table 89: MS16P2fsh_C traffic matrix connections

traffic matrix connections			OUTPUTS									
			A				B					
			Ww	Pw	We	Pe	Ww	Ew	Pw	We	Ee	Pe
INPUTS	A	Ww					X					
		Pw						X	X	X		
		We								X		
		Pe					X				X	X
	B	Ww	X			X						
		Ew		X								
		Pw		X								
		We		X	X							
		Ee				X						
		Pe				X						

In the sink direction (figure 113, from A to B), the signal output at the West [East] Working B MS16P2fsh connection point can be the signal received via either the associated West Working A capacity or the East Protection capacity; this is determined by the SF,SD conditions (relayed via CI_SSF,CI_SSD signals), the external commands and the information relayed via the APS signal.

In the source direction, the working A outputs are connected to the associated working B inputs. The protection A outputs are connected to a local unequipped VC generator, extra traffic input, or one of the working inputs at B as shown in figures 114 to 117.

NOTE 2: prETS 300 746 [6] states that protection AUs when not in use (for extra traffic or working traffic) must be source by VC unequipped signals. This must be performed in this MS16P2fsh_C functions as prETS 300 746 [6] also shows that the S4_C (S4-Xc_C) functions have permanent matrix connections for the protection timeslot capacity. The protection is a MS layer protection scheme and should not impact client layers. In the functional model, the MS16 layer knows the HO VC path multiplex structure, and is able to control HO VC unequipped signal insertion.

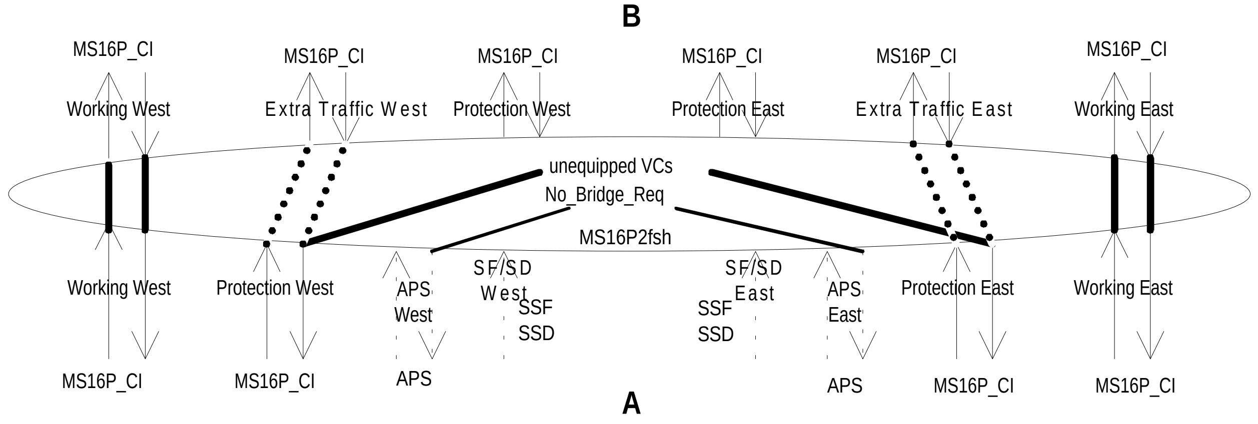


Figure 114: matrix connections in a network element within a ring without a fault; dotted lines represent the case of extra traffic support

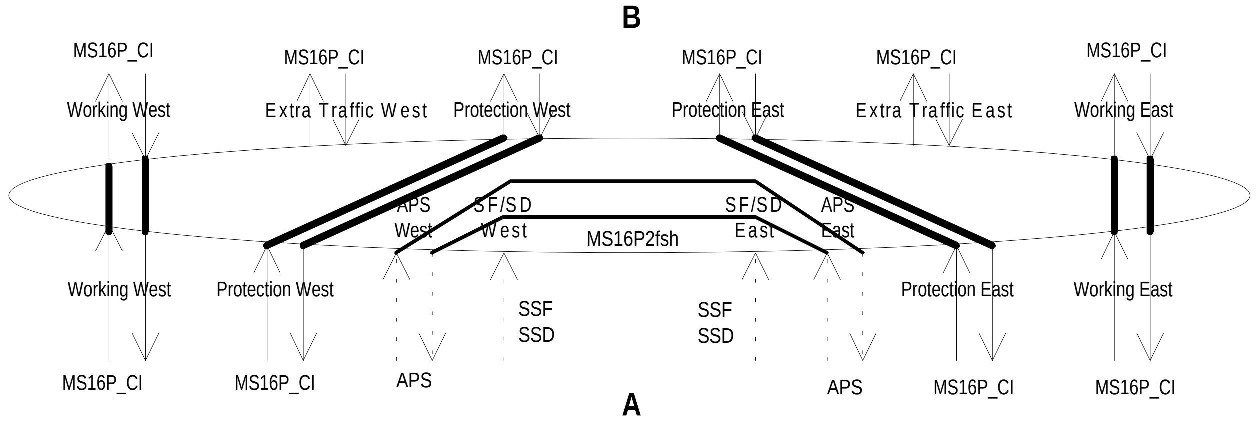


Figure 115: matrix connections in a network element not adjacent to a fault

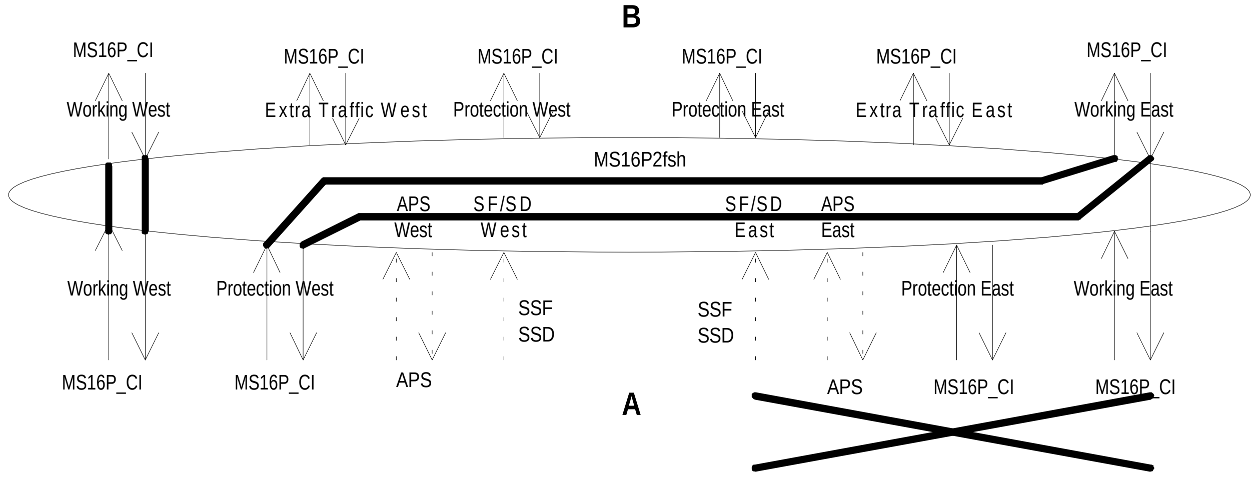


Figure 116: matrix connections in a network element adjacent to a fault on its East side

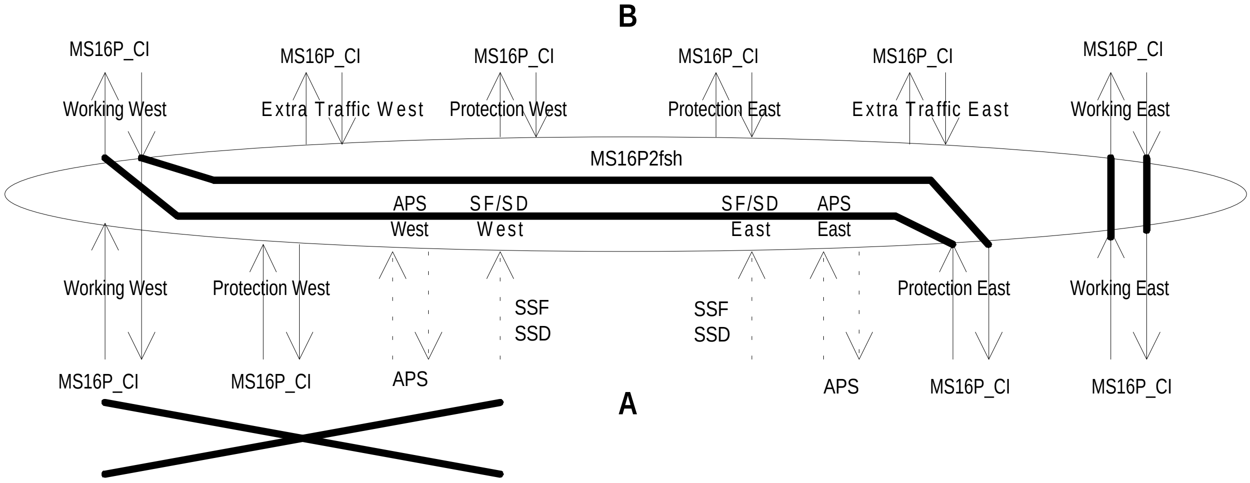


Figure 117: matrix connections in a network element adjacent to a fault on its west side

MS Protection Operation: The 2 fibre MS shared protection ring trail protection process shall operate as specified in prETS 300 746 [6].

Defects:

For further study.

Consequent Actions:

The function shall generate a VC-4 [VC-4-Xc] unequipped signal (plus valid AU-4 [AU-4-Xc] pointer) for each protection timeslot when the protection timeslot is not in use.

The function shall insert all-ONEs (AIS) (squelching) for an AU-4 [AU-4-xc] within protection timeslots that would otherwise be misconnected.

Defect Correlations:

For further study.

Performance Monitoring:

For further study.

9.6.2 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Trail Termination Functions

9.6.2.1 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Trail Termination Source MS16P2fsh_TT_So

Symbol:

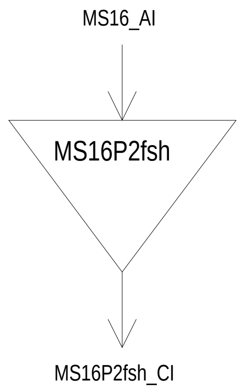


Figure 118: MS16P2fsh_TT_So symbol

Interfaces:

Table 90: MS16P2fsh_TT_So input and output signals

Input(s)	Output(s)
MS16P2fsh_AI_D MS16P2fsh_AI_CK MS16P2fsh_AI_FS	MS16P2fsh_CI_D MS16P2fsh_CI_CK MS16P2fsh_CI_FS

Processes:

No information processing is required in the MS16P2fsh_TT_So, the MS16_AI at its output being identical to the MS16P2fsh_CI at its input.

Defects: None.

Consequent Actions: None

Defect Correlations: None.

Performance Monitoring: None.

9.6.2.2 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Trail Termination Sink MS16P2fsh_TT_Sk

Symbol:

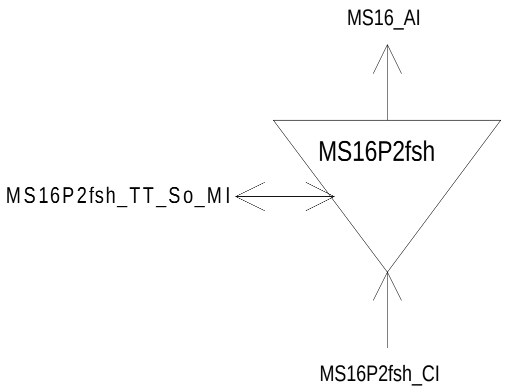


Figure 119: MS16P2fsh_TT_Sk symbol

Interfaces:

Table 91: MS16P2fsh_TT_Sk input and output signals

Input(s)	Output(s)
MS16P2fsh_CI_D MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_SSF MS16P2fsh_TT_Sk_MI_SSF_Reported	MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16P2fsh_TT_Sk_MI_cSSF

Processes:

The MS16P2fsh_TT_Sk function reports, as part of the MS16 layer, the state of the protected MS16 trail. In case all connections are unavailable the MS16P2fsh_TT_Sk reports the signal fail condition of the protected trail. This is applicable only for the working capacity.

Defects: None.

Consequent Actions:

aTSF ← CI_SSF

Defect Correlations:

cSSF ← CI_SSF and SSF_Reported

Performance Monitoring: None.

9.6.3 STM-16 Multiplex Section 2 Fibre Shared Protection Ring Adaptation Functions

9.6.3.1 STM-16 Multiplex Section to STM-16 Multiplex Section 2 Fibre Shared Protection Ring Adaptation Source MS16/MS16P2fsh_A_So

Symbol:

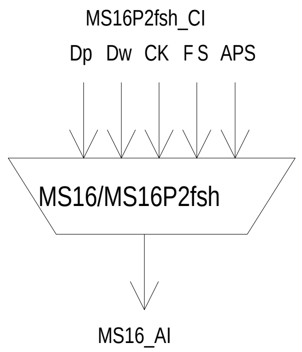


Figure 120: MS16/MS16P2fsh_A_So symbol

Interfaces:

Table 92: MS16/MS16P2fsh_A_So input and output signals

Input(s)	Output(s)
MS16P2fsh_CI_Dw MS16P2fsh_CI_Dp MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_APS	MS16_AI_D MS16_AI_CK MS16_AI_FS

Processes:

The function shall multiplex two groups of signals (CI_Dw, CI_Dp) into the MS16 payload (16 AU-4 timeslots). The working group signal shall be multiplexed into AU-4 timeslots 1 to 8 and the protection group signal shall be multiplexed into AU-4 timeslots 9 to 16.

The function shall map the MS16 2 fibre shared protection ring APS signal into bytes K1 and K2.

Defects: None.

Consequent actions: None.

Defect Correlations: None.

Performance Monitoring: None.

9.6.3.2 STM-16 Multiplex Section to STM-16 Multiplex Section 2 Fibre Shared Protection Ring Adaptation Sink MS16/MS16P2fsh_A_Sk

Symbol:

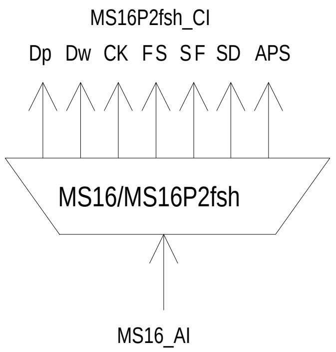


Figure 121: MS16/MS16P2fsh_A_Sk symbol

Interfaces:

Table 93: MS16/MS16P2fsh_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D MS16_AI_CK MS16_AI_FS MS16_AI_TSF MS16_AI_TSD	MS16P2fsh_CI_Dw MS16P2fsh_CI_Dp MS16P2fsh_CI_CK MS16P2fsh_CI_FS MS16P2fsh_CI_SSF MS16P2fsh_CI_SSD MS16P2fsh_CI_APS

Processes:

The function shall split the MS16 payload (i.e. 16 AU-4 timeslots) into two groups; the working group contains AU-4 timeslots 1 to 8 and the protection group contains AU-4 timeslots 9 to 16. The working group shall be output at MS16P2fsh_CI_Dw and the protection group at MS16P2fsh_CI_Dp.

K1K2: The function shall extract the 16 APS bits K1[1-8] and K2[1-8] from the MS16_AI_D signal. A new value shall be accepted when the value is identical for three consecutive frames. This value shall be output via MS16P2fsh_CI_APS.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

aSSD ← AI_TSD

Defect Correlations: None.

Performance Monitoring: None.

9.7 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Functions

For further study.

9.7.1 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Connection MS16P4fsh_C

For further study.

9.7.2 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Trail Termination Functions

9.7.2.1 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Trail Termination Source MS16P4fsh_TT_So

For further study.

9.7.2.2 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Trail Termination Sink MS16P4fsh_TT_Sk

For further study.

9.7.3 STM-16 Multiplex Section 4 Fibre Shared Protection Ring Adaptation Functions

9.7.3.1 STM-16 Multiplex Section to STM-16 Multiplex Section 4 Fibre Shared Protection Ring Adaptation Source MS16/MS16P4fsh_A_So

For further study.

9.7.3.2 STM-16 Multiplex Section to STM-16 Multiplex Section 4 Fibre Shared Protection Ring Adaptation Sink MS16/MS16P4fsh_A_Sk

For further study.

10 STM-64 Regenerator Section layer functions

For further study.

11 STM-64 Multiplex Section layer functions

For further study.

Annex A (normative): Generic specification of linear protection switching operation

NOTE 1: The text in this annex is a reworked copy of Annex A of ITU-T Recommendation G.783 [5] and presents an attempt to formalise the protection process specification to remove ambiguities present in ITU-T Recommendation G.783 [5].

The protection process described in this annex supports linear trail protection (ETS 300 417-1-1 [1], subclause 9.3.1) as well as linear connection (subnetwork, network) protection (ETS 300 417-1-1 [1], subclauses 9.4.1 and 9.4.2) in the combinations as listed in table A.1. This protection process controls the bridge and selector functionality (ETS 300 417-1-1 [1], subclause 9.2, figures 47, 49).

Table A.1: Supported linear protection process combinations

Protection type	Architecture type	Switching type	Operation type	APS signal	Extra traffic
MS-n trail	1+1	single-ended	non-revertive	yes	no
MS-n trail	1+1	single-ended	revertive	yes	no
MS-n trail	1+1	dual-ended	non-revertive	yes	no
MS-n trail	1+1	dual-ended	revertive	yes	no
MS-n trail	1:n (n ≤ 14)	dual-ended	revertive	yes	no
MS-n trail	1:n (n ≤ 14)	dual-ended	revertive	yes	yes
VC-m SNC/I	1+1	single-ended	non-revertive	no	no
VC-m SNC/I	1+1	single-ended	revertive	no	no
VC-m SNC/N	1+1	single-ended	non-revertive	no	no
VC-m SNC/N	1+1	single-ended	revertive	no	no
VC-m trail	1+1	single-ended	non-revertive	no	no
VC-m trail	1+1	single-ended	revertive	no	no
VC-m trail	1+1	dual-ended	non-revertive	yes	no
VC-m trail	1+1	dual-ended	revertive	yes	no

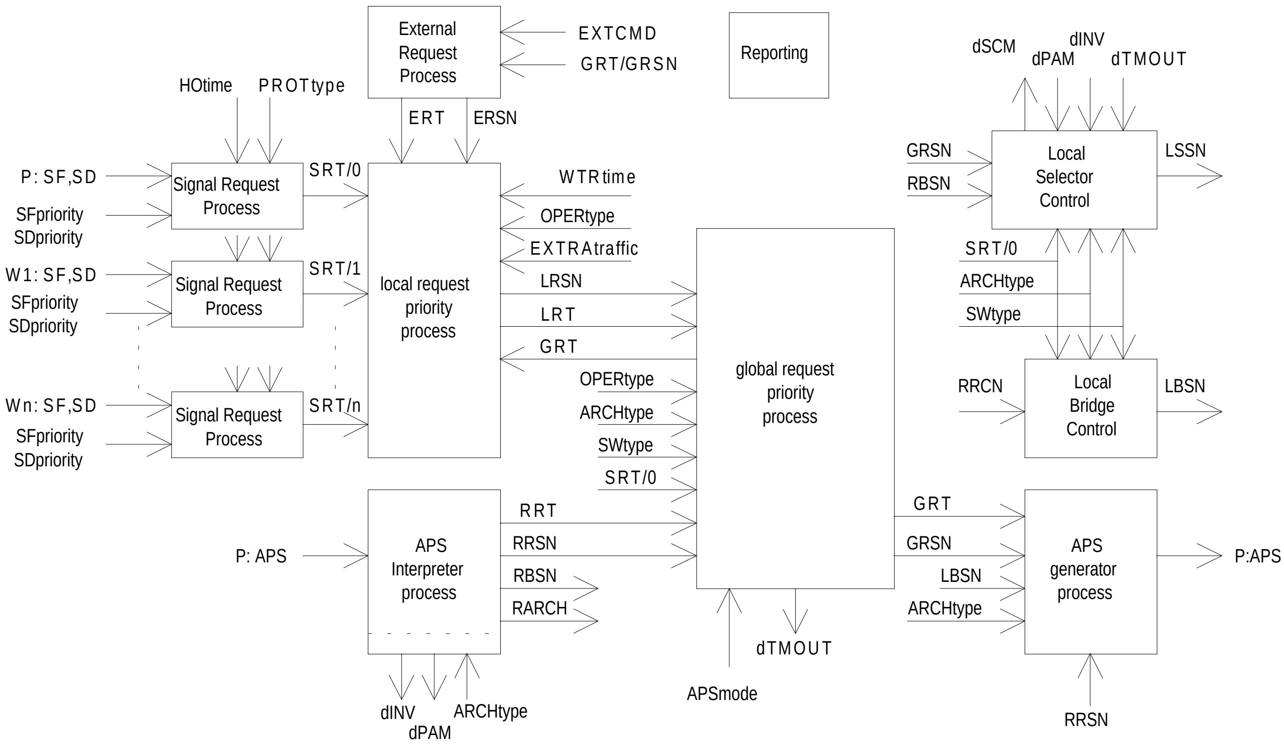
NOTE 2: Dual-ended switched 1+1 VC-m trail protection requires the definition and bit allocation of the VC-APS signal.

The remainder of this annex is organised as follows:
- protection process overview;
- external commands definition;
- conditions of protected trail/connection signals;
- states within protection process;
- numbering of working, protection, normal, extra traffic and null signals;
- numbering and priority of external commands, trail/connection signal conditions, and states;
- automatic protection switch (APS) signal definition;
- specification of subprocesses within protection process.

A.1 Protection process overview

Linear protection processes can be characterised by the following (super)set of subprocesses (figure A.1):

Signal Request	converts SF and SD signals of a working/protection trail/connection signal into a (signal) request type and trail/connection number
External Request	converts the external commands into an (external) request type and signal number
Local Request Priority	determines the highest priority local request
APS Interpretation	converts the APS signal into a (remote) request type, request signal number, bridged signal number, and architecture type (if applicable)
Global Request Priority	determines the highest global request type comparing local and remote (if applicable) requests
Local Bridge Control	determines which of the normal/extra traffic signals is bridged to the protection trail/connection
Local Selector Control	determines which of the normal/extra traffic signals is connected to/extracted from the protection trail/connection
APS Generation	converts the global request type, global request signal number, local bridged signal number, and local architecture into the APS signal
Reporting	reports the status (local, remote) of the protection process; remote status if APS signal is supported



LRT:	Local Request Type
LRSN:	Local Request Signal Number
LBSN:	Local Bridge Signal Number
LSSN:	Local Selector Signal Number
RRT:	Remote Request Type
RRSN:	Remote Request Signal Number
RBSN:	Remote Bridge Signal Number
RARCH:	Remote Architecture Type
ERT:	External Request Type
ERSN:	External Request Signal Number
GRT:	Global Request Type
GRSN:	Global Request Signal Number
SRT:	Signal Request Type
SRSN:	Signal Request Signal Number

Figure A.1: Subprocesses within generic linear trail/connection protection processes

A specific protection application is characterised by the following parameter set:

Table A.2

Parameter	Value options
Architecture type (ARCHtype)	1 + 1, 1:n
Switching type (SWtype)	single-ended, dual-ended
Operation type (OPERtype)	revertive, non-revertive
APS signal (APSmode)	true, false
Wait-To-Restore time (WTRtime)	in the order of 5-12 minutes
Switch time	50 ms
Hold-off time (HOtime)	0 to 10 seconds in steps of the order of 100 ms
Protection type (PROTtype)	SNC/I, SNC/N, SNC/S, trail
Signal switch conditions:	SF = SSF (SNC/I) SF = TSF (SNC/N, SNC/S, trail), SD = TSD (SNC/N, SNC/S, trail)
External commands (EXTCMD)	LO-#0, FSw-#i, MSw-#i, EXER-#i, CLR
Extra traffic (EXTRAtraffic)	true, false

A.2 External switch commands definition

A switch command issues an appropriate external request. Only one switch request can be issued per protection group. Switch commands are listed below in the descending order of priority and the functionality of each is described.

The function shall generate an automatic response confirming that the request was executed, or stating that the request was denied for a particular reason.

1) Clear (CLR): Clears all switch commands listed below.

2) Lockout of protection (LO): Request to deny all normal signals (and the extra traffic signal, if applicable) access to the protection trail/connection.

3) Forced switch #i (FSw-#i): Request to switch normal signal #i ($1 \leq i \leq n$, $n \leq n_{max}$) to the protection trail/connection, or request to switch extra traffic signal #n_{max}+1 to the protection trail/connection, or (for the case of 1+1 non-revertive systems) request (FSw-#0) to switch normal signal to working trail/connection.

   NOTE 1: Request is honoured unless an equal or higher priority switch command is in effect or (for the case an APS signal is in use) SF condition exists on the protection trail/connection. If the request is denied, it is released and forgotten.

   NOTE 2: For 1 + 1 non-revertive systems, "forced switch no normal signal (FSw-#0)" transfers the normal signal from protection to the working trail/connection, unless an equal or higher priority request is in effect. Since forced switch has higher priority than SF or SD on the working trail/connection, this command will be carried out regardless of the condition of the working trail/connection.

   NOTE 3: For 1: n architectures, “forced switch to extra traffic (FSw-#n_{max}+1)” forces the extra traffic signal to the protection trail/connection and prevents normal signals to be transported over protection.

4) Manual switch #i (MSw-#i): Request to switch normal signal #i ($1 \leq i \leq n$, $n \leq n_{max}$) to the protection trail/connection, or (for the case of 1+1 non-revertive systems) request (MSw-#0) to switch normal signal to working trail/connection.

   NOTE 4: Request is honoured unless a defect condition exists on other trail/connections (including the protection trail/connection) or an equal or higher priority switch command is in effect. If the request is denied, it is released and forgotten.

   NOTE 5: For 1 + 1 non-revertive systems, "manual switch no normal signal (MSw-#0)" transfers the normal signal back from protection to the working trail/connection, unless an equal or higher priority request is in effect. Since manual switch has lower priority than SF or SD on a working trail/connection, this command will be carried out only if the working trail/connection is not in SF or SD condition.

5) Exercise #i (EXER-#i): Request for an exercise to check responses on APS bytes for normal signal #i ($1 \leq i \leq n$, $n \leq n_{max}$). The switch is not actually completed, i.e. the selector is released by an exercise request on either the sent or the received and acknowledged K1 byte.

   NOTE 6: Request is honoured unless the protection signal is in use.

The following table presents alternative user interface external command strings for the case of 1+1 protection architectures. Note that the generic names will be used in this ETS.

Table A.3

generic	alternative for 1+1 revertive	alternative for 1+1 non-revertive	result
LO (#0)	LO	-	normal signal connected to working trail/connection
FSw-#0	-	FSw-(to)-W	normal signal connected to working trail/connection
FSw-#1	FSw-(to)-P	FSw-(to)-P	normal signal connected to protection trail/connection
MSw-#0	-	MSw-(to)-W	normal signal connected to working trail/connection
MSw-#1	MSw-(to)-P	MSw-(to)-P	normal signal connected to protection trail/connection

A.3 Conditions of working and protection trail/connections

Working and protection trail/connection (signals) have a condition associated with them: fault free, signal fail, signal degrade. The condition is communicated with the protection process by means of the SF and SD signals within the characteristic or adapted information of the working/protection trail/connection signal.

A.4 States within protection process

The protection process has a number of so called states associated with it: no request, do not revert, reverse request, and wait to restore. A description of the effect of the states is presented below:

Wait to restore (WTR): In the revertive mode of operation, the normal signal will be restored (i.e. the signal on the protection trail/connection will be switched back to the working trail/connection) when the working trail/connection has recovered from the fault.

To prevent frequent operation of the selector due to an intermittent fault, a failed working trail/connection must become fault-free. After the failed trail/connection meets this criterion, (and no other externally initiated commands are present) a fixed period of time will elapse before it is used again by the normal signal. During this WTR state, switching will not occur.

An SF or SD condition will override the WTR. After the WTR period is completed, a No Request state will be entered. Switching will then occur from the protection trail/connection to the working trail/connection.

Reverse request: For the case of dual-ended switching, a reverse request is returned for exerciser and all other requests of higher priority. This clearly identifies which end originated the switch request.

If the head end had also originated an identical request (not yet confirmed by a reverse request) for the same signal, then both ends would continue transmitting (in the APS signals) the identical request type (RT) and signal number (RSN) and perform the requested switch action.

In single-ended switching, reverse request is never indicated.

Both wait-to-restore and do not revert requests in the RT fields of the transmitted APS signal are normally acknowledged by a reverse request in the RT field of the received APS signal. However, no request is acknowledged by another no request received.

Do not revert: In the non-revertive mode of operation, assuming the normal signal is on protection when the working trail/connection is repaired or a switch command is released, the tail end maintains the selection and issues LRT/LRSN = DNR/1 (do not revert for normal signal 1).

For the case of dual-ended switching, the head end also maintains the selection and continues indicating reverse request. The do not revert is removed when pre-empted by a defect condition or an external request.

No request: This state represents the inactive state of the request processes (signal, external, local, remote, and global request processes). None of the trail/connection signal conditions is active, none of the external commands is active, and none of the states described above is active.

A.5 Numbering of working, protection, normal, extra traffic, null signals

The protection trail/connection shall be referred to as number “0”. The working trails/connections are numbered “1”, “2”, etc. The assignment of these numbers to physical entities in a network element is equipment specific and not within the scope of this ETS.

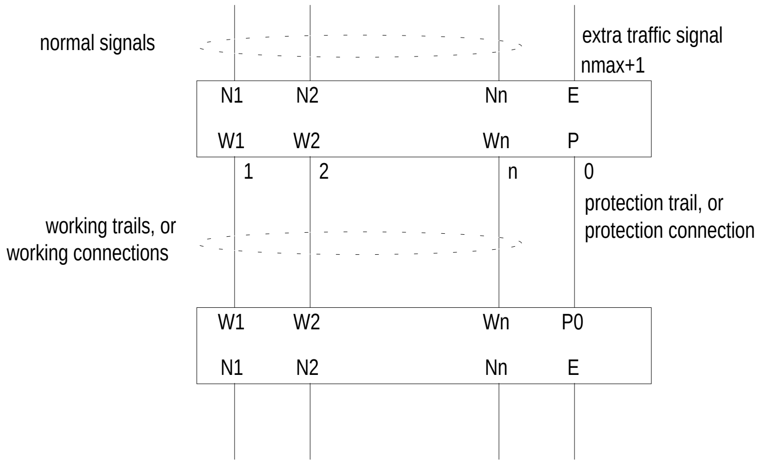


Figure A.2: Definitions of working trail/connection, protection trail connection, normal and extra traffic signal

The normal signals shall be numbered (equivalent to the working trails/connections) “1”, “2”, etc. In 1:n (n = 1,2,3,..,n_{max}) protection architectures normal signal #i shall be transported over working trail/connection #i or over the protection trail/connection. For the case of section layer protection, the assignment of these numbers to physical entities in a network element is equipment specific and not within the scope of this ETS. For the case of path layer protection, the assignment of these numbers to physical entities in a network element shall be provisionable via configuration management.

NOTE: The value of n_{max} is protection application dependent.

The extra traffic signal (supported in 1:n architectures only) shall be referred to as number n_{max}+1. The extra traffic signal shall be transported over the protection trail/connection when this one is not transporting a normal signal and the protection trail/connection is not “locked out”.

The null signal, present in 1:n architectures only, shall be referred to as number “0”. When none of the normal signals nor an extra traffic signal is transported over the protection trail/connection, the null signal shall be transported. This can be any signal (e.g. one of the normal signals, a test signal, an all-ONEs signal).

A.6 Priority of request types (conditions, external commands, states)

A request can be a local or remote:

1) condition (SF and SD) associated with a working or protection trail/connection. A condition has high or low priority.
2) state (wait-to-restore, do not revert, no request, reverse request) of the protection process.
3) external request (lockout of protection trail/connection, forced or manual switch of normal/extra traffic signal, exercise).

The basic priorities of the requests shall be as specified by table A.4. In addition, a SF-H or SF-L condition of the protection trail/connection has priority over FSw when an APS signal is supported.

NOTE: Requests are selected from the table, depending on the protection switching arrangements; i.e. in any particular case, only a subset of the requests may be required.

Table A.4: Request Type (RT) priority

Request Type with APS	Request Type without APS	Priority
LO	LO	highest
SF-H, SF-L on protection trail/connection	-	|
FSw	FSw	|
SF-H	SF-H	|
SF-L	SF-L	|
SD-H	SD-H	|
SD-L	SD-L	|
MSw	MSw	|
WTR	WTR	|
EXER	EXER	|
RR	RR	|
DNR	DNR	|
NR	NR	|
INV	-	lowest

A.7 Aps signal definition

A.7.1 APS signal fields

An automatic protection switch (APS) signal performs the communication function between the protection processes at the two ends of the protection span. For a linear protection application the following information will be passed:

- request type (RT);
- request signal number (RSN);
- local bridged signal number (LBSN);
- local architecture type (ARCH) (application dependent).

RT: 4 bits indicate the type of request, as listed in table A.5.

Table A.5: Request Type mapping into APS signal

RT	code in RT field [MSB-LSB]
NR	0000
DNR	0001
RR	0010
EXER	0100
WTR	0110
MSw	1000
SD-L	1010
SD-H	1011
SF-L	1100
SF-H	1101
FSw	1110
LO	1111

RSN: M bits [22] indicate the number of the signal (normal, extra, trail, connection) for which the request is issued, as shown in table A.6. The coding in the RSN field of the APS signal is binary.

Table A.6: Request signal number

Signal number	Refers to requesting switch action for
0	
1 to n_{max}	
n_{max}+1	

LBSN: M bits (M is application dependent) indicate the number of the signal (null, normal, or extra) that is bridged to the protection trail, as shown in table A.7. The coding in the LBSN field of the APS signal is binary.

Table A.7: Local bridged signal number

Signal number	Indication of
0	
1 to n_{max}	
n_{max}+1	

22 M is application dependent.

ARCH: 1 bit indicates the type of the architecture as shown in table A.8:

Table A.8: architecture type

ARCH	Architecture type
0	1 + 1
1	1 : n

A.7.2 STM-N MS-APS

The APS signal for 1+1 and 1:n linear STM-N MS protection consists of 13 bits organised in 4 groups as depicted in figure A.3. Refer to prETS 300 746 [6].

K1								K2				
1	2	3	4	5	6	7	8	1	2	3	4	5
request type				request signal number				local bridged signal number				arch

Figure A.3: STM-N MS-APS definition

A.7.3 STM-N VC-APS

VC APS definition and bit allocation is for further study.

Figure A.4: VC APS definition (to be defined)

A.8 Switch performance: switching and holdoff times

For automatically initiated conditions (i.e. SF and SD), the protection switch completion time shall be less than X ms. Protection switch completion time excludes the detection time necessary to initiate the protection switch, and hold-off time. It includes the transmission transfer delay time when dual-ended switching is selected.

NOTE 1: The trail/connection protection shall operate as fast as possible. A value of 50 ms has been proposed as a target switch completion time X. Concerns have been expressed over this proposed target time when many trails/connections are involved. This is for further study.

NOTE 2: When dual-ended switching is required, the transfer delay time may limit the length of the protected trail/connection. This is due to the transfer delay of protection information that is to be communicated between the two ends via the APS signals. Alternatively, the protection switch time for such a case could be defined as a value with 3 components: a fixed (basic) value, the length of the protection trail/connection, and the number of network elements and their processing level (e.g. AU only, AU and TU). This is for further study.

Hold-off times are useful for inter-working of protection schemes. The objective is that these times should be provisionable on an individual basis. The defect condition should be continuously monitored for the full duration of the hold-off time before switching occurs. The hold-off time should therefore be provisionable from 0 to 10 seconds in steps of TBD.

The service interruption due to the switching on an external command (CLR, LO, FSw, MSw) shall be limited to the switch-over time.

A.9 Subprocesses

This subclause specifies in a more or less formal manner the operation of the subprocesses within the protection process.

NOTE 1: SDL specification for the following pseudo code is for further study.

Signal request (type & signal number) processes

This process shall transfer the input SF and SD signals from a trail/connection (either protection (#0), or working #1, .. , or working #n) into a Signal Request Type (SRT) and Signal Request Signal Number (SRSN):

- The SRSN shall be "0" (zero) for the protection trail/connection and "i" ($1 \leq i \leq n$) for working trail/connection #i.
- The SRT shall be generated based on the inputs SF, SD, SFpriority, SDpriority, as follows:

```
if ( (SF==true) and (HOtimer==0) )
then   if (SFpriority==high)
       then SRT= SF-H
       else SRT=SF-L
       fi
else   if ( (SD==true) and (HOtimer==0) )
       then if (SDpriority==high)
            then SRT=SD-H
            else SRT=SD-L
            fi
       else SRT= NR
       fi
fi
```

A HoldOff timer (HOtimer) shall be supported. The holdoff period (HOtime) shall be provisionable in the order of 0 - 10 seconds, in steps of X ms. The timer shall be set to the provisioned value when the SF and SD defect conditions are cleared. The timer shall be started at the provisioned value when the SF or SD defect condition activates. The HO timer shall count down to zero.

The value of X is for further study.

External request (type & signal number) process

This process shall transfer the external commands (EXTCMD) into an External Request Type (ERT) and External Request Signal Number (ERSN):

- The ERSN shall be "0" (zero) if no normal signal is indicated, "i" ($1 \leq i \leq n_{max}$) for normal signal #i, and "n_{max}+1" for the extra traffic signal
- The ERT/ERN shall be generated as follows:

```
do on external command reception
       start 50 ms Completion Timer (CTimer)
       if (EXTCMD==clear)
       then ERT=NR
            ERSN=0
       else if (EXTCMD==lockout of protection)
            then   ERT=LO
                   ERSN=0
            else   if (EXTCMD==forced switch-#i)
                   then   ERT=FSw
                          ERSN=#i
                   else   if (EXTCMD==manual switch-#i)
                          then   ERT=MSw
                                 ERSN=#i
                          else   if (EXTCMD==exercise-#i)
                                 then   ERT=EXER
                                        ERSN=#i
                                 fi
                          fi
                   fi
            fi
       fi
```

```
        wait until CTimer expires
        then {check if FSw request is denied, then release external (FSw) request}
            if (ERT==FSw) and not [ ((GRT==FSw) or (GRT==RR)) and (GRSN==ERSN) ]
            then  ERT=NR
                  ERSN=0
            fi
            {after 50 ms MSw and EXER external requests will be terminated}
            if (ERT==MSw) or (ERT==EXER)
            then  ERT=NR
                  ERSN=0
            fi
        taiw
    od
```

Local request (type & signal number) priority process

This process shall determine the highest priority local request. It shall evaluate the status of the protection and working input signals (SRT/SRSN #0 to SRT/SRSN #n), the external command (ERT/ERSN), and protection parameters OPERtype and EXTRAtraffic by a three step priority logic:

1) The highest priority local request shall be determined over the set of SRT/0, SRT/1, .., SRT/n, ERT inputs based on the descending order of request type priorities in table 93;

2) If there is at least one SRT that is higher than the ERT, and if two or more trails/connections (working/protection) have the same highest request type (SRT), the trail/connection with the lowest number shall take priority, unless the priority of the highest SRT is identical to the current LRT.

NOTE 2: The protection trail/connection has the highest priority due to its number (#0).

NOTE 3: When normal signal number B is already transported via the protection trail/connection, it will not be replaced by normal signal number A (A < B) if both working trail/connection A and working trail/connection B have the same defect condition with the same priority (i.e. SRT/A == SRT/B is e.g. SF-H).

3) If highest priority request (SRT, ERT) detected under 1. and 2. is no-request (NR), the LRT depends on the history of the protection process, the operation type, and the presence of an extra traffic signal.

The following pseudo code describes this 3 step process:

```
    RTnew = ERT              {initialise process}
    LRSNnew=ERSN
    LRsource=external
    for i==0 to n
    do                       {find highest priority local request active}
        if (LRTnew < SRT/i)
        then LRTnew=SRT/i
            LRSNnew=i
            LRsource=signal
        fi
    od
    if LRTnew==NR)
    then                     {No-Request case}
        if (OPERtype==non-revertive)
        then                 {non-revertive case}
            if (LRSN==1)     {check if do not revert needs to be generated}
            then LRT= DNR
            else LRT=NR
            fi
```

```
          else                          {revertive case}
              if ( ((LRT==SF) or (LRT==SD) or (LRT==WTR)) and (WTRtimer > 0) )
              then          {previous request was a SF or SD, or a WTR running}
                  LRT=WTR
              else                  {previous request was no-request}
                  LRT=NR
                  if (EXTRAtraffic==true)
                  then          {extra traffic supported}
                                LRSN=n_max+1
                  else          {extra traffic not supported}
                                LRSN=0
                  fi
              fi
          fi
      else                              {Request case}
          if (LRsource==external)
          then                          {external local request has highest priority}
              LRT=LRTnew
              LRSN=LRSNnew
          else                          {a signal has highest local request priority}
              if (LRTnew≠LRT)
              then                  {new request not equal to existing local request}
                  LRT=LRTnew
                  LRSN=LRSNnew
              else                  {new request equal to existing local request}
                  if (SRT/LRSN≠LRTnew)
                  then          {existing local request source has changed request}
                      LRSN=LRSNnew
                  fi
              fi
          fi
      fi
```

In revertive mode of operation a wait-to-restore timer (WTRtimer) shall be supported. The wait-to-restore period (WTRtime) shall be provisionable in the order of 5 - 12 minutes, in steps of Y seconds. The timer shall be set to the provisioned value when the SF or SD defect condition is active (LRT=SF or LRT=SD). The timer shall be started when the last defect condition (SF, SD) clears; i.e. when all SRTs indicate No Request (NR). The WTR timer shall count down to zero. The WTR timer shall be reset to zero (deactivates earlier) if the Global Request Type (GRT) no longer indicates wait-to-restore, i.e. when any request of higher priority pre-empts this state.

The value of Y is for further study.

APS interpretation process

This process shall translate the accepted APS signal into the signals Remote Request Type (RRT), Remote Request Signal Number (RRSN), Remote Bridged Signal Number (RBSN) and Remote Architecture type (RARCH), as follows:

- RRT as specified in table A.9.
- RRSN = AcRSN
- RBCN = AcLBSN
- RARCH = AcARCH.

NOTE 4: AcRSN and AcLBSN can be out of range due to a fault or bit errors. For such case an invalid defect will be detected. See below.

Table A.9: Remote Request Type (RRT) interpretation from APS signal

AcRT	RRT
0000	NR
0001	DNR
0010	RR
0011	invalid
0100	EXER
0101	invalid
0110	WTR
0111	invalid
1000	MSw
1001	invalid
1010	SD-L
1011	SD-H
1100	SF-L
1101	SF-H
1110	FSw
1111	LO

Defects:

If the received APS Architecture (RARCH) value differs from the local architecture type (ARCHtype) for a period of 50 ms, a Protection Architecture Mismatch defect (dPAM) shall be detected. The defect shall be cleared when the there is a match again.

If the request type bits (RT) in the APS signal indicate an invalid request code, or the RSN or LBSC indicate a non-existing trail/connection/normal signal number, an invalid command defect (dINV) shall be detected when the condition exist for Y ms. The defect shall be cleared when the RT indicate a valid code and the RSN or LBSN indicate an existing signal number.

Global request priority process

The local request (LRT,LRSN) and the remote request (RRT,RRSN) shall be compared to decide which has priority. The priority shall be determined according to the descending order of priorities in table A.4. Note that a received reverse request shall not be considered in the comparison.

The result, Global Request Type (GRT) and Global Request Signal Number (GRSN) shall be determined as follows:

```
if ( (SWtype==dual-ended) and (SRT/0≠SF) and (RRT≠RR) and
          [ (RRT>LRT) or
           ((RRT==LRT) and (GRT==RR)) or
           ((RRT==LRT) and (GRT≠RR) and (RRSN<LRSN)) ] )
then                {dual ended switching, no SF on protection trail/connection, no reverse
                     request, and either "remote request overrules local request" or "remote
                     request equals local request and was already accepted" or "remote
                     request equals local request and remote signal number is lower than
                     local signal number"}
          GRT=RR
          GRSN=RRSN
else                {single ended switching or SF on protection trail/connection or reverse
                     request received or local request overrules remote request or local and
                     remote requests are equal and local signal number is less or equal
                     remote signal number}
          GRT=LRT
          GRSN=LRSN
fi
```

NOTE 5: Refer to subclause A.4.

Defects:

If a head end response on a tail end request does not comply to the protocol (i.e. “not (RRT==RR or RRT≥LRT)”) within a period of 50 ms, an acknowledge timeout defect (dTMOUT) shall be detected. The defect shall be cleared when the head-end response complies again or if the protection trail/connection is in SF condition.

Bridge control process

This process controls which of the normal/extra traffic signals is bridged to the protection trail/connection. Its operation shall be as follows:

```
if (ARCHtype==1+1)
then                {1+1 architecture}
      LBSN=1        {normal #1 signal permanent bridged}
else                {1:n architecture}
      if [ (SRT/0≠SF) and (not (dPAM or dSCM or dTMOUT or dINV)) ]
      then          {no SF on protection and no failure of protocol}
           LBSN=RRSN
      else          {SF on protection or failure of protocol}
           if (SWtype==dual-ended)
           then LBSN=0
           fi
      fi
fi
```

NOTE 6: When the protection trail/connection is not in use, null signal is indicated on both RSN and LBSN fields in the APS signal. Any normal signal may be bridged to the protection trail/connection at the head end. The tail end must not assume or require any specific signal.

Control of the selector

This process controls which of the normal/extra traffic signals is connected to/extracted from the protection trail/connection. Its operation shall be as follows:

```
if ( (ARCHtype==1+1) and (SWtype==single-ended) )
then
      if [ (SRT/0≠SF) or (APSmode==false) ]
      then LSSN=LRSN
      else LSSN=0{release the selector due to SF on protection when an APS
                  channel is in use}
      fi
else                        {1+1 dual-ended switching or 1:n single & dual-ended switching}
      if [ (GRSN==RRSN) and (SRT/0≠SF) and (not (dPAM or dSCM or dINV or dTMOUT))
]
      then LSSN=GRSN
      else LSSN=0           {release the selector due to protection SF or failure of protocol}
      fi
fi
```

NOTE 7: In 1 + 1 architecture in single-ended switching, each end operates independently of the other end, and APS signal is not needed to co-ordinate switch action. However, for the case an APS is supported it is still used to inform the other end of the local action.

NOTE 8: Note that selectors can be temporarily released when normal signal #i gets replaced by normal signal #j, due to temporary signal number mismatch on GRSN (RSN in transmitted APS signal) and RBSN (LBSN in received APS signal).

NOTE 9: The operation of 1 + 1 dual-ended switching is optimized for a network in which 1 : n protection switching is widely used and which is therefore based on compatibility with a 1 : n arrangement. Since the bridge is permanent, i.e. normal signal number 1 is always bridged, normal signal 1 is indicated on the LBSN field in the transmitted APS signal, unless the RSN field in the received APS signal indicates null signal (0). Switching is completed when both ends select the signal, and may take less time because LBSN indication does not depend on a bridging action.

NOTE 10: When the switch is no longer required, e.g. the failed working trail/connection has recovered from the fault and Wait-to-restore has expired, the tail end indicates No Request for Null Channel on the APS fields RT and RSN. This releases the selector due to signal number mismatch. The head end then releases the bridge and replies with the same indication on its RT and RSN fields and Null signal indication on LBSN. The selector at the head end is also released due to mismatch. Receiving Null signal on RSN causes the tail end to release the bridge. Since the LBSN fields now indicate Null Channel which matches the Null Channel on the RSN bytes, the selectors remain released without any mismatch indicated, and restoration is completed.

Defects:

If a mismatch between RRSN and GRSN persists for Y ms, a Selector Control Mismatch defect (dSCM) shall be detected. The dSCM shall be cleared when RRSN is identical to GRSN or if the protection trail/connection is in SF condition.

Consequent Actions:

The selector shall be released if one or more of the four defects dPAM, dSCM, dTMOUT, dINV is active.

APS generation process

This process shall translate the signals Global Request Type (GRT), Global Request Channel Number (RRSN), Local Bridged Signal Number (LBSN) and local Architecture type (ARCHtype) into a transmitted APS signal, as follows:

- TxRT as specified in table A.10
- TxRSN = GRSN
- if ((RRSN==0)
  then TxLBSN = 0
  else TxLBSN = LBSN
  fi
- if (ARCHtype==1+1)
  then TxARCH = 0
  else TxARCH = 1
  fi

Table A.10: Global Request Type (GRT) mapping into APS signal

GRT	TxRT
NR	0000
DNR	0001
RR	0010
EXER	0100
WTR	0110
MSw	1000
SD-L	1010
SD-H	1011
SF-L	1100
SF-H	1101
FSw	1110
LO	1111

Reporting

The function shall report the active external request, active local request, active remote request (if APS supported), reason of denial of an external command, and the condition (SF,SD) of the working and protection trails/connections.

The condition of the working and protection trails/connections shall be reported to present a complete set of information to allow unambiguous interpretation of the status of the protection entity and reaction on external commands.

MI_SignalStatus/i ← SRT/i

Defect Correlations:

cFOP ← dSCM or dPAM or dTMOUT or dINV

Performance Monitoring:

Every second the number of Protection Switch actions within that second shall be reported as pPSC (Protection Switch Count).

The function shall support an event log (containing date, time, and involved signals/trails/connections) of bridge and selector actions.

Annex B (informative): STM-16 regenerator functional model (example)

Figure B-1 presents the combination of atomic functions that represent the transport part of a STM-16 regenerator network element. In this example, a DCC, orderwire and user channel are supported; the physical section atomic functions of the orderwire (E0) and user channel (E0 or V11) are not shown.

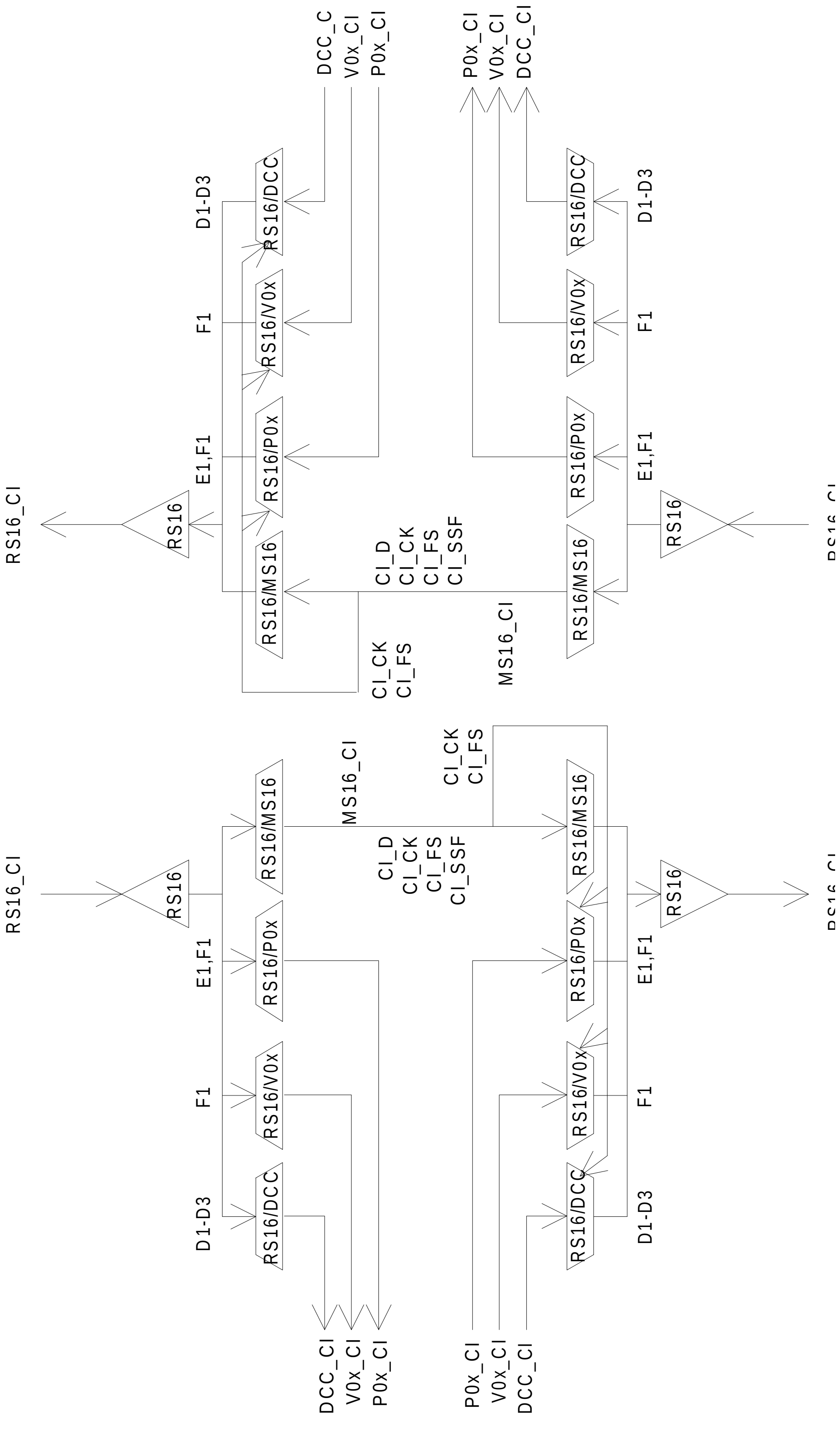


Figure B.1: STM-16 regenerator model (supporting DCC, OW, USR)

Annex C (informative): AU-4-Xc numbering scheme & pointer allocation

The following figures depict the AU-4 and AU-4-4c numbering scheme within an STM-16 signal.

The AU-4-4c will be numbered by means of the first AU-4 timeslot number that is occupied by the AU-4-4c: AU-4-4c/z, with z = 1,5,9,13. Each AU-4-4c is bound to a quadrant within the STM-16 AU structure as indicated in the range of values of “z”.

NOTE 1: Future extensions to this AU-4-4c allocation scheme (i.e. z=2,3,4,6,7,etc) are for further study.

Figures C-1 to C-3 show a small part of the STM-16 frame; figure C-1 in a parallel format [23] (16 x 155,520 MHz) and figures C-2 and C-3 in a serial format. Each block represents a byte. A byte is identified in the figures by (x,y), with x is the “155,520 Mbit/s” number (x = 1..16) and y is the number of the “AU-3” byte within an AU-4 (y = 1..3).

Figure C-1 shows AU byte allocation for AU-4 and AU-4-4c. The most right column shows the capacity allocation for the case of an STM-16 MS SPRING protection ring.

NOTE 2: The working capacity (i.e. 1,2 Gbit/s) can be provisioned. For the case extra traffic is not supported, the protection capacity can not be provisioned. Protection capacity, when used to recover from a defect condition in the ring, must automatically adapt to the AU multiplex structure that is received, as the provisioned working AU multiplex structure between any two nodes in the ring can be different, but will be transported via the same protection capacity (during a defect condition).

---

[23] Transmission in parallel format is from top to bottom and from left to right.

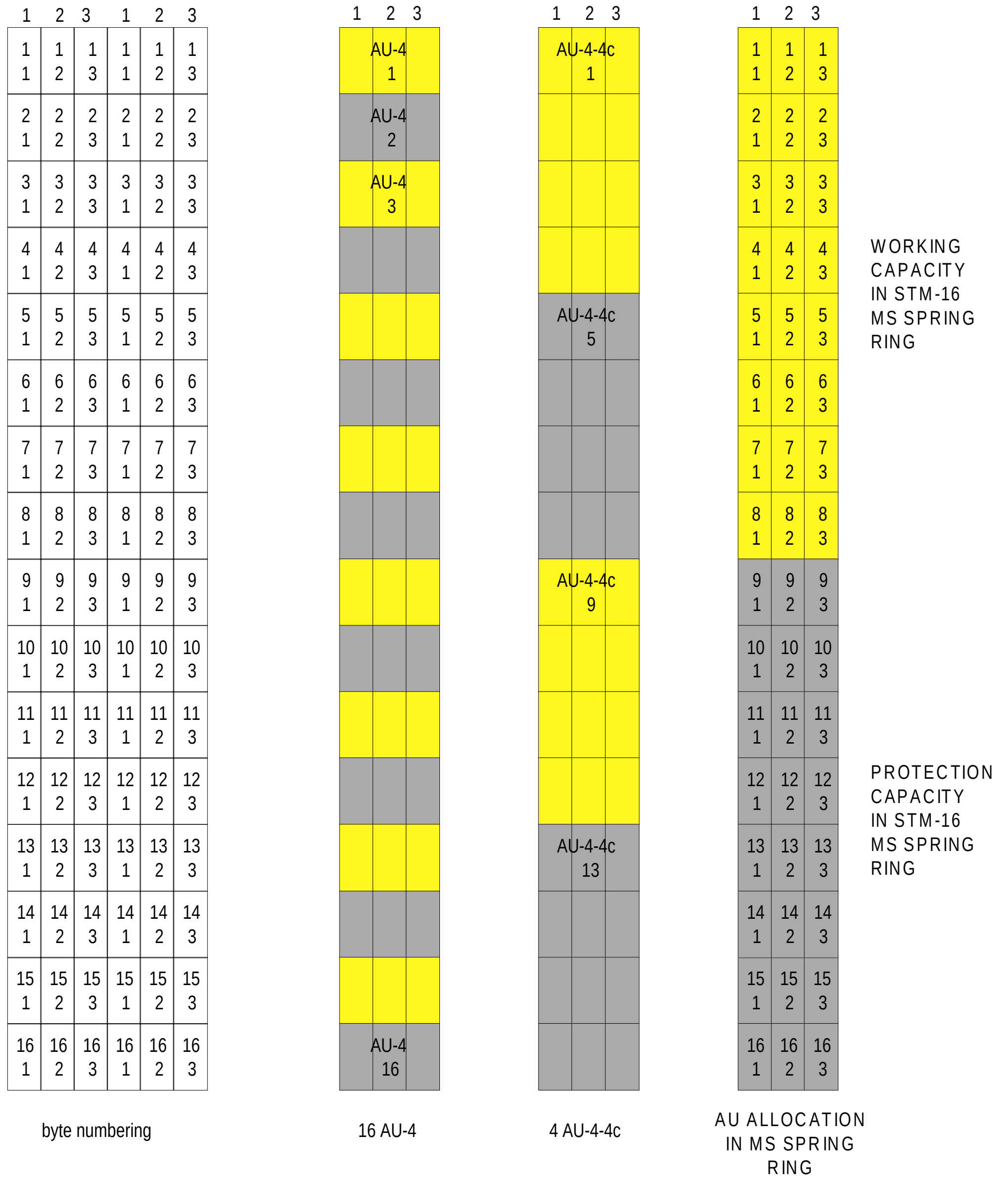


Figure C.1: AU bandwidth allocation in STM-16 and AU multiplex structures (in parallel format)

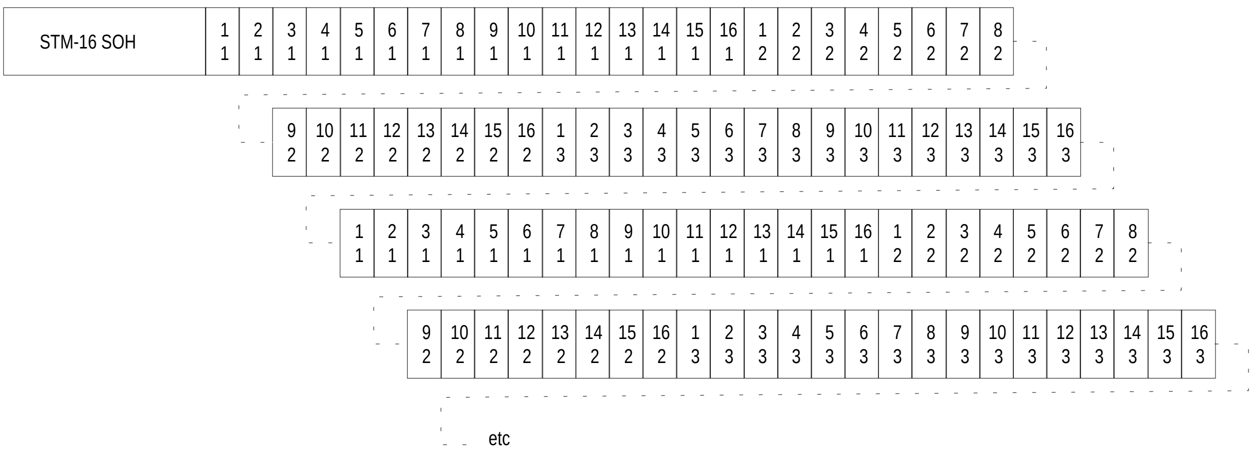


Figure C.2: AU bandwidth allocation in STM-16 (in serial format)

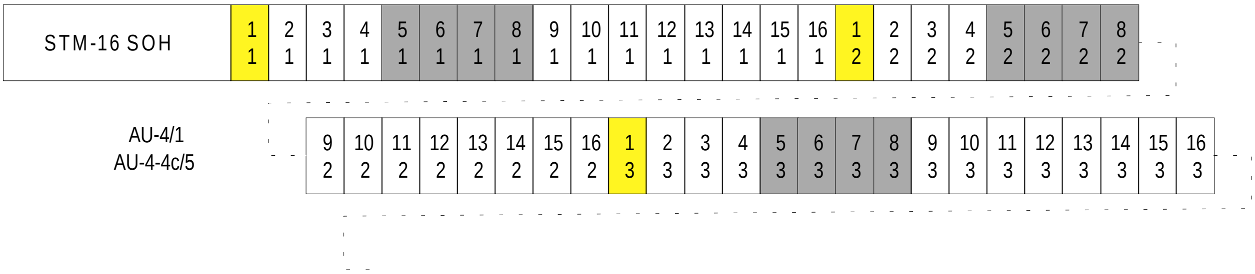


Figure C.3: Example of AU multiplex structure with an AU-4/1 and an AU-4-4c/5 (in serial format)

Figures C-4 and C-5 show the pointers, justification opportunity bytes (H3), and some payload bytes (P) of one AU-4 and one AU-4-4c.

STM-16 - ROW 4

	1	2	3	1	2	3	1	2	3	1	2	3
AU-4/1	H1	Y	Y	H2	1*	1*	H3	H3	H3	P	P	P
	2 1	2 2	2 3	2 1	2 2	2 3	2 1	2 2	2 3	2 1	2 2	2 3
	3 1	3 2	3 3	3 1	3 2	3 3	3 1	3 2	3 3	3 1	3 2	3 3
	4 1	4 2	4 3	4 1	4 2	4 3	4 1	4 2	4 3	4 1	4 2	4 3
	H1	Y	Y	H2	1*	1*	H3	H3	H3	P	P	P
AU-4-4c/5	Y	Y	Y	1*	1*	1*	H3	H3	H3	P	P	P
	Y	Y	Y	1*	1*	1*	H3	H3	H3	P	P	P
	Y	Y	Y	1*	1*	1*	H3	H3	H3	P	P	P
	9 1	9 2	9 3	9 1	9 2	9 3	9 1	9 2	9 3	9 1	9 2	9 3
	10 1	10 2	10 3	10 1	10 2	10 3	10 1	10 2	10 3	10 1	10 2	10 3
	11 1	11 2	11 3	11 1	11 2	11 3	11 1	11 2	11 2	11 1	11 2	11 3
	12 1	12 2	12 3	12 1	12 2	12 3	12 1	12 2	12 3	12 1	12 2	12 3
	13 1	13 2	13 3	13 1	13 2	13 3	13 1	13 2	13 3	13 1	13 2	13 3
	14 1	14 2	14 3	14 1	14 2	14 3	14 1	14 2	14 3	14 1	14 2	14 3
	15 1	15 2	15 3	15 1	15 2	15 3	15 1	15 2	15 3	15 1	15 2	15 3
	16 1	16 2	16 3	16 1	16 2	16 3	16 1	16 2	16 3	16 1	16 2	16 3

Figure C.4: Example of AU multiplex structure with an AU-4 and an two AU-4-4c (in parallel format)

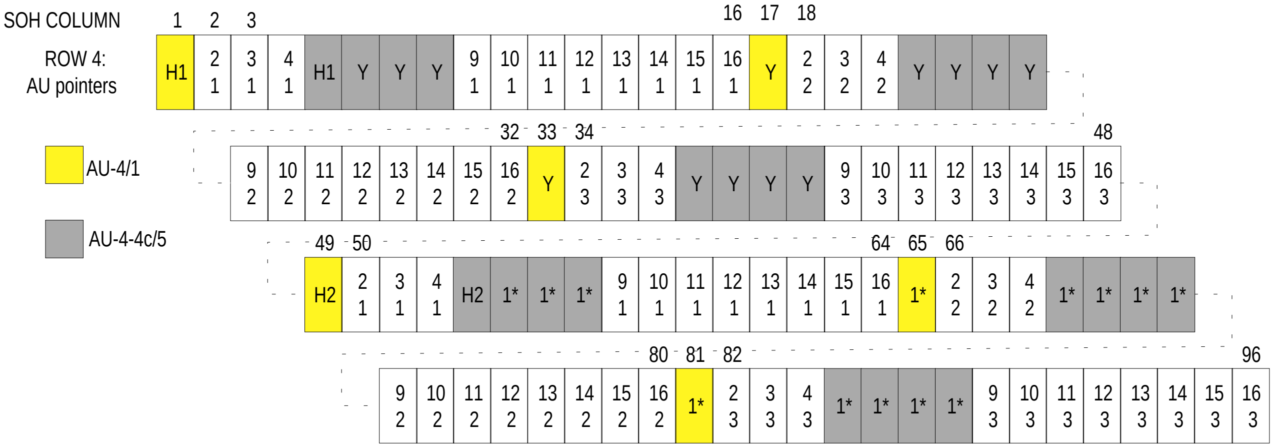


Figure C.5: AU pointers in STM-16 supporting AU examples in figure C-4 (in serial format)

Annex D (informative): MS protection examples

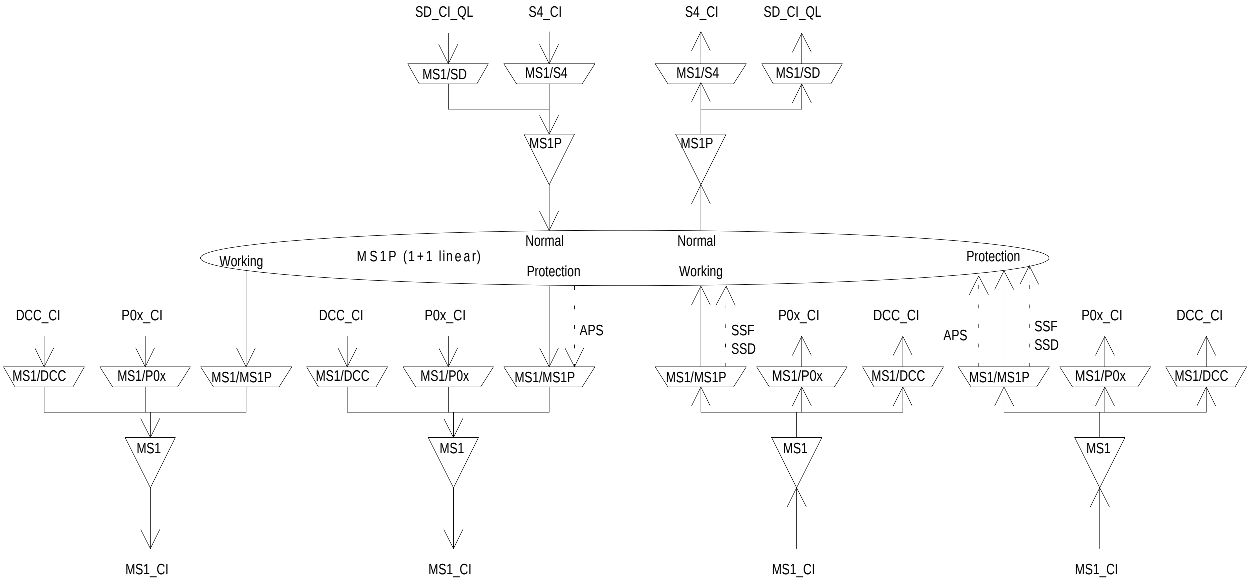


Figure D.1: 1+1 STM-1 Multiplex Section Linear Trail Protection model (unprotected DCC, OW, protected SSM)

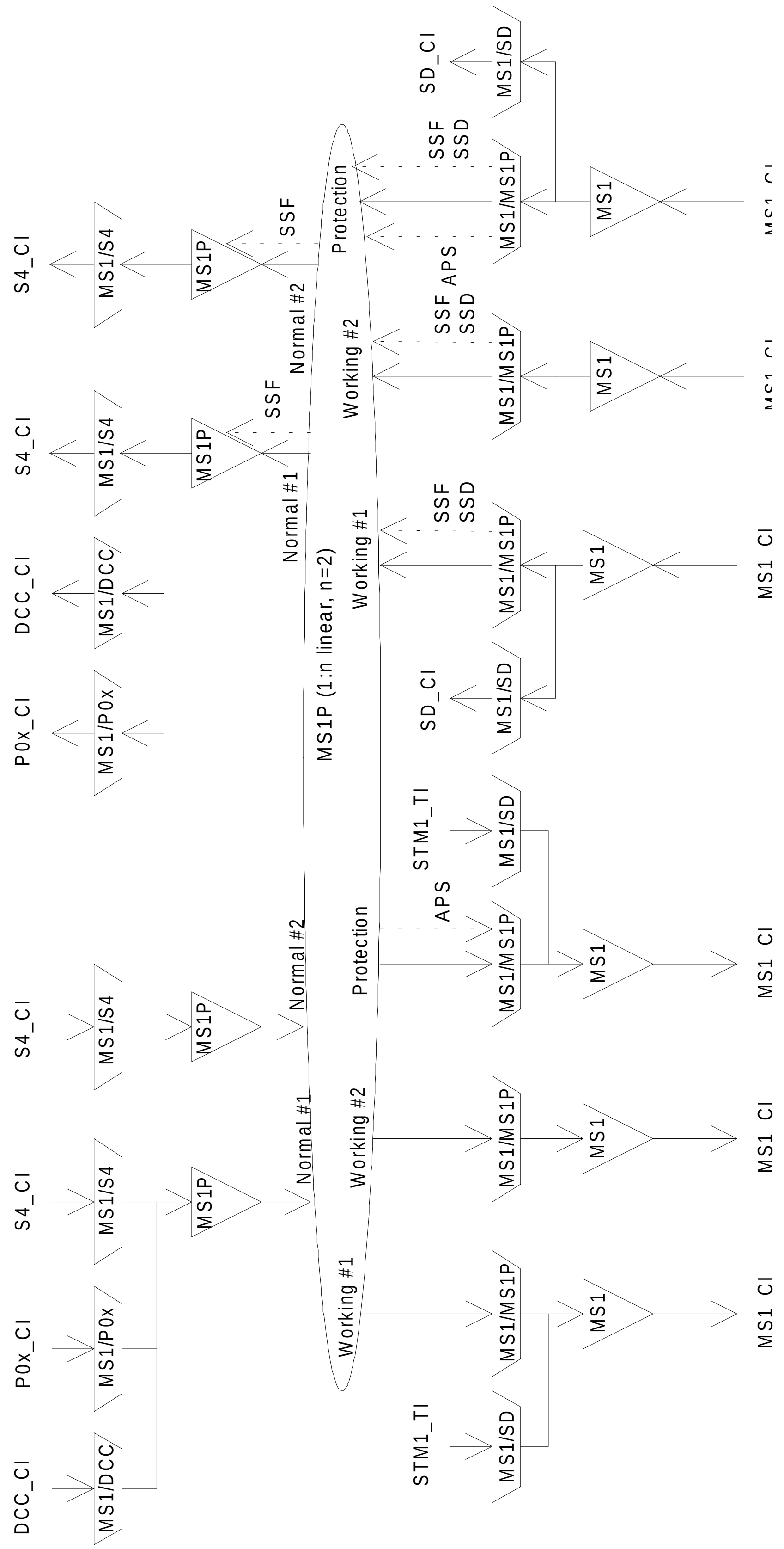


Figure D.2: 1:n STM-1 Multiplex Section Linear Trail Protection model (Working/Normal #1 supports (protected) OW,DCC and (unprotected) SSM: Working/Normal #2 does not support OW,DCC,SSM)

Annex E (informative): Bibliography

ETR 273: "Transmission and Multiplexing (TM); SDH network protection schemes; Types and characteristics".

History

Document history			
April 1996	Public Enquiry	PE 105:	1996-04-08 to 1996-08-30