

EUROPEAN TELECOMMUNICATION STANDARD

DRAFT pr ETS 300 337

November 1996

Second Edition

Reference: RE/TM-03056

Source: ETSI TC-TM

ICS: 33.020

Key words: Transmission, ATM, SDH, transport

Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s

ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE **Office address:** 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE **X.400:** c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 4 92 94 42 00 - Fax: +33 4 93 65 47 16

Copyright Notification: No part may be reproduced except as authorized by written permission. The copyright and the foregoing restriction extend to reproduction in all media.

© European Telecommunications Standards Institute 1996. All rights reserved.

Page 2 Draft prETS 300 337: November 1996

Whilst every care has been taken in the preparation and publication of this document, errors in content, typographical or otherwise, may occur. If you have comments concerning its accuracy, please write to "ETSI Editing and Committee Support Dept." at the address shown on the title page.

Contents

Forew	vord		5
1	Scope		7
2	Normativ	ve references	7
3	Definition 3.1	ns and abbreviations Definitions	
	3.2	Abbreviations	
4		tructure at 2 048 kbit/s	
	4.1 4.2	Basic frame structure Support of ATM cells in 2 048 kbit/s	
5		tructure at 34 368 kbit/s	
	5.1	Basic frame structure	
		5.1.1 General	-
	5.2	5.1.2 Path overhead Support of ATM cells in 34 368 kbit/s	
	5.2 5.3	Support of 14 SDH TU-12s in 34 368 kbit/s	
	5.5	5.3.1 Coding of multiframe indicator for TU multiframe indication	
6	Frame st	tructure at 139 264 kbit/s	
	6.1	Basic frame structure	
		6.1.1 General	
		6.1.2 Path overhead	
	6.2	Support of ATM cells in 139 264 kbit/s	
	6.3	Support of SDH elements in 139 264 kbit/s	
		6.3.1 Coding of multiframe indicator for TU multiframe indication6.3.2 Support of 20 x TUG-2	
		 6.3.2 Support of 20 x TUG-2 6.3.3 Support of 2 x TUG-3 and 5 x TUG-2 	
7	Conforma	nance testing	20
Annex	x A (inform	mative): Functions specific to the support of ATM cells	21
A.1	Cell rate	adaptation	21
A.2	Header E	Error Control (HEC) generation	21
A.3	Cell delin	neation	21
A.4	Cell head	der verification and extraction	21
Annex	x B (inform	mative): Bibliography	22
Histor	<i>т</i> у		23

Blank page

Foreword

This draft second edition European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI), and is now submitted for the Unified Approval Procedure phase of the ETSI standards approval procedure.

This ETS specifies generic frame structures for the transport of various signals at the ITU-T Recommendation G.702 [1] hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s. The support of Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) Tributary Units (TUs) in the Plesiochronous Digital Hierarchy (PDH) bit rates is also covered in this ETS.

This ETS takes into account the recommendations given in ITU-T Recommendation G.804 (annex B2) and G.832 (annex B 3) - see annex B (Bibliography) for details.

Proposed transposition dates			
Date of latest announcement of this ETS (doa):	3 months after ETSI publication		
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa		
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa		

Blank page

1 Scope

This second edition European Telecommunication Standard (ETS) specifies generic frame structures for the transport of various signals at the ITU-T Recommendation G.702 [1] hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s. The support of Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) Tributary Units (TUs) in the Plesiochronous Digital Hierarchy (PDH) bit rates is covered in this ETS. Functions specific to the support of ATM cells performed in the transmitter and receiver are not part of this interface standard but are given for information in annex A.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- [1] ITU-T Recommendation G.702 (1988): "Digital hierarchy bit rates".
- [2] ETS 300 167: "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".
- [3] ETS 300 147 (1995): "Transmission and Multiplexing (TM); Synchronous digital hierarchy; Multiplexing structure".
- [4] ITU-T Recommendation G.831 (1996): "Management capabilities of transport networks based on the Synchronous Digital Hierarchy (SDH)".
- [5] ITU-T Recommendation T.50 (1992): "Information technology 7-bit coded character set for information interchange".
- [6] ITU-T Recommendation G.707 (1995): "Synchronous Digital Hierarchy (SDH) bit rates".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of this ETS, the following definitions apply:

idle cell: A cell which is inserted and extracted by the adaptation function between the ATM virtual path layer network and the PDH path layer network in order to adapt the cell flow rate to the available payload capacity of the PDH path used.

valid cell: A cell whose header is declared by the cell Header Error Control (HEC) process to be free of errors.

NOTE: The order of transmission of information in all diagrams in this ETS is first from left to right and then top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left of all diagrams.

3.2 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

ATM	Asynchronous Transfer Mode
BIP-8	Bit Interleaved Parity - 8
CRC	Cyclic Redundancy Check
ETSI	European Telecommunications Standards Institute
HEC	Header Error Control
IEC	Incoming Error Count
MSB	Most Significant Bit
OAM	Operations, Administration and Maintenance
PDH	Plesiochronous Digital Hierarchy
RDI	Remote Defect Indication
REI	Remote Error Indication
SDH	Synchronous Digital Hierarchy
TS	Time Slot
TTI	Trail Trace Identifier
TU	Tributary Unit
TUG-n	Tributary Unit Group of level n
TUG-n	Tributary Unit Group of level n
TU-x	Tributary Unit - x

4 Frame structure at 2 048 kbit/s

4.1 Basic frame structure

The basic frame structure at 2 048 kbit/s as described in ETS 300 167 [2] shall be used. This comprises a generic path overhead, a signalling channel and a generic payload capacity of 1 920 kbit/s.

4.2 Support of ATM cells in 2 048 kbit/s

Valid or idle cells are supported in bits 9 to 128 and bits 137 to 256 of the 2 048 kbit/s frame with the octet structure of the cells aligned with the octet structure of the frame (see figure 1). Bits 129 to 136 correspond to Time Slot 16 (TS 16) in an octet structured frame and are reserved for future use. Valid or idle cells occupy the whole of the payload and a cell can cross a 125 μ s frame boundary. The ATM cell payload is scrambled using a self-synchronizing scrambler with the generator polynomial x^{43} + 1. Cell payload field scrambling is required to provide security against false cell delineation and to prevent the cell payload replicating the 2 048 kbit/s frame alignment word.

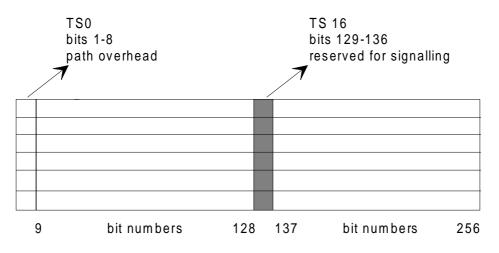


Figure 1: Frame structure at 2 048 kbit/s

5 Frame structure at 34 368 kbit/s

5.1 Basic frame structure

This frame structure is intended to be used in a generic way. When implementing this frame structure, care should be taken to ensure that the performance of the frame alignment mechanism is not compromised by the payload content.

5.1.1 General

The basic frame structure at 34 368 kbit/s comprises 7 octets of generic path overhead and 530 octets of payload capacity per 125 µs as shown in figure 2.

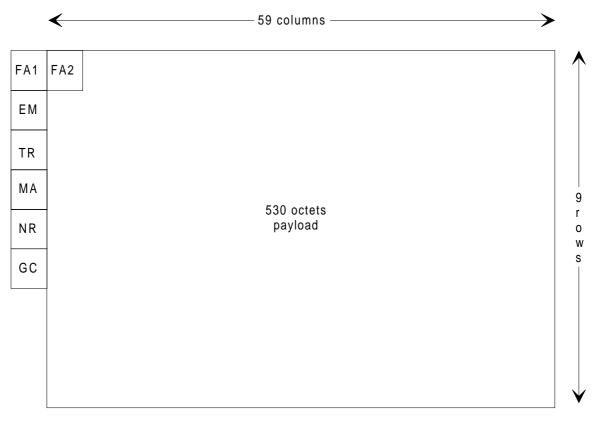
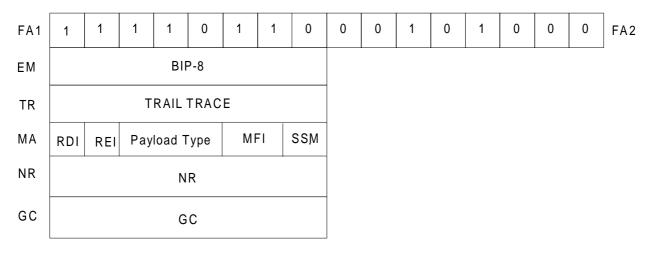


Figure 2: Frame structure at 34 368 kbit/s

Page 10 Draft prETS 300 337: November 1996

5.1.2 Path overhead

The values and allocation of the path overhead are shown in figure 3 and are described below.



MFI = Multiframe Indicator

SSM = Synchronization Status Message

Figure 3: Path overhead at 34 368 kbit/s

- FA1/FA2: Frame Alignment signal, this has the same pattern as defined in clause 7 of ETS 300 147 [3].
- EM: Error Monitoring, BIP-8. One byte is allocated for path error monitoring. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous 125 µs frame. The computed BIP-8 is placed in the EM byte of the current 125 µs frame.
- TR: Trail trace. This byte is used to transmit repetitively a trail access point identifier so that a trail receiving terminal can verify its continued connection to the intended transmitter. The trail access point identifier shall use the access point identifier format as defined in section 3 of ITU-T Recommendation G.831 [4].

Trail access point Identifier format:

A 16-byte frame is defined for the transmission of the access point identifier. The first byte of the string is a frame start marker and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 ITU-T Recommendation T.50 [5] characters required for the access point identifier. The 16-byte frame is given below:

1C ₁ CCCCCC ₇ :	frame start marker;
0XXXXXXX:	byte 2;
0XXXXXXX:	byte 16;
0XXXXXXX:	ITU-T Recommendation T.50 [5] character;
C ₁ CCCCCC ₇ :	result of the CRC-7 calculation over the previous frame.

The description of the CRC-7 calculation is given below.

Multiplication/division process

A particular CRC-7 word is the remainder after multiplication by x^7 and then division (modulo 2) by the generator polynomial $x^7 + x^3 + 1$, of the polynomial representation of the previous Trail Trace Identifier (TTI) multiframe.

When representing the contents of the block as a polynomial, the first bit in the block, (i.e. byte 1, bit 1) should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_7 to be the least significant bit of the remainder.

Encoding procedure

Contrary to e.g. the CRC-4 procedure in 2 Mbit/s signals, the CRC-7 word is static because the data is static (the TTI represents the source address). This means that the CRC-7 checksum can be calculated a priori over the TTI multiframe. For consistency with existing recommendations the CRC-7 checksum is to be calculated over the previous multiframe. In theory this means that the 16-byte string that is loaded in a device for repetition transmission should have the checksum as the last byte although in practice it does not really matter because the TTI is static.

The encoding procedure is as follows:

- a) the CRC-7 bits in the TTI are replaced by binary "0"s;
- b) the TTI is then acted upon by the multiplication/division process referred to above;
- c) the remainder resulting from the multiplication/division process is inserted into the CRC-7 location.

The CRC-7 bits generated do not affect the result of the multiplication/division process because, as indicated in a) above, the CRC-7 bit positions are initially set to "0" during the multiplication/division process.

Decoding procedure

The decoding procedure is as follows:

- a) a received TTI is acted upon by the multiplication/division process referred to above after having its CRC-7 bits extracted and replaced by "0"s;
- b) the remainder resulting from the division process is then compared on a bit-by-bit basis with the CRC-7 bits received;
- c) if the remainder calculated in the decoder exactly corresponds to the CRC-7 bits received, it is assumed that the checked TTI is error free.

Page 12 Draft prETS 300 337: November 1996

MA: Maintenance and Adaptation byte:

- bit 1 RDI (Remote Defect Indication);
- bit 2 REI (Remote Error Indication), this bit is set to "1" and sent back to the remote Path termination if one or more errors were detected by the BIP-8, and is otherwise set to zero;

bits 3-5 payload type:

Code	Signal
000 001 010	Unequipped; Equipped, non-specific; ATM;
011	SDH TU-12s;

- bits 6-7 Multiframe indicator;
- bit 8 This bit is used in a four frame multiframe. The phase of the multiframe is determined by the value of MA bits 6-7. The four bits of the multiframe are allocated to a Synchronization Status Message (SSM). The coding of the SSM is given in Table 5 of ITU-T Recommendation G.707 [6].

When interworking with "old" equipment which used bit 8 as a timing marker (non-multiframe), the "new" equipment implementing the above requirement should be capable of being configured to transmit the old" requirement as given below:

- bit 8 timing marker: This bit is set to "0" to indicate that the timing source is traceable to a Primary Reference Clock, and is otherwise set to "1".
- NR: Network operator byte. This byte is allocated for maintenance purposes specific to individual network operators. Its transparency from path termination to path termination is not guaranteed in cases where the path traverses operator domains. For tandem connection maintenance, the byte is used in accordance with annex D of ITU-T Recommendation G.707 [6].
- GC: General purpose Communications channel (e.g. to provide data/voice channel connection for maintenance purposes).

5.2 Support of ATM cells in 34 368 kbit/s

The octet structure of the valid or idle cells is aligned with the octet structure of the payload area. Valid or idle cells occupy the whole of the payload and a cell can cross a 125 μ s frame boundary. The ATM cell payload is scrambled using a self-synchronizing scrambler with the generator polynomial x⁴³+1. Cell payload field scrambling is required to provide security against false cell delineation and to prevent the cell payload replicating the 34 368 kbit/s frame alignment word.

5.3 Support of 14 SDH TU-12s in 34 368 kbit/s

14 x TU-12s are arranged in the payload as shown in figure 4.

Columns one (except the first octet), thirty and thirty one are occupied by fixed stuff, the 14 x TU-12s are 1-column interleaved into this structure and have a fixed phase relationship with respect to the frame structure. The TU pointers occupy the octets in the first row from columns two to fifteen.

Page 13 Draft prETS 300 337: November 1996

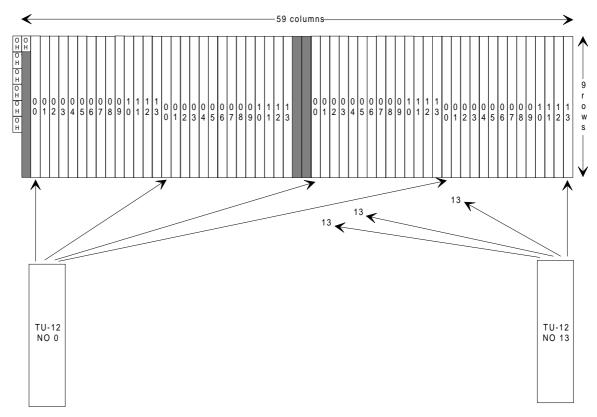


Figure 4: Support of 14 TU-12s in 34 368 kbit/s

5.3.1 Coding of multiframe indicator for TU multiframe indication

Table 1 shows the coding of the multiframe indicator in the case of TU-12s mapping.

l able 1	Та	b	le	1	
----------	----	---	----	---	--

Bit 6	Bit 7	TU-PTR content in the following frame
0	0	V1
0	1	V2
1	0	V3
1	1	V4

500 µs TU multiframe

Page 14 Draft prETS 300 337: November 1996

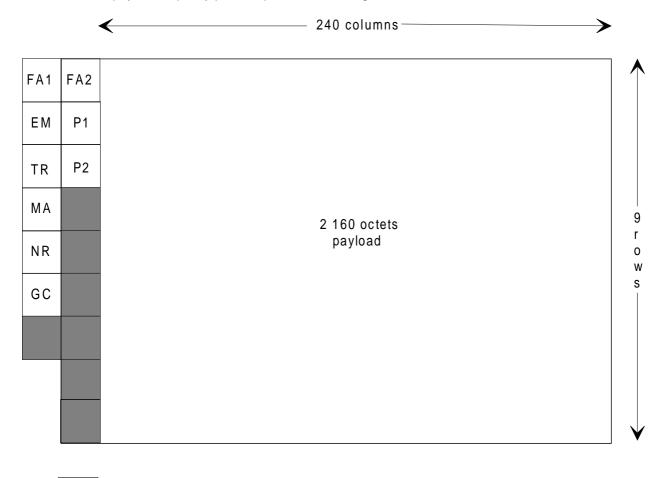
6 Frame structure at 139 264 kbit/s

6.1 Basic frame structure

This frame structure is intended to be used in a generic way. When implementing this frame structure, care should be taken to ensure that the performance of the frame alignment mechanism is not compromised by the payload content.

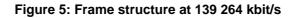
6.1.1 General

The basic frame structure at 139 264 kbit/s comprises 16 octets of generic path overhead and 2 160 octets of payload capacity per 125 µs as shown in figure 5.



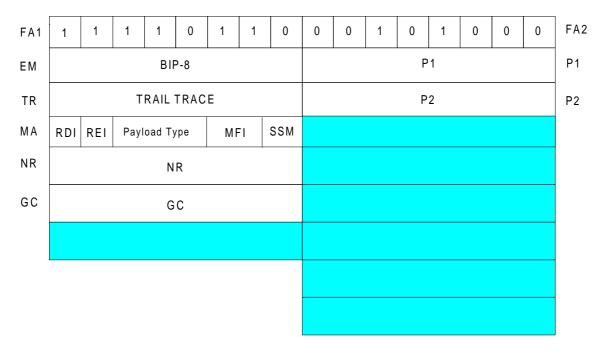


Undefined



6.1.2 Path overhead

The values and allocation of the first 9 octets of path overhead are shown in figure 6 and are described below. The use of the remaining 7 octets is not yet defined. However, if not used, the contents of these octets should be set to 00 HEX.



MFI = Multiframe Indicator SSM = Synchronization Status Message

Figure 6: Path overhead at 139 264 kbit/s

FA1/FA2: Frame Alignment signal. This has the same pattern as defined in clause 7 of ETS 300 147 [3].

EM: Error Monitoring, BIP-8. One byte is allocated for path error monitoring. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous 125 µs frame. The computed BIP-8 is placed in the EM byte of the current 125 µs frame.

TR: Trail trace. This byte is used to transmit repetitively a trail access point identifier so that a trail receiving terminal can verify its continued connection to the intended transmitter. The trail access point identifier shall use the access point identifier format as defined in section 3 of ITU-T Recommendation G.831 [4].

Trail access point Identifier format:

A 16-byte frame is defined for the transmission of the access point identifier. The first byte of the string is a frame start marker and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 ITU-T Recommendation T.50 [5] characters required for the access point identifier. The 16-byte frame is given below:

1C ₁ CCCCCC ₇ :	frame start marker;
0XXXXXXX:	byte 2;
0XXXXXXX:	byte 16;
0XXXXXXX:	ITU-T Recommendation T.50 [5] character;
C ₁ CCCCCC ₇ :	result of the CRC-7 calculation over the previous frame.

The description of the CRC-7 calculation is given below.

Multiplication/division process

A particular CRC-7 word is the remainder after multiplication by x^7 and then division (modulo 2) by the generator polynomial $x^7 + x^3 + 1$, of the polynomial representation of the previous TTI multiframe.

When representing the contents of the block as a polynomial, the first bit in the block, (i.e. byte 1, bit 1) should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_7 to be the least significant bit of the remainder.

Encoding procedure

Contrary to e.g. CRC-4 procedure in 2 Mbit/s signals, the CRC-7 word is static because the data is static (the TTI represents the source address). This means that the CRC-7 checksum can be calculated a priori over the TTI multiframe. For consistency with existing recommendations the CRC-7 checksum is to be calculated over the previous multiframe. In theory this means that the 16-byte string that is loaded in a device for repetitive transmission should have the checksum as the last byte although in practice it does not really matter because the TTI is static.

The encoding procedure is as follows:

- a) the CRC-7 bits in the TTI are replaced by binary "0"s;
- b) the TTI is then acted upon by the multiplication/division process referred to above;
- c) the remainder resulting from the multiplication/division process is inserted into the CRC-7 location.

The CRC-7 bits generated do not affect the result of the multiplication/division process because, as indicated in a) above, the CRC-7 bit positions are initially set to "0" during the multiplication/division process.

Decoding procedure

The decoding procedure is as follows:

- a) a received TTI is acted upon by the multiplication/division process referred to above after having its CRC-7 bits extracted and replaced by "0"s;
- b) the remainder resulting from the division process is then compared on a bit-by-bit basis with the CRC-7 bits received;
- c) if the remainder calculated in the decoder exactly corresponds to the CRC-7 bits received, it is assumed that the checked TTI is error free.

- MA: Maintenance and Adaptation byte
 - bit 1 RDI (Remote Defect Indication);
 - bit 2 REI (Remote Error Indication). This bit is set to "1" and sent back to the remote Path termination if one or more errors were detected by the BIP-8, and is otherwise set to zero;
 - bits 3-5 payload type:

Code Signal

- 000 Unequipped;
- 001 Equipped, non-specific;
- 010 ATM;
- 011 SDH elements mapping A 20 x TUG-2;
- 100 SDH elements mapping B 2 x TUG-3 and 5 x TUG-2.
- bits 6-7 Multiframe indicator;
- bit 8 This bit is used in a four frame multiframe. The phase of the multiframe is determined by the value of MA bits 6-7. The four bits of the multiframe are allocated to a Synchronization Status Message (SSM). The coding of the SSM is given in Table 5 of ITU-T Recommendation G.707 [6].

When interworking with "old" equipment which used bit 8 as a timing marker (non-multiframe), the "new" equipment implementing the above requirement should be capable of being configured to transmit the old" requirement as given below:

- bit 8 timing marker. This bit is set to "0" to indicate that the timing source is traceable to a Primary Reference Clock, and is otherwise set to "1".
- NR: Network operator byte. This byte is allocated for maintenance purposes specific to individual network operators. Its transparency from path termination to path termination is not guaranteed in cases where the path traverses operator domains. For tandem connection maintenance, the byte is used in accordance with annex D of ITU-T Recommendation G.707 [6].
- GC: General purpose Communications channel (e.g. to provide data/voice channel connection for maintenance purposes).
- P1/P2: automatic Protection switching.

6.2 Support of ATM cells in 139 264 kbit/s

The octet structure of valid and idle cells is aligned with the octet structure of the payload area. Valid or idle cells occupy the whole of the payload and a cell can cross a 125 μ s frame boundary. The ATM cell payload is scrambled using a self-synchronizing scrambler with the generator polynomial x⁴³+1. Cell payload field scrambling is required to provide security against false cell delineation and to prevent the cell payload replicating the 139 264 kbit/s frame alignment word.

Page 18 Draft prETS 300 337: November 1996

6.3 Support of SDH elements in 139 264 kbit/s

The payload can be used to support either one of the two following arrangements:

- A: 20 x TUG-2;

- B: 2 x TUG-3 and 5 x TUG-2.

6.3.1 Coding of multiframe indicator for TU multiframe indication

Table 2 shows the coding of the multiframe indicator in the case of TU-1xs mapping.

Table 2

	Bit 6	Bit 7	TU-PTR content in the following frame
	0	0	V1
	0	1	V2
	1	0	V3
ĺ	1	1	V4

500 µs TU multiframe

6.3.2 Support of 20 x TUG-2

The support of $20 \times TUG-2s$ in the 9 rows by 240 columns payload is as shown in figure 7. The $20 \times TUG-2s$ are 1-column interleaved into this structure and have a fixed phase relationship with respect to the frame structure.

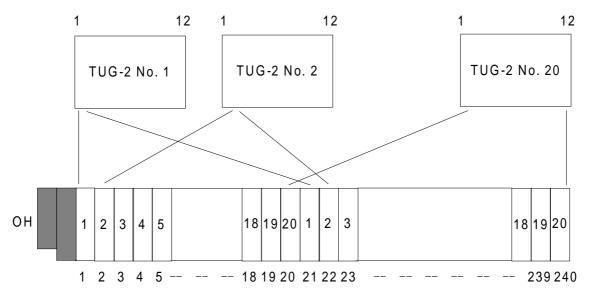


Figure 7: Support of 20 x TUG-2 in 139 264 kbit/s

6.3.3 Support of 2 x TUG-3 and 5 x TUG-2

The support of 2 x TUG-3s and 5 x TUG-2s in the 9 rows by 240 columns payload is as shown in figure 8.

Four fixed stuff columns are added to each TUG-3 structure in the leading positions, resulting in two 90 column structures ("A" and "B"). The 5 x TUG-2s are 1-column interleaved to form a 60 columns by 9 rows structure ("C"). These three intermediate structures are then column interleaved in the following sequence:

[ABACBABC]₁, [ABACBABC]₂,, [ABACBABC]₃₀.

Page 19 Draft prETS 300 337: November 1996

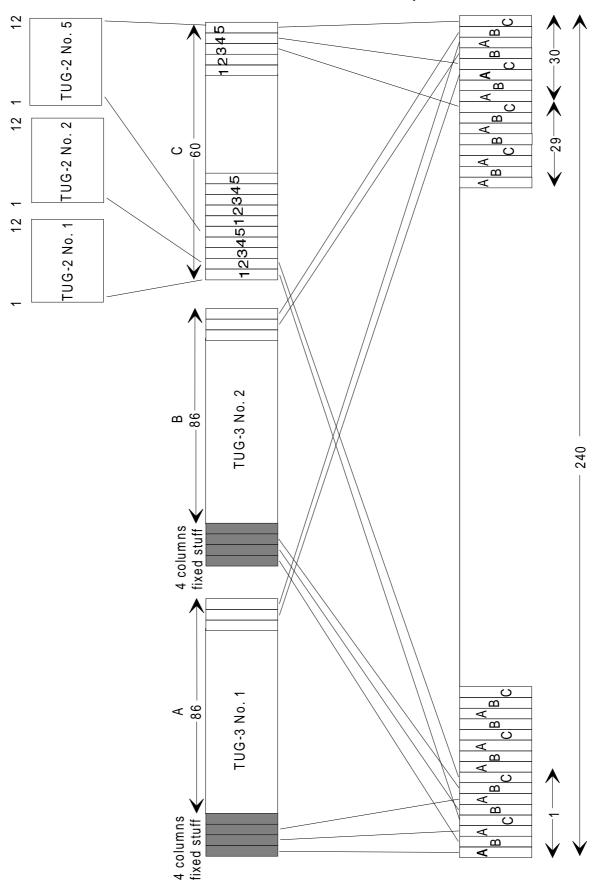


Figure 8: Support of 5 x TUG-2 and 2 x TUG-3 in 139 264 kbit/s

Page 20 Draft prETS 300 337: November 1996

7 Conformance testing

Conformance testing is concerned with testing the functional blocks contained within a network element. Conformance testing is performed using physical interface(s) to exercise the functional blocks. Conformance testing principles will, therefore, be associated with the relevant equipment function standards.

Annex A (informative): Functions specific to the support of ATM cells

A.1 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Recommendation I.432, § 4.4 (for details, see annex B, Bibliography), when no valid cells are available from the ATM layer.

A.2 Header Error Control (HEC) generation

The HEC value is generated and inserted in the appropriate field in accordance with ITU-T Recommendation I.432, § 4.3.2.

A.3 Cell delineation

At the receiving side the cell delineation is performed using the HEC mechanism as defined in ITU-T Recommendation I.432.

A.4 Cell header verification and extraction

The header verification is performed at the receiver side in accordance with ITU-T Recommendation I.432, § 4.3.1. All the physical layer cells shall be discarded and only valid cells are passed to the ATM layer.

Page 22 Draft prETS 300 337: November 1996

Annex B (informative): Bibliography

The following reference are used for informative purpose within this ETS.

- ITU-T Recommendation I.432 (1993): "B-ISDN user-network interface Physical layer specification".
- ITU-T Recommendation G.804 (1993): "ATM cell mapping into plesiochronous digital hierarchy (PDH)".
- ITU-T Recommendation G.832 (1995): "Transport of SDH elements on PDH networks Frame and multiplexer structures".

History

Document history				
February 1995	First Edition			
November 1996	Unified Approval Procedure	UAP 57:	1996-11-04 to 1997-02-28	