AMENDMENT

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A1

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This amendment A1 modifies
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Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate

ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE
Office address: 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
X.400: c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

Foreword

This amendment to ETS 300 233 (1994) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This amendment provides the annex C, which was left "To be provided" in ETS 300 233 (1994).

Amendment

Page 74, annex C

Replace the current annex C "To be provided" with the following annex C.

Annex C (normative): Conformance test principles for the ISDN primary rate access digital section

C.1 Scope and general information

C.1.1 Scope of this annex

This annex provides the test principles for the requirements of this ETS used to determine the compliance of an implementation under test to this ETS.

This annex does not specify test related to:

- safety requirements;
- interface or equipment overvoltage protection requirements;
- immunity requirements against electromagnetic interferences;
- emission limitation requirements.

Detailed test equipment accuracy and the specification tolerance of the test devices is not a subject of this annex. Where such details are provided then those test details are considered as being an informative addition to the test description.

The test configurations given do not imply a specific realisation of test equipment, or arrangement, or the use of specific test devices for conformance testing. However, any test configuration used shall provide those test conditions specified under "system state", "stimulus" and "monitor" for each individual test.

C.1.2 General information

For conformance test of the access digital section two relevant test points have to be identified:

- the T reference point covered by ETS 300 011 [1];
- the V3 reference point.

This annex is applicable to interfaces T and V3 as appropriate. The field of application is given at the beginning of each test.

As the transmission system is not specified in this ETS, only relevant signals inside the primary rate stream need to be checked. The coding and the frame organization of this bit stream is outside the scope of this ETS.

C.1.2.1 Additional information to support the test

The V3 interface is required to be a standard CCITT Recommendation G.703 [8] interface (either 120 Ω balanced or 75 Ω unbalanced) according to CCITT Recommendation Q.512 [4].

If the V3 reference point is not implemented as an interface, a suitable means such as either a local exchange or a Conformance Test Adaptor (CTA) enabling the monitoring of the V1 reference point and giving access to the B and D channels shall be provided by the manufacturer.

C.1.2.2 Abbreviations

For the purpose of this annex the following additional abbreviations apply:

FAS	Frame Alignment Signal
IUT	Item Under Test
MF	Multiframe
MFAS	Multiframe Alignment Signal
PRBS	Pseudo Random Bit Sequence
Rx	interface signal Receiver (of the IUT or simulator)
SMF	Sub-Multiframe
Tx	interface signal Transmitter of the IUT or simulator

C.1.2.3 Definitions

For the purpose of this annex the following additional definitions apply:

Primary rate access Digital Section (DS): the provision to transmit a digital signal of specified rate between two consecutive reference points. The term should be qualified by the type of access supported, or by a prefix denoting the V interface at the digital section boundaries. For example:

- basic rate access digital section;
- primary rate access digital section;
- V_5 digital section.

Item Under Test (IUT): Implementation of interfaces related functions for:

- the user side interface (T), i.e. NT1; and
- the exchange side interface (V_3), i.e. LT.

Simulator (terminal equipment, exchange): device generating a stimulus signal conforming to this ETS to bring the IUT into the required operational state and monitoring the receive signal from the IUT. It can either be a simulator for the user side or the exchange side of the interface.

C.1.3 Connection of the simulator to the IUT

For testing the electrical characteristics of the IUT, the simulator, or its relevant part, shall be connected directly to the interconnecting points for the interface wiring at the IUT unless otherwise stated.

All other tests may be performed with interface wiring complying with the requirements given in CCITT Recommendation G.703 [8] and in ETS 300 011 [1], table 1, clause 7.

C.1.4 Allocation of test

One test definition may cover more than one requirement for one or both interface points (interface T or V3). Requirements which do not need specific test definition are indicated by "N/R" (Not Relevant). Requirements which are not relevant for this ETS and which require testing defined by other ETSs are indicated by "N/A" (Not Applicable).

C.1.4.1 General

Table C.1: General requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Scope	1	N/R	
Normative references	2	N/R	
Definitions and abbreviations	3	N/R	
Definitions	3.1	N/R	
Abbreviations	3.2	N/R	

C.1.4.2 Type of configuration and applications requirements

Table C.2: Type of configuration and applications requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Configuration and application	4	N/R	
Configuration	4.1	N/R	
Application	4.2	N/R	
Modelling and relationship between the access DS and the ET	4.3	N/R	

C.1.4.3 Functional characteristics requirements

Table C.3: Functional characteristics requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Function	5	N/R	
B-channel	5.1	T and V3	C.2.1 and C.2.5.5
H0-channel	5.2	T and V3	C.2.1 and C.2.5.5
H1-channel	5.3	T and V3	C.2.1 and C.2.5.5
D-channel	5.4	T and V3	C.2.1
Bit timing	5.5	T and V3	C.2.5
Octet timing	5.6	T and V3	C.2.3, C.2.3.3, and C.2.5.5
Frame alignment	5.7	T and V3	C.4.1
CRC-4 procedure	5.8	T and V3	C.4.2
M channel	5.9	T and V3	C.2.1
Power feeding	5.10	T	C.5.1
Operation and maintenance of access digital section	5.11	T and V3	C.3.1

C.1.4.4 Signal delay and jitter requirements

Table C.4: Signal delay and jitter requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Signal transfer delay	6	T and V3	C.2.4
Jitter	7	N/R	
Output/Input jitter at T reference point	7.1	T	C.2.6.1 and C.2.6.3
Jitter at V3 reference point	7.2	V3	C.2.6.2

C.1.4.5 Operation and maintenance

Table C.5: Operation and maintenance requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Operation and maintenance	8	N/R	
Control facilities	8.1	N/R	
Loopbacks	8.1.1	N/R	
Loopbacks implementation	8.1.1.1		
i)		V3	C.7.1
ii)		V3	C.7.2
Loopback procedure	8.1.1.2		C.7
Monitoring	8.2	N/R	
Functions	8.2.1	N/R	
Defect conditions and consequent action	8.2.2	N/R	
Detection of defect conditions	8.2.2.1	N/R	

(continued)

Table C.5 (continued): Operation and maintenance requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Definition of defect indication signals	8.2.2.2		
- NF		T and V3	C.2.2
- Frames		T and V3	C.6
- Substituted frames		V3	C.3.1 and C.6.4
- LFA		T and V3	C.3.1
- Loss of power in NT1 or LT		T and V3	C.3.1 and C.6.6
- AUXP		T and V3	C.6.8
Detection of defect indication signals	8.2.2.3		
- LOS or LFA at line side of NT1		V3	C.8.3
- LOS at line side of LT		V3	C.8.8
- Loss of power at NT1		V3	C.8.6
- AIS at line side of NT1		V3	C.2.5.1
- LOS at V3		V3	C.6.3
- LOS at T		T and V3	C.6.2
- Loss of power at T		T and V3	C.3.1
Definition of detection algorithm	8.2.2.4		
- NOF		T and V3	C.2.1
- LFA		T and V3	C.4.3
- Loss of signal at T and V3		T and V3	C.3.1 and C.6.1
- AIS		T and V3	C.3.1
- Loss of power in the NT1		T and V3	C.3.1 and C.6.6
- Loss of power in the LT		T and V3	C.3.1
Consequent action	8.2.2.5	T and V3	C.6
Error performance monitoring	8.3	V3	C.4.2 and C.4.3
Operation and maintenance procedures	9	N/R	
Partitioning of function	9.1	N/R	
Definitions of signals at T reference point	9.2	N/R	
Definitions of signals at V3 reference point	9.3	N/R	

(continued)

Table C.5 (continued): Operation and maintenance requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
FEs related to operation and maintenance	table 2		
- normal DS->ET		V3	C.2.2 and C.6
- normal DS<-ET		N/A	
- unintentional loopback		V3	C.3.1 and C.6
- LOS/LFA at TE (FC2)		T and V3	C.3.1, C.4.1, and C.6.2
- LOS at line side of NT1 or at V3 (FC3)		T and V3	C.3.1 and C.6.3
- LOS/LFA at V3 of ET (FCL)		N/A	
- LOS/LFA at T (FC4)		T and V3	C.3.1 and C.6.4
- FC3 and FC4 simultaneously		T and V3	C.3.1 and C.6.5
- Loss of power at NT1		T and V3	C.3.1 and C.6.6
- Loss of power at NT1 and LOS/LFA at TE simultaneously		T and V3	C.6.7 and C.6.2
- LOS at line side of LT		V3	C.6.8 and C.3.1
- Reception of AIS at V3 of LT (reaction to FCDL or FCET)		V3	C.3.1 and C.2.5.1
- Reception of AIS at V3 of LT and FC4 simultaneously		V3	C.2.5.1
- Defect FCET in ET or FCDL between V3 and V3'		N/A	
- Defect FCDLu between V3 and V3'		N/A	
FEs related to loopback operation	table 3		
- loopback 1 command		V3	C.7
- loopback 2 command		V3	C.7
- loopback acknowledge		V3	C.7
- loopback release command		V3	C.7

(continued)

Table C.5 (concluded): Operation and maintenance requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
FEs related to CRC-4 error detection	table 4		
- CRC error report from NT1		V3	C.4.3
- CRC error information from ET		V3	C.4.3
- CRC error report from TE		V3	C.4.3
- CRC error detection at T of NT1		V3	C.4.3
- Simultaneously occurrence of FE W and FE X		V3	C.4.3
Definition of ET layer 1 state machine	9.5	N/R	
DS states	9.5.1	N/R	
DS states trans. table	9.5.2	N/R	
Assumptions	9.5.2.1	N/R	
Classification of DS states	9.5.2.2	N/R	
Definition of notations	9.5.2.3	N/R	
Notes to DS state table	9.5.2.4	N/R	

C.1.4.6 System management requirements

Table C.6: System management requirements

Functions	Clause/ subclause	Relevant interface T, V3, or T and V3	Test defined in
Introduction	A.1	N/A	
System management requirements	A.2	N/A	
General	A.2.1	N/A	
Error indications	A.2.2	N/A	
Loopback operations	A.2.3	N/A	
Information to be sent in the D channel during loopback operation	A.2.4	N/A	
Configuration control	A.2.5	N/A	
Handling of CRC error information in the ET	A.3	N/A	
Definition of ET layer 1 state machine	A.4	N/A	
ET layer 1 states	A.4.1	N/A	
PH and MPH primitives	A.4.2	N/A	
The repertoire of PH and MPH primitives	A.4.2.1	N/A	
ET layer 1 state transition table	A.4.3	N/A	
Definition of notations	A.4.3.1	N/A	
Classification of ET states	A.4.3.2	N/A	

C.2 Signal requirements

C.2.1 Access digital section transparent signal transfer

Test applicable at T and V3 reference points.

Purpose: To check the access digital section's transparent transfer of B-channel, H0-channel, H1-channel, M-channel, D-channel, A-bit, Sa7-bit and Sa8-bit between T and V3 reference points.

Test configuration:

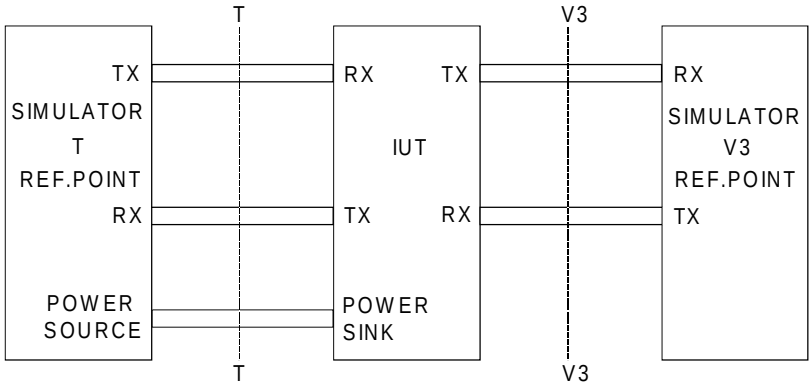

Figure C.1: Test configuration for access digital section transparent signal transfer

System state: State DS 1.11 (normal operation).

Stimulus: A PRBS is used to fill appropriate channels or bits under test.

Monitor: The IUT output signal at both T and V3 reference point.

Results: The monitored output signal has to match the stimulus signal.

C.2.2 HDB3 coding and normal operational frame

Test applicable at T and V3 reference points.

Purpose: To check the coding, decoding, and the binary organization of normal operational frame.

Test configuration:

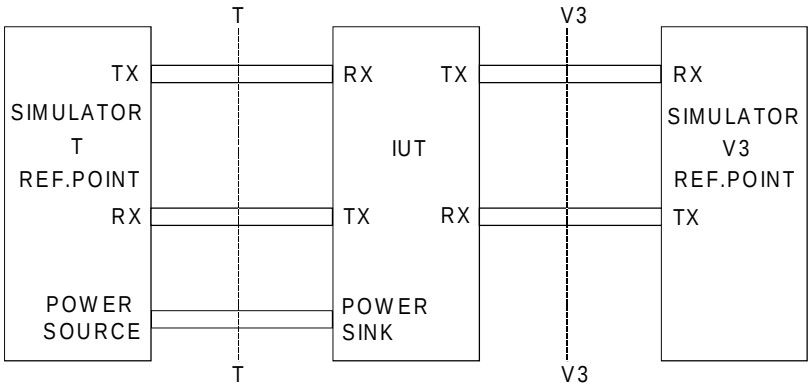

Figure C.2: Test configuration for HDB3 coding and normal operational frame

System state: State DS 1.11 (normal operation):

- network timing and layer 1 services are available;
- the network side transmits and receives operational frames with associated CRC bits and temporary CRC error information;
- the network side checks the received frames and the associated CRC bits, and transmits to the user side operational frames containing the CRC error information, if a CRC error is detected.

Stimulus: Normal operational frame sent continuously from the Simulators with valid time slot 0 including active CRC and without CRC error. A PRBS $2^{15} - 1$ shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Monitor: The coding and the frame structure of the signal sent from the IUT.

Results: The signal received shall be encoded according to the HDB3 coding rule (annex A of CCITT Recommendation G.703 [8]). The frame shall comprise valid time slot 0 with A bit set to ZERO, E bit set to ONE and including correct CRC without CRC blocks in error.

C.2.3 Frame structure

These tests check the frame composition.

C.2.3.1 Number of bits per time slot

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

C.2.3.2 Number of time slots per frame

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

C.2.3.3 Generation of frame alignment word

Test applicable at T and V3 reference point.

Purpose: To check the correct generation of frame alignment word, Multiframe (MF) alignment word, CRC bits C1 to C4.

Test configuration:

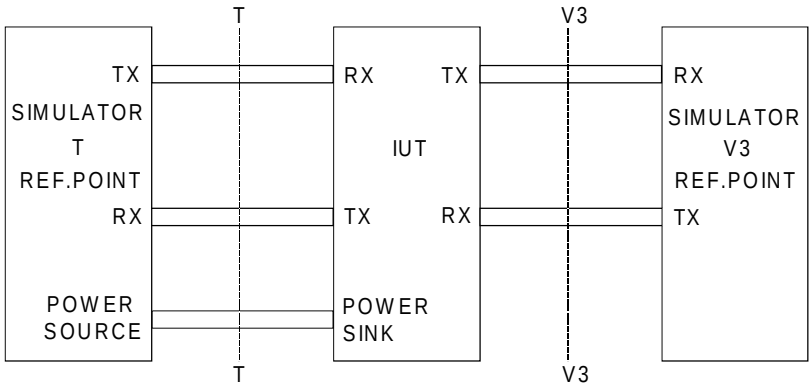

Figure C.3: Test configuration for generation of frame alignment word

System state: State DS 1.11 (normal operation).

Stimulus: Normal operational frames with PRBS 2^{15} - 1 in time slot 1 to 31.

A PRBS 2^{15} - 1 shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Monitor: Correct frame alignment word, MF alignment word, CRC bits.

Results: No detection of incorrect frame alignment word, MF alignment word, and no received Sub-Multiframes (SMFs) in error within 1 s measured in any state.

During this test the E bit is not considered.

C.2.4 Signal transfer delay

Test applicable at T and V3 reference points.

Purpose: To test the mean one way delay between T and V3 interfaces in the two directions of transmission.

Test configuration:

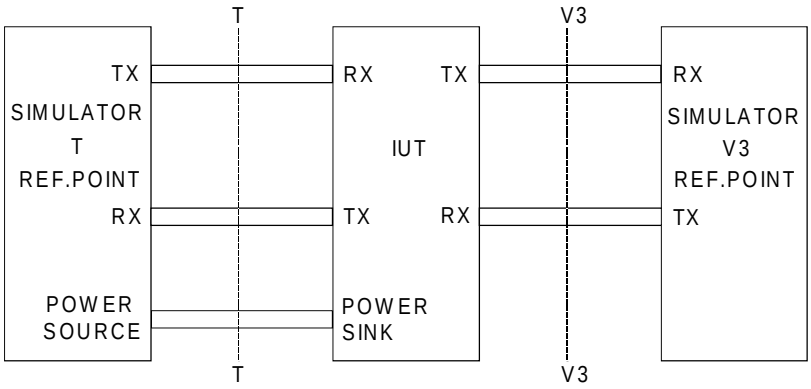

Figure C.4: Test configuration for signal transfer delay

System state: State DS 1.11 (normal operation):

- network timing and layer 1 services are available.

Stimulus: An appropriate sequence sent in the B channels.

Monitor: Measure the delay to receive this sequence in the B channels at the reception side.

Results: Mean value < 1 250 μs.

C.2.5 Timing considerations

C.2.5.1 AIS recognition

Test applicable at V3 reference point.

Purpose: To check the ability of the IUT to recognize AIS.

Test configuration:

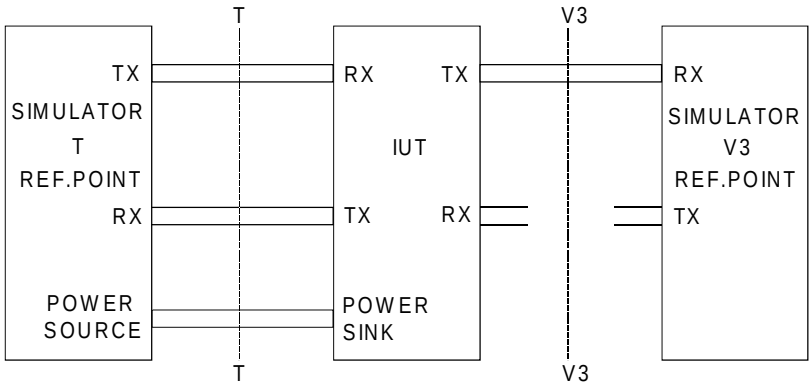

Figure C.5: Test configuration for timing considerations, AIS recognition

System state: State DS 6.66

Stimulus: AIS signal at V3 reference point with nominal clock frequency 2 048 kbit/s, nominal clock frequency + 50 ppm, nominal clock frequency - 50 ppm.

The user side transmits, through the DS, to the network side operational frames with associated CRC bits and RAI.

Monitor: The frames transmitted by the IUT.

Results: The IUT shall remain in state DS 6.66, therefore no change of error indication shall occur.

AIS shall be detected at T reference point, FE M and associated CRC bits at V3 reference point.

C.2.5.2 AIS generation

Test applicable at T reference point.

Purpose: To check the frequency of the AIS signal generated by the IUT.

Test configuration:

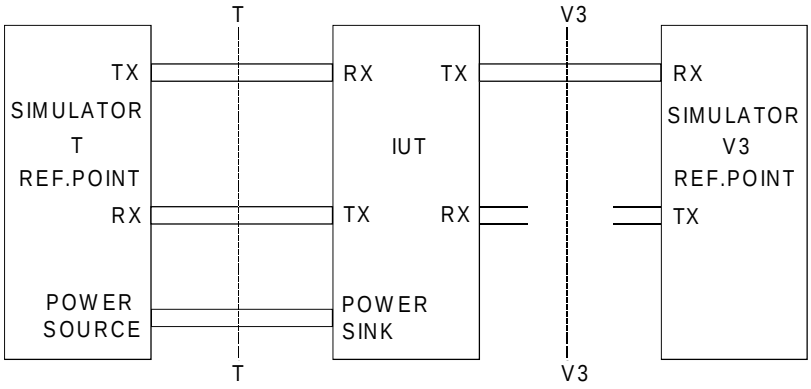

Figure C.6: Test configuration for timing considerations, AIS generation

System state: State DS 4.32.

Stimulus: LOS of signal at V3 reference point (FV 3).

Monitor: The frequency of the signal generated by the IUT at the T reference point.

Results: The frequency has to be in the range 2 048 kbit/s ± 50 ppm.

C.2.5.3 Synchronisation at V3 reference point

Test applicable at V3 reference point.

Purpose: The ability of the IUT to synchronize its timing on the signal received from the network and its ability to transfer this timing at T reference point.

Test configuration:

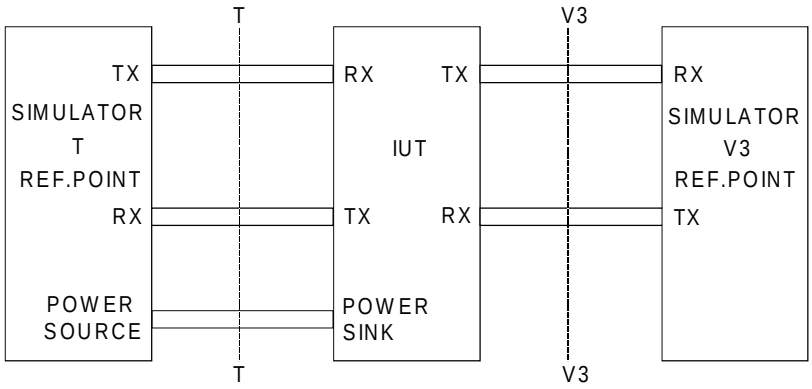

Figure C.7: Test configuration for timing considerations, synchronisation at V3 reference point

System state: State DS 1.11 (normal operation):

- network timing and layer 1 services are available.

Stimulus: Normal operational frames with clock frequency variation from the nominal value in the range 2 048 kbit/s ± 5 ppm.

A PRBS 2^{15} - 1 shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Monitor: The frames transmitted by the IUT.

Results:

1) the IUT shall remain in state DS 1.11, no LFA/LOS shall be detected at T and V3 reference point;

2) the frequency of the outgoing signal at each access has to follow the frequency of the stimulating input signal.

C.2.5.4 Synchronisation at T interface

Purpose: The ability of the IUT to synchronise to a frame signal at the T interface during FC 2.

Test configuration:

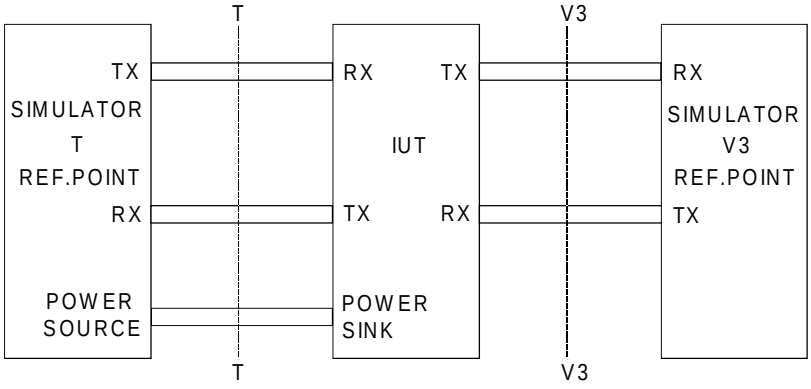

Figure C.8: Test configuration for timing considerations, synchronisation at T interface

System state: State DS 1.11 with FC 2:

- network timing at network side and layer 1 services are available.

Stimulus: NF at V3 reference point with nominal clock frequency.

NF at T reference point with A = 1 and clock frequency variation from the nominal value of 2 048 kbit/s + 50 ppm and 2 048 kbit/s - 50 ppm.

A PRBS 2^{15} - 1 shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Monitor: A bit, Sa5 bit and Sa6 bit at V3 reference point.

Results: Verify that A = 1, Sa5 = 1 and Sa6 = 00xx (x representing any value ONE or ZERO).

C.2.5.5 Octet Timing and B channels octet transparency

Test applicable at T and V3 reference points.

Purpose: To check the access digital section's transparent transfer of B-channel octets between T and V3 reference points.

Test configuration:

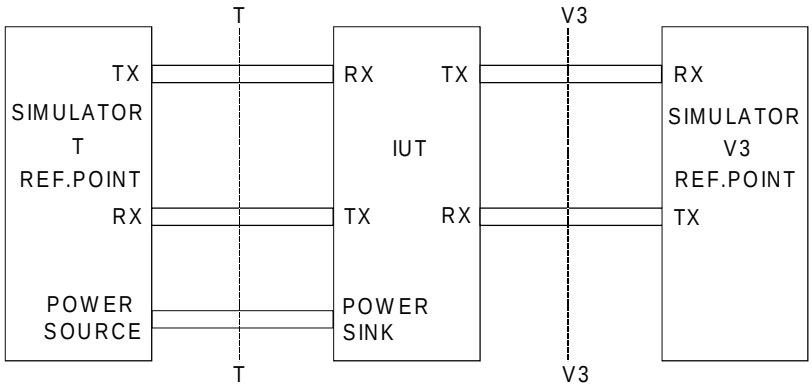

Figure C.9: Test configuration for timing considerations, octet timing and B channels octet transparency

System state: State DS 1.11 (normal operation).

Stimulus 1: Alternatively a fixed word is inserted in a selected B channel chosen in the range from B_1 to B_{15} and B_{17} to B_{31}. The stimulus is applied at the T reference point.

Stimulus 2: Alternatively a fixed word is inserted in a selected B channel chosen in the range from B_1 to B_{15} and B_{17} to B_{31}. The stimulus is applied at the V3 reference point.

Monitor 1: The words in the selected B channel at the V3 reference point.

Monitor 2: The words in the selected B channel at the T reference point.

Results: No bit errors.

C.2.6 Jitter

C.2.6.1 Minimum tolerance to jitter and wander at inputs

Test applicable at T reference point.

Purpose: To check the ability of the IUT to tolerate on the 2 048 kbit/s incoming signal a sinusoidal jitter/wander in accordance with ETS 300 011 [1], table 1, subclause 5.4.2.

Test configuration:

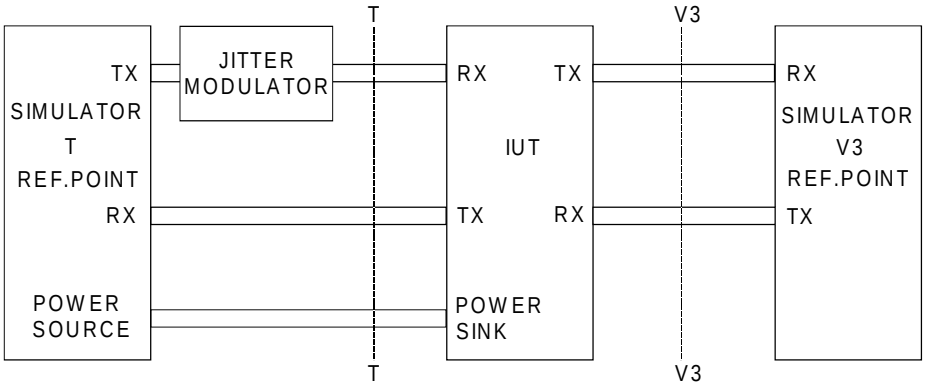

Figure C.10: Test configuration for minimum tolerance to jitter and wander at inputs

System state: State DS 1.11 (normal operation):

- network timing and layer 1 services are available;
- the network side transmits and receives operational frames with associated CRC bits and temporary CRC error information;
- the network side checks the received frames and the associated CRC bits, and transmits to the user side operational frames containing the CRC error information, if a CRC error is detected.

Stimulus: Normal operational frames with jitter/wander according to the table C.7 (reference: ETS 300 011 [1], table 1, subclause 5.4.2) and with a PRBS 2^{15} - 1 in time slots 1 to 31. The PRBS 2^{15} - 1 shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Table C.7

A0	A1	A2	f0	f1	f2	f3	f4
20,5 UI p-p	1,0 UI p-p	0,2 UI p-p	$12x10^{-6}$ Hz	20 Hz	3,6 Hz	18 kHz	100 kHz

This test shall be performed twice with clock frequency varying from the nominal value + 5 ppm and - 5 ppm.

Points A1 - f2 and A2 - f4 shall be measured. For the range between A0 - f0 to A1 - f1 the jitter behaviour can be determined from the Q factor.

Monitor: The frames transmitted by the IUT.

Results: The IUT shall remain in state DS 1.11 (operational state), no LFA report shall be detected by the simulator at V3 reference point.

NOTE 1: This test relies on the correct operation of the CRC error information report by the IUT.

C.2.6.2 Output jitter at V3 reference point

Test applicable at V3 reference point.

Purpose: To measure the jitter generated by the IUT.

Test configuration:

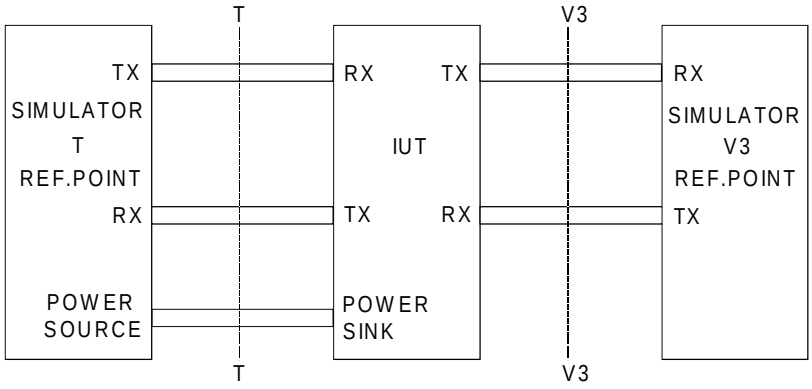

Figure C.11: Test configuration for output jitter at V3 reference point

System state: State DS 1.11 (normal operation).

Stimulus: Normal operational frames with jitter according to the table C.8, provided to the synchronizing input of the IUT (i.e. connected at T reference point to the access digital section) and with a PRBS $2^{15} - 1$ in time slots 1 to 31. The PRBS $2^{15} - 1$ shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s) with frequency variation in the range 2 048 kbit/s ± 5 ppm (two different measurements).

Table C.8

Modulating frequency	Input jitter UI peak to peak
40 Hz	1,1
100 kHz	0,11

Monitor: The jitter extracted from the signal transmitted by the IUT.

Results: The peak to peak jitter shall comply with the limits given in CCITT Recommendation G.823 [6].

C.2.6.3 Output jitter at T reference point

Test applicable at T reference point.

Purpose: To measure the jitter generated by the IUT.

Test configuration:

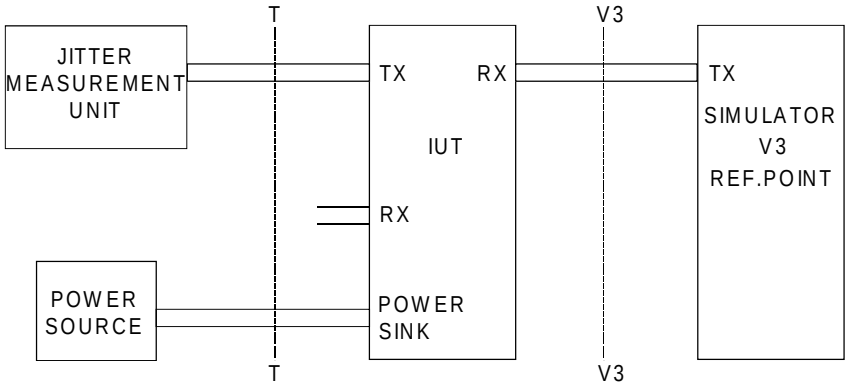

Figure C.12: Test configuration for output jitter at T reference point

The jitter measurement shall be done using equipment that has an external timing reference to the jitter measurement set which has no phase variation energy in the jitter region under test.

System state: State DS 1.11 (normal operation).

Stimulus: Normal operational frames without jitter provided by the simulator (i.e. connected at V3 reference point to the access digital section) and with a PRBS $2^{15} - 1$ in time slots 1 to 31. The PRBS $2^{15} - 1$ shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s) with frequency variation in the range 2 048 kbit/s ± 5 ppm (two different measurements).

Monitor: The jitter extracted from the signal transmitted by the IUT.

Results: The peak to peak jitter shall comply with table C.9.

Table C.9

Measurement filter bandwidth		**Output jitter**
Lower cut off (high pass)	**Upper cut off (low pass)**	**UI peak to peak**
20 Hz	100 kHz	≤ 1 UI
18 kHz	100 kHz	≤ 0,2 UI

C.3 State matrix

C.3.1 State matrix of the IUT

Test applicable at T and V3 reference point.

Purpose: The tests defined in this subclause intend to check the different stable states at the IUT sides and the possible transitions between them. These tests are performed by simulating the opposite side (and simulating internal fault in the IUT), monitoring the IUT at the interfaces and verifying appropriate state transition.

As a minimum, all transitions from and returning to normal state DS 1.11 shall be tested in accordance with clauses C.6 and C.7.

C.4 Interface procedure tests

Definition of test sequences

FAS	Frame with correct Frame Alignment Signal (FAS), correct bits C1 to C4 and correct CRC Multiframe Alignment Signal (MFAS) in time slot 0.
/FAS	Frame with incorrect FAS, correct bits C1 to C4 and correct MFAS in time slot 0.
BIT 2	Bit 2 of time slot 0 not containing the FAS.
FRAME A	Two consecutive frames having FAS in the first time slot 0, BIT 2 = 1 in the second time slot 0 and no contiguous group of seven bits which simulates the FAS in time slots 1 to 31.
FRAME B	Two consecutive frames having FAS in the first time slot 0, BIT 2 = 1 in the second time slot 0, simulated BIT 2 = 1 in the first time slot 31 and simulated FAS (no corresponding MFAS) in the second time slot 31.
FRAME C	Two consecutive frames having /FAS in the first time slot 0, BIT 2 = 1 in the second time slot 0, simulated BIT 2 = 1 in the first time slot 31 and simulated FAS (no corresponding MFAS) in the second time slot 31.
SMF A	SMF having correct generation of C1 to C4 bits.
SMF B	SMF having incorrect generation of C1 to C4 bits.
MF A	MF having correct FAS, BIT 2 = 1, MFAS and correct C1 to C4 bits.
MF B	MF having correct FAS, BIT 2 = 1, but incorrect MFAS and correct C1 to C4 bits.
# n	# indicates that the sequence defined in the previous line may be repeated before entering the next sub-sequence. If the parameter "n" is defined this sequence shall be repeated ≥ "n" times.

Additional information regarding interface procedure tests:

- when monitoring interfaces it has to be recognized that a time delay period independent of actual response times of interfaces receivers/transmitters may be introduced (e.g. delays attributable to the implementation of transmission systems between the NT and LT inside the access digital section). Therefore it is to be expected that test state transitions may show a delay when monitored;

- separate test response descriptions for interfaces T and V3 are provided. Indication of state transition is given only where stimulus is repeated (indicated by a #). The expected signal response to a repeated stimulus may however still display a time delay.

C.4.1 Frame alignment (without the test of CRC procedure)

Test applicable at T and V3 reference point.

Purpose: To test that the IUT correctly executes the frame alignment procedure.

Test configuration:

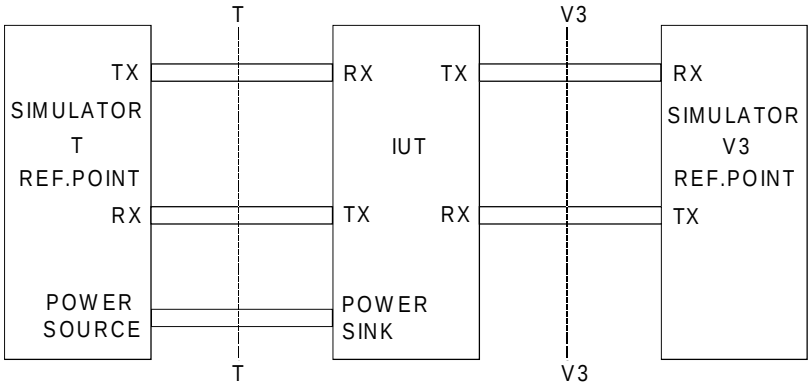

Figure C.13: Test configuration for frame alignment (without the test of CRC procedure)

System state: Various states.
(according to ETS 300 011 [1], subclause C.4.3)

Stimulus: Consecutive correct and errored frame sequences (but including correct MF alignment signal and correct bits C1 to C4) from the simulator at V3 reference point, i.e. bit 2 to 8 of time slot 0 containing the FAS and bit 2 of time slot 0 not containing the FAS, as given below.

The test signal shall not contain any other contiguous group of seven bits which simulates the FAS.

Monitor: Output signals from the IUT.

Results: As listed in table C.10.

Table C.10

STIMULUS	MONITOR	COMMENT
BIT 2 = 1, FAS (note 1)		
#	NOF	Frame alignment tests
BIT 2 = 1, /FAS	NOF	
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS	NOF	
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS	RAI	
BIT 2 = 1, FAS, BIT 2 = 1, FAS	NOF	
#		

(continued)

Table C.10 (concluded)

BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS	RAI	
BIT 2 = 1, FAS, BIT 2 = 1, /FAS	RAI	
#		
BIT 2 = 1, FAS	RAI	
BIT 2 = 0, FAS	RAI	
#		
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 0, FAS, BIT 2 = 1, FAS, BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 0, FAS, BIT 2 = 0, FAS, BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 0, FAS, BIT 2 = 0, FAS, BIT 2 = 0, FAS	RAI or NOF (note 2)	
#		
BIT 2 = 1, FAS	NOF	
#		
BIT 2 = 1		
FRAME B	NOF	Correct frame alignment
#		
6 X FRAME C	RAI -> NOF	Loss of frame alignment and frame alignment with simulated frame alignment word
FRAME B	NOF	
# 4 to 8 ms	RAI and back to NOF will occur (if MF alignment is operating properly), (note 3)	No MF alignment on the simulated frame alignment word
	No further RAI shall occur within a time period of 20 ms	

NOTE 1: This stimulus shall be repeated in order to allow clock synchronisation of the IUT, the time taken to synchronise may be dependent on the implementation.

NOTE 2: RAI or NOF depending on the implementation options described in CCITT Recommendation G.706 [7], subclause 4.1.1 and ETS 300 011 [1], clause 5.

NOTE 3: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

C.4.2 CRC MF alignment

Test applicable at T and V3 reference point.

Purpose: To test if the IUT correctly executes the CRC MF alignment.

Test configuration:

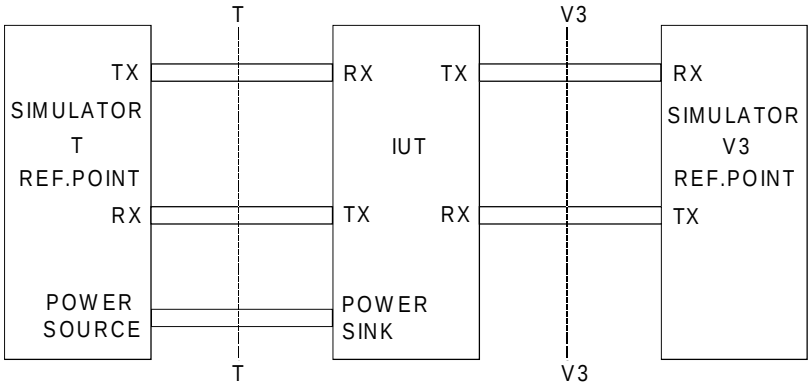

Figure C.14: Test configuration for CRC MF alignment

System state: Various states.

Stimulus: Consecutive correct and errored CRC MF alignment signals from the simulator, i.e. bit 1 in frames not containing the FAS as given below.

Monitor: Output signal from the IUT as given below.

Results: As listed in table C.11.

Table C.11

STIMULUS	MONITOR	COMMENT
FRAME B (note 1)		
#	NOF	
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1	RAI	Initial condition
MF A	NOF	
4 X MF B	RAI	No MF alignment
MF A	NOF	
37 X MF B	NOF, transition to RAI and back to NOF (note 2)	2 MFAS within 8 ms in the limit of 100 ms
MF A, MF B, MF A, MF B, MF A, MF B	NOF	
MF B	NOF	
# 251	Stable NOF	No RAI 500 ms after a loss of MF alignment
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1	RAI	Initial condition
MF B	NOF	Correct frame alignment but not MF alignment
# 250		No MF alignment within 500 ms
MF B	RAI	
MF A, 4 X MF B	RAI	
MF A, 2 X MF B, MF A		Undefined condition
MF A, 2 X MF B, 2 X MF A	NOF	MF alignment reached
MF B, MF A	NOF	
#		

NOTE 1: This stimulus shall be repeated in order to allow clock synchronisation of the IUT, the time taken to synchronise may be dependent on the implementation.

NOTE 2: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

C.4.3 CRC processing

Test applicable at T and V3 reference points.

Purpose: To test the correct execution of CRC calculation, comparison with the received bits C1 to C4 and generation of the CRC error report with bit E.

Test configuration:

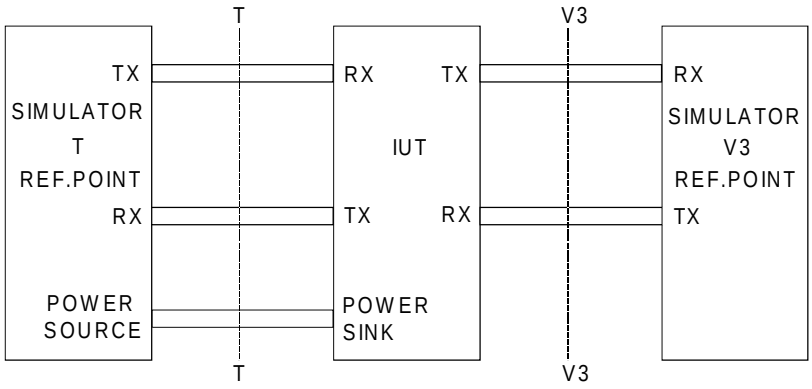

Figure C.15: Test configuration for CRC processing

System state: State DS 1.11 (normal operation).

Stimulus: SMF A and SMF B at interface of the test as given below.

Monitor: Output signal at the IUT, i.e. E bits as given below.

Results: As listed in tables C.12 and C.13.

A CRC error report, indicated by an E bit set to ZERO, shall be received within 1 s after the generation of a SMF in error. Definition of a SMF in error is given in CCITT Recommendation G.704 [3], subclause 2.3.3.5.3.

Table C.12

STIMULUS	**MONITOR**	
at T ref. point	**T**	**V3 (DS --> ET)**
SMF A	No E bit set to ZERO	FE A
# Repeat more than 1 s		
SMF B	One E bit set to ZERO	FE X
SMF A	No E bit set to ZERO	FE A
SMF B, SMF B	Two contiguous E bits set to ZERO	FE X
SMF A	No E bit set to ZERO	FE A
# Repeat more than 1 s		
914 X SMF B	914 contiguous E bits set to ZERO	FE X
86 X SMF A		
914 X SMF B	914 contiguous E bits set to ZERO	FE X
SMF A	No E bit set to ZERO	FE A
# Repeat more than 1 s		
915 X SMF B		
85 X SMF A	Less than 85 contiguous E bits set to ONE	Temporarily FE G (note)
915 X SMF B		
SMF A	No E bit set to ZERO	FE A
#		
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1,	No E bit set to ONE	FE G
/FAS, BIT 2 = 1		
#	No E bit set to ONE	FE G
E bit set to ZERO	No E bit set to ZERO	FE W
SMF B with E bit set to ZERO	one E bit set to ZERO	FE Y
NOTE: Due to possible delay FE G may not be generated.		

Table C.13

STIMULUS at V3 ref. point	**MONITOR**	
	T	**V3 (DS -> ET)**
SMF A	NOF	FE A (no E bit set to ZERO)
# Repeat more than 1 s		
SMF B	NOF	FE U (one E bit set to ZERO)
SMF A	NOF	FE A (no E bit set to ZERO)
SMF B, SMF B	NOF	FE U (two E bits set to ZERO)
SMF A	NOF	FE A (no E bit set to ZERO)
# Repeat more than 1 s		
914 X SMF B	NOF	914 contiguous E bits set to ZERO
86 X SMF A	NOF	No E bit set to ZERO
914 X SMF B	NOF	914 contiguous E bits set to ZERO
SMF A	NOF	FE A (no E bit set to ZERO)
# Repeat more than 1 s		
915 X SMF B 85 X SMF A 915 X SMF B	Temporarily AIS (note 2)	Temporarily FE E FE G (note 1)
SMF A	NOF	FE A (no E bit set to ZERO)
#		
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1,	AIS	FE E (no E bit set to ZERO)
/FAS, BIT 2 = 1		
#		No E bit set to ONE

NOTE 1: Due to possible delay FE E may not be generated.

NOTE 2: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

C.5 Power feeding

C.5.1 Power consumption and interchange of wires

Test applicable at the T reference point.

Purpose: To verify that the power consumption is within the specified limits and that no damage shall occur in case of interchanging of the power feeding wires.

Test configuration:

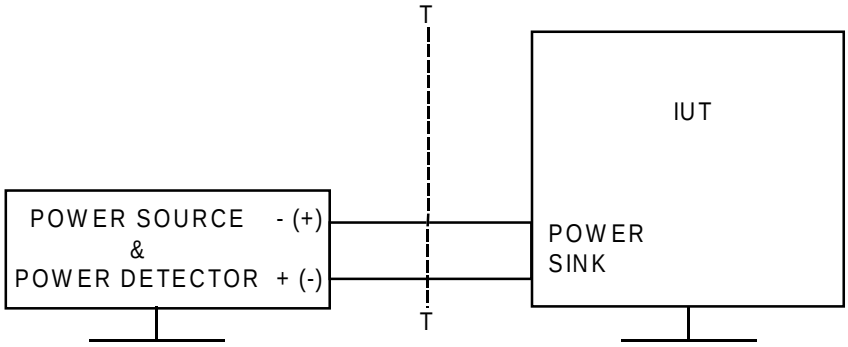

Figure C.16: Test configuration for power consumption and interchange of wires

System state: Any state.

Stimulus:
1) feeding voltage: - 20 Volts to - 57 Volts (1 minute);
2) feeding voltage: + 20 Volts to + 57 Volts (5 minutes);
3) feeding voltage: - 20 Volts to - 57 Volts.

Result: The power drawn by the IUT shall not exceed 7 Watts. The IUT shall be able to operate correctly when fed in step 1 and 3.

C.6 Detection of defect conditions

C.6.1 Loss of signal at T and V3 reference points

Test applicable at the V3 reference point.

Purpose: To check the ability of the IUT to recognize LOS.

Test configuration:

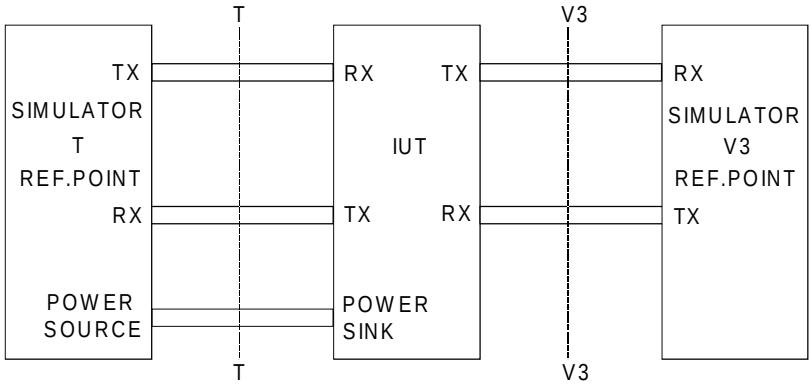

Figure C.17: Test configuration for detection of loss of signal at T and V3 reference points

System state: State DS 1.11 (normal operation).

Stimulus 1: The incoming signal at T reference point is kept 20 dB below the nominal amplitude (as defined in CCITT Rec. G.703 [8]) for ≥ 1 ms.

Stimulus 2: The incoming signal at V3 reference point is kept 20 dB below the nominal amplitude (as defined in CCITT Rec. G.703 [8]) for ≥ 1 ms.

Monitor 1: Sa5 bit and $Sa6_1$...$Sa6_4$ bits at V3 reference point.

Monitor 2: The signal transmitted by the DS to the ET and to the TE.

Results 1: LFA is assumed by the IUT. Sa5 = 1 and Sa6 = 1100.

Results 2: LFA is assumed by the IUT. AUXP has to be sent toward NT. AIS is detected in direction of the TE, Sa6 = 1110 has to be sent toward the ET.

C.6.2 Detection of FC2 at the TE

Test applicable at V3 reference point.

Purpose: To check signal exchange between the DS and the ET when LOS/LFA is detected at T reference point of the TE (FC2).

Test configuration:

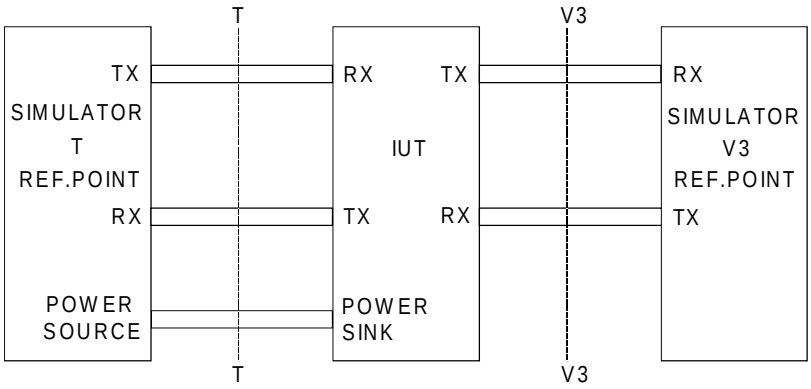

Figure C.18: Test configuration for detection of FC2 at the TE

System state: State DS 1.11 (normal operation).

Stimulus: A FC2 is induced at T reference point by disconnecting the interface signal Receiver (Rx) of the simulator. Normal Frame sent continuously from the simulators with valid time slot 0 including active CRC and without CRC error. A PRBS 2^{15} - 1 shall fill continuously all the frame except time slot 0 (net bit rate 1 984 kbit/s).

Monitor: Sa5 bit and $Sa6_1$ ... $Sa6_4$ bits.

Results: Verify that A = 1, Sa5 = 1 and Sa6 = 00xx (x representing any value ONE or ZERO).

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.3 LOS at line side of NT1 or at the V3 reference point (FC3)

Test applicable at the V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when FC3 is detected.

Test configuration:

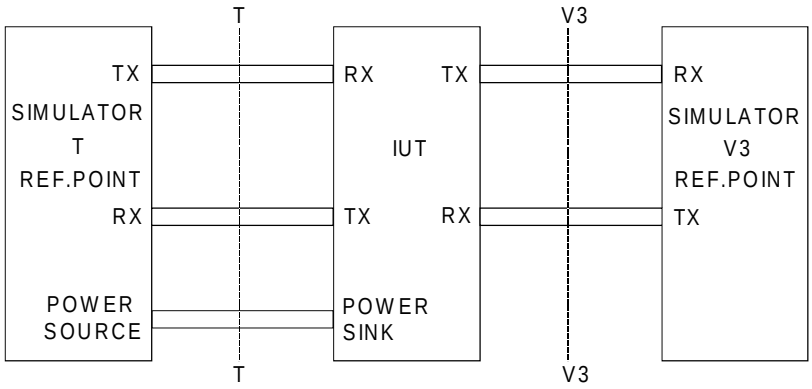

Figure C.19: Test configuration for detection of LOS at line side of NT1 or at the V3 reference point (FC3)

System state: State DS 1.11 (normal operation).

Stimulus 1: A FC3 is induced at the V3 reference point by disconnecting the V3 wiring cable of the V3 reference point simulator transmitter (Tx).

Stimulus 2: A FC3 is induced inside the DS by interrupting the signal at the NT1 receiver on the network side.

Monitor: A bit, Sa5 bit and $Sa6_1$ ... $Sa6_4$ bits.

Results: Verify that A = 1, Sa5 = 1 and Sa6 = 1110.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.4 LOS/LFA at T reference point of NT1 (FC4)

Test applicable at the V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when FC4 is detected at T reference point.

Test configuration:

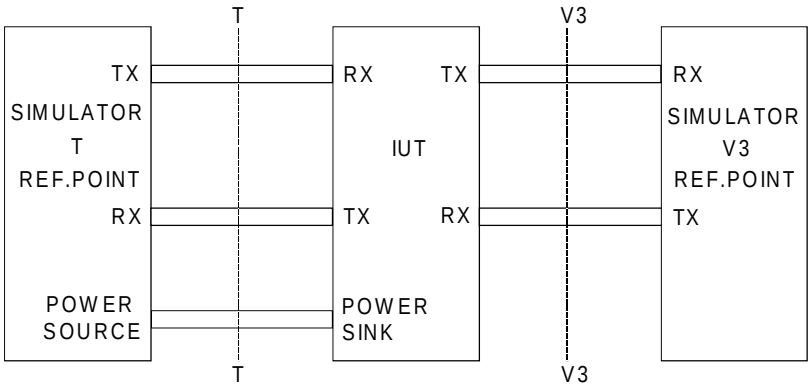

Figure C.20: Test configuration for detection of LOS/LFA at T reference point of NT1 (FC4)

System state: State DS 1.11 (normal operation).

Stimulus 1: A FC4 is induced at the T reference point by disconnecting the Tx of the T reference point simulator.

Stimulus 2: A FC4 is induced at the T reference point by the T simulator sending a signal with nominal bit rate without any framing.

Monitor: The signal transmitted by the DS toward the ET.

Results: When LOS or LFA defect conditions occur at T reference point (FC4), the DS generates and sends toward the ET frames where Sa4-bits , Sa5-bits , Sa7-bits and Sa8-bits as well as the bits in time slots 1 to 31 are set to ONE. The A bit is set to ZERO, the $Sa6_1...Sa6_4$ bits contain the coded defect condition message reported to the ET i.e. Sa6 = 1100.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.5 FC3 and FC4 simultaneously

Test applicable at the V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when FC3 and FC4 occur together.

Test configuration:

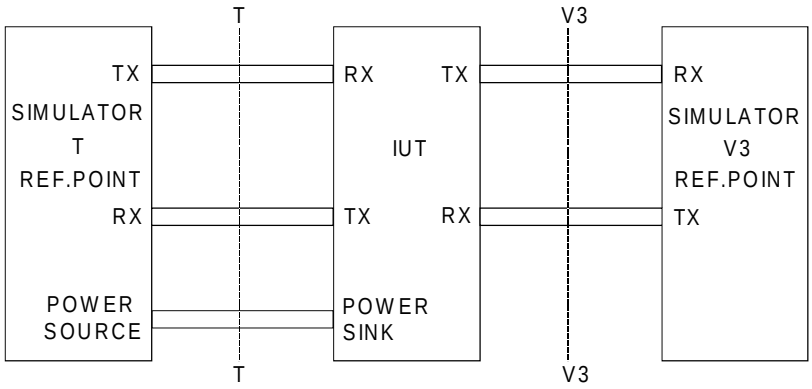

Figure C.21: Test configuration for detection of FC3 and FC4 simultaneously

System state: State DS 1.11 (normal operation).

Stimulus: An FC3 and FC4 fault condition is induced simultaneously as in tests defined in subclauses C.6.3 and C.6.4 by disconnecting the appropriate simulator wiring cables at the T and V3 reference points.

Monitor: A bit, Sa5 bit and $Sa6_1$ ... $Sa6_4$ bits.

Results: Verify that A = 0, Sa5 = 1 and Sa6 = 1110 (detection of FE H at V3 reference point).

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.6 Loss of power at NT

Test applicable at the V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when the NT1 detects loss of power.

Test configuration:

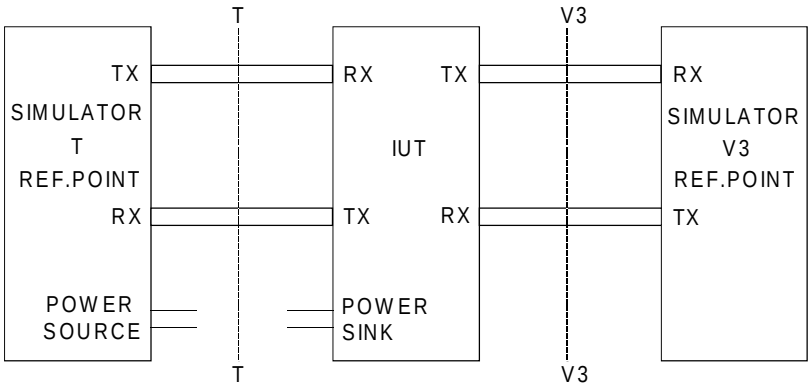

Figure C.22: Test configuration for detection of loss of power at NT

System state 1: State DS 1.11 (normal operation).

System state 2: State DS 5.15 (loopback 2).

Stimulus: The power supply to the NT1 is interrupted.

Monitor: A bit, Sa5 bit and $Sa6_1$ ... $Sa6_4$ bits.

Results 1: Verify that A = 0, Sa5 = 1 and Sa6 = 1000 is indicated for ≥ 60 ms.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

Results 2: Verify that Sa5 = 0 and Sa6 = 1000 is indicated for ≥ 60 ms.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.7 Loss of power at the NT1 and LOS/LFA at the TE simultaneously

Test applicable at T and V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when Loss of power at NT1 and LOS/LFA at the TE occur together.

Test configuration:

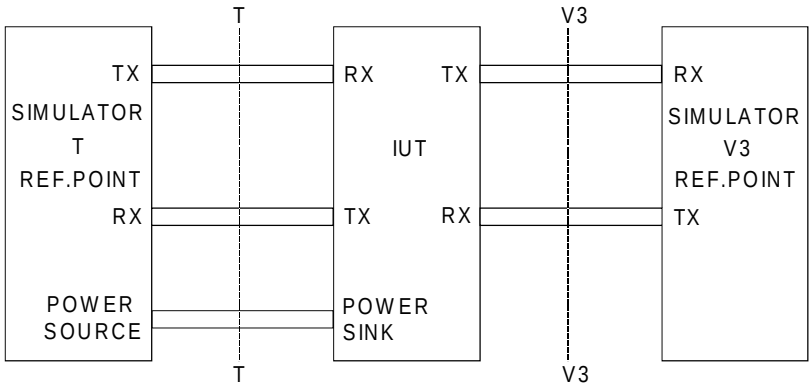

Figure C.23: Test configuration for detection of loss of power at the NT1 and LOS/LFA at the TE simultaneously

System state: State DS 1.11 (normal operation).

Stimulus: A LFA/LOS defect condition is induced at the T reference point by disconnecting the Tx of the T reference point simulator. Also the power supply to the NT1 is interrupted.

Monitor: A bit, Sa5 bit and $Sa6_1$...$Sa6_4$ bits.

Results: Verify that A = 1, Sa5 = 1 and Sa6 = 1000 (detection of FE K at the V3 reference point) is indicated for ≥ 60 ms.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.6.8 LOS at line side of the LT

Test applicable at the V3 reference point.

Purpose: To check the signal exchange between the DS and the ET when LOS is detected at the line side of the LT.

Test configuration:

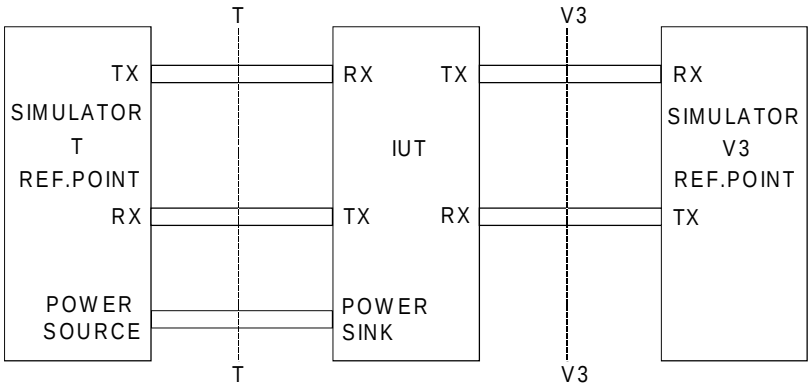

Figure C.24: Test configuration for detection of LOS at line side of the LT

System state: State DS 1.11 (normal operation).

Stimulus: A LOS defect condition at the line side of the LT is induced by disconnecting the wiring cable at the line side receiver of the LT.

Monitor: The signal transmitted by the DS to the ET.

Results: AUXP shall be sent toward the ET.

The defect indication to the ET shall be sent or removed with a maximum delay of 10 ms.

C.7 Loopback operations

FAS	Frame with correct FAS correct bits C1 to C4 and correct MFAS (CRC MFAS in time slot 0).
# n	# indicates that the sequence defined in the previous line may be repeated before entering the next sub-sequence. If the parameter "n" is defined this sequence shall be repeated ≥ "n" times.
PRBS(x)	Pseudo Random Bit Sequence 2^x - 1.
SMF A	SMF having loopback 1 command. Bit A = 1 and bit Sa6 = 1111 (FE Q).
SMF B	SMF having loopback 2 command. Bit A = 1 and bit Sa6 = 1010 (FE R).
SMF C	SMF having loopback release command. Bit A = 0 and bit Sa6 = 0000 (FE T).
SMF D	4 x FAS. SMF having correct Frame Alignment Signal (FAS) correct bits C1 to C4 and correct CRC MFAS in time slot 0 and without any loopback command request.

Additional information regarding interface procedure tests:

- when monitoring interfaces, a time delay period independent of actual response times of interfaces receivers/transmitters may be introduced (e.g. delays attributable to the implementation of transmission systems between the NT and ET inside the access digital section). Therefore, test state transitions may show a delay when monitored;

- separate test response descriptions for interfaces T and V3 are provided. Indication of state transition is given only where stimulus is repeated (indicated by a #). However, the expected signal response to a repeated stimulus may still display a time delay.

C.7.1 Loopback 1 procedure

Test applicable at V3 reference point.

Purpose: To check the correct loopback 1 activation deactivation procedure in the relevant DS states.

Test configuration:

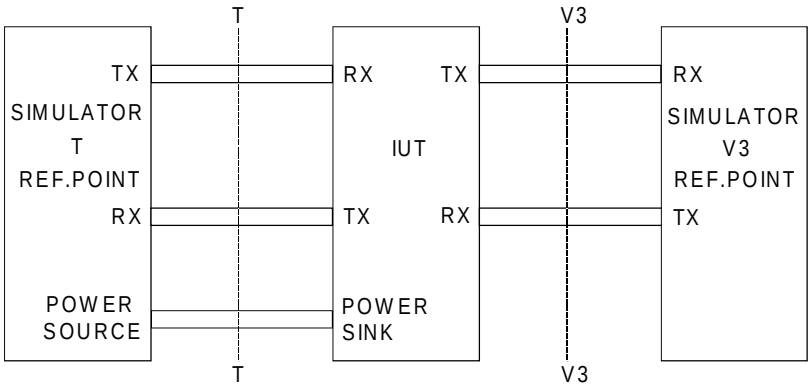

Figure C.25: Test configuration for loopback 1 procedure

System state: State DS 1.11 (normal operation).
State DS 3.13 (FC 4).
State DS 2.21 (FC 1).

Stimulus: For each state indicated a sequence of SMF A, SMF C and SMF D as given below.

A PRBS 2^{15} - 1 is in B channels 1 to 31 from the simulator at the V3 reference point.

A PRBS 2^{11} - 1 is in B channels 1 to 31 from the simulator at the T reference point.

Monitor: Bits A, Sa5, $Sa6_1$ ... $Sa6_4$.

B channels 1 to 31.

Results: As listed in table C.14.

Table C.14

STIMULUS		MONITOR V3 (DS -> ET)
SMF D	Operational SMF	FE A
# Repeat more than 1 s		
SMF A	SMF having loopback 1 request	
# 8		FE S loopback acknowledge
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF C	SMF having loopback release	
# 8	Loopback release	FE A
SMF D		FE A PRBS(11) in B channels
# Repeat more than 1 s		
SMF A	SMF having loopback 1 request	
# 7	Loopback 1 request not complete	FE A PRBS(11) in B channels No bit error
SMF D	Correct operational SMF	FE A
# Repeat more than 1 s		
SMF A	SMF having loopback 1 request	
# 8		FE S
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF C	SMF having loopback release	
# 7	Incorrect loopback release request	FE S PRBS(15) in B channels No bit error
SMF D		FE A PRBS(11) in B channels
# Repeat more than 1 s		
SMF A	SMF having loopback 1 request	
# 8		FE S PRBS(15) in B channels
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF D	Correct operational SMF	
# 8	Loopback release	FE A
SMF D	Correct operational SMF	FE A
# Repeat more than 1 s		
SMF A	SMF having loopback 1 request	
# 8		FE S
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF D	Correct operational SMF	
# 7	Incorrect loopback release sequence	FE S PRBS(15) in B channels No bit error

C.7.2 Loopback 2 procedure

Test applicable at the V3 reference point.

Purpose: To check the correct loopback 2 activation deactivation procedure in the relevant DS state.

Test configuration:

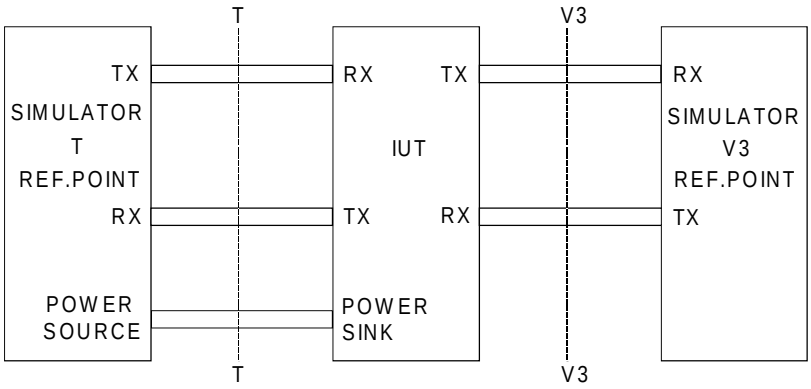

Figure C.26: Test configuration for loopback 2 procedure

System state 1: State DS 1.11 (normal operation).

System state 2: State DS 3.13 (FC 4).

Stimulus: For both system states 1 and 2 indicated above, a sequence of SMF B, SMF C and SMF D as given below.

A PRBS 2^{15} - 1 is in B channels 1 to 31 from the simulator at the V3 reference point.

A PRBS 2^{11} - 1 is in B channels 1 to 31 from the simulator at the T reference point.

Monitor: Bits A, Sa5, $Sa6_1$ ... $Sa6_4$.

B channels 1 to 31.

Results: As listed in table C.15.

Table C.15

STIMULUS		MONITOR V3 (DS -> ET)
SMF D	Operational SMF	FE A
# Repeat more than 1 s		
SMF B	SMF having loopback 2 request	
# 8		FE S loopback acknowledge
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF C	SMF having loopback release	
# 8	Loopback release	FE A
SMF D		FE A PRBS(11) in B channels
# Repeat more than 1 s		
SMF B	SMF having loopback 2 request	
# 7	Loopback 2 request not complete	FE A PRBS(11) in B channels No bit error
SMF D	Correct operational SMF	FE A
# Repeat more than 1 s		
SMF B	SMF having loopback 2 request	
# 8		FE S
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF C	SMF having loopback release	
# 7	Incorrect loopback release request	FE S PRBS(15) in B channels No bit error
SMF D		FE A PRBS(11) in B channels
# Repeat more than 1 s		
SMF B	SMF having loopback 2 request	
# 8		FE S PRBS(15) in B channels
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF D	Correct operational SMF	
# 8	Loopback release	FE A
SMF D	Correct operational SMF	FE A
# Repeat more than 1 s		
SMF B	SMF having loopback 2 request	
# 8		FE S
# Repeat more than 1 s		FE S PRBS(15) in B channels
SMF D	Correct operational SMF	
# 7	Incorrect loopback release sequence	FE S PRBS(15) in B channels No bit error

History

Document history	
May 1994	First Edition of ETS 300 233
March 1995	First Edition
January 1996	Converted into Adobe Acrobat Portable Document Format (PDF)
Note:	The references to the changed pages in the standard refer to an old presentation. See history box at the end of the standard. The new presentation format, applied from 1 December 1995, might have different page numbering. The clause numbering has not changed.

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