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## Foreword

This European Telecommunication Standard (ETS) has been prepared by the Network Aspects (NA) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS details the physical layer convergence procedure for a European Metropolitan Area Network (MAN) based on the Distributed Queue Dual Bus (DQDB) access method as defined in IEEE Standard 802.6 [6] operating at a transmission rate of 155,520 Mbit/s in accordance with CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3].

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## 1 Scope

This European Telecommunication Standard (ETS) defines the physical layer convergence procedure at 155,520 Mbit/s for use in the context of a subnetwork of a Metropolitan Area Network (MAN). Use of methods defined in this ETS for other purposes is outside the scope of this ETS.

Methods of testing will be the subject of separate arrangements.

## 2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to, or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- [1] CCITT Recommendation G.707 (1991): "Synchronous digital hierarchy bit rates".
- [2] CCITT Recommendation G.708 (1991): "Network node interface for the synchronous digital hierarchy".
- [3] CCITT Recommendation G.709 (1991): "Synchronous multiplexing structure".
- [4] CCITT Recommendation G.783 (1991): "Characteristics of synchronous digital hierarchy (SDH) multiplexing equipment functional blocks".
- [5] CCITT Recommendation I.432 (1991): "B-ISDN user-network interface - Physical layer specification".
- [6] IEEE Standard 802.6 (1990): "Distributed Queue Dual Bus (DQDB) Subnetwork of a Metropolitan Area Network (MAN)".

## 3 Definitions

For the purposes of this ETS, the definitions as defined in IEEE Standard 802.6 [6] apply.

## 4 Symbols and abbreviations

For the purposes of this ETS, the symbols and abbreviations as defined in IEEE Standard 802.6 [6] apply.

## 5 Physical Layer Convergence Procedure (PLCP) for 155,520 Mbit/s CCITT Recommendations G.707, G.708, G.709 SDH based systems

### 5.1 Introduction

This ETS defines a convergence procedure for transfer of Distributed Queue Dual Bus (DQDB) slots using the Synchronous Digital Hierarchy (SDH) at a 155,520 Mbit/s physical medium rate. The rates, formats, and other attributes of SDH are defined in CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3]. DQDB slots are mapped into VC-4 virtual containers, and the VC-4s are transported using synchronous transport modules. A mapping of Asynchronous Transfer Mode (ATM) cells into VC-4 can be found in CCITT Recommendation I.432 [5]. As ATM cells and DQDB slots are identical in length (53 octets) and nearly identical in format, the mapping of DQDB slots into VC-4 is identical to the ATM cell mapping into VC-4 except for the following:

- the use of the user channel (F2) and growth (Z3) octets for carrying DQDB layer management information octets (M1 and M2);
- the use of two bit positions in the multiframe indicator (H4) octet for providing the DQDB Link Status Signal (LSS);

- the use of VC-4 for propagating the DQDB layer 125  $\mu$ s timing along the DQDB buses;
- the optional use of either six bit positions in the multiframe indicator (H4), or the Header Check Sequence (HCS) method for providing slot boundary indication. The HCS method for slot delineation is identical to the Header Error Control (HEC) method for ATM cell delineation described in CCITT Recommendation I.432 [5], section 4.5.1.1, except for the fact that the HCS is calculated over three octets of the DQDB slot header, whereas the ATM HEC is calculated over four octets of the ATM cell header.

CCITT Recommendations G.707 [1], G.708 [2], and G.709 [3] shall be the primary references for providing an SDH based physical layer for DQDB with the above modifications. Descriptions of Path OverHead (POH) field definitions in this ETS other than (M1, M2) and H4 fields are included for clarity and completeness only.

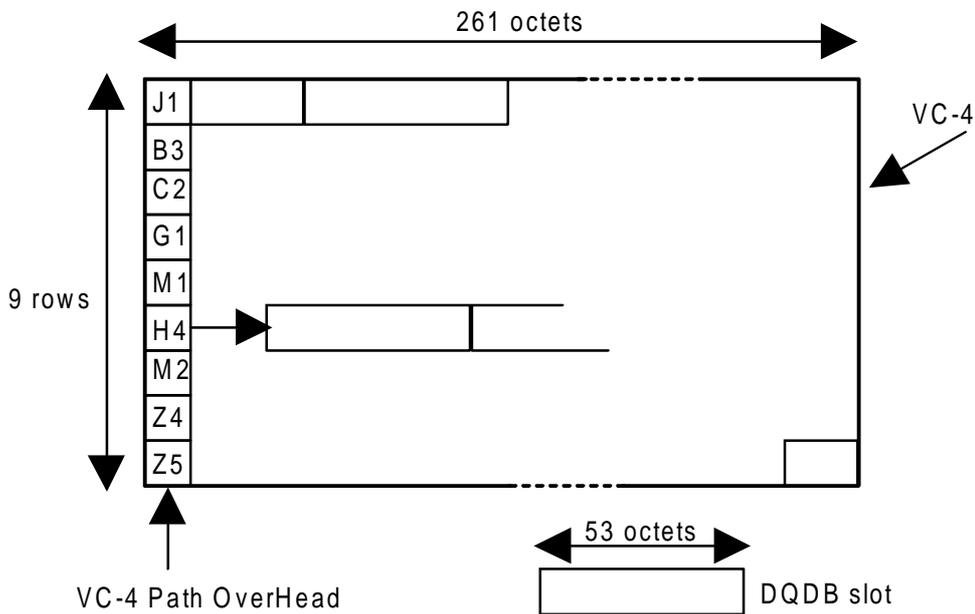
The SDH PLCP makes use of the optional status parameter in Ph-DATA indication and Ph-DATA request primitives (see IEEE Standard 802.6 [6], section 4.2). Hence, the status parameter is mandatory for the service provided by the SDH PLCP.

In this ETS , the terms bus x, bus y, Ph-SAP\_x, and Ph-SAP\_y (x = A or B; y = B or A) will be used. Bus x enters a DQDB node at Ph-SAP\_x and exits at Ph-SAP\_y whereas bus y enters a DQDB node at Ph-SAP\_y and exits at Ph-SAP\_x.

**5.2 The PLCP frame format**

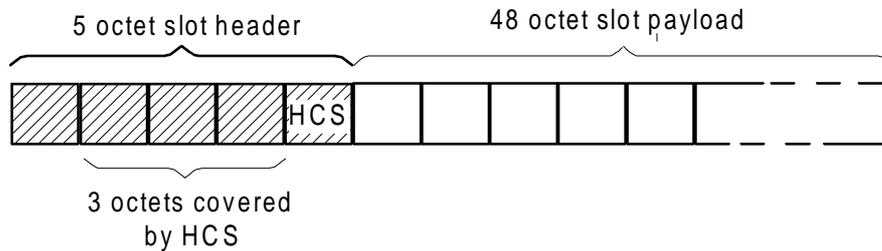
The PLCP frame format is a virtual container VC-4 that consists of 9 rows by 261 octets. The VC-4 has a nominal duration of 125  $\mu$ s. The VC-4 frame rate shall provide the 125  $\mu$ s timing information. The VC-4 frames are transported between peer PLCPs by the SDH transmission system.

DQDB slots are mapped into the VC-4 as illustrated in figure 1. The VC-4 consists of one column (nine octets) of POH plus a 9 row by 260 column payload capacity.



**Figure 1: VC-4 PLCP mapping for DQDB**

The DQDB slots are located horizontally (by row) in the VC-4 payload capacity with the slot boundaries aligned with the VC-4 octet boundaries. Because the VC-4 payload capacity (2 340 octets) is not an integer multiple of the DQDB slot length (53 octets), a slot is allowed to cross the VC-4 boundary. Slot boundary indication shall be provided on a 125  $\mu$ s basis by use of the POH H4 octet.



**Figure 2: DQDB slot format**

The slot format is illustrated in figure 2. The slot payload of 48 octets shall be scrambled before VC-4 framing. The scrambler operates for the duration of the 48 octet slot payload. Operation is suspended and the scrambler state is retained at all other times. A self-synchronous scrambler with generator polynomial  $x^{43}+1$  shall be used. In the reverse operation, following termination of the VC-4 signal and slot delineation, the slot payload shall be de-scrambled. The de-scrambler operates for the duration of the assumed slot payload according to the derived slot delineation (see subclause 5.6.1.1). Operation is suspended and the de-scrambler state is retained at all other times.

At the transmitting PLCP, an eight bit pattern shall be added (modulo 2) to the HCS field of the slot headers. At the receiving PLCP, the same bit pattern shall be subtracted (equal to add modulo 2) from the HCS field of the assumed slot headers. The bit pattern shall be (01010101).

### 5.3 PLCP path overhead field definitions

The first column of the VC-4 contains the path overhead octets. The following subclauses describe each of the VC-4 path overhead octets and their functions. As previously noted, these descriptions are consistent with CCITT Recommendation G.709 [3] except for the use of the user channel (F2), growth (Z3), and multiframe indicator (H4) octets. Values of octets are described as bit patterns. The leftmost bit of each octet is most significant.

The PLCP path is defined between two adjacent peer PLCP entities. All path overhead octets other than M1 and M2 are related to PLCP operation and are terminated/generated at each PLCP on the subnetwork. The M1 and M2 octets are provided for the transport of DQDB layer management information octets and shall not be processed by the PLCP.

#### 5.3.1 Path trace (J1)

The J1 octet is used to repetitively transmit a 64 octet, fixed length string so that a receiving PLCP can verify its continued connection to the intended transmitter PLCP.

#### 5.3.2 Bit Interleaved Parity - 8 (B3)

The B3 octet is allocated for the PLCP path error monitoring function. This function shall be a Bit Interleaved Parity-8 (BIP-8) code using even parity. The PLCP path BIP-8 is calculated over all bits of the previous VC-4. The computed BIP-8 is placed in the B3 octet of the current VC-4. The BIP-8 is calculated after the PLCP scrambling of the slot payload.

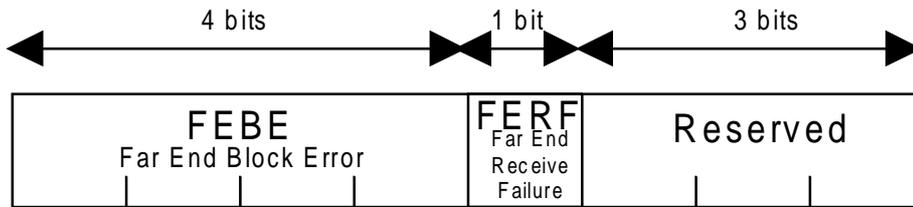
A BIP-8 is an 8 bit code in which the first bit of the BIP-8 code calculates even parity over the first bit of each octet in the VC-4, the second bit of the BIP-8 code calculates even parity over the second bit of each octet in the VC-4, etc. Therefore, the BIP-8 code provides for 8 separate even parity codes covering the corresponding bit of each octet in the VC-4.

**5.3.3 Signal label (C2)**

The C2 octet is allocated to indicate the construction of the VC-4 payload. The value of this octet shall be set to code (14 hex), which indicates an IEEE Standard 802.6 [6] payload and overhead structure.

**5.3.4 Path status (G1)**

The G1 octet is allocated to convey the received PLCP status and performance to the transmitting PLCP. This octet permits the status and performance of the complete duplex PLCP path to be monitored by either PLCP entity. The coding of the G1 octet is illustrated in figure 3.



**Figure 3: Path status (G1) coding**

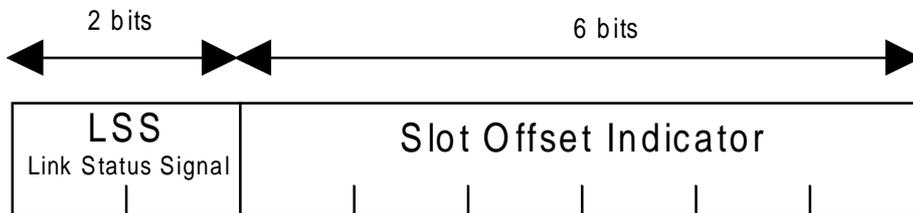
The four most significant bits of the G1 octet are the Far End Block Error (FEBE) code which shall be used to convey the count of interleaved-bit blocks that have been detected to be in error by the PLCP BIP-8 code in the preceding VC-4. This count has nine legal values, namely zero (0000) to eight (1000) errors. The remaining seven possible codes (1001 through 1111) shall be interpreted as zero errors.

The fifth bit is the Far End Receive Failure (FERF) signal. The FERF alerts the transmitting PLCP that a received failure indication has been declared along the PLCP path. When an incoming failure (i.e. the framing state machine in loss-of-frame or loss-of-slot-delineation states (see subclause 5.6.1.2) is detected on bus x (x = A or B) that persists for  $2,5 \pm 0,5$  seconds, a FERF shall be generated on bus y (y = B or A) by setting the fifth bit of the G1 octet to one (1). FERF shall be detected by a one (1) in the fifth bit of the G1 octet for ten consecutive VC-4s. When the incoming failure has ceased for  $15 \pm 5$  seconds, FERF shall be removed from bus y by setting the fifth bit of the G1 octet to zero (0). Removal of FERF shall be detected by a zero (0) in the fifth bit of the G1 octet for ten consecutive VC-4s.

The remaining three least significant bits are reserved for future standardisation. The transmitting PLCP shall encode these bits to the default code of (000). The receiver PLCP shall be capable of ignoring the values contained in these bits.

**5.3.5 Multiframe indicator (H4)**

The H4 octet is the multiframe indicator for payloads. The coding of the H4 octet is illustrated in figure 4.



**Figure 4: Multiframe indicator (H4) coding**

The two most significant bits are used for the Link Status Signal (LSS) code as described in IEEE Standard 802.6 [6], section 11.3.2. The LSS is used to communicate information about the status of the transmission link between two adjacent PLCP entities.

The LSS codes for the H4 octet are shown in table 1.

**Table 1: Link status signal codes**

LSS code	LSS name	Link status
00	Connected	Received link connected
11	rx_link_dn	Received link down, no input or forced down
01	rx_link_up	Received link up
10	hob_incapable	Lack of upstream head of bus capability.

The six least significant bits of the H4 octet form the slot offset indicator. The slot offset indicator shall contain a binary number indicating the offset in octets between the H4 octet and the first slot boundary following the H4 octet. The valid range of the slot offset indicator value shall be 0 to 52. A received value of 53 to 63 corresponds to an error condition.

### 5.3.6 DQDB layer management information octets (M1, M2)

The M1 and M2 octets carry the DQDB layer management information octets which are described in IEEE Standard 802.6 [6], section 10.1. The DQDB layer management information octets are generated at the head of a bus as described in IEEE Standard 802.6 [6], section 4.2, and are operated on by each DQDB node management protocol entity as described in IEEE Standard 802.6 [6], sections 5.4.3.3, 10.2 and 10.3. There need be no correlation between TYPE = 0 or TYPE = 1 octets and the M1 or M2 octets.

### 5.3.7 Growth octets

The Z4 and Z5 growth octets are reserved for future standardisation. The transmitter PLCP shall encode these octets to the default code of (00000000). The receiver PLCP shall be capable of ignoring the values contained in these octets.

## 5.4 PLCP behaviour during faults

There are two types of conditions that directly influence the operation of the PLCP: DQDB layer out-of-service, and faults introduced by the PLCP or the SDH transmission system. Faults shall force the PLCP out-of-frame or out-of-slot-delineation (see subclause 5.6.1.2).

The out-of-frame state is entered when a loss of pointer or alarm indication signal is declared by the SDH transmission system pointer interpretation state machine (see CCITT Recommendation G.783 [4], Annex B). The out-of-slot-delineation state is entered when lost slot synchronism is declared by the slot delineation state machine (see subclause 5.6.1.1).

When the PLCP declares a out-of-frame or out-of-slot-delineation condition, it shall start the Timer\_P\_x (x = A or B). This timer (Timer\_P\_x) shall be set to 1 ms ± 10 µs. The PLCP shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP\_x. This will lead to the transmission of void slots on bus x (see subclause 5.6.2).

If the PLCP enters the in-slot-delineation state before the timer, Timer\_P\_x, expires, the timer shall be stopped. The PLCP shall send to the DQDB layer Ph-DATA indication octets marked as VALID at Ph-SAP\_x. The PLCP shall resume its normal operation of processing and generating VC-4s, i.e. process/generate path overhead octets, perform the mapping of DQDB slots and DQDB layer management information octets into and out of the VC-4s, scramble/de-scramble slot payloads, and add/subtract the (01010101) bit pattern to/from the HCS field.

If the timer expires before the SDH transmission system pointer interpretation state machine declares normal pointer or before slot synchronism is declared by the slot delineation state machine (see subclause 5.6.1.1), then the PLCP shall enter the loss-of-frame state or loss-of-slot-delineation state respectively. The PLCP shall send to the DQDB layer a Ph-STATUS indication equal to DOWN at Ph-SAP\_x. The PLCP shall transmit on bus y (y = B or A) an LSS equal to rx\_link\_dn (see subclause 5.6.3).

If the DQDB layer is capable of becoming head of bus (i.e. HOB\_CAPABLE flag is set to YES, see IEEE Standard 802.6 [6], section 11.6.2), then when the DQDB layer receives the Ph-STATUS indication equal to DOWN at Ph-SAP\_x, the DQDB layer shall start the head of bus arbitration timer, Timer\_H\_w (w = 1 or 2), as defined in IEEE Standard 802.6 [6], section 7.1.2, and shall send the HOB subfield value of WAITING as defined in IEEE Standard 802.6 [6], section 10.2.3.4 on bus x. Thus, the PLCP shall generate EMPTY octets of type SLOT\_START, SLOT\_DATA, and DQDB\_MANAGEMENT marked as VALID at Ph-SAP\_x. Octets received at Ph-SAP\_y from the DQDB layer are transmitted on bus x.

If the DQDB layer is not capable of becoming head of bus (i.e. HOB\_CAPABLE flag is set to NO, see IEEE Standard 802.6 [6], section 11.6.2), then the PLCP shall transmit on bus x an LSS code equal to hob\_incapable irrespective of the incoming LSS code on bus y (see subclause 5.6.3).

## 5.5 PLCP behaviour during DQDB layer out of service

The physical layer subsystem of a DQDB node shall always be powered-up in normal operation. However, if for some reason the physical layer subsystem of a DQDB node is powered-down, the nodes downstream and upstream of this node can quickly detect this condition as a transmission system fault and the DQDB subnetwork would begin the fault detection process to reconfigure around the powered-down node.

The PLCP shall have the ability to by-pass the DQDB layer when the DQDB layer is out-of-service. The PLCP can use this by-pass function to isolate the DQDB node from the subnetwork when the conditions in IEEE Standard 802.6 [6], section 11.5.2 are met. When the PLCP by-passes the DQDB layer, the PLCP, as well as the SDH transmission system, shall continue normal operation (i.e. process/generate the PLCP path overhead octets etc.). The DQDB slot octets and DQDB layer management information octets (M1 and M2) shall be relayed unmodified through the PLCP. The PLCP shall assume EITHER\_BUS as the clock source request.

## 5.6 PLCP operation

### 5.6.1 Receiver operation

The PLCP has a receiver function for each bus. In the following, the bus x (x = A or B) receiver function is described.

#### 5.6.1.1 Slot delineation

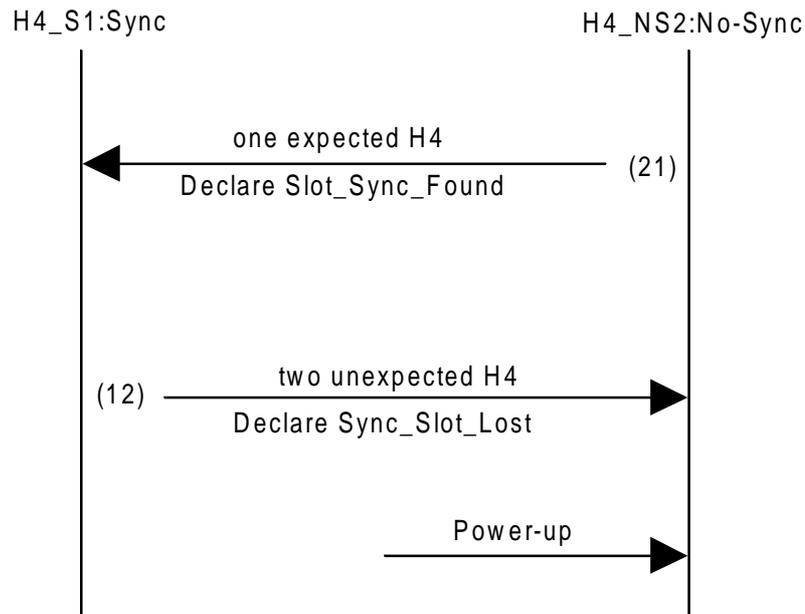
Slot delineation shall be achieved using either the H4 octet slot offset indicator method as described in subclause 5.6.1.1.1, or the HCS method as described in subclause 5.6.1.1.2.

##### 5.6.1.1.1 The H4 octet slot offset indicator method

When using the H4 octet slot offset indicator method, the H4 slot offset indicator value provides slot boundary indication (see subclause 5.3.5). As the VC-4 payload capacity (2 340 octets) is not an integer multiple of the DQDB slot length (53 octets), the received H4 slot offset indicator value in two consecutive VC-4s shall be expected to increase by 45 modulo 53. A H4 slot offset indicator value out of range shall be regarded as an unexpected slot offset indicator value.

The transition diagram for the H4 slot delineation state machine is defined in figure 5. If the H4 octet slot offset indicator method is used, then each DQDB node has two PLCP H4 slot delineation state machines, one at the receiver for each bus.

The H4 slot delineation state machine can be in one of two states: Sync (H4\_S1) and No-sync (H4\_NS2). The state machine is powered up in the No-sync (H4\_NS2) state.



**Figure 5: H4 slot delineation state machine transition diagram**

- State H4\_S1: Sync

in this state, the expected slot offset indicator value is calculated by adding 45 modulo 53 to the previously received H4 slot offset indicator value. If the received H4 slot offset indicator value matches the expected H4 slot offset indicator value, this value is used. If a VC-4 is received with an unexpected slot offset indicator value, the bus x (x = A or B) receiver function shall use the expected slot offset indicator value. If the slot offset indicator value of the next received VC-4 matches the expected slot offset indicator value calculated from either of the two previous received slot offset indicator values, this value shall be used.

- Transition 12:

if the slot offset indicator value of the received VC-4 does not match the expected slot offset indicator value calculated from either of the two previous received slot offset indicator values, the state machine shall enter the H4\_NS2 state. The H4 slot delineation state machine shall declare a Slot\_Sync\_Lost event to the framing state machine described in subclause 5.6.1.2.

- State H4\_NS2: No-Sync

in this state, the expected slot offset indicator value is calculated by adding 45 modulo 53 to the previously received H4 slot offset indicator value.

- Transition 21:

if the slot offset indicator value of the received VC-4 matches the expected slot offset indicator value calculated from the previous received slot offset indicator value, the state machine shall enter the H4\_S1 state. The H4 slot delineation state machine shall declare a Slot\_Sync\_Found event to the framing state machine described in subclause 5.6.1.2.

5.6.1.1.2 The header check sequence method

When using the HCS method, slot boundaries are derived within the VC-4 payload using the correlation between the 3 slot header octets that are protected by the HCS, and the slot header HCS octet itself (see figure 2). The HCS is a Cyclic Redundancy Check (CRC) with generating polynomial  $x^8 + x^2 + x + 1$ .

The transition diagram for the HCS slot delineation state machine is defined in figure 6. If the HCS method is used, then each DQDB node has two PLCP HCS slot delineation state machines, one at the receiver for each bus.

The HCS slot delineation state machine can be in one of three states: Sync (HCS\_S1), Presync (HCS\_P2), and Hunt (HCS\_H3). The state machine shall be powered up in the Hunt (HCS\_H3) state.

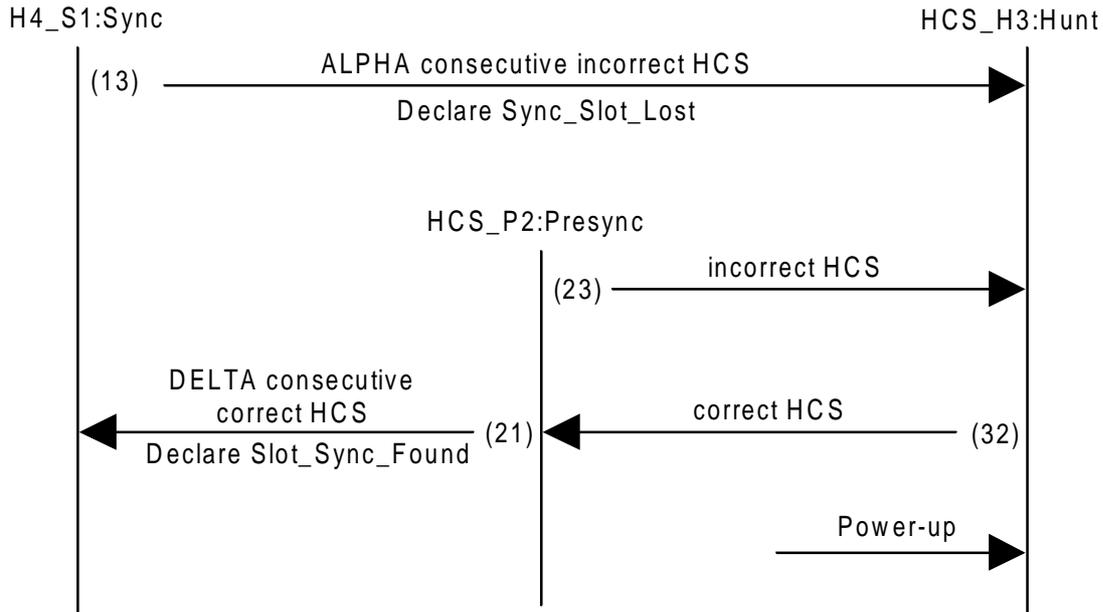


Figure 6: HCS slot delineation state machine transition diagram

Values are for ALPHA=7 and DELTA=6 in accordance with CCITT Recommendation I.432 [5], section 4.5.1.1.

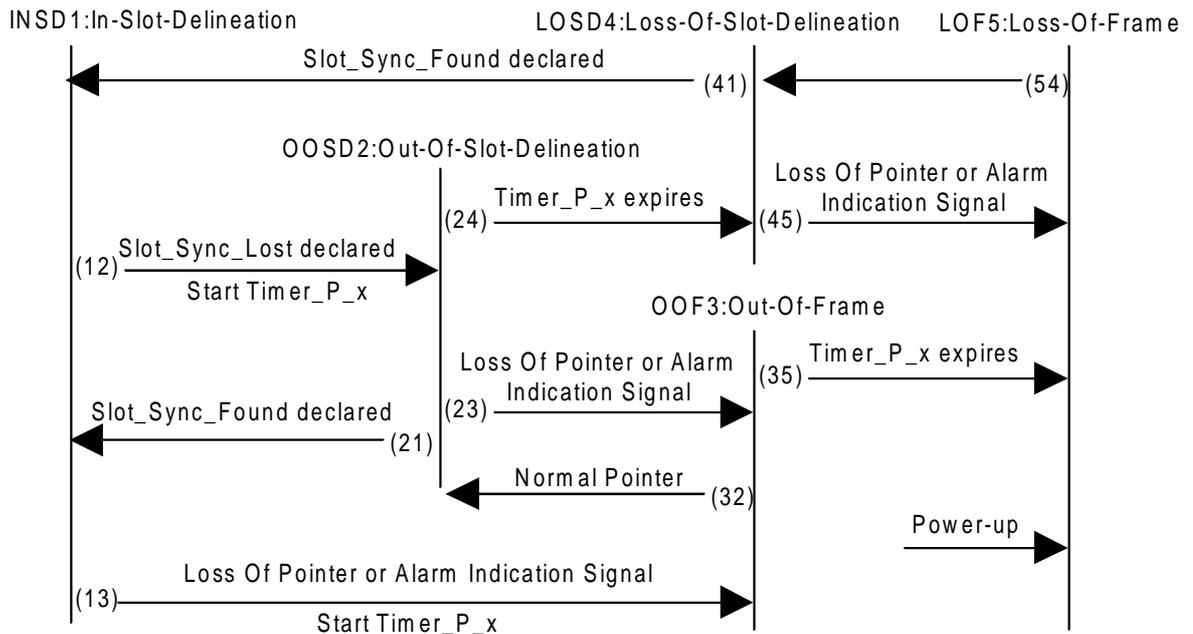
- State HCS\_S1: Sync  
 in this state, the bus x receiver function checks the HCS coding law slot by slot.
- Transition 13:  
 if the HCS coding law is recognized incorrectly ALPHA times consecutively, then the state machine shall enter the HCS\_H3 state. The state machine shall declare a Slot\_Sync\_Lost event to the framing state machine described in subclause 5.6.1.2.
- State HCS\_P2: Presync  
 in this state, the bus x receiver function checks the HCS coding law slot by slot.
- Transition 23:  
 if the HCS coding law is recognised incorrectly, then the state machine shall enter the HCS\_H3 state.

- Transition 21:  
 if the HCS coding law is recognised correctly DELTA times consecutively, then the state machine shall enter the HCS\_S1 state. The state machine shall declare a Slot\_Sync\_Found event to the framing state machine described in subclause 5.6.1.2.
- State HCS\_H3: Hunt  
 in this state, the bus x receiver function checks the HCS coding law octet by octet.
- Transition 32:  
 if the HCS coding law is recognized correctly, then the state machine shall enter the HCS\_P2 state.

**5.6.1.2 Framing state machine**

The transition diagram for the framing state machine is defined in figure 7. Each DQDB node has two framing state machines, one at the receiver for each bus. In the following, the framing state machine at the receiver for bus x (x = A or B) is described. References are made to the loss of pointer, alarm indication signal, and normal pointer states of the SDH transmission system pointer interpretation state machine (see CCITT Recommendation G.783 [4], Annex B).

The state machine may be in one of five states: In-Slot-Delineation (INSD1), Out-Of-Slot-Delineation (OOSD2), Out-Of-Frame (OOF3), Loss-Of-Slot-Delineation (LOSD4), and Loss-Of-Frame (LOF5). The state machine shall be powered up in the Loss-Of-Frame (LOF5) state.



**Figure 7: Framing state machine transition diagram**

- DState INSD1: In-Slot-Delineation  
 in this state, the bus x (x = A or B) receiver function shall process VC-4s, i.e. process path overhead octets, perform the mapping of DQDB slots and DQDB layer management information octets out of the VC-4s, subtract the (01010101) bit pattern from the HCS field of slot headers, and de-scramble slot payloads. The bus x receiver function shall send to the DQDB layer Ph-DATA indication octets of types SLOT\_START (first slot octet), SLOT\_DATA (remaining 52 slot octets), and DQDB\_MANAGEMENT (M1 and M2) marked as VALID at Ph-SAP\_x.

- Transition 12:  
  
if a Slot\_Sync\_Lost event is declared by the slot delineation machine (see subclause 5.6.1.1), then the state machine shall enter the OOSD2 state. The bus x receiver function shall start the Timer\_P\_x.
- Transition 13:  
  
if a loss of pointer or alarm indication signal is declared by the SDH transmission system, then the state machine shall enter the OOF3 state. The bus x receiver function shall start the Timer\_P\_x.
- State OOSD2: Out-Of-Slot-Delineation  
  
the bus x (x = A or B) receiver function shall send to the DQDB layer Ph-DATA indication octets marked as INVALID except for octets of type DQDB\_MANAGEMENT (M1 and M2) marked as VALID at Ph-SAP\_x. This will lead to the transmission of void slots on bus x (see subclause 5.6.2).
- Transition 21:  
  
if a Slot\_Sync\_Found event is declared by the slot delineation machine (see subclause 5.6.1.1), then the state machine shall enter the INSD1 state. The bus x receiver function shall stop and reset the timer, Timer\_P\_x.
- Transition 23:  
  
if a loss of pointer or alarm indication signal is declared by the SDH transmission system, then the state machine shall enter the OOF3 state. The timer, Timer\_P\_x, shall remain active.
- Transition 24:  
  
if the Timer\_P\_x expires, then the state machine shall enter the LOSD4 state.
- State OOF3: Out-Of-Frame  
  
the bus x receiver function shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP\_x. This will lead to the transmission of void slots on bus x (see subclause 5.6.2).
- Transition 32:  
  
if normal pointer is declared by the SDH transmission system, then the state machine shall enter the OOSD2 state. The timer, Timer\_P\_x, shall remain active.
- Transition 35:  
  
if the Timer\_P\_x expires, then the state machine shall enter the LOF5 state.
- State LOSD4: Loss-Of-Slot-Delineation  
  
when entering this state, the bus x (x = A or B) receiver function shall send to the DQDB layer a Ph-STATUS indication equal to DOWN at Ph-SAP\_x. If the HOB\_CAPABLE flag is set to YES, the bus x receiver function shall send to the DQDB layer EMPTY Ph-DATA indication octets of types SLOT\_START (first slot octet), SLOT\_DATA (remaining 52 slot octets), and DQDB\_MANAGEMENT (M1 and M2) marked as VALID at Ph-SAP\_x. If the HOB\_CAPABLE flag is set to NO, the bus x receiver function shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP\_x. This will lead to the transmission of void slots on bus x (see subclause 5.6.2). Furthermore, the PLCP shall transmit on bus x an LSS code equal to hob\_incapable irrespective of the incoming LSS code on bus y.

- Transition 41:  
  
if a Slot\_Sync\_Found event is declared by the slot delineation machine (see subclause 5.6.1.1), then the state machine shall enter the INSD1 state.
- Transition 45:  
  
if a loss of pointer or alarm indication signal is declared by the SDH transmission system, then the state machine shall enter the LOF5 state.
- State LOF5: Loss-Of-Frame  
  
when entering this state, the bus x (x = A or B) receiver function shall send to the DQDB layer a Ph-STATUS indication equal to DOWN at Ph-SAP\_x. If the HOB\_CAPABLE flag is set to YES, the bus x receiver function shall send to the DQDB layer EMPTY Ph-DATA indication octets of types SLOT\_START (first slot octet), SLOT\_DATA (remaining 52 slot octets), and DQDB\_MANAGEMENT (M1 and M2) marked as VALID at Ph-SAP\_x. If the HOB\_CAPABLE flag is set to NO, the bus x receiver function shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP\_x. This will lead to the transmission of void slots on bus x (see subclause 5.6.2). Furthermore, the PLCP shall transmit on bus x an LSS code equal to hob\_incapable irrespective of the incoming LSS code on bus y.
- Transition 54:  
  
if normal pointer is declared by the SDH transmission system, then the state machine shall enter the LOSD4 state.

### 5.6.2 Transmitter operation

The PLCP has a transmitter function for each bus. In the following, the bus x (x = A or B) transmitter function will be described.

The bus x transmitter function shall continuously generate VC-4s, i.e. generate path overhead octets, and perform the mapping of DQDB slots and DQDB layer management information octets received from Ph-SAP\_y (y = B or A) into VC-4s. The VC-4s shall be generated at the rate of the selected 125 µs timing mark (see subclause 5.6.4).

Octets received from the DQDB layer at Ph-SAP\_y of type DQDB\_MANAGEMENT shall be transmitted in the M1 and M2 path overhead octets on bus x.

Octets received from the DQDB layer at Ph-SAP\_y of type SLOT\_START (first slot octet) and SLOT\_DATA (remaining 52 slot octets) shall be transmitted on bus x. Slots shall be mapped into the VC-4 payload as described in subclause 5.2.

Continuous octets marked as INVALID or no octets received from the DQDB layer at Ph-SAP\_y shall cause void slots to be transmitted on bus x. A void slot is defined as 53 octets each with the default code of (00000000). Slots shall be mapped into the VC-4 payload as described in subclause 5.2.

The H4 slot offset indicator shall provide slot boundary information, and the PLCP shall add the (01010101) bit pattern to the HCS field and scramble slot payloads.

### 5.6.3 Link status signal operations table

The operations table for the LSS is defined in table 2. The operations table determines the status of the transmission link according to the state of the framing state machine, the incoming LSS, and the Physical Layer Connection State Machine (PLCSM) control. This table supplements IEEE Standard 802.6 [6], table 11.1. Additional states from IEEE Standard 802.6 [6], table 11.1, corresponding to rows 4 and 5, are shown shaded.

**Table 2: Link status signal operations table**

INPUT			OUTPUT	
Framing state	PLCSM control	Incoming LSS at bus x	Ph_STATUS at PH_SAP_x	Outgoing LSS at bus y
INSD1	Normal	connected	UP	Connected
INSD1	Normal	rx_link_up	UP	Connected
INSD1	Normal	rx_link_dn/ hob_incapble	DOWN	rx_link_up
<b>OOSD2/OOF3</b>	<b>Normal</b>	<b>DC</b>	<b>NO CHANGE</b>	<b>rx_link_up</b>
<b>LOSD4/LOF5</b>	<b>Normal</b>	<b>DC</b>	<b>DOWN</b>	<b>rx_link_dn</b>
DC	FORCE_DN	DC	DOWN	rx_link_dn
Key: DC = Don't Care.				

If a DQDB node with HOB\_CAPABLE flag set to NO declares a Ph-STATUS indication equal to DOWN at Ph-SAP\_x, then the PLCP shall transmit on bus x an LSS code equal to hob\_incapable irrespective of the incoming LSS code on bus y. This node adjacent to a failure would, therefore, be isolated from the DQDB subnetwork.

**5.6.4 Physical layer frame timing operations table**

The physical layer frame timing operations table shown in table 3 determines which 125 µs timing shall be used when the timing source used so far is no longer available. The 125 µs timing is dependent on three inputs:

- the state of the framing state machine at the receiver for bus A;
- the state of the framing state machine at the receiver for bus B;
- the timing source request outputs from the CC\_z operations tables in the DQDB layer, defined in IEEE Standard 802.6 [6], tables 10.10(b), 10.11 and 10.12 respectively.

This table supplements the timing source information of IEEE Standard 802.6 [6], tables 10.10(b), 10.11 and 10.12.

**Table 3: Physical layer frame timing operation table**

INPUT			OUTPUT
Ph_TIMING_SOURCE request	Receiver bus A framing state machine state	Receiver bus B framing state machine state	Timing Source
EXTERNAL_CLOCK	DC	DC	EXTERNAL_CLOCK
NODE_CLOCK	DC	DC	NODE_CLOCK
BUS_A or EITHER_BUS currently using BUS_A	INSD1/OOSD2/LOSD4	DC	BUS_A
BUS_A or EITHER_BUS currently using BUS_A	OOF3/LOF5	DC	NODE_CLOCK or EXTERNAL_CLOCK (NOTE)
BUS_B or EITHER_BUS currently using BUS_B	DC	INSD1/OOSD2/LOSD4	BUS_B
BUS_B or EITHER_BUS currently using BUS_B	DC	OOF3/LOF5	NODE_CLOCK or EXTERNAL_CLOCK (NOTE)

Key: DC = Don't Care.

NOTE: Selection between NODE\_CLOCK and EXTERNAL\_CLOCK is determined by IEEE Standard 802.6 [6], tables 10.10(b), 10.11 and 10.12.

## History

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