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Foreword

This European Telecommunication Standard (ETS) has been prepared by the Network Aspects (NA) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS details the physical layer convergence procedure for an European Metropolitan Area Network (MAN) based on the Distributed Queue Dual Bus (DQDB) access method as defined in IEEE Standard 802.6 [6] operating at a transmission rate of 34,368 Mbit/s in accordance with CCITT Recommendation G.751 [1].

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1 Scope

This European Telecommunication Standard (ETS) defines the physical layer convergence procedure at 34,368 Mbit/s for use in the context of a subnetwork of a Metropolitan Area Network (MAN). Additional slot mappings for use in the transit network and use of methods defined in this ETS for other purposes are outside the scope of this ETS.

Methods of testing will be the subject of separate arrangements.

2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed below. For dated references, subsequent amendments to, or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation G.751 (1988): "Digital multiplexing equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification".

[2] CCITT Recommendation G.703 (1991): "Physical/electrical characteristics of hierarchical digital interfaces".

[3] CCITT Recommendation G.707 (1991): "Synchronous digital hierarchy bit rates".

[4] CCITT Recommendation G.708 (1991): "Network node interface for the synchronous digital hierarchy".

[5] CCITT Recommendation G.709 (1991): "Synchronous multiplexing structure".

[6] IEEE Standard 802.6 (1990): "Distributed Queue Dual Bus (DQDB) Subnetwork of a Metropolitan Area Network (MAN)".

3 Definitions

For the purposes of this ETS, the definitions as defined in IEEE Standard 802.6 [6] shall apply.

4 Symbols and abbreviations

For the purposes of this ETS, the symbols and abbreviations as defined in IEEE Standard 802.6 [6] shall apply.

5 Physical Layer Convergence Procedure (PLCP) for E3[1) based systems

5.1 Introduction

This ETS provides a convergence procedure in which the Distributed Queue Dual Bus (DQDB) layer is mapped into a standard transmission system according to CCITT Recommendations G.751 [1] and G.703 [2] operating at 34,368 Mbit/s as used in public networks. Beyond the provisions of CCITT Recommendations G.751 [1] and G.703 [2], a 125 µs framing period shall be provided to support n x 64 kbit/s channels based on octets.

5.1.1 E3 relationship to the PLCP

The rate, format, electrical characteristics and other attributes of the E3 signal shall be as defined in CCITT Recommendations G.751 [1] and G.703 [2]. The first 2 octets of each CCITT Recommendation G.751 [1] frame shall not be used for the PLCP. They are left for E3 synchronisation (i.e. frame alignment) and overhead bits compatible with existing equipment.

> NOTE 1: Only 12 bits of the first two octets are used for the synchronisation pattern, alarm indication to the remote end (A) and national use (N). The remaining 4 bits shall be set to (1100). Thus the two octets will be (1111010000 A N 1100). The "sliding" of the two octets through the 125 µs frame shall be done via full octets.

Thus the net bit rate available to the PLCP is 34,010 Mbit/s. The nominal frame rate is 22,375 kHz.

> NOTE 2: The PLCP shall provide sufficient buffering or other provisions to accommodate the "jump" resulting from the passing of the 2 unavailable octets.

The 125 µs frame is not in any way aligned with the 44,6927 µs (22,375 kHz) frame of the transmission system. The E3 payload slots are only octet aligned to the E3 overhead octets.

[1) The designation E3 is used for a 34,368 Mbit/s transmission system according to CCITT Recommendation G.751 [1]. It is the 3rd level of the plesiochronous digital hierarchy.

5.2 The PLCP frame format

A frame duration of 125 µs is chosen to easily accommodate n x 64 kbit/s channels based on octets. 4 octets shall be added to each DQDB slot of 53 octets to provide framing and overhead functions so that each row contains 57 octets. 9 of these rows are placed into one 125 µs frame. 18 to 20 octets (nominal) shall be left as a trailer depending on whether 2 or 3 E3 overhead double octets occurred during the 125 µs frame. The complete frame structure is shown in figure 1. Each row of bits in the PLCP frame format illustrated in figure 1 shall be transmitted in order, from left to right, top to bottom.
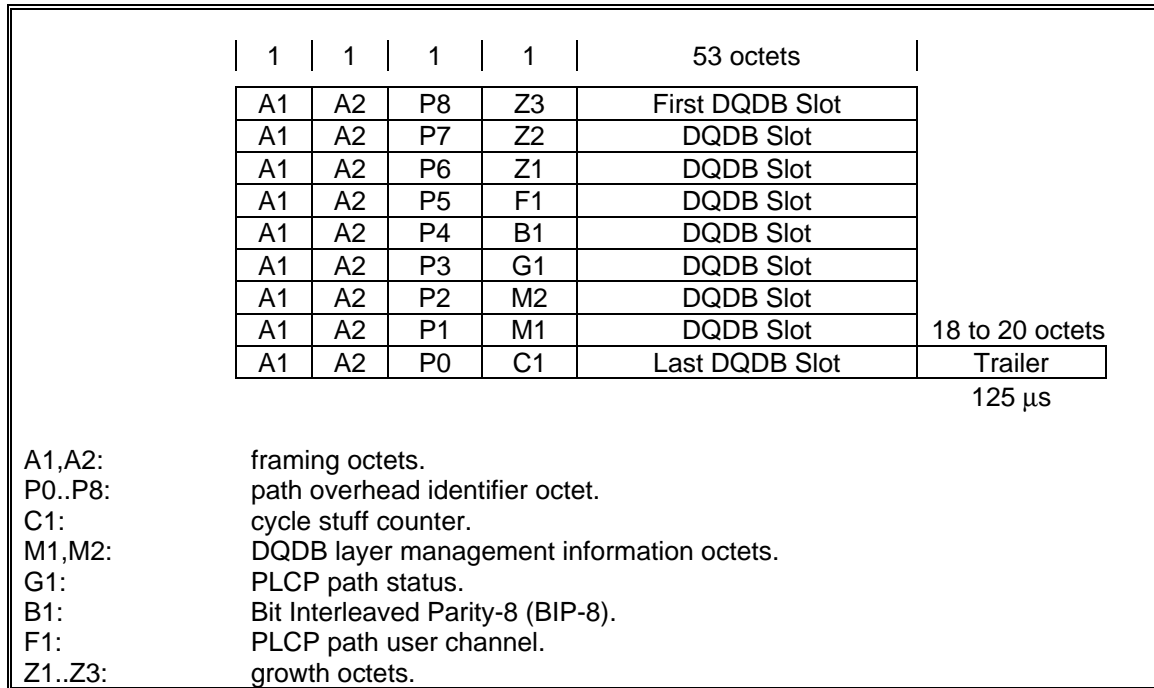
1	1	1	1	53 octets	
A1	A2	P8	Z3	First DQDB Slot	
A1	A2	P7	Z2	DQDB Slot	
A1	A2	P6	Z1	DQDB Slot	
A1	A2	P5	F1	DQDB Slot	
A1	A2	P4	B1	DQDB Slot	
A1	A2	P3	G1	DQDB Slot	
A1	A2	P2	M2	DQDB Slot	
A1	A2	P1	M1	DQDB Slot	18 to 20 octets
A1	A2	P0	C1	Last DQDB Slot	Trailer

125 µs

A1,A2:	framing octets.
P0..P8:	path overhead identifier octet.
C1:	cycle stuff counter.
M1,M2:	DQDB layer management information octets.
G1:	PLCP path status.
B1:	Bit Interleaved Parity-8 (BIP-8).
F1:	PLCP path user channel.
Z1..Z3:	growth octets.

Figure 1: PLCP frame format

5.3 PLCP field definitions

(Refer to figure 1). The values of fields are described as bit patterns. The leftmost bit of each octet is the most significant.

5.3.1 Framing octets (A1, A2)

The first two columns (A1, A2) may be used to provide slot delineation. The encoding of the A1 and A2 octets is:

A1	A2
11110110	00101000

These codes are the same patterns as used in the Synchronous Digital Hierarchy (SDH) (CCITT Recommendations G.707 [3], G.708 [4] and G.709 [5]. Alternatively, slot delineation based on the Header Check Sequence (HCS) of the DQDB header may be used.

5.3.2 Path overhead identifier (P0..P8)

The third column identifies the PLCP overhead octets contained in the fourth column of figure 1. The leftmost 6 bits of these octets provide numbering of the 9 rows. The 7th bit is reserved and the rightmost bit, Least Significant Bit (LSB), is a parity bit. The reserved bit shall be set to (0). The parity bit provides odd parity over this field.

Table 1 defines the codes P0..P8, which shall be generated by the PLCP at each node. All other codes shall be invalid. A code shall also be considered invalid if the parity bit contained in the LSB is not correct. The response to invalid codes is described in subclause 5.6.

Table 1: Path overhead identifier codes

P8	001 000	0	0
P7	000 111	0	0
P6	000 110	0	1
P5	000 101	0	1
P4	000 100	0	0
P3	000 011	0	1
P2	000 010	0	0
P1	000 001	0	0
P0	000 000	0	1

5.3.3 PLCP path overhead octets

The PLCP path is defined between two adjacent peer PLCP entities. The F1, B1, G1 and C1 PLCP path overhead octets are related to PLCP operation and shall be terminated/generated at each PLCP on the subnetwork. The M1 and M2 octets are provided for the transport of DQDB layer management information octets and shall not be processed by the PLCP sublayer.

5.3.3.1 PLCP path user channel (F1)

The F1 octet is the user channel, which is allocated for user communication purposes between adjacent PLCPs. The use of this octet in DQDB subnetworks is for further study. The default code for this octet shall be (00000000).

5.3.3.2 Bit interleaved parity - 8 (B1)

One octet is allocated for PLCP path error monitoring. This function shall be a Bit Interleaved Parity - 8 (BIP-8) code using even parity. The PLCP path BIP-8 is calculated over the 9 x 54 octet structure (columns 4 to 57, 1 PLCP path overhead octet and 53 DQDB slot octets per row) of the previous PLCP frame and inserted into the B1 octet of the current PLCP frame.

A BIP-8 is an 8 bit code in which the first bit represents even parity calculated over the first bit of each octet in the 9 x 54 octet structure, the second bit represents even parity over the second bit of each octet in the 9 x 54 octet structure, etc. Therefore the BIP-8 code provides for 8 separate even parity codes covering the corresponding bit of each octet in the 9 x 54 octet structure.

5.3.3.3 PLCP path status (G1)

The G1 octet is allocated to convey the received PLCP status and performance back to the transmitting PLCP. This octet permits the status of the full duplex PLCP path to be monitored at either PLCP entity. The G1 octet shall consist of:

- 4 bits for the Far End Block Error (FEBE) code;

- 1 bit for the Alarm Signal (AS);

- 3 bits for a Link Status Signal (LSS).

This is illustrated in figure 2.

FEBE (4)	AS (1)	LSS (3)
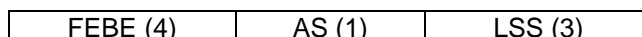
Figure 2: PLCP path status (G1)

The first four bits of the G1 octet are the FEBE code which may be used to convey the count of interleaved-bit blocks that have been detected to be in error by the BIP-8 code in the preceding frame. If implemented, this count shall have nine legal codes, namely zero (0000) to eight (1000) errors. If not implemented, the code shall be (1111). The remaining six possible codes (1001 through 1110) would have been the result of an error condition and shall be interpreted as zero errors.

The fifth bit may be used for the AS. The AS alerts the transmitting PLCP that a received failure indication has been declared along the PLCP path. When an incoming failure (i.e. PLCP LOF) is detected on bus x (x = A or B) that persists for 2,5 ± 0,5 s, an AS shall be generated on bus y (y = B or A) by setting the fifth bit of the G1 octet to one (1). The AS shall be detected by a one (1) in the fifth bit of the G1 octet for ten consecutive frames. When the incoming failure has ceased for 15 ± 5 s, the AS shall be removed from bus y by setting the fifth bit of the G1 octet to zero (0). Removal of the AS shall be detected by a zero (0) in the fifth bit of the G1 octet for ten consecutive frames. If the AS is not implemented, the default code shall be (0).

The remaining three bits shall be used for the LSS as described in IEEE Standard 802.6 [6], section 11.3.2. The LSS is used to communicate information about the status of the transmission link between two adjacent PLCP entities. This information is conveyed only between these two entities.

The LSS codes for the G1 octet are shown in table 2. All other codes shall be invalid and shall be ignored by the receiver.

Table 2: Link status signal codes

LSS code	LSS name	Link status
000	Connected	Received link connected
011	rx_link_dn	Received link down, no input or forced down
110	rx_link_up	Received link up

5.3.3.4   DQDB layer management information octets (M1, M2)

The octets M1 and M2 carry the DQDB layer management information octets which are described in IEEE Standard 802.6 [6], section 10.1. The layer management octets shall be generated at the head of bus as described in IEEE Standard 802.6 [6], section 4.2 and shall be operated on by the DQDB layer management protocol entity as described in IEEE Standard 802.6 [6], secttions 5.4.3.3, 10.2 and 10.3. There need be no correlation between type = 0 or 1 octets and the M1 and M2 octets.

5.3.3.5   Stuffing (octet C1)

The C1 octet shall provide a generalised stuffing indicator for the PLCP frames. The C1 octet indicates the PLCP frame in which an octet stuffing shall occur and contains the number of trailer octets transmitted (17 to 21). Each PLCP entity on the subnetwork shall be frame cycle aligned (i.e. the phase of the incoming frame in the cycle shall be the same as the phase of the outgoing frame in the cycle).

The external timing source shall octet stuff, given the opportunity to stuff in order to provide for a nominal 125 µs time period by adding/deleting one (1) trailer octet. When the HOB is using its own local clock generator to generate the timing information, no stuffing shall be used. The allowed C1 codes shall be:

17:	001 1101 1
18:	010 0111 1
19:	011 1010 1
20:	100 1110 1
21:	101 0011 1

The C1 codes above provide error correction capability for 1 bit error and 2 adjacent bit errors and error detection capability for 3 random bit errors using the Abramson code:

$$(x^3 + x + 1)(x + 1)$$

The leftmost 3 bits contain the numbering, the middle 4 bits provide the protection code and the rightmost bit is not used in the coding process.

    NOTE: C1 evaluation shall always use the error correction mode.

5.3.3.6   Growth octets (Z1..Z3)

The octets Z1..Z3 are reserved for future standardisation. The PLCP shall encode these octets to the default code of (00000000).

5.3.4   Trailer octets

Each of the 17 to 21 trailer octets shall be encoded as (11001100).

5.4   PLCP behaviour during faults

There are three types of conditions that directly influence the operation of the PLCP; transmission system faults, PLCP faults, and DQDB layer out-of-service. The PLCP shall not differentiate between transmission system faults and PLCP faults. Therefore all transmission system faults shall force the PLCP out-of-frame.

When the PLCP declares a PLCP out-of-frame condition (see subclause 5.5), it shall start the Timer_P_x (x = A or B). This timer (Timer_P_x) shall be set to 1 ms ± 10 µs. The PLCP shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP_x. The PLCP shall generate a jam signal on bus x. The jam signal is defined as an unframed continuous bit pattern contained within the framed E3 information payload. The bit pattern shall be a repeating (1100) sequence (starting with a one-one (11) after each E3 synchronisation double octet for the E3 application).

>   NOTE: The jam signal is not needed in point-to-point configurations. It shall however be generated in any configuration.

If the PLCP detects the jam signal for at least 20 µs, the PLCP shall reset and start the Timer_P_x. The PLCP shall continue to send the jam signal on bus x and shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP_x.

If the PLCP enters the in-frame state before the timer, Timer_P_x, expires, the timer shall be stopped. The PLCP shall send Ph-DATA indication octets marked as VALID at Ph-SAP_x. The PLCP shall resume its normal operation of processing/generating PLCP framing and PLCP path overhead octets and of performing its local stuffing.

If the timer expires before the detection of valid PLCP framing octets, the PLCP sublayer shall enter the loss-of-frame state and shall send to the DQDB Layer a Ph-STATUS indication equal to DOWN at Ph-SAP_x. The PLCP shall transmit on bus y (y = B or A) an LSS equal to rx_link_dn.

If the DQDB layer is capable of becoming HOB (i.e. the HOB_CAPABLE flag is set to 1), then when the DQDB layer receives the Ph-STATUS indication equal to DOWN at the Ph-SAP_x, the DQDB layer shall start the HEAD of bus arbitration timer, Timer_H_w (w = 1 or 2), as defined in IEEE Standard 802.6 [6], section 7.1.2, and shall send the HOB subfield value of WAITING as defined in IEEE Standard 802.6 [6], section 10.2.3.4 on bus x. Thus, the PLCP shall generate a valid PLCP frame with the appropriate PLCP framing octets and PLCP path overhead octets and shall perform the cycle/stuffing mechanism.

If the DQDB layer is not capable of becoming HOB (i.e. the HOB_CAPABLE flag is set to 0), the PLCP layer shall continue to generate the jam signal on bus x.

5.5   PLCP behaviour during DQDB layer out of service

The physical layer subsystem of a DQDB node connected to an E3-based transmission system shall always be powered-up in normal operation. However, if for some reason the physical layer subsystem of a DQDB node is powered-down, the stations downstream and upstream of this node can quickly detect this condition as a transmission system fault and the DQDB subnetwork would begin the fault detection process, as defined in subclause 5.4, to reconfigure around the powered-down node.

The DQDB layer shall have the ability of going in and out-of-service without interrupting the operation of the physical layer. When the DQDB layer goes out-of-service the PLCP, as well as transmission system, shall continue normal operation (i.e. perform the stuffing mechanism and process/generate the PLCP path overhead octets). The DQDB layer management octets (M1 and M2) shall be relayed unmodified through the PLCP.

5.6 PLCP framing

The transition diagram for PLCP framing state machine is defined in figure 3. Each DQDB node has two PLCP framing state machines, one at the receiver for each bus.

- PLCP framing transition diagram:

  the state machine can be in one of four states: In-Frame (INF3), Out-Of-Frame (OOF1a), Out-Of-Frame_Jam (OOF_J1b), and Loss-Of-Frame (LOF2). The state machine shall be powered up in the Loss-Of-Frame (LOF2) state.
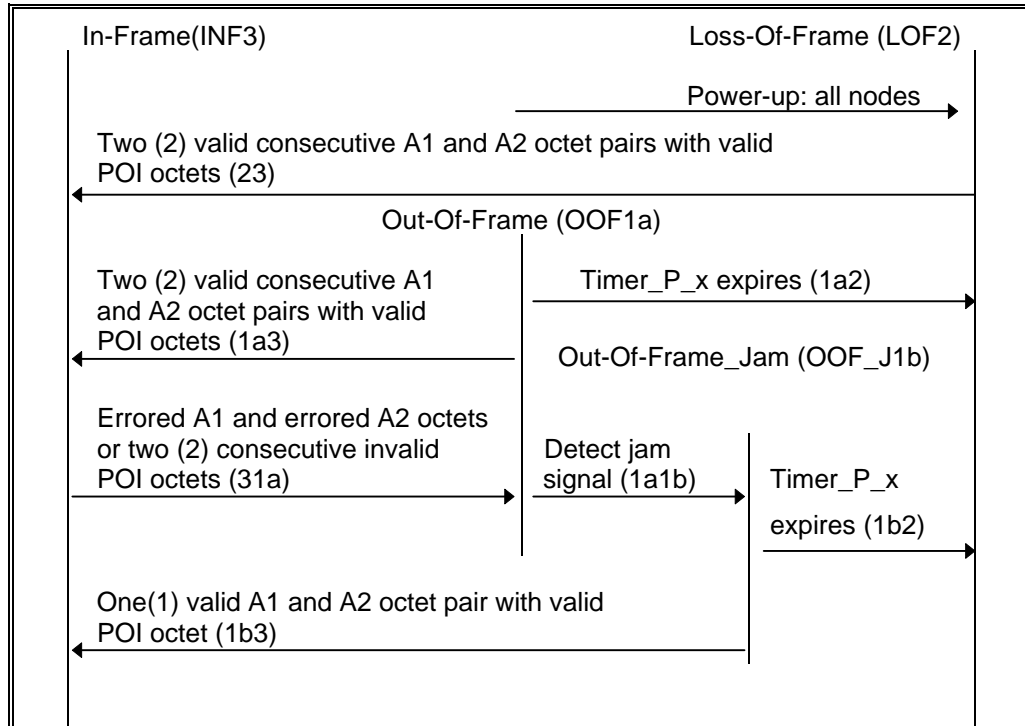

Figure 3: PLCP framing state machine transition diagram

- State OOF1a: Out-Of-Frame

  when entering this state, the PLCP out-of-frame timer, Timer_P_x, shall be started, and the PLCP shall start generating the jam signal on bus x. However, if the node contains an HOB_OPERATION value of HEAD_OF_BUS_x, the PLCP shall continue to generate a framed PLCP signal on bus x. The PLCP shall remain in this state until the Timer_P_x expires or until valid framing is found. The PLCP shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP_x.

- Transition 1a3:

  if the PLCP detects two consecutive valid A1 and A2 octet pairs with two consecutive valid and sequential Path Overhead Identifier (POI) octets, then the state machine shall enter the INF3 state. The PLCP shall stop and reset the timer, Timer_P_x.

- Transition 1a2:

  if the Timer_P_x expires, then the state machine shall enter the LOF2 state.

- Transition 1a1b:

  if the PLCP detects a jam signal for at least 20 μs, then the state machine shall enter the OOF_J1b state. The PLCP shall reset and start the timer, Timer_P_x.

- State OOF_J1b: Out-Of-Frame_Jam

  the PLCP shall remain in this state until the Timer_P_x expires or until valid framing is found. The PLCP shall send to the DQDB layer Ph-DATA indication octets marked as INVALID at Ph-SAP_x. The PLCP shall continue to generate the jam signal. However, if the node contains an HOB_OPERATION value of HEAD_OF_BUS_x, then the PLCP shall continue to generate a framed PLCP signal.

- Transition 1b2:

  if the Timer_P_x expires, then the state machine shall enter the LOF2 state.

- Transition 1b3:

  if the PLCP detects one valid A1 and A2 octet pair with a valid POI octet, then the state machine shall enter the INF3 state.
  The PLCP shall stop and reset the timer, Timer_P_x.

- State LOF2: Loss-Of-Frame

  when entering this state, the PLCP shall transmit on bus y an LSS equal to rx_link_dn and shall send to the DQDB layer a Ph-STATUS indication equal to DOWN at Ph-SAP_x. If the HOB_CAPABLE flag is set to 1, the PLCP shall generate a framed PLCP signal on bus x starting with an A1 and A2 framing pattern sequence. If the HOB_CAPABLE flag is set to 0, the PLCP shall generate the jam signal on bus x. The PLCP shall remain in this state until valid PLCP framing is found.

- Transition 23:

  if the PLCP detects two consecutive valid A1 and A2 octet pairs with two consecutive valid and sequential POI octets, then the state machine shall enter the INF3 state. The PLCP shall send to the DQDB Layer a Ph-STATUS indication equal to UP at Ph-SAP_x.

- State INF3: In-Frame

  the PLCP shall process/generate PLCP framing octets, POI octets, and PLCP Path Overhead octets as in normal operations and shall perform the stuffing mechanism. When the PLCP enters this state, it shall always begin transmission of the PLCP frame on bus x with an A1 and A2 framing pattern sequence, and the PLCP shall send to the DQDB layer Ph-DATA indications of type DQDB_MANAGEMENT (M2 and M1 octets) marked as INVALID at Ph-SAP_x until the PLCP detects the P8 octet. After the PLCP has detected the P8 octet, the PLCP shall send to the DQDB layer Ph-DATA indications of type DQDB_MANAGEMENT marked as VALID at Ph-SAP_x. The PLCP shall remain in this state until errored A1 and errored A2 octets or two consecutive invalid or nonsequential POI octets are detected.

- Transition 31a:

  if the PLCP detects one or more errors in the A1 octet and one or more errors in the A2 octet of an A1 and A2 octet framing pair or two consecutive invalid or nonsequential POI octets, then the state machine shall enter the OOF1a state. The PLCP shall start the Timer_P_x.

5.6.1 Link status signal operations table

The operations table for the LSS is defined in table 3. The operations table determines the status of the transmission link according to the state of the PLCP framing state machine, the incoming LSS, and the Physical Layer Connection State Machine (PLCSM) control. This table supplements IEEE Standard 802.6 [6], table 11.1. Additional states from IEEE Standard 802.6 [6], table 11.1, corresponding to rows 4 to 6, are shown shaded.

Table 3: Link status signal operations table

INPUT				OUTPUT	
PLCP frame	PLCSM	Incoming	Detect	Ph-	Outgoing
state	control	LSS	jam	Status	LSS
INF3	Normal	connected	DC	UP	connected
INF3	Normal	rx_link_up	DC	UP	connected
INF3	Normal	rx_link_dn	DC	DOWN	rx_link_up
OOF1a/ OOF_J1b	**Normal**	**DC**	**DC**	**NO CHANGE**	**rx_link_up**
LOF2	**Normal**	**DC**	**NO**	**DOWN**	**rx_link_dn**
LOF2	**Normal**	**DC**	**YES**	**DOWN**	**rx_link_up**
DC	FORCE_DN	DC	DC	DOWN	rx_link_dn
Key: DC = Don't Care.					

If a DQDB node with HOB_CAPABLE flag set to zero receives an LSS code equal to rx_link_dn on bus x, then the PLCP shall transmit on bus x an LSS code equal to rx_link_dn irrespective of the incoming LSS code on bus y. This node adjacent to a failure would, therefore, be isolated from the DQDB subnetwork.

5.6.2 Physical layer frame timing operations table

The physical layer frame timing operations table shown in table 4 determines whether unframed jam or a framed PLCP signal will be transmitted on the outgoing bus and what frame timing is used to generate the outgoing framed PLCP signal. The transmission on the outgoing bus is dependent on the PLCP framing state machine states of both incoming buses, the HOB_CAPABLE flag, and the frame timing source and HOB_OPERATION_ outputs from the CC_x operations tables in the DQDB layer. This table supplements the timing source information of IEEE Standard 802.6 [6], tables 10.10(b), 10.11, and 10.12.

Table 4: Physical layer frame timing operations supplementary table

INPUT			OUTPUT	
Bus x PLCP frame state	HOB_ OPERATION_z (NOTE 2)	HOB_CAP flag	Bus x Tx frame	125 μs timing
OOF1a/OOF_J1b	not HOB_x	DC	Jam	N/A
OOF1a/OOF_J1b	HOB_x	YES	PLCP signal	NODE_CLOCK or EXT_CLOCK (NOTE 1)
LOF2	not HOB_x	NO	Jam	N/A
LOF2	DC	YES	PLCP signal	NODE_CLOCK or EXT_CLOCK (NOTE 1)

Key:

      DC   = Don't Care.
      N/A   = Not Applicable.

NOTE 1:   Selection between NODE_CLOCK and EXT_CLOCK is determined by IEEE Standard 802.6 [6], tables 10.10(b), 10.11 and 10.12 when the bus x PLCP frame state is OOF1a, OOF_J1b or LOF2.

NOTE 2:   The HOB_OPERATION_z column refers to the value of the HOB_OPERATION for the CC_z associated with Ph-SAP_x at the node.

History

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