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**Transmission and Multiplexing (TM);
Physical and electrical characteristics of hierarchical digital
interfaces for equipment using the 2 048 kbit/s -
based plesiochronous or synchronous digital hierarchies**

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Foreword

This European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS specifies the physical and electrical characteristics of hierarchical interfaces based on CCITT Recommendation G.703 [2] but it does not intend to preclude the use of interfaces covered in other standards.

The aim of this ETS is to provide inter-vendor and inter-operator compatibility.

The conformance testing requirements corresponding to the specifications contained in this ETS are to be specified in a different ETS.

Physical parameters for optical interfaces for the Synchronous Digital Hierarchy (SDH) are to be specified in a different standard which is under development.

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1 Scope

This ETS describes the requirements for the physical and electrical parameters of interfaces based on CCITT Recommendations G.702 [1], G.703 [2] and G.707 [3] for interconnection of digital network elements:

- in-station (i.e. for distances below a few hundred metres);
- using metallic (symmetrical or coaxial) pairs;
- at 64, 2 048, 8 448, 34 368 and 139 264 kbit/s hierarchical levels of the Plesiochronous Digital Hierarchy (PDH) and at the first level of the Synchronous Digital Hierarchy (SDH) (STM-1 at 155 520 kbit/s).

This ETS also describes the requirements for the physical and electrical parameters of the 2 048 kHz synchronisation interface.

2 Normative references

This ETS incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- [1] CCITT Recommendation G.702 (1990): "Digital hierarchy bit rates".
- [2] CCITT Recommendation G.703 (1991): "Physical/electrical characteristics of hierarchical digital interfaces".
- [3] CCITT Recommendation G.707 (1991): "Synchronous digital hierarchy bit rates".
- [4] CCITT Recommendation I.431 (1988): "Primary rate user/network interface - Layer 1 specification".
- [5] CCITT Recommendation O.9 (1988): "Measuring arrangements to assess the degree of unbalance about earth".
- [6] CCITT Recommendation G.704 (1991): "Synchronous frame structures used at primary and secondary hierarchical levels".

3 Definitions

For the purposes of this ETS, there are no terms needing a specific definition.

4 Symbols and abbreviations

For the purposes of this ETS, the following abbreviations apply:

PDH	Plesiochronous Digital Hierarchy
PRBS	Pseudo-Random Binary Sequence
SDH	Synchronous Digital Hierarchy

5 Requirements

As CCITT Recommendation G. 703 [2] was written as a recommendation, for the purpose of compliance with this ETS the statements given in table 1 provide an indication of the status of the requirements (i.e. normative, informative or not relevant).

Definitions:

N = normative: requirements with which it is necessary to comply in order to be able to claim compliance with this ETS. Therefore, functions and features in Clauses/subclauses of CCITT Recommendation G. 703 [2], stated as being normative in this ETS, shall be implemented and followed even if the text is given as a recommendation or an example.

I = informative: the text of this Clause/subclause is provided for information only. Titles for Clauses and subclauses are marked as informative when the requirements are given in further subclauses.

N/R = not relevant: this Clause/subclause is not relevant to this ETS.

Table 1: Modifications and statements to CCITT Recommendation G.703 [2]

Clause/subclause	Title	Statement
1	Interface at 64 kbit/s	I
1.1	Functional requirements	I
1.1.1	The following basic requirements for the design of the interface are recommended	I
1.1.2	In both directions of transmission three signals can be carried across the interface	N
1.1.3	Bit sequence independence	N
1.1.4	Three types of envisaged interfaces	I
1.1.4.1	Co-directional interface	N
1.1.4.2	Centralised clock interface	N/R
1.1.4.3	Contra directional interface	N/R
1.2	Electrical characteristics	I
1.2.1	Electrical characteristics of 64 kbit/s co-directional interface	N
Tolerable longitudinal voltage shall be according to subclause 5.1 of this ETS.		
Output signal balance shall be according to subclause 5.2 of this ETS.		
Output return loss shall be according to subclause 5.3 of this ETS.		
1.2.2	Electrical characteristics of 64 kbit/s centralised clock interface	N/R
Continued		

Table 1 (continued): Modifications and statements to CCITT Recommendation G.703 [2]

Clause/subclause	Title	Statement
1.2.3	Electrical characteristics of 64 kbit/s contra directional interface	N/R
2	Interface at 1 544 kbit/s	N/R
3	Interface at 6 312 kbit/s	N/R
4	Interface at 32 064 kbit/s	N/R
5	Interface at 44 736 kbit/s	N/R
6	Interface at 2 048 kbit/s	N
For symmetric interfaces: Tolerable longitudinal voltage shall be according to subclause 5.1 of this ETS.		
For symmetric interfaces: Output signal balance shall be according to subclause 5.2 of this ETS.		
Output return loss shall be according to subclause 5.3 of this ETS.		
NOTE 1: For signals with bit rates of $n \times 64$ kbit/s ($n = 2$ to 31) which are routed through multiplexing equipment specified for the 2 048 kbit/s based hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2 048 kbit/s interface.		
NOTE 2: The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to signal ground both at the input port and at the output port.		
7	Interface at 8 448 kbit/s	N
The output return loss requirement according to subclause 5.3 of this ETS shall be fulfilled.		
NOTE 3: The outer conductor of the coaxial pair shall be connected to signal ground both at the input port and at the output port.		
8	Interface at 34 368 kbit/s	N
The output return loss requirement according to subclause 5.3 of this ETS shall be fulfilled.		
NOTE 4: The outer conductor of the coaxial pair shall be connected to signal ground both at the input port and at the output port.		
9	Interface at 139 264 kbit/s	N
NOTE 5: The outer conductor of the coaxial pair shall be connected to signal ground both at the input port and at the output port.		
10	2 048 kbit/s synchronisation interface	N
NOTE 6: The outer conductor of the coaxial pair shall be connected to signal ground both at the input port and at the output port.		
Continued		

Table 1 (concluded): Modifications and statements to CCITT Recommendation G.703 [2]

Clause/subclause	Title	Statement
11	Interface at 97 728 kbit/s	N/R
12	Interface at 155 520 kbit/s	I
12.1	General characteristics	N
12.2	Specifications at the output ports	N
12.3	Specifications at the input ports	N
12.4	Specifications at the cross-connect points	N/R
12.5	Earthing the outer conductor or screen	N
NOTE 7:	The outer conductor of the coaxial pair shall be connected to signal ground both at the input port and at the output port.	
Annex A	Definition of codes	N
Annex B	Specification of over voltage protection requirements	N

5.1 Tolerable longitudinal voltage

For minimum tolerance to longitudinal voltage at input ports the receiver shall operate without errors with any valid input signal in the presence of a longitudinal voltage V_1 .

$V_1 = 2 V_{rms}$ over the frequency range 10 Hz to 30 MHz.

The test configuration is given in CCITT Recommendation I.431 [4], figure 9/I.431.

5.2 Output signal balance

Output signal balance, which is measured in accordance with CCITT Recommendation O.9 [5], § 2.7, shall meet the following requirements:

- a) at $f_b/2$: ≥ 40 dB;
- b) $f_b/2$ to 30 MHz: minimum value decreasing from 40 dB with a slope of 20 dB/decade,

where $f_b =$ 256 kHz for 64 kbit/s co-directional interfaces;

2 048 kHz for 2 048 kbit/s interfaces.

5.3 Minimum output return loss

The return loss at the output shall have the following minimum values:

Frequency range	Return loss
0,025 fb to 0,05 fb	6 dB
0,05 fb to 1,5 fb	8 dB

where fb = 256 kHz for 64 kbit/s co-directional interfaces;

2 048 kHz for 2 048 kbit/s interfaces;

8 448 kHz for 8 448 kbit/s interfaces;

34 368 kHz for 34 368 kbit/s interfaces.

The output return loss should be measured under dynamic conditions with PRBS 2¹⁵-1 transmitted at the output. For equipment which does not generate a CCITT Recommendation G.704 [6] framed signal, the PRBS shall be transmitted in the whole bit stream. For equipment which does generate a CCITT Recommendation G.704 [6] frame, the PRBS shall be transmitted in every traffic channel. The power transmitted into the output of the device under test by the measurement equipment should be less than -10 dBm₀. The return loss can be measured with a selective bandwidth analyser with the bandwidth set to 1 kHz or less.

NOTE: The CCITT Recommendation G.703 [2] interfaces to existing equipment or being under development may not comply with this output return loss requirement.

History

Document history	
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