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Foreword

This draft second edition European Telecommunication Standard (ETS) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI), and is now submitted for the Public Enquiry phase of the ETSI standards approval procedure.

This ETS concerns the basic User Network Interface (UNI) for the Integrated Services Digital Network (ISDN) and consists of 7 parts as follows:

Part 1: "Layer 1 specification";

Part 2: "Implementation Conformance Statement (ICS) and Implementation Extra Information for Testing (IXIT) for interface I_A";

Part 3: "Implementation Conformance Statement (ICS) and Implementation Extra Information for Testing (IXIT) for interface I_B";

Part 4: "Conformance test specification for interface I_A";

Part 5: "Conformance test specification for interface I_B";

Part 6: "Abstract Test Suite (ATS) specification for interface I_A";

Part 7: "Abstract Test Suite (ATS) specification for interface I_B".

and is based on ITU-T Recommendation I.430 [10].

Proposed transposition dates	
Date of latest announcement of this ETS (doa):	3 months after ETSI publication
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa

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1 Scope

This part 1 of ETS 300 012 specifies requirements for the ISDN basic rate UNI including the physical, electrical and functional characteristics and the information exchange with higher layers. This ensures that interface implementations in an ISDN equipment for use with ISDN basic access is portable within Europe with regard to layer 1 interface aspects and that interworking with higher layer protocols for ISDN is supported.

This ETS is applicable to equipment having interface I_A or I_B for the connection to the ISDN basic access intended to be installed on customer premises according to ITU-T Recommendation I.411 [1], this ETS is for application to interfaces at reference points S, T and S/T (coincident S and T) of the ISDN reference configuration.

For the case where this ETS is applied to the T and the S/T reference point, the main body of this part 1 of the ETS and the parts 6 and 7 are normative.

For the case where this ETS is applied to the S reference point, annex A to this part 1 of the standard is also normative.

This ETS does not specify:

- safety requirements;
- interface or equipment overvoltage protection requirements;
- immunity requirements against electromagnetic interferences;
- emission limitation requirements.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] ITU-T Recommendation I.411 (1993): "ISDN user-network interfaces - reference configurations".

[2] CCITT Recommendation I.412 (1988): "ISDN user-network interfaces - interface structures and access capabilities".

[3] CCITT Recommendation X.211 (1988): "Physical service definition of open systems interconnection for CCITT applications".

[4] EN 28877 (1993): "Information technology - Telecommunications and information exchange between systems - Interface connector and contact assignment for ISDN Basic Access Interface located at reference points S and T (ISO/IEC 8877:1992)"

[5] EN 60603-7 (1993): "Connectors for frequencies below 3 MHz for use with printed boards - Part 7: Detail specification for connectors, 8-way, including fixed and free connectors with common mating features; (IEC 603-7:1990)".

[6] ETS 300 047-3 (1992): "Integrated Services Digital Network (ISDN); Basic access - safety and protection; Part 3: Interface I_A - protection".

[7] ENV 41004: "Reference Configuration for Calls, based on ISDN Connection Types, as provided by Private Telecommunication Network Exchange".

[8] ISO/IEC 9646-1 (1994): Information technology - Open Systems Interconnection - Conformance Testing Methodology and Framework - Part 1: General concepts".

[9] CCITT Recommendation G.117 (1988): "Transmission aspects of unbalance about earth (definitions and methods)".

[10] ITU-T Recommendation I.430 (1995): "Basic user-network interface - layer 1 specification".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this ETS, the following definitions apply:

3.1.1 General definitions

basic access: A user-network access arrangement that corresponds to the interface structure composed of two B-channels and one D-channel. The bit rate of the D-channel for this type of access is 16 kbit/s.

Implementation Conformance Statement (ICS): See ISO/IEC 9646-1 [8], §3.4.6.

Integrated Services Digital Network (ISDN): An integrated services network that provides digital connections between UNIs.

interface: This ETS defines the layer 1 characteristics of the UNI to be applied at the S or T reference points for the basic interface structure defined in CCITT Recommendation I.412 [2]. The reference configuration for the interface is defined in ITU-T Recommendation I.411 [1] and is reproduced in figure 1.

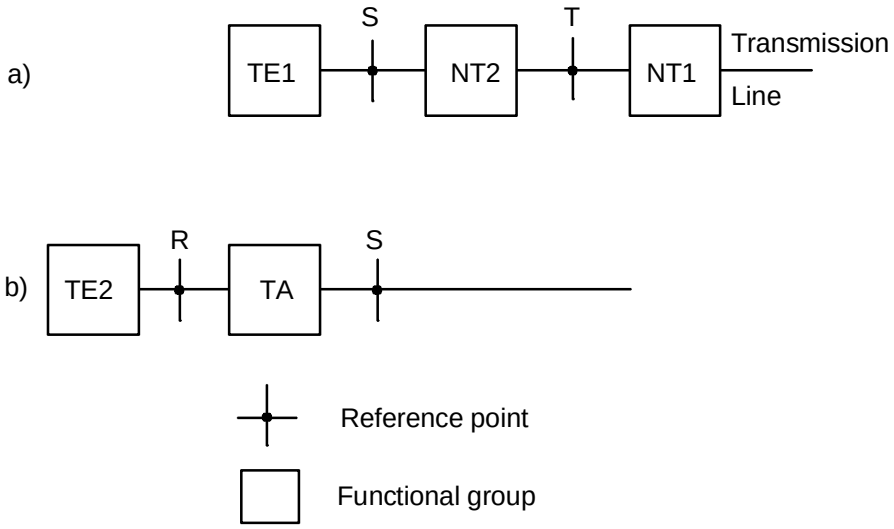


Figure 1: Definition of interface points according to the ISDN reference configuration

Network Termination (NT): The term NT is used to indicate network terminating layer 1 aspects of NT1 and NT2 functional groups unless otherwise indicated. However, in subclauses 3.1.5 and 7.2 the term NT is used to indicate the layer 1 network side of the basic access interface.

Terminal Equipment (TE): The term TE is used to indicate terminal terminating layer 1 aspects of TE1, TA and NT2 functional groups, unless otherwise indicated. However, in subclauses 3.1.5 and 7.2, the term TE is used to indicate the layer 1 terminal side of the basic access interface.

3.1.2 Definition of services

services required from the physical medium: Layer 1 of this interface requires a balanced metallic transmission medium, for each direction of transmission, capable of supporting 192 kbit/s.

services provided to layer 2: Layer 1 provides the following services to layer 2 and the management entity.

transmission capability: Layer 1 provides the transmission capability, by means of appropriately encoded bit streams, for the B- and D-channels and the related timing and synchronization functions.

activation/deactivation: Layer 1 provides the signalling capability and the necessary procedures to enable customer TEs and/or NTs to be deactivated when required and reactivated when required. The activation and deactivation procedures are defined in subclause 7.2.

D-channel access: Layer 1 provides the signalling capability and the necessary procedures to allow TEs to gain access to the common resource of the D-channel in an orderly fashion while meeting the performance requirements of the D-channel signalling system. These D-channel access control procedures are defined in subclause 7.1.

maintenance: Layer 1 provides the signalling capability, procedures and necessary functions at layer 1 to enable maintenance functions to be performed.

status indication: Layer 1 provides an indication to the higher layers of the status of layer 1.

3.1.3 Primitives between layer 1 and other entities

Primitives represent, in an abstract way, the logical exchange of information and control between layer 1 and other entities. They neither specify nor constrain the implementation of entities or interfaces.

3.1.4 Modes of operation

Both point-to-point and point-to-multipoint modes of operation, as described below, are intended to be accommodated by the layer 1 characteristics of the UNI. In this ETS, the modes of operation apply only to the layer 1 procedural characteristics of the interface and do not imply any constraints on modes of operation at higher layers.

Point-to-point operation: This mode of operation at layer 1 implies that only one source (transmitter) and one sink (receiver) are active at any one time in each direction of transmission at an S or T reference point. (Such operation is independent of the number of interfaces which may be provided on a particular wiring configurations - see clause 5).

Point-to-multipoint operation: This mode of operation at layer 1 allows more than one TE (source and sink pair) to be simultaneously active at an S or T reference point. (The multipoint mode of operation may be accommodated, as discussed in clause 5, with point-to-point or point-to-multipoint wiring configurations).

3.1.5 Definition of states

3.1.5.1 TE states

State F1 (INACTIVE): In this inactive (powered-off) state, the TE is not transmitting and cannot detect the presence of any input signals. In the case of locally powered TEs which cannot detect the appearance/disappearance of power source 1 or 2, this state is entered when local power is not present. For TEs which can detect power source 1 or power source 2, this state is entered whenever loss of power (required to support all TEI functions) is detected, or when the absence of power from source 1 or 2, whichever power source is used for determining the connection status, is detected.

State F2 (SENSING): This state is entered after the TE has been powered on but has not determined the type of signal (if any) that the TE is receiving. When in this state, a TE may go to a low-power consumption mode as specified in subclause 6.1.8.

State F3 (DEACTIVATED): This is the deactivated state of the physical protocol. Neither the NT nor the TE is transmitting. When in this state, a TE may go to a low-power consumption mode as specified in subclause 6.1.8.

State F4 (AWAITING Signal): When the TE is requested to initiate activation by means of a PH-ACTIVE REQUEST primitive, it transmits a signal (INFO 1) and waits for a response from the NT.

State F5 (IDENTIFYING Input): At the first receipt of any signal from the NT, the TE ceases to transmit INFO 1 and awaits identification of signal INFO 2 or INFO 4.

State F6 (SYNCHRONIZED): When the TE receives an activation signal (INFO 2) from the NT, it responds with a signal (INFO 3) and waits for normal frames (INFO 4) from the NT.

State F7 (ACTIVATED): State F7 is the only state where B and D channel contain operational data.

State F8 (LOST Framing): This is the condition when the TE has lost frame synchronization and is awaiting re-synchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

3.1.5.2 NT States

State G1 (DEACTIVE): In this deactivated state, the NT is not transmitting. When in this state, an NT may go to a low-power consumption mode as specified in subclause 6.1.8.

State G2 (PENDING Activation): In this partially active state the NT sends INFO 2 while waiting for INFO 3. This state will be entered on request by higher layers, by means of a PH-ACTIVATE REQUEST primitive, or on the receipt of INFO 0 or lost framing while in the active state (G3). The choice to eventually deactivate is up to higher layers at the network side.

State G3 (ACTIVE): This is the normal active state where the NT and TE are active with INFO 4 and INFO 3, respectively. A deactivation may be initiated by the NT system management, by means of an MPH-DEACTIVATE REQUEST primitive, or the NT may be the active state all the time, under non-fault conditions.

State G4 (PENDING Deactivation): When the NT wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state.

3.2 Symbols

For the purposes of this ETS, the following symbols apply:

ONE	Binary "1"
ZERO	Binary "0"

3.3 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

APS	Auxiliary Power Source
dc	direct current
HDLC	High level Data Link Control
ICS	Implementation Conformance Statement
IUT	Implementation Under Test
IXIT	Implementation eXtra Information for Testing
NT	Network Termination
PTNX	Private Telecommunication Network Exchange
TE	Terminal Equipment
TEI	Terminal Endpoint Identifier

4 Primitives associated with layer 1

The primitives to be passed across the layer 1/2 boundary or to the management entity and parameter values associated with these primitives are defined and summarized in table 1. For description of the syntax and use of the primitives, refer to CCITT Recommendation X.211 [3] and relevant detailed descriptions in clause 7.

Table 1: Primitives associated with layer 1

Generic	Specific name		Parameter		Message unit content
	REQUEST	**INDICATION**	**Priority indicator**	**Message unit**	
L1<->L2					
PH-DATA	X (note 1)	X	X (note 2)	X	Layer 2 peer-to-peer message
PH-ACTIVATE	X	X	-	-	
PH-DEACTIVATE	-	X	-	-	
M<->L1					
MPH-ERROR	-	X	-	X	Type of error or recovery from a previously reported error
MPH-ACTIVATE	-	X	-	-	
MPH-DEACTIVATE	X	X	-	-	
MPH-INFORMATION	-	X	-	X	Connected/disconnected
NOTE 1: PH-DATA REQUEST implies underlying negotiation between layer 1 and layer 2 for the acceptance of the data.					
NOTE 2: Priority indication applies only to the request type.					

5 Wiring configurations and location of interface points

5.1 General

The electrical characteristics of the UNI are determined on the basis of certain assumptions about the various wiring configurations which may exist in the user premises. These assumptions are identified in two major configuration descriptions, subclause 5.1.1 and subclause 5.1.2, together with additional material contained in annex A. Figure 2 shows a general reference configuration for wiring in the user premises.

5.1.1 Point-to-point configuration

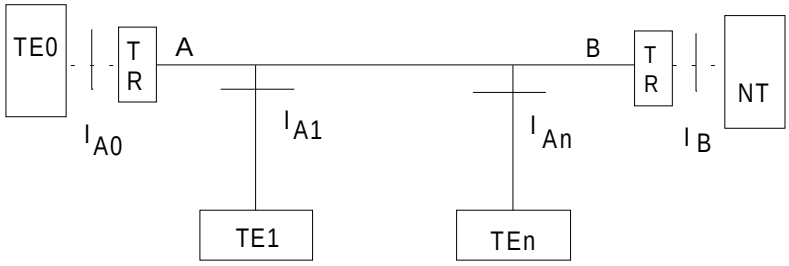
A point-to-point wiring configuration implies that only one source (transmitter) and one sink (receiver) are interconnected on an interchange circuit.

5.1.2 Point-to-multipoint configuration

A point-to-multipoint wiring configuration allows more than one source to be connected to the same sink or more than one sink to be connected to the same source on an interchange circuit. Such distribution systems are characterized by the fact that they contain no active logic elements performing functions (other than possibly amplification or regeneration of the signal).

5.1.3 Location of the interfaces

The wiring in the user premises is considered to be one continuous cable run with jacks for the TEs and NT attached directly to the cable or using stubs less than one metre in length. The jacks are located at interface points I_A and I_B (see figure 2). One interface point, I_A, is adjacent to each TE. The other interface point I_B, is adjacent to the NT. However, in some applications, the NT may be connected to the wiring without the use of a jack or with a jack which accommodates multiple interfaces (e.g., when the NT is a port on a PBX). The required electrical characteristics (described in clause 9) for I_A and I_B are different in some aspects.



TR Terminating Resistor
I Electrical Interface
A Location of I_A when the terminating resistor (TR) is included in the TE
B Location of I_B when the terminating resistor (TR) is included in the NT

Figure 2: Reference configuration for wiring in the user premises location

5.2 Support of wiring configurations

5.2.1 Wiring polarity integrity

For a point-to-point wiring configuration, the two wires of the interchange circuit pair may be reversed. However, for point-to-multipoint wiring configuration, the wiring polarity integrity of the interchange circuit (TE-to-NT direction) shall be maintained between TEs (see the reference configuration given in subclause 10.1, figure 20).

In addition, the wires of the optional pairs, which may be provided for powering, may not be reversed in either configuration.

5.2.2 NT and TE associated wiring

The wiring from the TE or the NT to its appropriate jack affects the interface electrical characteristics. A TE, or an NT that is not permanently connected to the interface wiring, shall be equipped with either of the following for connection to the interface point (I_A and I_B, respectively):

- a hard wired connecting cord (of not more than ten metres in the case of a TE, and not more than three metres in the case of an NT) and a suitable plug, or;

- a jack with a connecting cord (of not more than ten metres in the case of a TE, and not more than three metres in the case of an NT) which has a suitable plug at each end.

Normally, these requirements apply to the interface point (I_A and I_B, respectively), and the cord forms part of the associated TE or NT. However, as a national option, where the terminating resistors are connected internally to the NT, the connecting cord shall be considered as an integral part of the interface wiring. In this case, the requirements of this ETS shall be applied to the NT at the connection of the connecting cord to the NT. Note that the NT shall attach directly to the interface wiring without a detachable cord. Also note that the connector, plug and jack used for the connection of the detachable cord to the NT is subject to standardization.

Although a TE may be provided with a cord of less than five metres in length, it shall meet the requirements of this ETS with a cord having a minimum length of five metres. As specified above, the TE cord may be detachable. Such a cord may be provided as a part of the TE, or the TE may be designed to conform to the electrical characteristics specified in clause 9 with a standard ISDN basic access TE cord conforming to the requirements specified in subclause 9.9 of this ETS and having the maximum permitted capacitance.

The use of an extension cord, of up to 25 metres in length, with a TE is permitted but only on point-to-point wiring configurations. (The total attenuation of the wiring and of the cord in this case should not exceed 6 dB.)

6. Functional characteristics

6.1 Interface functions

6.1.1 B-channel

This function provides, for each direction of transmission, two independent 64 kbit/s channels for use as B-channels as defined in CCITT Recommendation I.412 [2].

6.1.2 Bit timing

This function provides bit (signal element) timing at 192 kbit/s to enable the TE and NT to recover information from the aggregate bit stream.

6.1.3 Octet timing

This function provides 8 kHz octet timing for the NT and TE.

6.1.4 Frame alignment

This function provides information to enable NT and TE to recover the time division multiplexed channels.

6.1.5 D-channel

This function provides, for each direction of transmission, one D-channel at a bit rate of 16 kbit/s, as defined in CCITT Recommendation I.412 [2].

6.1.6 D-channel access procedure

This function is specified to enable TEs to gain access to the common resource of the D-channel in an orderly controlled fashion. The functions necessary for these procedures include an echoed D-channel at a bit rate of 16 kbit/s in the direction NT to TE. For the definition of the procedures relating to D-channel access see subclause 7.1.

6.1.7 Power feeding

This function provides for the capability to transfer power across the interface. The direction of power transfer depends on the application. In a typical application, it may be desirable to provide for power transfer from the network side towards the terminals in order to, for example, maintain a basic telephony service in the event of failure of the locally provided power. The detailed specification of power feeding capability is contained in clause 10.

6.1.8 Deactivation

This function is specified in order to permit the TE and NT to be placed in a low power consumption mode when no calls are in progress. For TEs that are power fed across the interface from power source 1 and for remotely power fed NTs, deactivation places the functions that are so powered into a low power consumption mode (see clause10). The procedures and precise conditions under which deactivation takes place are specified in subclause 7.2 and figure 5 respectively.

6.1.9 Activation

This function restores all the functions of a TE or an NT, which may have been placed into a lower power consumption mode during deactivation, to an operating power mode (see clause10), whether under normal or restricted power conditions. The procedures and precise conditions under which activation takes place are defined in subclause 7.2 and figure 5 respectively.

6.2 Interchange circuits

Two interchange circuits, one for each direction of transmission, shall be used to transfer digital signals across the interface. All of the functions described in subclause 6.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in subclause 6.4.

6.3 Connected/disconnected indication

The appearance/disappearance of power is the criterion used by a TE to determine whether it is connected/disconnected at the interface. This is necessary for TEI (Terminal Endpoint Identifier) assignments according to the procedures described in ITU-T Recommendation I.411 [1].

A TE which considers itself connected, when unplugged, can cause duplication of TEI values after reconnection. When duplication occurs, procedures described in ITU-T Recommendation I.411 [1] will permit recovery.

6.3.1 TEs powered across the interface

A TE which is powered from power source 1 or 2 across the interface shall use the detection of power source 1 or 2, respectively, to establish the connection status. (See clause 10 and figure 19 for a description of the power sources.)

6.3.2 TEs not powered across the interface

A TE which is not powered across the interface may use either:

a) the detection of power source 1 or power source 2, whichever may be provided, to establish the connection status; or
b) the presence/absence of local power to establish the connection status.

TEs which are not powered across the interface and are unable to detect the presence of power source 1 and 2 shall consider themselves connected/disconnected when local power is applied/removed.

A TE shall use the detection of power source 1 or 2 to establish the connection status when automatic TEI selection procedures are used within the management entity.

6.3.3 Indication of connection status

TEs which use the detection of power source 1 or 2, whichever is used to determine connection/disconnection, to establish the connection status shall inform the management entity (for TEI purposes) using:

a) MPH-INFORMATION INDICATION (connected),
when operational power and the presence of power source 1 or 2, whichever is used to determine connection/disconnection, is detected; and

b) MPH-INFORMATION INDICATION (disconnected),
when the disappearance of power source 1 or 2, whichever is used to determine connection/disconnection, is detected, or power in the TE is lost.

TEs which are unable to detect power source 1 or 2, whichever may be provided, and, therefore, use the presence/absence of local power to establish the connection status (see subclause 6.3.2 b), shall inform the management entity using:

a) MPH-INFORMATION INDICATION (disconnected),
when power in the TE is lost (note);

b) MPH-INFORMATION INDICATION (connected),
when power in the TE is applied (note).

NOTE: The term "power" could be the full operational power or backup power. Backup power is defined such that it is enough to hold TEI values in memory and maintain the capability of receiving and transmitting layer 2 frames associated with the TEI procedures.

6.4 Frame structure

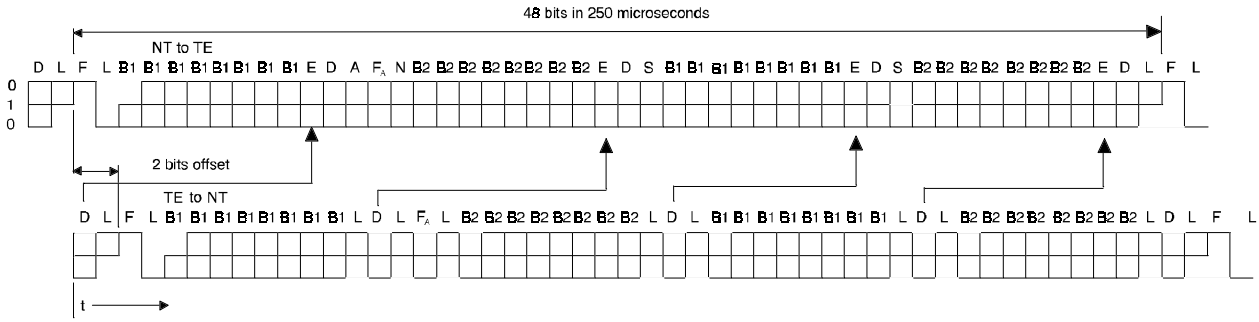
In both directions of transmission, the bits shall be grouped into frames of 49 bits each. The frame structure shall be identical for all configurations (point-to-point and point-to-multipoint).

6.4.1 Bit rate

The nominal transmitted bit rate at the interfaces shall be 192 kbit/s in both directions of transmission.

6.4.2 Binary organization of the frame

The frame structures are different for each direction of transmission. Both structures are illustrated diagrammatically in figure 3.



F	Framing bit	N	Bit set to a binary value N=F_A (NT to TE)
L	dc balancing bit	B1	Bit within B-channel 1
D	D-channel bit	B2	Bit within B-channel 2
E	D-echo-channel bit	A	Bit used for activation
F_A	Auxiliary framing bit (see Clause 8)	S	Reserved for future standardization
		M	Multiframing bit

NOTE 1: Dots demarcate those parts of the frame that are independently dc balanced.

NOTE 2: The nominal 2-bit offset is as seen from the TE (I_A in figure 2). The corresponding offset at the NT may be greater due to delay in the interface cable and varies by configuration

Figure 3: Frame structure at reference points S and T

6.4.2.1 TE to NT

Each frame consists of the groups of bits shown in table 2; each individual group is dc-balanced by its last bit (L bit).

Table 2

Bit position	Group
1 and 2	Framing signal with balance bit
3 - 11	B1-channel (first octet) with balance bit
12 and 13	D-channel bit with balance bit
14 and 15	F_A auxiliary framing bit for Q bit with balance bit
16 - 24	B2-channel (first octet) with balance bit
25 and 26	D-channel bit with balance bit
27 - 35	B1-channel (second octet) with balance bit
36 and 37	D-channel bit with balance bit
38 - 46	B2-channel (second octet) with balance bit
47 and 48	D-channel bit with balance bit

6.4.2.2 NT to TE

Frames transmitted by the NT contain an echo channel (E bits) used to retransmit the D bits received from the TEs. The D-echo channel is used for D-channel access control. The last bit of the frame (L bit) is used for balancing each complete frame.

The bits are grouped as shown in table 3.

Table 3

Bit position	Group
1 and 2	Framing signal with balance bit
3 - 10	B1-channel (first octet)
11	E, D-echo-channel bit
12	D-channel bit
13	Bit A used for activation
14	F_A auxiliary framing bit
15	N bit (coded as defined in clause 8)
16 - 23	B2-channel (first octet)
24	E, D-echo-channel bit
25	D-channel bit
26	M, multiframing bit
27 - 34	B1-channel (second octet)
35	E, D-echo-channel bit
36	D-channel bit
37	S - reserved for future standardization
38-45	B2-channel (second octet)
46	E, D-echo-channel bit
47	D-channel bit
48	Frame balance bit
NOTE: S shall be set to ZERO. F_A and M shall also set to ZERO except for NT 2 providing multiframing.	

6.4.2.3 Relative bit positions

At the TEs, timing in the direction TE to NT shall be derived from the frames received from the NT.

The first bit of each frame transmitted from a TE towards the NT shall be delayed, nominally, by two bit periods with respect to the first bit of the frame received from the NT. Figure 3 illustrates the relative bit positions for both transmitted and received frames.

6.5 Line code

For both directions of transmission, pseudo-ternary coding is used with 100 % pulse width as shown in figure 4. Coding is performed in such a way that a ONE is represented by no line signal, whereas a ZERO is represented by a positive or negative pulse. The first ZERO following the frame bit-balance bit is of the same polarity as the framing bit-balance bit. Subsequent ZEROs shall alternate in polarity.

A balance bit is a ZERO if the number of ZEROs following the previous balance bit is odd. A balance bit is a ONE if the number of ZEROs following the previous balance bit is even.

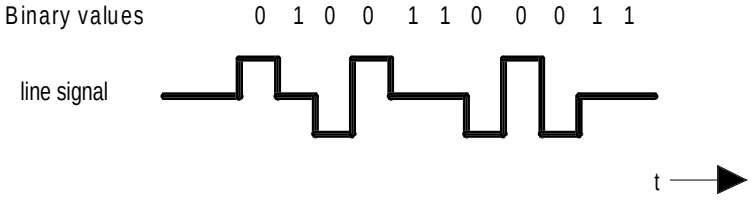


Figure 4: Pseudo-ternary code - example of application

6.6 Timing considerations

The NT shall derive its timing from the network clock. A TE shall derive its timing (bit, octet, frame) from the signal received from the NT and use this derived timing to synchronize its transmitted signal.

7 Interface procedures

7.1 D-channel access procedure

The following procedure allows for a number of TEs connected in a multipoint configuration to gain access to the D-channel in an orderly fashion. The procedure always ensures that, even in cases where two or more TEs attempt to access the D-channel simultaneously, one, but only one, of the TEs will be successful in completing transmission of its information. This procedure relies upon the use of layer 2 frames delimited by flags consisting of the binary pattern "01111110" and the use of zero bit insertion to prevent flag imitation (see ITU-T Recommendation I.411 [1]).

The procedure also permits TEs to operate in a point-to-point manner.

7.1.1 Interframe (layer 2) time fill

When a TE has no layer 2 frames to transmit, it shall send ONEs on the D-channel, i.e, the interframe time fill to the TE-to-NT direction shall be ONEs.

When an NT has no layer 2 frames to transmit, it shall send ONEs or HDLC flags, i.e., the interframe time fill in the NT-to-TE direction shall be either all ONEs or repetitions of the octet "01111110". When the interframe time fill is HDLC flags, the flag which defines the end of a frame may define the start of the next frame.

7.1.2 D-echo channel

The NT, on receipt of a D-channel bit from TE or TEs, shall reflect the binary value in the next available D-echo channel bit position towards the TE.

In case a transparent loopback 2 is applied, the NT shall send INFO 4 frames toward the user with the D-echo channel bit is set to ZERO. It may be necessary to force the D-echo channel bits to all ZEROs during other loopbacks.

7.1.3 D-channel monitoring

A TE, while in the active condition, shall monitor the D-echo channel, counting the number of consecutive ONEs. If a ZERO bit is detected, the TE shall restart counting the number of consecutive ONE bits. The current value of the count is called C.

NOTE: C need not be incremented after the value eleven has been reached.

7.1.4 Priority mechanism

Layer 2 frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information (priority class 2). Furthermore, to ensure that within each priority class all competing TEs are given a fair access to the D-channel, once a TE has successfully completed the transmission of a frame, it is given a lower level of priority within the class. The TE is given back its normal level within a priority class when all TEs have had an opportunity to transmit information at the normal level within that priority class.

The priority class of a particular layer 2 frame may be a characteristic of the TE which is preset at manufacture or at installation, or it may be passed down from layer 2 as a parameter of the PH-DATA REQUEST primitive.

The priority mechanism is based on the requirement that a TE may start layer 2 frame transmission only when C (see subclause 7.1.3) is equal to, or exceeds, the value X_1 for priority class 1 or is equal to, or exceeds, the value X_2 for priority class 2. The value of X_1 shall be eight for the normal level and nine for

the lower level of priority. The value of X_2 shall be ten for the normal level and eleven for the lower level of priority.

In a priority class the value of the normal level of priority is changed into the value of the lower level of priority (i.e. higher value) when a TE has successfully transmitted a layer 2 frame of that priority class.

The value of the lower level of priority is changed back to the value of the normal level of priority when C (see subclause 7.1.3) equals the value of the lower level of priority (i.e. higher value).

Annex E describes an example of how the priority system may be implemented.

7.1.5 Collision detection

While transmitting information in the D-channel, the TE shall monitor the received D-echo channel and compare the last transmitted bit with the next available D-echo bit. If the transmitted bit is the same as the received echo, the TE shall continue its transmission. If, however, the received echo is different from the transmitted bit, the TE shall cease transmission immediately and return to the D-channel monitoring state.

7.2 Activation/deactivation

7.2.1 Activate primitives

The following primitives should be used between layers 1 and 2 and between layer 1 and the management entity in the activation procedures. For use in state diagrams etc., abbreviations of the primitive names are also given.

PH-ACTIVATE REQUEST (PH-AR)

PH-ACTIVATE INDICATION (PH-AI)

MPH-ACTIVATE INDICATION (MPH-AI)

7.2.2 Deactivate primitives

The following primitives shall be used between layers 1 and 2 and between layer 1 and the management entity in the deactivation procedures. For use in state diagrams etc., abbreviations of the primitive names are also given.

MPH-DEACTIVATE REQUEST (MPH-DR)

MPH-DEACTIVATE INDICATION (MPH-DI)

PH-DEACTIVATE INDICATION (PH-DI)

7.2.3 Management primitives

The following primitives shall be used between layer 1 and the management entity. For use in state diagrams etc., abbreviations of the primitive names are also given.

MPH-ERROR INDICATION (MPH-EI)

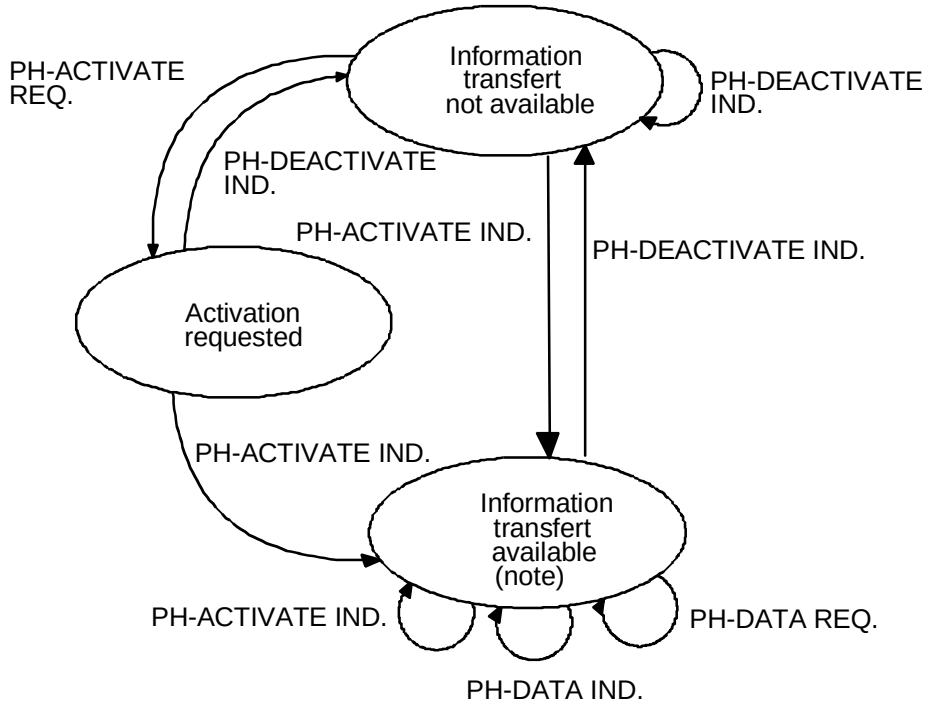
Message unit contains type of error or recovery from a previously reported error.

MPH-INFORMATION INDICATION (MPH-II)

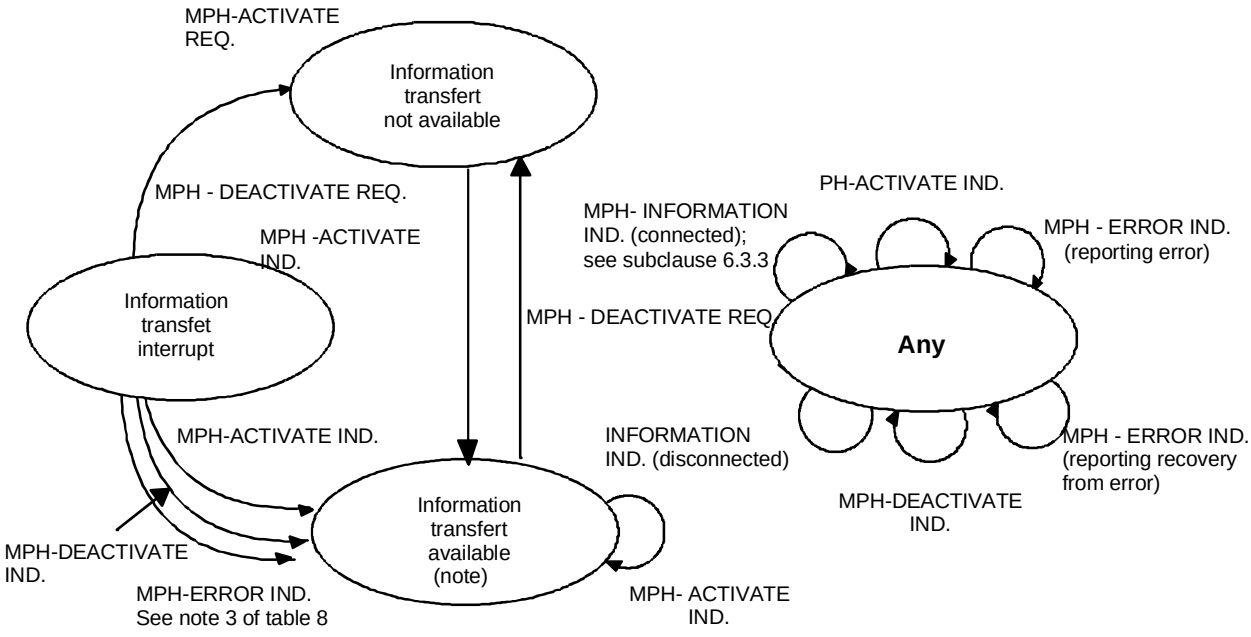
7.2.4 Valid primitive sequences

The primitives defined in subclauses 7.2.1, 7.2.2 and 7.2.3 specify, conceptually, the service provided by layer 1 to layer 2 and the layer 1 management entity. The constraints on the sequence in which the primitives may occur are specified in figure 5. These diagrams do not represent the states which shall exist for the layer 1 entity. However, they do illustrate the condition that the layer 2 and management

entities perceive layer 1 to be in at a result of the primitives transferred between entities. Furthermore, figure 5 does not represent an interface and is used only for modelling purposes.



a) Layer 1 - Layer 2



b) Layer 1 - Management

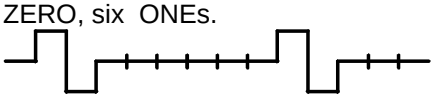
NOTE: Layer 2 is not aware if the information transfer capability is temporarily interrupted.

Figure 5: Valid primitive sequences as perceived by layer 2 and management entities

7.3 Signals

The identification of specific signals across the S/T reference point are given in table 4. Also included is the coding for these signals.

Table 4: Definition of INFO signals (note 1)

Signals from NT to TE		Signals from TE to NT	
INFO 0 (note 3)	No signal.	INFO 0 (note 3)	No signal.
		INFO 1 (note 2)	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs.  Nominal bit rate = 192 kbit/s
INFO 2 (note 3)	Frame with all bits of B, D, and D-echo channels set to ZERO. Bit A set to ZERO. N and L bits set according to the normal coding rules.		
		INFO 3	Synchronized frames with operational data on B and D channels.
INFO 4	Frames with operational data on B, D and D-echo channels. Bit A set to ONE.		

NOTE 1: For configurations where the wiring polarity may be reversed (see subclause 5.2.1) signals may be received with the polarity of the ZEROs inverted. All NT and TE receivers shall be designed to tolerate wiring polarity reversals.

NOTE 2 : TEs which do not need the capability to initiate activation of a deactivated I.430 interface (e.g., TEs required to handle only incoming calls) need not have the capability to send INFO 1. In all other respects, these TEs shall be in accordance with subclauses 3.1 and 7.2. It should be noted that in the point-to-multipoint configuration more than one TE transmitting simultaneously will produce a bit pattern, as received by the NT, different from that described above, e.g., two or more overlapping (asynchronous) instances of INFO 1.

NOTE 3: For the transmission of INFO 0, the duration of a state in which the signal "consecutive ONEs" is transmitted is relevant rather than the definition of INFO 0 in terms of a time.
The duration of a state depends on events (e.g. service primitives) and may be indefinitely short.

7.4 Activation/deactivation procedure for TEs

7.4.1 General TE procedures

All TEs shall conform to the following (these statements are an aid to understanding; the complete procedures are specified in subclause 7.4.2):

a) TEs, when first connected, when power is applied, or upon the loss of frame alignment (see subclause 8.1.1) shall transmit INFO 0. However, a TE that is disconnected but powered is a special situation and could be transmitting INFO 1 when connected;

b) TEs shall transmit INFO 3 when frame alignment is established (see subclause 8.1.2). However, the satisfactory transmission of operational data cannot be assured prior to the receipt of INFO 4;

c) TEs that are locally powered shall, when power is removed, initiate the transmission of INFO 0 before frame alignment is lost.

7.4.2 Specification of the procedure

The procedure for TEs which can detect power source 1 and 2 is shown in the form of a finite state matrix table 5. An SDL representation of the procedure is outlined in annex F. The finite state matrices for two other TE types are given in tables 5 and 6. The finite state matrix and SDL representations reflect the requirements necessary to assure proper interfacing of a TE with an NT conforming to the procedures described in table 7. They also describe primitives at the layer 1/2 boundary and layer 1/management entity boundary.

7.5 Activation/deactivation for NTs

The procedure is shown in the form of a finite state matrix in table 6. An SDL representation of the procedure is outlined in annex F. The finite state matrix and SDL representations reflect the requirements necessary to assure proper interfacing of an activating/deactivating NT with a TE conforming to the procedures described in table 8. They also describe primitives at the layer 1/2 boundary and layer 1/mangement entity boundary.

7.5.1 Non-activating/non-deactivating NTs

The behaviour of such NTs is the same as that of an activating/deactivating NT never receiving MPH-DEACTIVATE REQUEST from the management entity. States G1 (deactive), G4 (pending deactivation) and timers 1 and 2 may not exist from such NTs.

7.6 Timer values

The finite state matrix tables show timers on both the TE and the NT. The following values are defined for timers:

TE: Timer 3, not to be specified (the value depends on the subscriber loop transmission technique. The worst case value is 30s);
NT: Timer 1, not to be specified. Timer 2,25 to 100 ms.

7.7 Activation times

7.7.1 TE activation times

A TE in the deactivated state (F3) shall, upon the receipt of INFO 2 or INFO 4, establish frame synchronization and initiate the transmission of INFO 3 within 100 ms. In state F6 a TE shall recognize the receipt of INFO 4 within two frames (in the absence of errors).

A TE in the "awaiting signal" state (F4) shall, upon the receipt of INFO 2 or INFO 4, cease the transmission of INFO 1 and initiate the transmission of INFO 0 within 5 ms and then respond to INFO 2 or INFO 4, within 100 ms, as above.

NOTE: Note that in table 5, the transition from F4 to F5 is indicated as the result of the receipt of "any signal" which is in recognition of the fact that a TE may not know that the signal being received is INFO 2 or INFO 4 until after it has recognized the presence of a signal.

Table 5: Activation/deactivation layer 1 finite state matrix for TEs
TEs powered from power source 1 or 2

State name	Inactive	Sensing	Deactivated	Awaiting signal	Identifying input	Synchro-nized	Activated	Lost framing
State number	**F1**	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
Event / INFO sent	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 1**	**INFO 0**	**INFO 3**	**INFO 3**	**INFO 0**
Power on and detection of Power S (note 2 and note 3)	F2	-	-	-	-	-	-	-
Loss of power (note 2)	-	F1	MPH-II(d), F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1
Disappearance of Power S (note 3)	-	F1	MPH-II(d), F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1
PH-ACTIVATE REQUEST	/	|	ST T3; F4 (note 8)	|	|	-	|	|
Expiry T3	/	/	-	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI,	/	MPH-DI PH-DI F3
RECEIVE INFO 0 (note 6 and note 7)	/	MPH-II(c), F3	-	-	-	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI MPH-EI2, F3
Receive any signal (note 4)	/	-	-	F5	-	/	/	-
Receive INFO 2	/	MPH-II(c), F6	F6	F6 (note 5)	F6	-	MPH-EI1, F6	MPH-EI2, F6
Receive INFO 4	/	MPH-II(c), PH-AI, MPH-AI, F7	PH-AI, MPH-AI, F7 Stop and reset timer T3	PH-AI, MPH-AI, F7 (note 5) Stop and reset timer T3	PH-AI, MPH-AI, F7 Stop and reset timer T3	PH-AI, MPH-AI, MPH-EI2, F7 Stop and reset timer T3	-	PH-AI, MPH-AI, MPH-EI2, F7 Stop and reset timer T3
Lost framing	/	/	/	/	/	MPH-EII, F8	MPH-EII, F8	-

- No change, no action
| Impossible by the definition of the layer 1 service
/ Impossible situation
a, b, Fn Issue primitives "a" and "b" and then go to state "Fn"
PH-AI Primitive PH-ACTIVATE INDICATION
PH-DI Primitive PH-DEACTIVATE INDICATION
MPH-AI Primitive MPH-ACTIVATE INDICATION
MPH-DI Primitive MPH-DEACTIVATE INDICATION
MPH-EI1 Primitive MPH-ERROR INDICATION reporting error
MPH-EI2 Primitive MPH-ERROR INDICATION reporting recovery from error
MPH-II(c) Primitive MPH-INFORMATION INDICATION (connected)
MPH-II(d) Primitive MPH-INFORMATION INDICATION (disconnected)
ST T3 Start Timer T3
Power S Power source 1 or power source 2.

(continued)

Table 5 (concluded): Activation/deactivation layer 1 finite state matrix for TEs
TEs powered from power source 1 or 2

NOTE 1:	Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time.
NOTE 2:	The term "power" could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI value in memory and maintain the capability of receiving and transmitting layer 2 frames associated with the TEI procedures.
NOTE 3:	The procedures described in table 5 require the provision of power source 1 or power source 2 to enable their complete operation. A terminal which determines that it is connected to a network not providing power source 1 or 2 should default to the procedures described in table 6.
NOTE 4:	This event reflects the case where a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.
NOTE 5:	If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs shall go to F5. To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs shall be verified where the received signal is any bit pattern (containing at least 3 ZEROs in each frame interval) to which TEs conforming to subclause 8.1.2 are not able to synchronize.
NOTE 6:	INFO 0 shall be detected when 48 or more contiguous ONEs have been received and the TE shall perform the actions specified in table 5. Conformance shall be tested with a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1 000 kHz, preferably 100 kHz). TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms.
NOTE 7:	To prevent the loss of an on-going communication caused by spurious effects a timer is started when leaving state F7 or F8 upon the reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter an active state before expiry of this timer. The value of this timer is in the range of 500 ms to 1 000 ms.
NOTE 8:	No reaction to the event PH-ACTIVATE REQUEST shall be accomplished if the TE is receiving signals at the interface other than INFO 0, INFO 2 or INFO 4. This is requested to avoid disruption of activity at the bus (between other terminals and the network side of the interface) by superimposing INFO 1 to normal data (INFO 3) from other TEs when a failure occurs at the receiver of this TE. The failure could be caused also by the interruption of a single wire in the cord.

Table 6: Activation/deactivation for TEs
TEs locally powered and unable to detect power source 1 or 2

STATE name	Inactive	Sensing	Deactivated	Awaiting signal	Identifying input	Synchro-nized	Activated	Lost framing
STATE number	**F1**	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
EVENT INFO sent	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 1**	**INFO 0**	**INFO 3**	**INFO 3**	**INFO 0**
Loss of local power (note 2)	/	F1	MPH-II(d); F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d), MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1
Power on and detection of power (note 2)	F2	-	-	-	-	-	-	-
Detect Power Source	Event not applicable to this type of terminal							
Disappearance of Power Source	Event not applicable to this type of terminal							
PH-Act Request	/	/	ST T3; F4 (note 6)	|	|	-	|	-
Expiry T3	/	/	-	MPH-DI, PH-DI, F3	MPH-DI PH-DI F3	MPH-DI, PH-DI	/	MPH-DI, PH-DI, F3
Receiving INFO 0 (note 4 and note 5)	/	MPH-II(c), F3	-	-	-	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, MPH-EI2, F3
Receiving any signal (note 1)	/	-	-	F5	-	/	/	-
Receiving INFO 2	/	MPH-II(c), F6	F6	F6 (note 3)	F6	-	MPH-EI1 F6	MPH-EI2 F6
Receiving INFO 4	-	MPH-II(c), PH-AI, MPH-AI; F7	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI; S/R T3 F7 (note 3)	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI, MPH-EI2; S/R T3 F7	-	PH-AI, MPH-AI, MPH-EI2 S/R T3 F7
Lost framing	/	/	/	/	/	MPH-EI1, F8	MPH-EI1, F8	-

NOTE 1: This event reflects the case in which a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.

NOTE 2: The term power could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI values in memory and maintain the capability of receiving and transmitting layer-2 frames associated with the TEI procedures.

NOTE 3: If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs shall go to F5. To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs shall be verified where the received signal is any bit pattern (containing at least three ZEROs in each frame interval) to which TEs conforming to subclause 8.1.2 are not able to synchronize.

NOTE 4: To avoid disruption of on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer is in the range of 500 ms to 1 000 ms.

NOTE 5: INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in this table.
Conformance shall be tested with a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1 000 kHz, preferably 100 kHz).
TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms.

NOTE 6: No reaction to the event PH-ACTIVATE REQUEST shall be accomplished if the TE is receiving signals at the interface other than INFO 0, INFO 2 or INFO 4.
This is requested to avoid disruption of activity at the bus (between other terminals and the network side of the interface) by superimposing INFO 1 to normal data (INFO 3) from other TEs when a failure occurs at the receiver of this TE.
The failure could be caused also by the interruption of a single wire in the cord.

Table 7: Activation/deactivation for TEs
TEs locally powered and able to detect power source 1 or 2

STATE name	Inactive		Sensing	Deactivated	Awaiting signal	Identifying input	Synchro-nized	Activated	Lost framing
STATE number	**F1.0**	**F1.1**	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**
EVENT INFO sent	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 0**	**INFO 1**	**INFO 0**	**INFO 3**	**INFO 3**	**INFO 0**
Loss of power (note 2)	/	F1.0	F1.0	MPH-II(d); F1.0	MPH-II(d) MPH-DI, PH-DI; F1.0	MPH-II(d), MPH-DI, PH-DI; F1.0	MPH-II(d) MPH-DI, PH-DI; F1.0	MPH-II(d) MPH-DI, PH-DI; F1.0	MPH-II(d) MPH-DI, PH-DI; F1.0
Power on and detection of power (note 2)	F1.1	-	-	-	-	-	-	-	-
Detect Power S	/	F2	/	/	/	/	-	-	/
Disappearance of Power Source	/	/	F1.1	MPH-II(d); F1.1	MPH-II(d), F1.1	MPH-II(d), MPH-DI, PH-DI; F1.1	-	-	MPH-II(d), MPH-DI, PH-DI; F1.1
PH-Act Request	/	|	|	ST T3; F4 (note 7)	|	|	-	|	-
Expiry T3	/	-	-	-	MPH-DI, PH-DI, F3	MPH-DI PH-DI F3	MPH-DI, PH-DI	/	MPH-DI PH-DI F3
Receiving INFO 0 (note 4 and note 5)	/	/	MPH-II(c), F3	-	-	-	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, F3	MPH-DI, PH-DI, MPH-EI2, F3
Receiving any signal (note 1)	/	/	-	-	F5	-	/	/	-
Receiving INFO 2	/	note 6	-	F6	F6 (note 3)	F6	-	MPH-EI1 F6	MPH-EI2 F6
Receiving INFO 4	/	note 6	MPH-II(c) PH-AI MPH-AI; F7	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI; S/R T3 F7 (note 3)	PH-AI, MPH-AI; S/R T3 F7	PH-AI, MPH-AI, MPH-EI2; S/R T3; F7	-	PH-AI, MPH-AI, MPH-EI2; S/R T3; F7
Lost framing	/	/	/	/	/	/	MPH-EI1, F8	MPH-EI1, F8	-

(continued)

Table 7 (concluded): Activation/deactivation for TEs
TEs locally powered and able to detect power source 1 or 2

NOTE 1:	This event reflects the case in which a signal is received and the TE has not (yet) determined whether it is INFO 2 or INFO 4.
NOTE 2:	The term power could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI values in memory and maintain the capability of receiving and transmitting layer-2 frames associated with the TEI procedures.
NOTE 3:	If INFO 2 or INFO 4 is not recognized within 5 ms after the appearance of a signal, TEs shall go to F5. To ensure that a TE will go to state F5 when receiving a signal to which it cannot synchronize, operation of TEs should be verified where the received signal is any bit pattern (containing at least three ZEROs in each frame interval) to which TEs conforming to subclause 8.1.2 are not able to synchronize.
NOTE 4:	To avoid disruption of on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO 0. The corresponding PH-DI will be delivered to layer 2 only, if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer may be in the range of 500 ms to 1 000 ms.
NOTE 5:	INFO 0 shall be detected when 48 or more contiguous binary ONEs have been received and the TE shall perform the actions specified in this table. Conformance shall be tested with a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1 000 kHz, preferably 100 kHz). TE being in state F6 or F7 shall react on receipt of this signal by transmitting INFO 0 within a period of time 250 µs to 25 ms.
NOTE 6:	Two possibilities exist for the reaction in these cases Case 1:MPH-II(c), MPH-AI, PH-AI, stop and reset T3, F7; this reaction is appropriate when INFO 4 is detected to supplement the connection status. MPH-II(c), stop and reset T3, F6; this reaction is appropriate when INFO 2 is detected to supplement the connection status. Case 2: "/" (impossible); this reaction is to be applied when the connection status is determined by the presence or absence of power.
NOTE 7:	No reaction to the event PH-ACTIVATE REQUEST shall be accomplished if the TE is receiving signals at the interface other than INFO 0, INFO 2 or INFO 4. This is requested to avoid disruption of activity at the bus (between other terminals and the network side of the interface) by superimposing INFO 1 to normal data (INFO 3) from other TEs when a failure occurs at the receiver of this TE. The failure could be caused also by the interruption of a single wire in the cord.

Table 8: Activation/deactivation layer 1 finite state matrix for NTs

State name	Deactive	Pending Activation	Active	Pending deactivation
State number	G1	G2	G3	G4
Event / INFO sent	INFO 0	INFO 2	INFO 4	INFO 0
PH-ACTIVATE REQUEST	Start timer T1 G2	|	|	Start timer T1 G2
MPH-DEACTIVATE REQUEST	|	Start timer T2, PH-DI;G4 (note 3)	Start timer T2, PH-DI,G4 (note 3)	|
Expiry T1 (note 2)	-	Start timer T2, PH-DI;G4 (note 3)	/	-
Expiry T2	-	-	-	G1
Receiving INFO 0 (note 6)	-	-	MPH-DI,MPH-EI; G2 (note 4)	G1
Receiving INFO 1	Start timer 1 G2	-	/	-
Receiving INFO 3	/	Stop timer T1 PH-AI, MPH-AI; G3 (note 5)	-	-
Lost Framing	/	/	MPH-DI,MPH-EI; G2 (note 4)	-

-	No state change
/	Impossible by the definition of peer-to-peer physical layer procedures or system internal reasons
|	Impossible by the definition of the physical layer service
a, b; Gn	Issue primitives "a" and "b" then go to state "Gn"
PH-AI	Primitive PH-ACTIVATE INDICATION
PH-DI	Primitive PH-DEACTIVATE INDICATION
MPH-AI	Primitive MPH-ACTIVATE INDICATION
MPH-DI	Primitive MPH-DEACTIVATE INDICATION
MPH-EI	Primitive MPH-ERROR INDICATION

NOTE 1: Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals which are available all the time.

NOTE 2: Timer 1 (T1) is a supervisory timer which has to take into account the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-TE portion of the customer access. ET is the exchange termination.

NOTE 3: Timer 2 (T2) prevents unintentional reactivation. Its value is 25 ms ≤ value ≤ 100 ms. This implies that a TE has to recognize INFO 0 and to react on it within 25 ms. If the NT is able to unambiguously recognize INFO 1, then the value of timer 2 may be 0, and an MPH-DEACTIVATE REQUEST would cause a direct transition from state G2 or G3 to G1. It should be noted that the unambiguous detection of INFO 1 may not be possible in passive bus configurations, considering all possible implementations.

NOTE 4: These notifications (MPH-DI, MPH-EI) need not be transferred to a management entity at the NT.

NOTE 5: As an implementation option, to avoid premature transmission of information (i.e., INFO 4), layer 1 may not initiate the transmission of INFO 4 or send the primitives PH-ACTIVATE INDICATION and MPH-ACTIVATE INDICATION (to layer 2 and management, respectively) until a period of 100 ms has elapsed since the receipt of INFO 3. Such a delay time should be implemented in the ET, if required.

NOTE 6: INFO 0 shall be detected when 48 or more contiguous ONEs have been received and the NT shall perform the actions specified in table 8.
For conformance test purposes, in the state G3 when receiving a sinusoidal signal having a voltage of 100 mV peak-to-peak (with a frequency in the range of 2 kHz to 1 000 kHz, preferably 100 kHz), the NT shall react by transmitting INFO 2 within a period of time 250 ms to 25 ms.
It is recognized that the action in state G4 cannot be observed or verified at the interface.

7.7.2 NT activation times

An NT in the deactivated state (G1) shall, upon the receipt of INFO 1, initiate the transmission of INFO 2 (synchronized to the network) within 1 s under normal conditions. Delays, "Da", as long as 30 s are acceptable under abnormal (non-fault) conditions, e.g., as a result of a need for retrain for an associated loop transmission system.

An NT in the "pending activation" state (G2) shall, upon the receipt of INFO 3, initiate the transmission of INFO 4 within 500 ms under normal conditions. Delays, "Db", as long as 15 s are acceptable under abnormal (non-fault) conditions provided that the sum of the delays "Da" and "Db" is not greater than 30 s.

7.8 Deactivation times

A TE shall respond to the receipt of INFO 0 by initiating the transmission of INFO 0 within 25 ms.

An NT shall respond to the receipt of INFO 0 or the loss of frame synchronization by initiating the transmission of INFO 2 within 25 ms; however, the layer 1 entity does not deactivate in response to INFO 0 from a TE.

8 Frame alignment procedures

The first bit of each frame is the framing bit, F; it is a ZERO.

The frame alignment procedure makes use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse (line code violation). This allows rapid reframing.

According to the coding rule, both the framing bit and the first ZERO bit following the framing bit-balance bit (in position 2 in the same frame) produce a line code violation. To guarantee secure framing, the auxiliary framing bit pair F_A and N in the direction NT to TE or the auxiliary framing bit F_A with the associated balancing bit L in the direction TE to NT are introduced. This ensures that there is a line code violation at 14 bits or less from the framing bit F, due to F_A or N being a ZERO bit (NT to TE) or to F_A being a ZERO bit (TE to NT) if the F_A bit position is not used as a Q bit. The framing procedures do not depend on the polarity of the framing bit F, and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N, in the direction NT to TE, is such that N is the binary opposite of F_A ($N = F_A$). The F_A and L bits in the direction TE to NT are always coded such that the binary values of F_A and L are equal.

8.1 Frame alignment procedure in the direction NT to TE

Frame alignment, on initial activation of the TE, shall comply with the procedures defined in subclause 7.2.

8.1.1 Loss of frame alignment

Loss of frame alignment may be assumed when a time period equivalent to n 48-bit frames has elapsed without having detected valid pairs of the line code violations obeying the ≤14 bit criterion as described in clause 8. The TE shall cease transmission immediately.

NOTE: $2 \leq n \leq 5$.

8.1.2 Frame alignment

Frame alignment may be assumed to occur when m consecutive pairs of line code violations obeying the ≤ 14 bit criterion have been detected.

NOTE: $3 \leq m \leq 6$.

8.2 Frame alignment in the direction TE to NT

The criterion of a line code violation at 13 bits or less from the framing bit (F) shall apply.

8.2.1 Loss of frame alignment

The NT may assume loss of frame alignment if a time period equivalent to at least n 48-bit frames has elapsed since detecting consecutive violations according to the 13 bit criterion, if all F_A bits have been set to ZERO. Otherwise, a time period equivalent to at least three 48-bit frames shall be allowed before assuming loss of frame alignment. On detection of loss of frame alignment the NT shall continue transmitting towards the TE.

NOTE: $2 \leq n \leq 5$.

8.2.2 Frame alignment

The NT may assume that frame alignment has been regained when m consecutive pairs of the line code violations obeying the 13 bit criterion have been detected.

NOTE: $3 \leq m \leq 6$.

8.3 Multiframing

The multiframing mechanism is intended to provide extra layer 1 capacity in the TE-to-NT direction (Q channel). The use of multiframing is out of the scope of this ETS. The NT 1 shall not provide multiframing, therefore the F_A bit in the frame NT-to-TE (see figure 3) shall be set to ZERO. The terminal side may provide multiframing in accordance with annex G to this ETS.

However, TEs shall provide for identification of the bit positions which provide this extra capacity, designated Q bits.

The TE shall echo the binary value of the received F_A bits in the corresponding F_A bit position of the frame transmitted to the NT.

8.4 Idle channel code on the B channels

A TE shall send ONEs in any B channel that is not assigned to it.

9 Electrical characteristics

9.1 Bit rate

9.1.1 Nominal rate

The nominal bit rate is 192 kbit/s.

9.1.2 Tolerance

The tolerance (free running mode) is ± 100 ppm.

9.2 Jitter and bit-phase relationship between TE input and output

9.2.1 Test configurations

The jitter and phase deviation measurements are carried out with four different waveforms at the TE input, in accordance with the following configurations:

i) point-to-point configuration with 6 dB attenuation measured between the two terminating resistors at 96 kHz (high capacitance cable);
ii) short passive bus with 8 TEs (including the TE under test) clustered at the far end from the signal source (high capacitance cable);
iii) short passive bus with the TE under test adjacent to the signal source and the other seven TEs clustered at the far end from the signal source. Configuration a) high capacitance cable; configuration b) low capacitance cable;
iv) ideal test signal condition, with one source connected directly to the receiver of the TE under test (i.e., without artificial line).

Examples of waveforms that correspond to the configurations i), ii), iiia) and iiib) are given in figure 6 to figure 9. Test configurations which can generate these signals are given in annex D.

9.2.2 Timing extraction jitter

Timing extraction jitter, as observed at the TE output, shall be within -7 % to +7 % of a bit period, when the jitter is measured using a high pass filter with a cut-off frequency (3 dB point) of 30 Hz and an asymptotic roll off of 20 dB per decade under the test conditions described in subclause 9.2.1. The limitation applies with an output data sequence having ONEs in both B-channels and with input data sequences described

in a) to c) below. The limitation applies to the phase of all zero-volt crossings of all adjacent ZEROs in the output data sequence.

a) a sequence consisting of continuous frames with all ONEs in D-, D-echo and both B-channels;

b) a sequence, repeated continuously for at least 10 seconds, consisting of:

- 40 frames with continuous octets of "10101010" (the first bit to be transmitted is binary ONE) in both B-channels and continuous ONEs in D- and D-echo channels; followed by

- 40 frames with continuous ZEROs in D-, D-echo and both B-channels;

c) a sequence consisting of a pseudo random pattern with a length of 2^{19}-1 in D-, D-echo, and both B-channels. (This pattern may be generated with a shift register with 19 stages with the outputs of the first, the second, the fifth and the nineteenth stages added together (modulo 2) and fed back to the input).

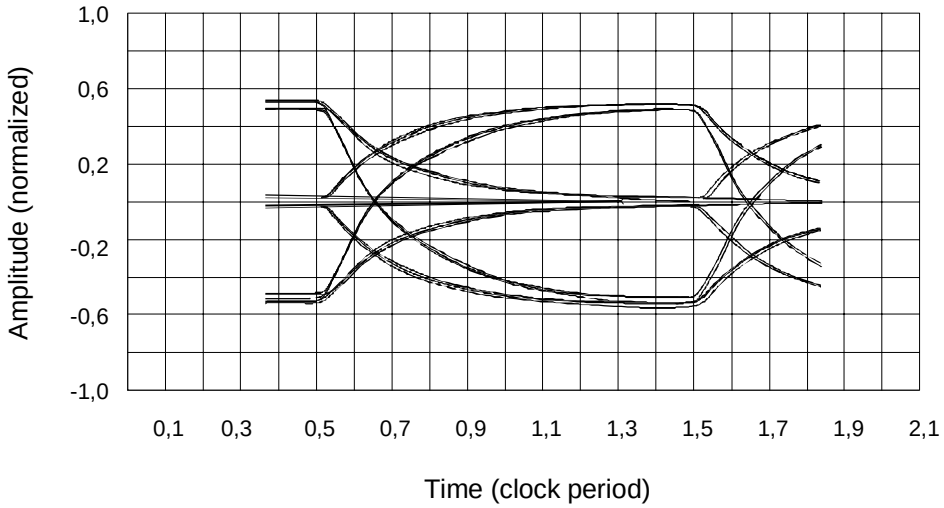


Figure 6: Waveform for test configuration i) - point-to-point (6 dB) (C = 120 nF/km)

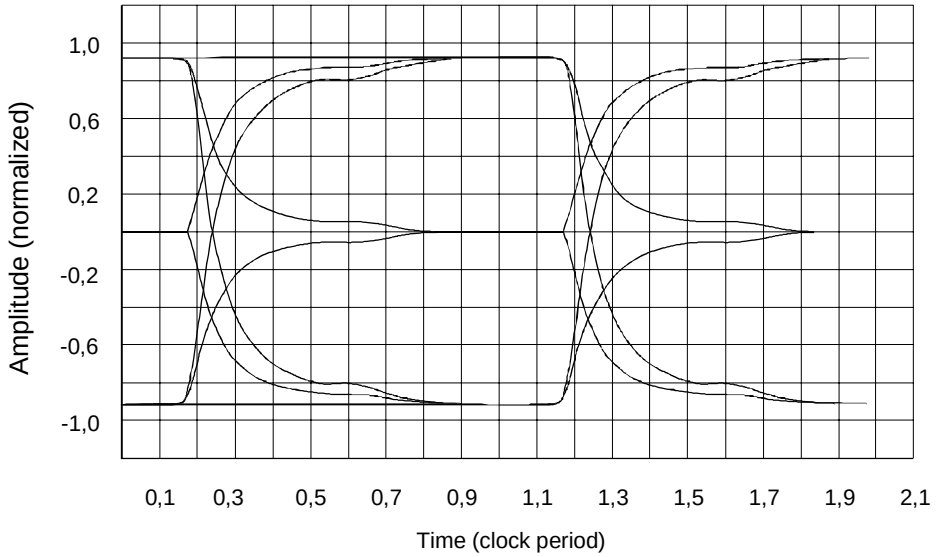


Figure 7: Waveform for test configuration ii) - short passive bus with eight clustered TEs at the far end (C = 120 nF/km)

9.2.3 Total phase deviation input to output

The total phase deviation (including effects of timing extraction jitter in the TE), between the transitions of signal elements at the output of the TE and the transitions of signal elements associated with the signal applied to the TE input, should not exceed the range of -7 % to +15 % of a bit period. This limitation applies to the output signal transitions of each frame with the phase reference defined as the average phase of the crossing of zero, which occurs between the framing pulse and its associated balance pulse at the start of the frame and corresponding crossings at the start of the three preceding frames of the input signal.

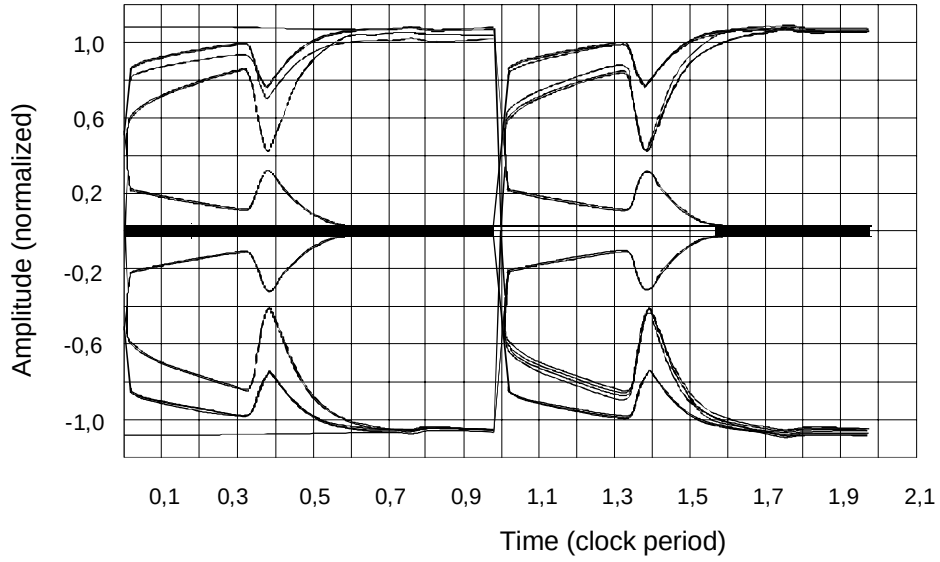


Figure 8: Waveform for test configuration iii) a) - short passive bus with one TE near to NT, and seven TEs at the far end (C = 120 nF/km)

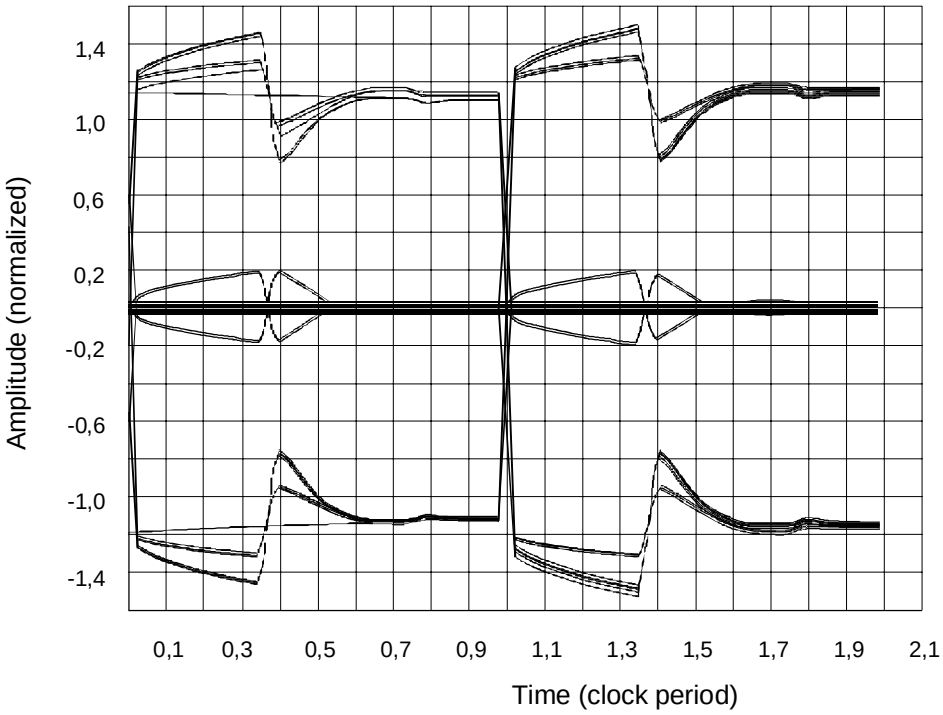


Figure 9: Waveform for test configuration iii) b) - short passive bus with one TE near to NT, and seven TEs at the far end (C = 30 nF/km)

For the purpose of demonstrating compliance of an equipment, it is sufficient to use (as the input signal phase reference) only the crossing of zero volts between the framing pulse and its associated balance pulse of the individual frame. This latter method, requiring a simpler test set, may create additional jitter at frequencies higher than about 1 kHz and is therefore more restrictive. The limitation applies to the phase

of the zero-volt crossings of all adjacent ZEROs in the output data sequence, which shall be as defined in subclause 9.2.2. The limitation applies under all test conditions described in subclause 9.2.1, with the additional input signal conditions specified in a) to d) below, and with the superimposed jitter as specified in figure 10 over the range of frequencies from 5 Hz to 2 kHz. The limitation applies for input bit rates of 192 kbit/s ± 100 ppm.

a) A sequence consisting of continuous frames with all ONEs in the D-, D-echo and both B-channels;
b) A sequence consisting of continuous frames with the octet "10101010" (the first bit to be transmitted is y ONE) in both B-channels and ONEs in D- and D-echo channels;
c) A sequence of continuous frames with ZEROs in D, D-echo and both B-channels;
d) A sequence of continuous frames with a pseudo random pattern, as described in subclause 9.2.2 c), in D-, D-echo and both B-channels.

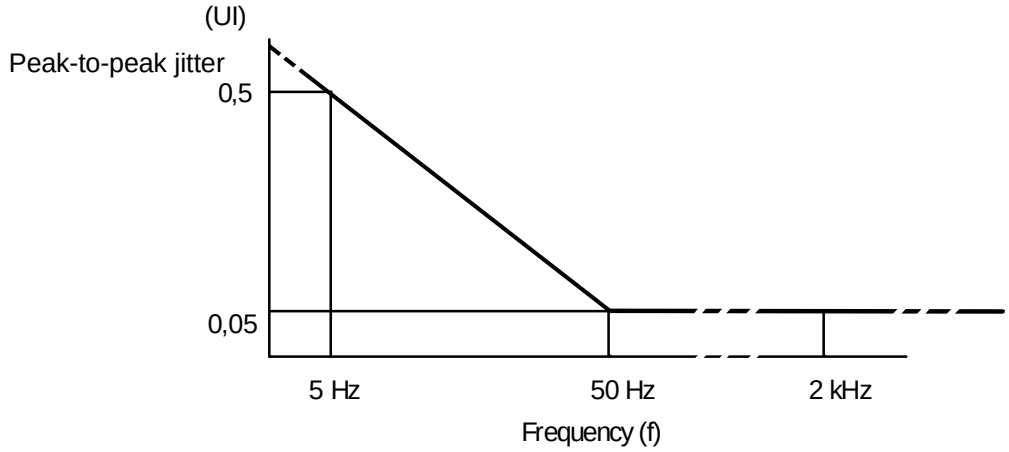


Figure 10: Lower limit of maximum tolerable jitter at TE input (log-log scale)

9.3 NT jitter characteristics

The maximum jitter (peak-to-peak) in the output sequence of an NT shall be 5 % of a bit period when measured using a high pass filter having a cut-off frequency (3 dB point) of 50 Hz and an asymptotic roll off of 20 dB per decade. The limitation applies for all data sequences, but for the purpose of demonstrating the compliance of an equipment, it is sufficient to measure jitter with an output data sequence consisting of ONEs in D- and B-channels and with an additional sequence as described in subclause 9.2.2 c) in D- and B-channels. The limitation applies to the phase of all zero-volt crossings of all adjacent ZEROs in the output data sequence.

9.4 Termination of the line

The interchange circuit pair termination (resistive) should be 100 Ω ± 5 % (see figure 2).

9.5 Transmitter output characteristics

9.5.1 Transmitter output impedance

The following requirements apply at interface point I_A (see figure 2) for TEs and at interface point I_B for NTs (see subclauses 5.2.2 and 9.9 regarding capacitance of the cord).

9.5.1.1 NT transmitter output impedance

a) At all times except when transmitting a ZERO, the output impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the impedance indicated by the template in figure 11. This requirement is applicable with an applied sinusoidal voltage of 100 mV (rms value).

   NOTE: In some applications, the terminating resistor can be combined with the NT (see point B of figure 2). The resulting impedance is the impedance needed to exceed the combination of the template and the 100 Ω termination.

b) When transmitting a ZERO, the output impedance shall be ≥ 20 Ω.

The output impedance limit shall apply for the 50 Ω nominal load condition. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10 %. The peak amplitude is defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

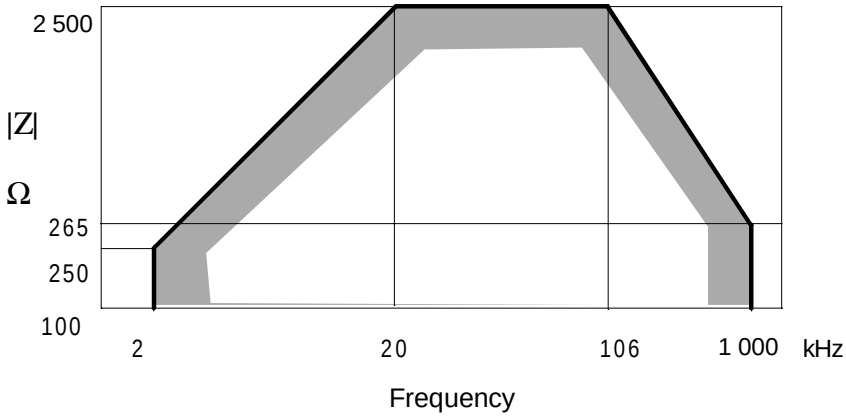


Figure 11: NT impedance template (log-log scale)

9.5.1.2 TE transmitter output impedance

a) At all times except when transmitting a ZERO, the following requirements apply:

i) The output impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the impedance indicated by the template in figure 12. This requirement is applicable with an applied sinusoidal voltage of 100 mV (rms value).

ii) At a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1,2 V (peak value) shall not exceed 0,6 mA (peak value).

b) When transmitting a ZERO, the output impedance shall be ≥ 20 Ω.

The output impedance limit shall apply for two nominal load impedance (resistive) conditions : 50 Ω and 400 Ω. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10 %. The peak amplitude is defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

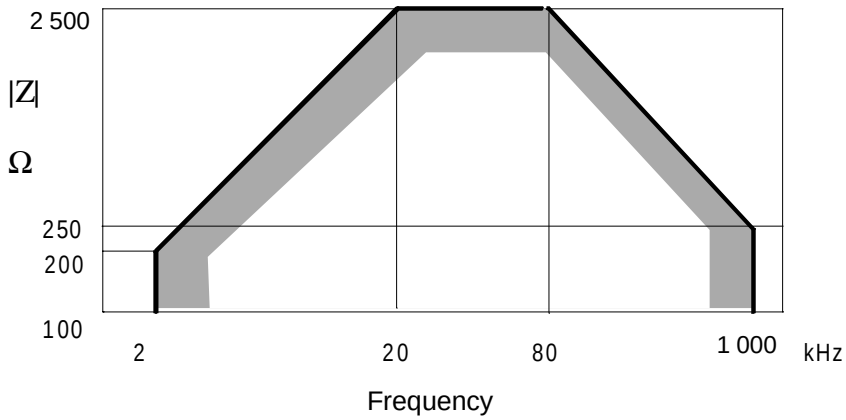


Figure 12: TE impedance template (log-log scale)

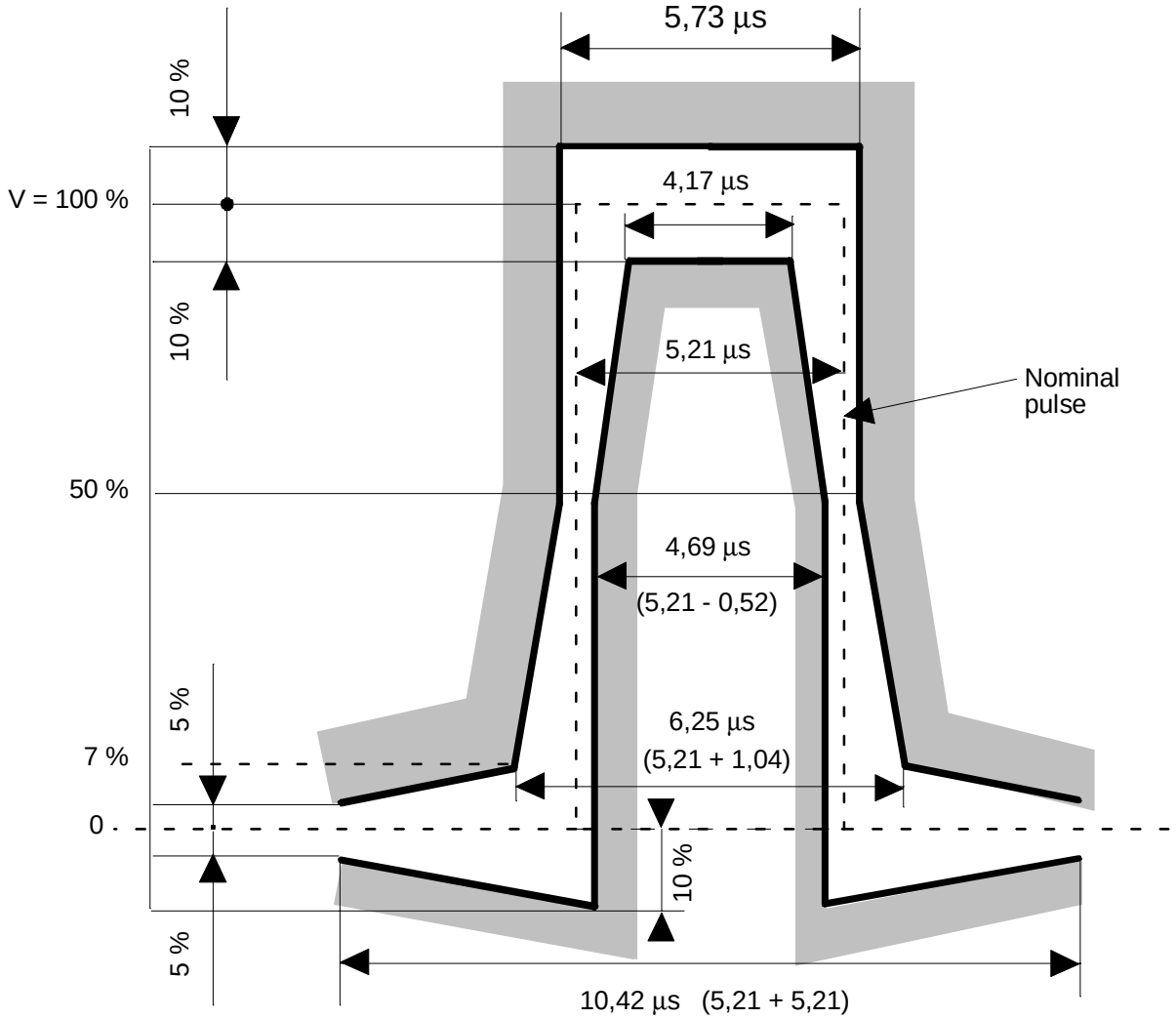
9.5.2 Test load impedance

The test load impedance shall be 50 Ω (unless otherwise indicated).

9.5.3 Pulse shape and amplitude (binary ZERO)

9.5.3.1 Pulse shape

Except for overshoot, limited as follows, pulses shall be within the mask of figure 13. Overshoot, at the leading edge of pulses, of up to 5 % of the pulse amplitude at the middle of a signal element, is permitted, provided that such overshoot has, at 1/2 of its amplitude, a duration of less than 0,25 µs.



NOTE: For clarity of presentation, the above values are based on a pulse width of 5,21 ms. See subclause 9.1 for a precise specification of the bit rate.

Figure 13: Transmitter output pulse mask

9.5.3.2 Nominal pulse amplitude

The nominal pulse amplitude shall be 750 mV, zero to peak.

A positive pulse (in particular, a framing pulse) at the output port of the NT and TE is defined as a positive polarity of the voltage measured between access leads e to f and d to c respectively (see figure 20). (See table 12 for the relationship to connector pins.)

9.5.4 Pulse unbalance

The unbalance may be consequence of integrated circuits tolerance or circuit design but also the consequence of the dynamic behaviour of the power feeding circuit of the transmitter which may result in a pattern dependent pulse amplitude.

9.5.4.1 Pulse amplitude when transmitting a high density pattern

For both positive and negative pulses, two thresholds are set, corresponding to the minimum and maximum amplitude defined by the pulse mask (nominal amplitude ± 10 %).

When transmitting 40 frames with continuous ZERO in at least both B-channels into a test load of 50 Ω the pulse amplitude in the middle of the pulse shall be within the threshold as given in figure 13.

9.5.4.2 Pulse unbalance of an isolated couple of pulses

The absolute sum of $\int U(t)dt$ for a positive pulse (one bit) and $\int U(t)dt$ for a negative pulse (one bit) shall be < 5 % of the nominal pulse. Therefore the reference voltage is given by the signal when transmitting INFO 0. the edge between two adjacent pulses shall be the crossing of the zero voltage. From this edge the integral shall be defined for a time period of 1,5 UI in each direction.

For TEs the conformance test shall be performed with the first frame INFO 3 containing all ONEs in both B-channels and in the D-channel following INFO 0.

For NTs the conformance test shall be performed with the signal INFO 4. In the B1-channel two alternated octets 1111 1111 and 1111 1100 shall be inserted so that the two ZEROs are set in the bit position 33 and 34 (see table 3). All B2-, D- and E-bits shall be set to ONE.

9.5.5 Voltage on other test loads (TE only)

The following requirements are intended to assure compatibility with the condition where multiple TEs are simultaneously transmitting pulses on a passive bus.

9.5.5.1 400 Ω load

A pulse (ZERO) shall conform to the limits of the mask shown in figure 14 when the transmitter is terminated in a 400 Ω load to prevent pulses adding when 2 to 8 drivers are in parallel.

9.5.5.2 5,6 Ω load

To limit the current flow with two drivers having opposite polarities, the pulse amplitude (peak) with a 5,6 Ω load shall be ≤ 20 % of the nominal pulse amplitude.

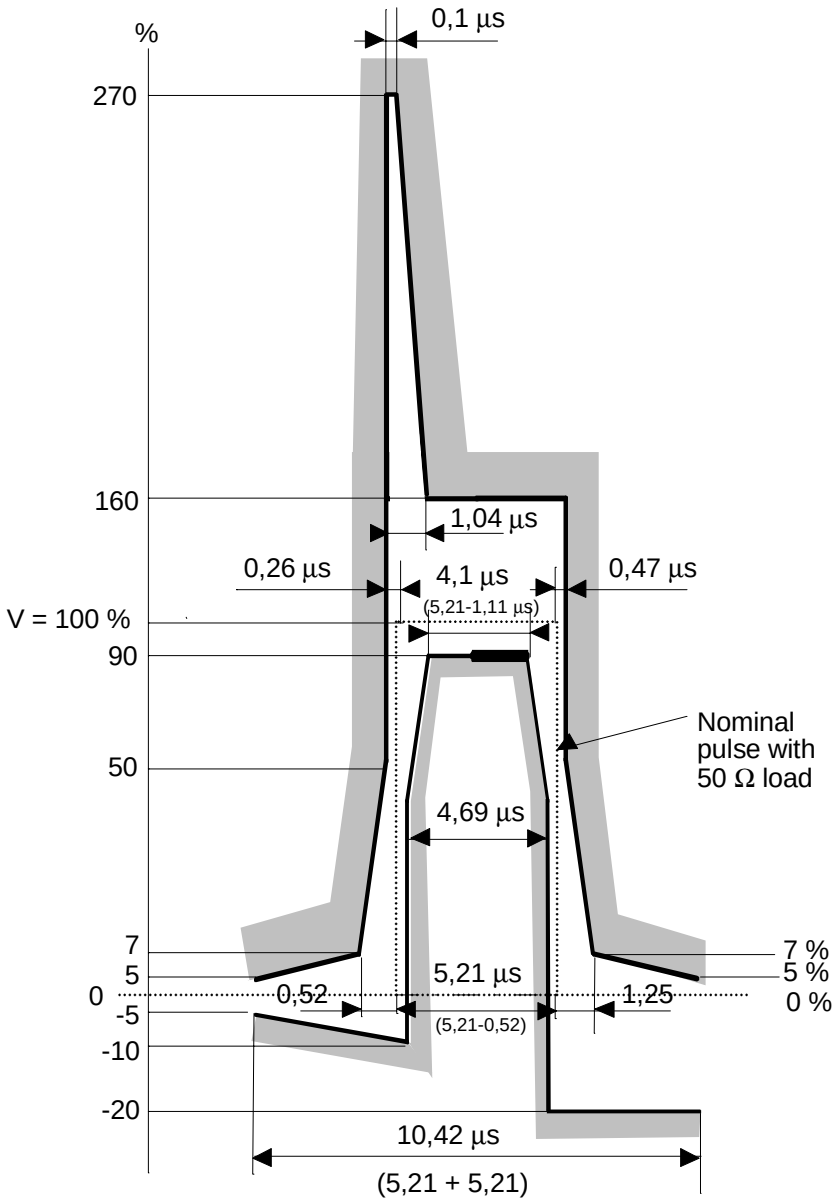
9.5.6 Unbalance about earth

The following requirement applies under all possible power feeding conditions, under all possible connections of the equipment to ground, and with two 100 Ω terminations across the transmit and receive ports.

9.5.6.1 Longitudinal conversion loss

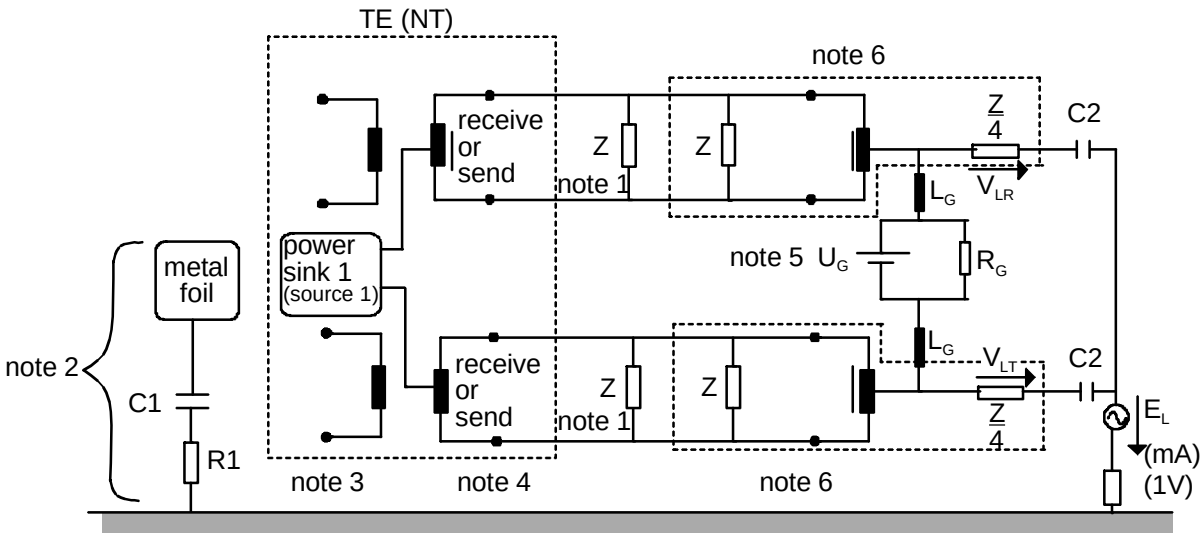
Longitudinal conversion loss (LCL) which is measured in accordance with CCITT Recommendation G.117 [9], § 4.1.3 (see figure 15), shall meet the following requirements:

a) 10 kHz ≤ f ≤ 300 kHz: ≥ 54 dB
b) 300 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB at 20 dB/decade.



NOTE: For clarity of presentation, the above values are based on a pulse width of 5,21 ms. See subclause 9.1 for a precise specification of the bit rate.

Figure 14: Voltage for an isolated pulse with a test load of 400 Ω



C1 = 200 pF $L_G \geq 50$ mH $Z = 100\ \Omega$

C2 = 10 μF R1 = 500 Ω $\frac{Z}{4} = 25\ \Omega$

The longitudinal conversion loss (LCL):

$$LCL = 20\log_{10}\left|\frac{E_L}{V_T}\right| \text{ dB}$$

The voltages V_T and E_L should be measured within the frequency range from 10 kHz up to 1 MHz using selective test measuring equipment.

The measurement should be carried out in the states:

- deactivated (receive, send);
- power off (receive, send);
- activated (receive).

The interconnecting cord shall lie on the metal plate.

NOTE 1: This resistor shall be omitted if the termination is already built into the TE (NT).

NOTE 2: Hand imitation is a thin metal foil approximately the size of a hand.

NOTE 3: TE (NT) with a metallic housing shall have a galvanic connection to the metal plate. Other TE (NT) with non-metallic housing shall be placed on the metal plate.

NOTE 4: The power cord for mains-powered TE (NT) shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

NOTE 5: If there is no power source 1 in the NT, R_G and L_G are not required.

NOTE 6: This circuit provides a transverse termination of 100 Ω and a balanced longitudinal termination of 25 Ω. Any equivalent circuit is acceptable. However, for equivalent circuits given in CCITT Recommendation G.117 [9] , powering cannot be provided.

Figure 15: Receiver input or transmitter output unbalance about earth

9.5.6.2 Output signal balance

The output signal balance requirements are found in ITU-T Recommendation I.411 [1].

9.6 Receiver input characteristics

9.6.1 Receiver input impedance

9.6.1.1 TE receiver input impedance

TEs shall meet the same input impedance requirements as specified in subclause 9.5.1.2 a), i) and ii) for the output impedance, independently of the state of the terminal (F1 to F8).

9.6.1.2 NT receiver input impedance

a) NT without internal terminating resistor
At all times, the following requirements apply:

   i) the input impedance in the frequency range of 2 kHz to 1 MHz, should exceed the impedance indicated by the template in figure 11. This requirement is applicable with an applied sinusoidal voltage of 100 mV (rms value);
   ii) at a frequency of 96 kHz, the peak current which results from an applied voltage of up to 1,2 V (peak value) should not exceed 0,5 mA (peak value).

b) NT with internal 100 Ω terminating resistor (see point B of figure 2)
At all times, the following requirements apply:

   i) after the disconnection of the terminating resistor the requirements as given in a) shall be met.

9.6.2 Receiver sensitivity - Noise and distortion immunity

Requirements applicable to TEs and NTs for three different interface wiring configurations are given in the following sections. TEs and/or NTs shall receive, without errors (for a period of at least one minute), an input with a pseudo-random sequence (word length ≥ 511 bits) in all information channels (combination of B-channel, D-channel and, if applicable, the D-echo channel).

The receiver shall operate, with any input sequence, over the full range indicated by the waveform mask.

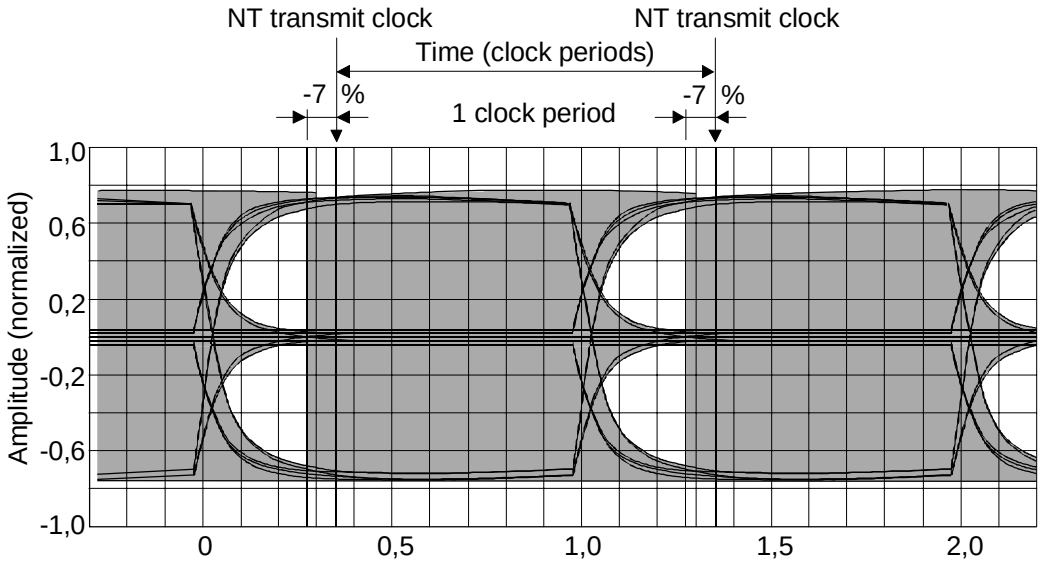
9.6.2.1 TEs

TEs shall operate with the input signals conforming to the waveforms specified in subclause 9.2.1. For the waveforms in figures 7 to 9, TEs shall operate with the input signals having any amplitude in the range of +1,5 dB to -3,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. For signals conforming to the waveform in figure 6, operation shall be accomplished for signals having any amplitude in the range of +1,5 dB to -7,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. In addition, TEs shall operate with signals conforming to each waveform with jitter up to the maximum permitted (see subclause 9.3) in the output signal of NTs superimposed on the input signals.

Additionally, for input signals having the waveform shown in figure 6, the TEs shall operate with sinusoidal signals having an amplitude of 100 mV (peak-to-peak value) at frequencies of 200 kHz and 2 MHz superimposed individually on the input signals along with jitter.

9.6.2.2 NTs for short passive bus (fixed timing)

NTs designed to operate with only short passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in figure 16. NTs shall operate, with the input signals having any amplitude in the range of +1,5 dB to -3,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2.



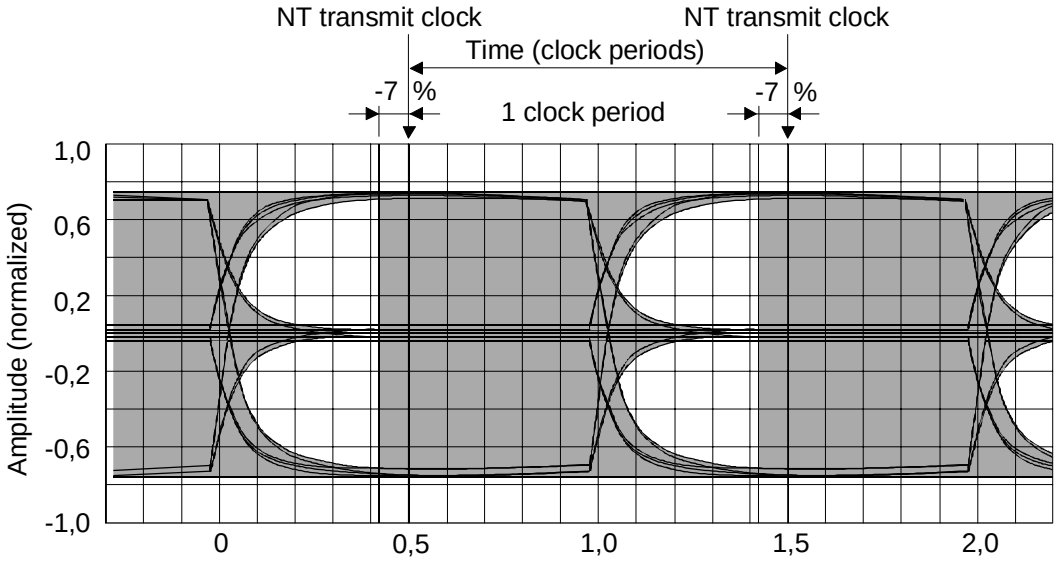
NOTE 1: Shaded area is the region in which pulse transitions may occur.

NOTE 2: The waveform mask is based on the "worst case" configuration shown in annex D. Figure D-1 and waveforms ii) and iii) in subclause 9.2.1. The shaded area of -7 % of one clock period accounts for the situation of a single TE connected directly to the NT with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

Figure 16: Short passive bus receive pulse waveform mask

9.6.2.3 NTs for both point-to-point and short passive bus configurations (adaptive timing)

NTs designed to operate with either point-to-point or short passive wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in figure 17. These NTs shall operate with the input signals having any amplitude in the range of +1,5 dB to -3,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. These NTs shall also operate when receiving signals conforming to the waveform in figure 6. For signals conforming to this waveform, operation shall be accomplished for signals having any amplitude in the range of +1,5 dB to -7,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in subclause 9.6.2.1, and with jitter up to the maximum permitted in the output signal of TEs (see subclause 9.2.2), superimposed on the input signals having the waveform in figure 6.



NOTE 1: Shaded area is the region in which pulse transitions may occur.

NOTE 2: The waveform mask is based on the same "worst case" passive bus configuration as the waveform mask in figure 16 except that the permitted round trip delay of the cable is reduced. The shaded area of -7 % of one clock period accounts for the situation of a single TE connected directly to the NT with a zero length passive bus. However, the waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

Figure 17: Passive bus receive pulse waveform mask
(NTs designed to operate with either point-to-point or short passive bus wiring configurations)

9.6.2.4 NTs for extended passive bus wiring configurations

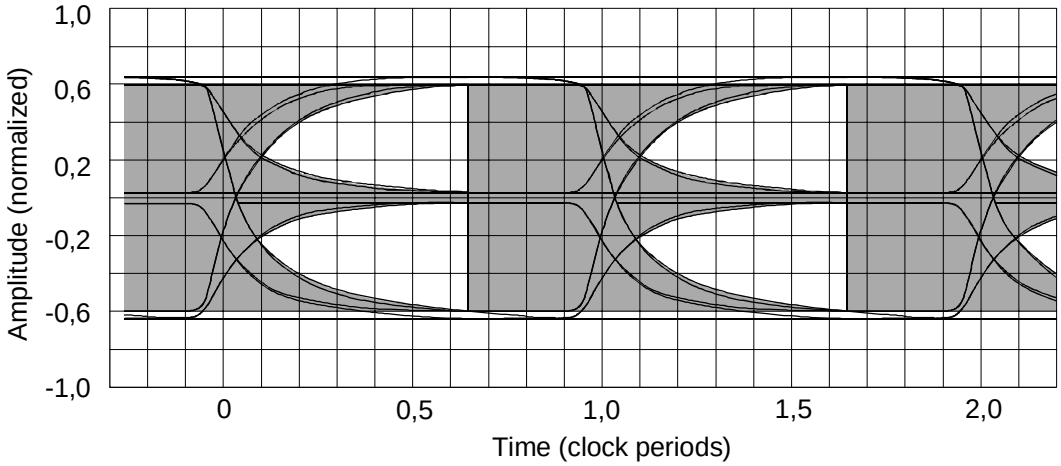
NTs designed to operate with extended passive bus wiring configurations shall operate when receiving input signals indicated by the waveform mask shown in figure 18. These NTs shall operate with the input signals having any amplitude in the range of +1,5 dB to -5,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in subclause 9.6.2.1, superimposed on the input signals having the waveform shown in figure 18. (The above values assume a maximum cable loss of 3,8 dB. NTs may be implemented to accommodate higher cable loss).

9.6.2.5 NTs for point-to-point configurations only

NTs designed to operate with only point-to-point wiring configurations shall operate when receiving input signals having the waveform shown in figure 6. These NTs shall operate with the input signals having any amplitude in the range of +1,5 dB to -7,5 dB relative to the nominal amplitude of the transmitted signal as specified in subclause 9.5.3.2. Additionally, these NTs shall operate with the sinusoidal signals, as specified in subclause 9.6.2.1, and with jitter up to the maximum permitted in the output signal of TEs (see subclause 9.2.2) superimposed on the input signals having the waveform shown in figure 6.

9.6.3 NT receiver input delay characteristics

NOTE: Round trip delay is always measured between the zero-volt crossings of the framing pulse and its associated balance bit pulse at the transmit and receive side of the NT (see also annex A).



NOTE 1: Shaded area is the region in which pulse transitions may occur.

NOTE 2: The waveform mask is based on the worst case extended passive bus wiring configuration. It consists of a cable having a characteristic impedance of 75 Ω, a capacitance of 120 nF/km, a loss of 3,8 dB at 96 kHz, with four TEs connected such that the differential delay is at the maximum permitted by subclause 9.6.3.3. The waveform mask does not show the higher possible amplitude of framing and D-channel bit pulses and their associated balancing bits. It should be noted that the above waveform mask does not account for transient effects.

Figure 18: Extended passive bus receive pulse waveform mask

9.6.3.1 NT for short passive bus

NTs shall accommodate round trip delays of the complete installation, including TEs, in the range 10 µs to 14 ms.

9.6.3.2 NT for both point-to-point and passive bus

NTs shall accommodate round trip delays (for passive bus configurations) in the range 10 µs to 13 µs.

NTs shall accommodate round trip delays (for point-to-point configurations) in the range 10 µs to 42 ms.

9.6.3.3 NT for extended passive bus

NTs shall accommodate round trip delays in the range 10 µs to 42 µs, provided that the differential delay of signals from different TEs is in the range 0 µs to 2 ms.

9.6.3.4 NT for point-to-point only

NTs shall accommodate round trip delays in the range 10 µs to 42 µs.

9.6.4 Unbalance about earth

Longitudinal Conversion Loss (LCL) of receiver inputs, measured in accordance with CCITT Recommendation G.117 [9], § 4.1.3, by considering the power feeding and two 100 Ω terminations at each port, shall meet the following requirements (see figure 15):

a) 10 kHz ≤ f ≤ 300 kHz: ≥ 54 dB;

b) 300 kHz < f ≤ 1 MHz: minimum value decreasing from 54 dB with 20 dB/decade.

9.7 Isolation from external voltages

These requirements are defined in ETS 300 047 [6].

9.8 Interconnecting media characteristics

Interface cables (or cabling) shall include twisted metallic pairs (two up to four as required). Such pairs are frequently part of the customers' distribution systems. The transmission characteristics of the transmit and receive pairs shall be such that satisfactory operation is assured when used to interconnect (I_A to I_B) equipment having interfaces conforming to the requirements of this ETS. Examples of cable systems parameters that shall be considered are loss, frequency response, crosstalk loss, longitudinal balance and noise. Note that cable characteristics assumed in defining the requirements specified in this ETS at interface point I_A and I_B are discussed in annex A and table B.1. Longitudinal balance, e.g. ≥ 43 dB at 96 kHz, is of particular importance to assure compliance with EMI limitations which shall also be considered in determining suitable interface cables.

9.9 Standard ISDN basic access TE cord

A connection cord for use with a TE designed for connection with a "standard ISDN basic access TE cord" shall have a maximum length of ten metres and shall conform to the following:

a) Cords having a maximum length of seven metres:
- the maximum capacitance of pairs for transmit and receive functions shall be less than 300 pF;
- the characteristic impedance of pairs used for transmit and receive functions shall be greater than 75 Ω at 96 kHz;
- the crosstalk loss, at 96 kHz, between any pair and a pair to be used for transmit or receive functions shall be greater than 60 dB with terminations of 100 Ω.
- The resistance R of an individual shall not exceed 3 Ω. The difference in the resistance of the conductors of a pair shall not exceed 60 mΩ + 0,04 R.
- cords shall be terminated at both ends in identical plugs (individual conductors shall be connected to the same contact in the plug at each end);

b) Cords having a length greater than seven metres:
- cords shall conform to the above requirements except that a capacitance of 350 pF is permitted;

TEs may be designed that include a connecting cord which is part of the TE. In this case the requirements for a standard ISDN basic access TE cord do not apply.

10 Power Feeding

10.1 Reference configuration

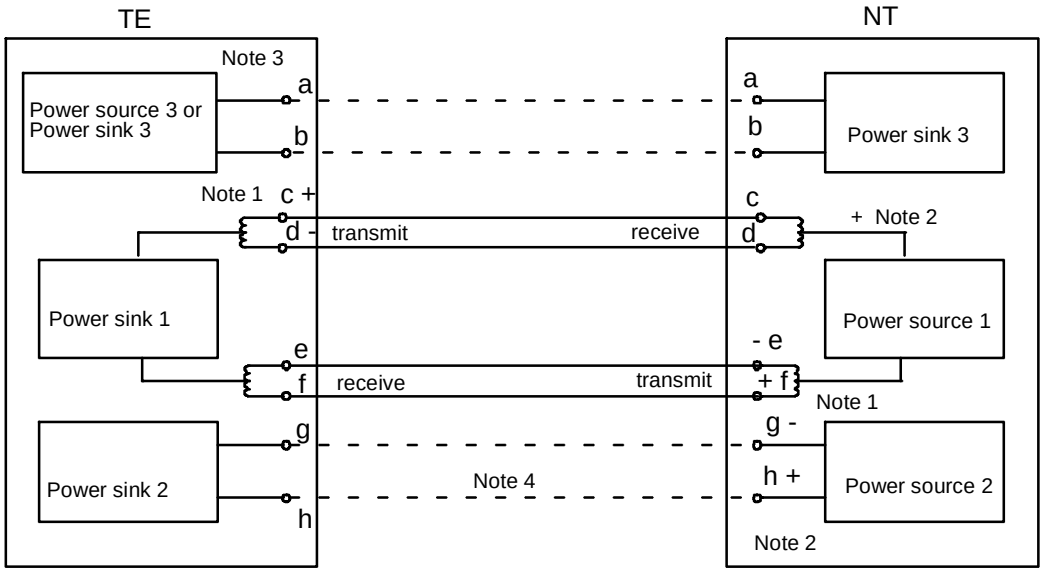
The reference configuration for power feeding, which is based on an eight pin interface connector, is described in figure 19. The access lead designations, "a" through "h", are not intended to reflect particular pin assignments, which as indicated in clause 11, are specified in EN 28877 [4]. The use of leads c, d, e, and f is mandatory. The use of leads a, b, g and h is optional.

This reference configuration allows unique physical and electrical characteristics, for the interface at reference points S and T, which are independent of the choice of internal or external power source arrangements.

Power source 1 may derive its power from the network and/or locally (mains and/or batteries). While the source for restricted power is an integral part of the NT, the source for normal conditions may be physically separate and may be connected at any point in the interface wiring. Note that such a separate source should be considered functionally part of the NT. However, the provision of such a source is subject to the approval of the Administration/network provider. To avoid interworking problems, it is not permitted to connect such a separate source of phantom mode power in wiring associated with NTs having an internal source for normal conditions. Where a separate source of phantom mode power is provided, its compatibility with a source for restricted power that is part of the associated NT shall be

assured by the provider of the separate source. In particular, the resolution of power contention, which may result from the provision of the separate source, between the separate source and a restricted power condition source internal to an NT, is not specified in this ETS and shall be taken into account. In addition, any effects of the transmission characteristics of interface cabling shall also be accounted for, e.g., the impedance of a power source that bridges the interchange circuit pairs may require a reduction in the number of TEs that can be accommodated on a passive bus.

Power source 2 derives its power locally (mains and/or batteries). Power source 2 may be located in (or associated with) the NT as indicated, or it may be located separately.



NOTE 1: This symbol refers to the polarity of framing pulses.

NOTE 2: This symbol refers to the polarity of power during normal power conditions (reversed for restricted conditions).

NOTE 3: The access lead assignments indicated in this figure are intended to provide for direct interface cable wiring, i.e. each interface pair is connected to a pair of access leads having the same two letters at TEs and NTs.

NOTE 4: Power source 2 may also be implemented as a separate device and attached to the interface wiring outside of NT.

NOTE 5: NT requiring remote power feeding from a TE via the interface shall implement a power sink.

NOTE 6: In TE-to-TE application remote power feeding of a TE from an other TE may be performed by application of power source 3.

Figure 19: Reference configuration for signal transmission and power feeding in normal operating mode

10.1.1 Functions specified at the access leads

The eight access leads for TE and NT shall be applied as follows:

i) Access lead pairs c-d and e-f are for the bidirectional transmission of the digital signal and may provide a phantom circuit for power transfer from NT to TE (power source 1);
ii) Access lead pair g-h may be used for additional power transfer from the NT to TE (power source 2);
iii) Access lead pair a-b may also be used for power transfer in TE-TE interconnection and power transfer from TE to NT (power source 3).

10.1.2 Provision of power sources and sinks

The provision of power source 1 (normal) is optional.

Optional in this case refers only to the responsibility of the network provider for the provision of power source 1. The capability of the provision of power source 1 shall always be available, either:

- as an integral part of the NT1; and/or

- physically separate and connected at any point in the interface wiring.

The provision of power source 1 (restricted) is mandatory.

Mandatory in this case refers only to the responsibility of the network provider for the provision of power source 1 (restricted) in a single basic access configuration. In the case of a multiple basic access to an NT2 configuration, power source 1 (restricted) shall be mandatory for at least one of the NT1 accesses.

In some cases the provision of power source 1 (restricted) can be guaranteed only for a limited period of time.

The provision of power source 2 is optional. The provision of power source 3 is outside the scope of this ETS.

Power sinks 1 and 2 are optional.

10.2 Power available from NT

10.2.1 Power source 1 normal and restricted mode

Power source 1 may provide either normal or restricted power conditions or both:

i) where power is provided under normal conditions, the power available from power source 1 is the responsibility of the individual administration/network provider. However, power source 1 together with any separate power source as described in subclause 10.1, shall provide at least the power for the consumption of 1 watt (the maximum specified in subclause 10.3.1 that a TE may draw) at TE interfaces. The power required to be available from the NT may depend upon the possible provision of a separate source and the cable configuration;

ii) under restricted power conditions, the minimum power available from power source 1 shall be 420 mW. When power source 1 enters a condition where it is able to supply only restricted power, it shall indicate this condition by reversing its polarity. In this condition, only the restricted power functions of TEs are allowed to consume power from power source 1;

iii) if power source 1 (and any separate source combination) can supply power in both normal and restricted power conditions, the change of condition of power source 1 from the normal to restricted power condition may occur when power source 1 (and any separate source combination) is unable to supply the "nominal" level of power. [The "nominal" level of power is defined as the minimum power that the power source 1 (or separate power source) is designed to supply]. In any case, the transition from normal to restricted condition shall occur when the power described in subclause 10.2.1 i) is not available from power source 1 (as a result of a loss of its source of power).

10.2.2 Minimum voltage at NT from power source 1

10.2.2.1 Normal power conditions

Under normal power conditions, the nominal value of the voltage of power source 1, if provided, at the output of the NT shall be 40 V and the tolerances shall be +5 % and -15 % when supplying up to the maximum available power.

10.2.2.2 Restricted power conditions

Under restricted power conditions, the nominal value of the voltage of power source 1, if provided, at the output of the NT shall be 40 V and the tolerances shall be +5 % and -15 % when supplying up to 420 mW.

10.2.3 Minimum voltage of power source 2

The nominal voltage of power source 2 (optional third pair) shall be 40 V. The maximum voltage shall be 40 V +5 % and the minimum voltage shall assure compliance with the requirements specified in subclause 10.3.2 concerning power available at a TE.

10.3 Power available at a TE

10.3.1 Power source 1 - phantom mode

10.3.1.1 Normal power conditions

Under normal power conditions, the maximum voltage at the interface of a TE shall be 40 V +5 % and the minimum voltage shall be 40 V - 40 % (24 V) when drawing up to the maximum permitted power consumption of 1 W.

10.3.1.2 Restricted power conditions

Under restricted power conditions, the nominal value of the voltage at the inputs of a TEs (from power source 1) shall be 40 V and the tolerance shall be +5 % and -20 % when drawing a power of up to 401 mW (380 mW for designated TEs and 21 mW for other TEs).

10.3.2 Power source 2 - optional third pair

10.3.2.1 Normal power conditions

Under normal power conditions, the voltage at the interface of a TE shall be a maximum of 40 V +5 % and a minimum of 40 V - 20 % when the TE is drawing a power of up to the minimum available power of 7 watts.

10.3.2.2 Restricted power conditions

When power source 2 is unable to provide 7 W, it goes to a restricted power condition (indicated by reversing its polarity) where it shall provide a minimum of 2 W. The provision of this restricted power conditions subject to the power source 2 provider’s assumed responsibility. The nominal value of the voltages at the inputs of the TEs shall be 40 V and the tolerance shall be +5 % and - 20 % when drawing a power of up to 2 W.

10.4 Power source 1 consumption

The different values concerning the TE power source 1 consumption are summarized in table 9.

10.4.1 Normal power conditions

Under normal power conditions and in the activated state, a TE which draws power from power source 1 shall draw no more than 1 W. When a TE is not involved in a call, it is desirable that it minimize its power consumption (see note below).

When in the deactivated state, a TE which draws power from power source 1 shall draw no more than 100 mW. However, if a local action has to be initiated in the TE when the interface is not activated, this TE shall enter a "local action" state.

In this "local action" state, the TE may consume up to 1 W, if the following conditions are assured:

- the corresponding power is provided by the NT (e.g. this service is supported by the NT);

- the "local action" state is not a permanent one. (Typical examples of the use of this state are the modification of prestored dialling numbers in the TE or setting the volume of the "ring-tone").

NOTE: The definition of "not involved in a call" mode may be based on the knowledge of the status of layer 2 (link established or not). When this limitation is applied in the design of a TE, a maximum value of 380 mW is recommended.

10.4.2 Restricted power conditions

10.4.2.1 Power Available to a TE "designated" for restricted power operation

A TE which is permitted to draw power from power source 1 under restricted power conditions shall consume no more than 380 mW. In restricted power conditions, a designated TE which is in low-power mode shall consume power from power source 1 only to maintain a line activity detector and to retain its Terminal Endpoint Identifier (TEI) value. The value of the low-power mode consumption shall be ≤ 25 mW.

Table 9: Summary of the different possible TE power source 1 consumptions

TE Type and state	Maximum consumption
Normal conditions	
TE drawing power from PS1 Active state	1 W
TE drawing power from PS1 Deactivated state	100 mW
TE drawing power from PS1 Local action state	1 W
Restricted conditions	
TE drawing power from PS1 Designated TE: Active state	380 mW
TE drawing power from PS1 Designated TE: Deactivated state	25 mW
TE drawing power from PS1 Not designated	0 mW (note)
TE drawing power from PS1 Designated: Local action state	380 mW
Locally powered TE using connected detector: Any state	3 mW
Locally powered TE not using connected detector: Any state	0 mW (note)
NOTE: See subclause 10.4.2.2.	

10.4.2.2 Power available to "non-designated" TEs

TEs not powered from power source 1 having a disconnection detector which utilizes the phantom voltage shall not draw more than 3 mW from the interface.

TEs not powered from power source 1 not having a disconnection detector which utilizes the phantom voltage and non-designated TEs which are normally powered from power source 1 (normal conditions) shall not consume any power from power source 1 in restricted power conditions.

NOTE: Permitted leakage current is defined in subclause 10.6.1.

10.5 Galvanic isolation

TEs that provide power sinks 1 or 2 shall provide galvanic isolation between power sources 1 and 2 and the earths of additional sources of power and/or of other equipment. Isolation shall be a minimum of 1 MΩ when measured at 500 V dc between an interface conductor and any one of the following points:

- AC mains earth;
- all pins of any external interfaces;
- or any conductive surface.

Equipment shall also comply with the applicable IEC safety specifications. (This provision is intended to preclude earth loops or paths which could result in currents that would interfere with the satisfactory operation of the TE. It is independent of any requirement, for such isolation, related to safety which may result from the study under way in IEC-ACOS/TES. It shall not be interpreted to require isolation which conflicts with necessary provision for safety).

10.6 Current transient

The rate of change of current drawn by a TE from power source 1 shall not exceed 5 mA/µs.

This requirement is not applicable during 100 ms or a time C according to figure 20 as elapsed (see also annex C) after the connection of the terminal.

10.6.1 Current/time limitations for TEs

To limit the current that each terminal can sink from the phantom circuit when connected to power source 1 in the normal power condition, or when power source 1 changes from restricted to normal condition, the terminal shall conform to the mask given in figure 20, with the values given in table 10, when tested in accordance with figure 21 (for TEs designed to minimize power disturbance see subclause 10.6.2).

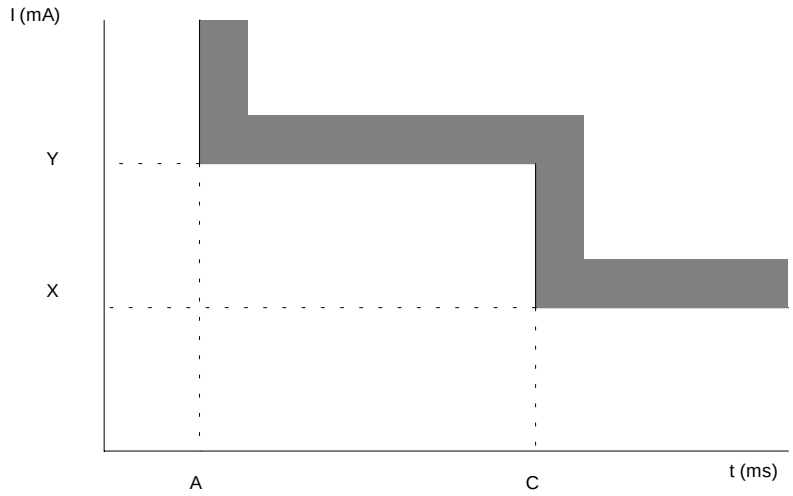


Figure 20: Current/time limitations for TEs

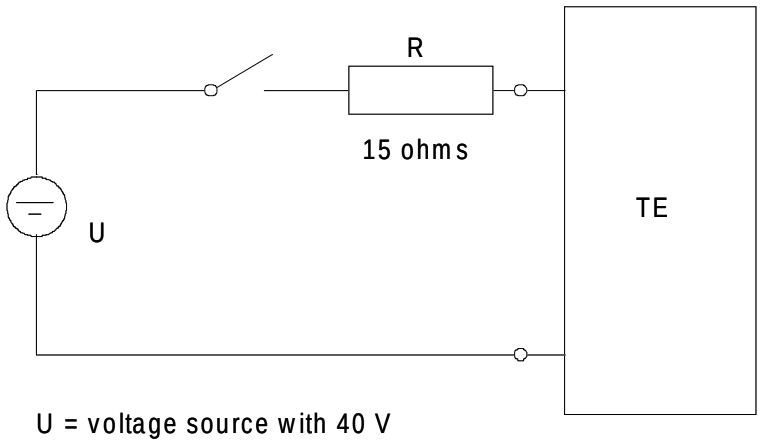


Figure 21: Test circuit to figure 21

Table 10: Parameters for the normal condition

A	5 µs	Y	55 mA
C	100 ms	X	Current equivalent to 1 Watt never exceeding 55 mA independent of the input voltage

To limit the current that a designated terminal can sink from the phantom circuit when connected to power source 1 in the restricted condition, a designated terminal shall conform to the mask given in figure 20, with the values given in table 11, when tested in accordance with figure 21.

Table 11: Parameters for the restricted condition

A	5 µs	Y	55 mA
C	100 ms	X	Current equivalent to 380 mW never exceeding 55 mA independent of the input voltage

To limit the current that a non-designated terminal can sink from the phantom when connected to power source 1 in the restricted condition a non-designated terminal shall conform to the values given below, when tested in accordance with figure 21.

The power consumption for TEs with connection detector when measured 100 µs after closing the switch shall be ≤ 3 mW.

These TEs shall not assume disconnection (transition from any of the states F2 to F8 to state F1) until the voltage of the interface has remained below 24 V for at least 500 ms.

The current consumption for TEs without connection detector when measured 100 µs after closing the switch shall be ≤ 10 µA.

NOTE: The total effective capacitance at the power source 1 input to the TE is expected to be less than 100 µF under all conditions of normal operation, startup and switch-over between normal and restricted mode, or vice versa.

10.6.2 TE designed to minimize power disturbance

To improve the performance of a TE for power transient conditions (connection, switch-on and switch-over between normal and restricted power conditions), consideration should be given to further limit the TE transient current within the mask given in subclause 10.6.1. By appropriate design of the TE, the transient current can be effectively eliminated, keeping its value below the steady-state current drawn by the TE.

10.6.2.1 Optimized current/time mask

For the first alternative the revised current/time mask is shown in figure 22 for normal mode and in figure 23 for restricted mode.

Other TE requirements would remain unchanged, except that the maximum effective capacitance limit should be reduced from 100 µF to 2 µF.

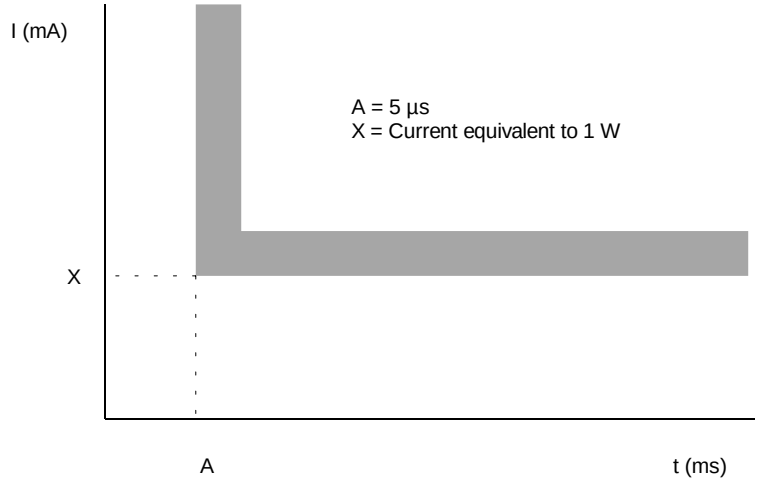


Figure 22: Current/time limitation for TE in normal mode

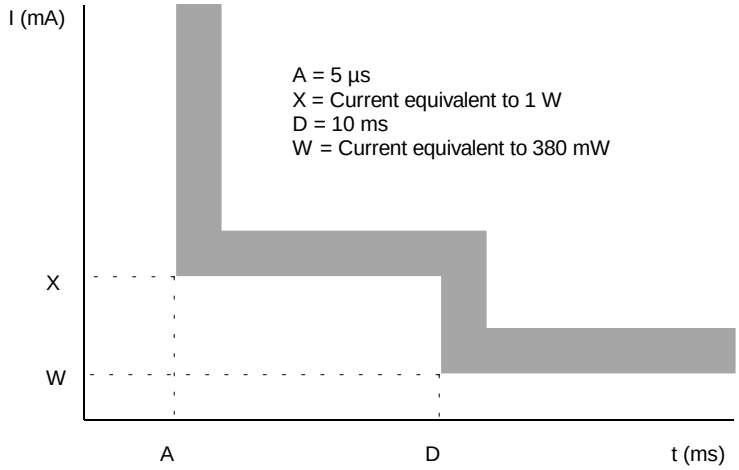


Figure 23: Current/time limitation for TE in restricted mode

NOTE 1: The 2 µF limit is for capacitance measured directly at the PS 1 input to the TE.

NOTE 2: Additional capacitance required to meet the holdover requirements has to be implemented so that it can still provide power for the dc-to-dc converter when needed. A possible implementation is suggested in figure 24.

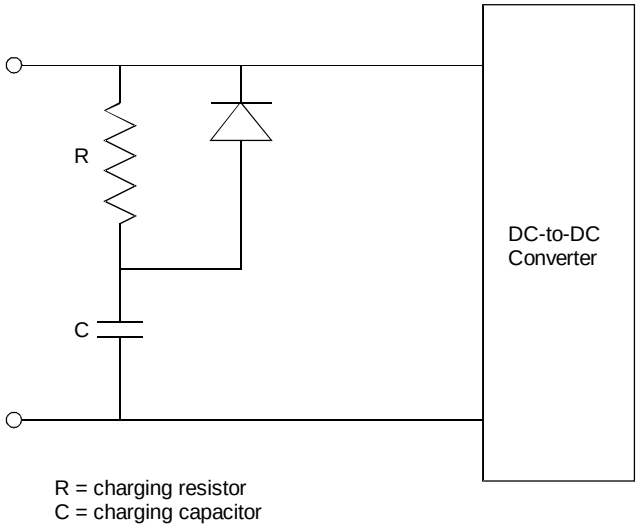


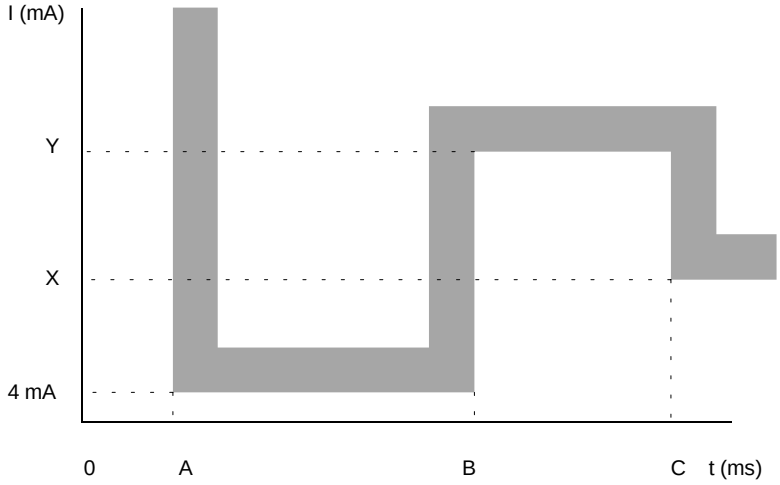
Figure 24: TE holdover capacity

The TE discussed above will be fully capable of interworking with the power source as described in subclause 10.6.5. TEs meeting either specified limit can therefore be mixed within the same network and will provide basic functionality.

Furthermore, if all TEs connected to a given NT1 comply with the limits given in clause 10, then all TEs will potentially offer improved functionality during transient conditions. In addition, some of the power source requirements listed in subclause 10.6.5 can be simplified although in this case the power source may reduce interworking capability with terminals following the template given in subclause 10.6.1. Exact details of the revised power source requirements are for further study.

10.6.2.2 Alternative current/time mask for optimized TEs

For the second alternative the revised current/time mask is shown in figure 25.



A = 5 µs
5 µs ≤ B < 900 ms
C = B + 100 ms
X, Y: see tables 10 and 11

Figure 25: Alternative current/time limitation for TEs

The current drawn should conform to the mask given in figure 25.

In this case the current consumption during the waiting period (time between A and B) is limited to 4 mA. The maximum time between A and C is 1 s.

10.6.3 Power source switch-over

10.6.3.1 Power source switch-over time

when changing from normal to restricted mode, or from restricted to normal mode, the transition of the voltage between + 34 V and - 34 V (or vice versa) shall be less than 5 ms. This time is measured with fixed resistive loads, for both normal and restricted power condition, connected to the source, with diodes where necessary. The values of the resistors shall be chosen so that the load draws 420 mW in restricted and n x 1 Watt in normal condition when the source voltage is at its nominal operating value.

10.6.3.2 Restricted mode power source requirements under overload conditions

After the switch-over from normal mode to the restricted mode the power source shall provide a minimum current of 9 mA when the voltage is forced to a level below 1 V (overload condition).

After the switch-over from normal mode to the restricted mode the power source shall be able to provide a minimum current of 11 mA when the source voltage is forced to 34 V.

For conformance test purposes the current shall be measured with a load resistor applied for at least 1 second.

10.6.4 Other TE requirements

10.6.4.1 Minimum TE start-up current

A TE designed to operate in restricted power mode shall be able to reach operational condition. In order to check the operational condition INFO 2 is fed permanently at the input of the TE. Operational condition is considered to be reached when the TE starts to send INFO 3. This shall occur when connected to the test circuit given in figure 26, using the parameters given in table 12.

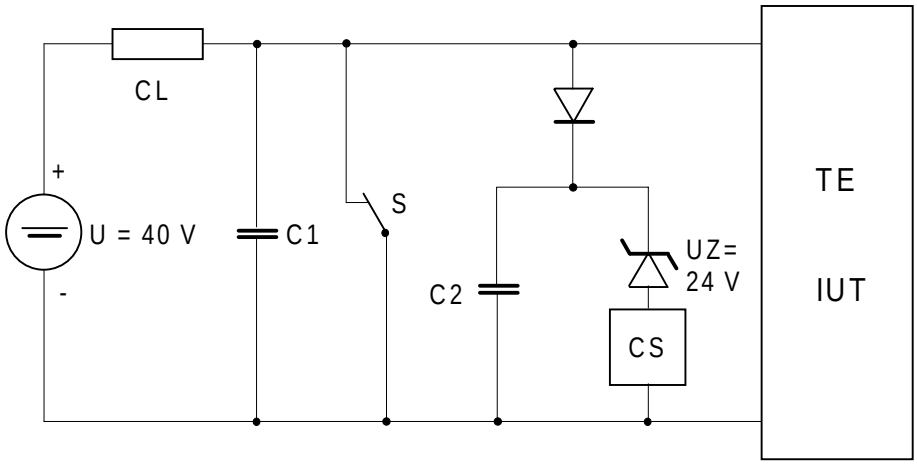
Table 12: parameters for restricted mode

Test a	CL = 9 mA	C1 = 0 µF	C2 = 0 µF	CS = 0 mA
Test b	CL = 11 mA	C1 = 300 µF	C2 = 0 µF	CS = 0 mA
CL: current limitation CS: current sink				

A TE designated to operate in normal power mode shall be able to reach operational condition. In order to check the operational condition INFO 2 is fed permanently at the input of the TE. Operational condition is considered to be reached when the TE starts to send INFO 3. This shall occur when connected to the test circuit given in figure 26, using the parameters given in table 13.

Table 13: Paramenters for normal mode

Test a	CL = 72 mA	C1 = 0 µF	C2 = 300 µF	CS = 45 mA
Test b	CL = 72 mA	C1 = 300 µF	C2 = 300 µF	CS = 45 mA
CL: current limitation CS: current sink				



NOTE: UZ is the Zener voltage.

Figure 26: Power start-up test for TE

The test is to be performed with the given parameters for the restricted and the normal mode respectively if applicable. before starting each test, capacitor C2 shall be discharged and switch S shall be closed.

The switch is then opened to allow the TE to power up.

10.6.4.2 Protection against short term interruptions

A TE shall not lose an on-going communication when the provision of power in normal or restricted power mode is interrupted for ≤ 5 ms.

10.6.4.3 Behaviour at the switch-over

A designated TE being in normal mode may change to the restricted mode including power power consumption limitation immediately after detection of an interruption of power (in order to protect an on-going communication by reducing its power consumption).

When the change from normal mode with 32 V to the restricted mode occurs, the designated TE shall not lose an established call when the power source for the restricted mode provides an open circuit voltage of 40 V with a limited current of 11 mA. The TE shall be able to reach the steady state which allows the power source to leave the current limiting condition.

A designated and activated TE being in restricted mode and detecting transition to normal mode shall not change its power consumption limit (380 mW) to 1 W before 500 ms after detection of the reversed polarity.

10.6.5 Other power source requirements

10.6.5.1 Power source 1 restricted

The power source shall be able to increase the output voltage from 1 V to 34 V within 1,5 s, within 10 s after removal of a short circuit applied for up to 30 minutes, at its output with a test load of 100 µF connected to it.

10.6.5.2 Power source 1 normal

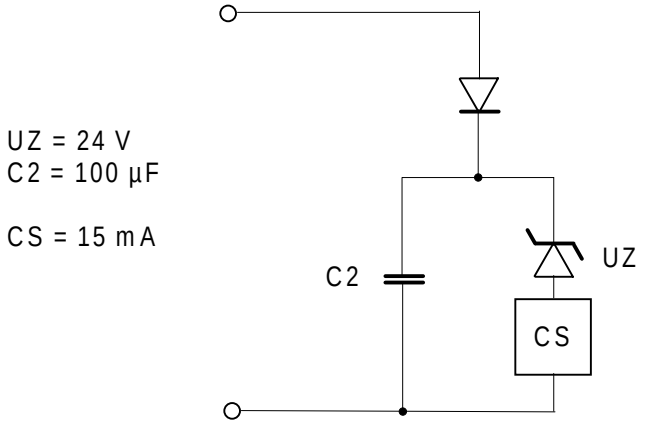
Two alternative power source implementations concerning overload and short-circuit protection were taken into account:

a) sources limiting the output current (fall back characteristic);

b) sources with switch off/switch on characteristic.

10.6.5.3 Requirements for type (a) sources

The power source shall be able to increase the output voltage from 1 V to 34 V within 350 ms, within 10 s after removal of a short circuit applied for 30 minutes, at its output with a test load of n times the TE equivalent (as defined in figure 27) connected to it (with the lowest acceptable voltage level at the mains interface of power source 1).



NOTE: UZ is the Zener voltage.

Figure 27: TE equivalent

10.6.5.4 Requirements for both types of sources

It should be noted that in the following subclauses the term n is used for the maximum number of terminals to be fed via the interface.

10.6.5.4.1 Switch-on surge capability

When switching power on to the interface, or after the change from restricted to normal condition, the power source 1 shall provide a minimum current of n times 45 mA for at least 100 ms and the voltage shall be at least 30 V during this time period. After the time of 100 ms, the power source shall be able to provide the power of n times 1 W and the power drop on the interface with the output voltage within the specified limits.

10.6.5.4.2 TE connection surge capability

Power source 1 normal shall be able to provide, for at least 100 ms, an additional current of 50 mA when the constant current drawn from the source was (n - 1) times 30 mA before this current surge and shall be n times 30 mA after it. The output voltage shall not drop below the minimum value of 34 V during the test.

10.7 Current unbalance

10.7.1 Direct current unbalance

The unbalanced maximum direct current flowing in the transformer windings can be caused by:

a) resistance unbalance of the transformer circuit of NTs;

b) resistance unbalance of the transformer circuit of TEs having power sink 1;

c) differential resistance in a pair of the installation wiring.

10.7.1.1 dc unbalance of power source 1

The direct current unbalance (X) of the power source 1 shall be less than 3 % of the current I ($I_1 + I_2$) flowing through both phantom pairs when the maximum power provided by power source 1 is drawn.

Conformance shall be demonstrated with a test circuit as shown in figure 28 with resistors R (2 Ω) to simulate a minimum equivalent of the TE cord and the installation.

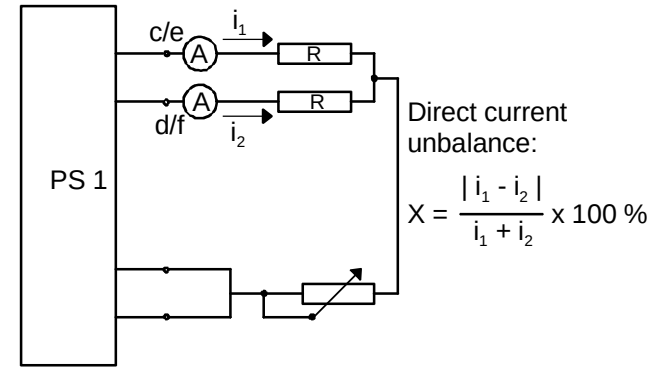


Figure 28: Test circuit for power source 1 dc unbalance measurement

10.7.1.2 dc unbalance of power sink 1

The direct current unbalance (X) of the power sink 1 shall be less than 3 % of the current i ($i_1 + i_2$) flowing through both phantom pairs.

Conformance shall be demonstrated with a test circuit as shown in figure 29.

The resistor R (2 Ω) represent the TE cord equivalent. When the TE under test is not provided with a cord, a cord having an ohmic resistance of at least 2 Ω per conductor shall be used.

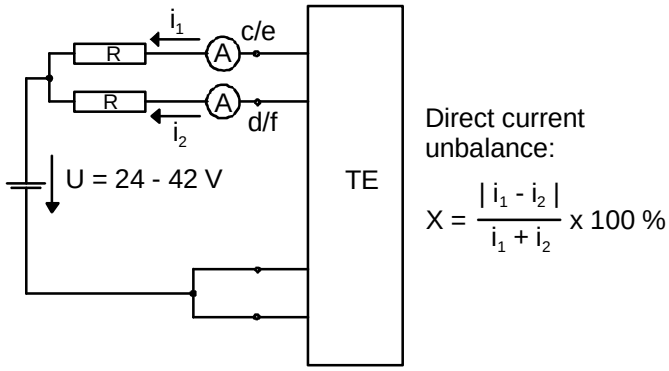


Figure 29: Test circuit for power sink 1 dc unbalance measurement

10.7.1.3 Differential resistance in a pair of the installation wiring

The difference of the ohmic resistance of the conductors of a pair shall be less than 3 % of the ohmic loop resistance of that pair, if the loop resistance is greater than 5 Ω.

10.7.2 Current unbalance in a pair

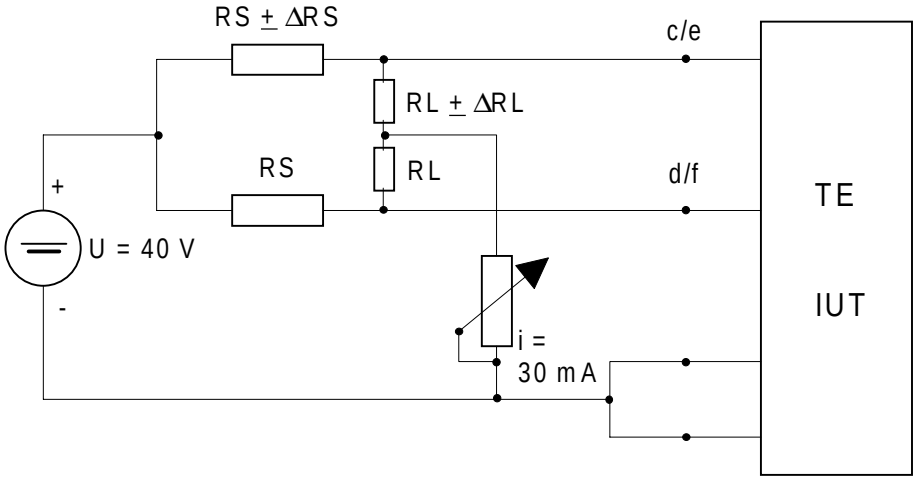
A TE shall meet the specified electrical characteristics when an external current unbalance of X = 3 % is applied to its transformer.

Conformance shall be demonstrated with the test configuration as given in figure 30.

The impedance of the receiver and transmitter shall exceed the impedance indicated by the template in figure 12 in the frequency range of 2 kHz to 20 kHz.

An NT shall meet the specified electrical characteristics as given in figure 11 measured as defined in subclauses 9.5.1.1 and 9.6.1.2 in the frequency range of 2 kHz to 20 kHz, when an external dc unbalance of X = 3 % is adjusted and the maximum power provided by power source 1 is drawn.

NOTE: Wiring with different resistances unbalance (e. g. the use of existing wiring) may impose constraints on the application of the interface (i. e. limitation of the maximum number of Watts available from power source 1 via the interface).



RS = 6 Ω	DRS = 360 mΩ
RL = 5 Ω	DRL = 300 mΩ

$$X = \frac{\Delta RS}{2RS} = \frac{\Delta RL}{2RL}$$

Figure 30: Test circuit for applied current unbalance

10.8 Additional requirements for an APS

Unless stated otherwise, all power source 1 requirements for the normal power conditions apply.

10.8.1 Power available for an APS

The APS shall support n terminals, where n is an integer number greater than or equal to 1. The APS shall provide an output power of 1 Watt for each terminal supported, multiplied by a bus-wiring loading factor. The minimum loading factor is 1,1.

If the APS is to be capable of being connected at any interface point I_A on a short passive bus the required loading factor is at least 1,5. For a given loading factor the APS may support more terminals if connected in close proximity to the other terminals so that less power is consumed by the wiring.

10.8.2 APS switch-on time

When the APS switches power on to the interface (e. g. due to the application or restoration of its input power) or when first connected to the bus the voltage across the phantom at the APS output shall rise from 1 V to ≥ 34 V (but shall not exceed 42 V) within 2,5 ms and shall not fall below 34 V for a further period of 2,5 ms.

10.8.3 APS switch-off time

When the APS is no longer able to supply 34 V (for example when it no longer has its required input power) the voltage across the phantom at the APS output shall decay from 34 V to ≤ 1V within 2,5 ms (and shall not rise above 1 V within a further 2,5 ms when tested in isolation from the NT1).

In the case where the APS has battery back-up, a considerable delay may occur between loss of input power to the APS and APS switch-off. In this case the provision of a battery low indication is an acceptable alternative.

10.8.4 APS power consumption when off

The APS shall not consume more than 3 mW from power source 1 restricted mode when connected to the bus and the APS input power is not available.

10.8.5 Dynamic behaviour of an APS

The same requirements as for power source 1 normal located inside the NT1 also apply to an APS except that the APS shall meet the requirements for m = n + 1. The additional capability (equivalent to an additional terminal) allows for the support of n terminals plus the charge required to force the power source 1 restricted mode to back-off.

10.9 Additional requirements for NT1 restricted mode source for compatibility with an APS

The NT1, designed to be compatible with an APS, shall not have a power source 1 normal mode source.

Unless stated otherwise, all power source 1 requirements for the restricted mode source apply.

The APS can also be located inside the same physical equipment as a TE. in this case such a terminal shall not to be connected to a network that cannot support the APS (i. e. they do not have "Terminal portability").

10.9.1 Power source 1 restricted mode back-off

The power source 1 restricted mode source may have a detector to detect when the normal mode voltage appears on the phantom circuit and can switch-off the restricted mode source.

When a normal mode voltage appears at the interface point I_B the NT1 shall conform to the mask given in figure 20, with the values given in table 14, when tested in accordance with figure 21. In addition, a restricted mode load of 420 mW shall be connected to the NT1.

Table 14: Parameters for NT1 in restricted mode

A	5 µs	Y	45 mA
C	100 ms	X	Current equivalent to 3 mW never exceeding 45 mA independent of the input voltage

10.9.2 Power source 1 restricted mode power up

When the normal mode voltage at interface point I_B falls below 5 V, and before it falls to 2 V, the restricted mode source shall drive the phantom voltage into the restricted mode. The rise time from this voltage (2 V to 5 V) to ≤ - 34 V (but not below - 42 V) shall be < 2,5 ms. The power source 1 voltage shall be in the range of - 34 V to - 42 V during the following 2,5 ms.

10.9.3 NT1 power consumption from APS normal mode

When the phantom voltage at interface point I_B is within the voltage range 24 V to 42 V the NT1 shall consume ≤ 3 mW.

11 Interface connector contact

The interface connector and the contact assignments are defined in prEN 28 877 [4] and EN 41 001 [5]. For the transmit and receive leads, pole numbers 3 through 6, the polarity indicated is for the polarity of the framing pulses. For the power leads, pole numbers 1, 2, 7 and 8, the polarity indicated is for the polarity of the dc voltages under normal power conditions. See figure 20 for the polarity of the power provided in the phantom mode. In that figure, the leads that are lettered a, b, c, d, e, f, g and h, correspond with pole numbers 1, 2, 3, 6, 5, 4, 7 and 8, respectively.

Table 15: Pole (contact) assignments for 8-pole connections (plugs and jacks)

Pole number	Function		Polarity
	TE	NT	
1	Power source 3 or Power sink 3	Power sink 3	+
2	Power source 3 or Power sink 3	Power sink 3	-
3	Transmit	Receive	+
4	Receive	Transmit	+
5	Receive	Transmit	-
6	Transmit	Receive	-
7	Power sink 2	Power source 2	-
8	Power sink 2	Power source 2	+

Annex A (informative): Wiring configurations and round trip delay considerations used as a basis for electrical characteristics

A.1 Introduction

In clause 5, two major wiring arrangements are identified. These are point-to-point configuration and a point-to-multipoint configuration using a passive bus.

While these configurations may be considered to be the limiting cases for the definition of the interfaces and the design of the associated TE and NT equipments, other significant arrangements should be considered.

The values of overall length, in terms of cable loss and delay assumed for each of the possible arrangements, are indicated below.

Figure 2 is a composite of the individual configurations. These individual configurations are shown in this annex.

A.2 Wiring configurations

A.2.1 Point-to-multipoint

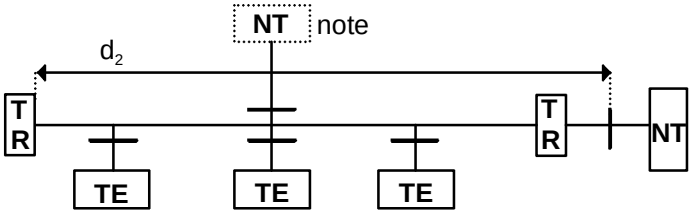
The point-to-multipoint wiring configuration identified in subclause 5.1.1 may be provided by the "short passive bus" or other configurations such as an "extended passive bus".

A.2.1.1 Short passive bus (Figure A.1)

An essential configuration to be considered is a passive bus in which the TE devices may be connected at random points along the full length of the cable. This means that the NT receiver should cater for pulses arriving with different delays from various terminals. For this reason, the length limit for this configuration is a function of the maximum round trip delay and not of the attenuation.

An NT receiver with fixed timing can be used if the round trip delay is between 10 to 14 μs. This relates to a maximum operational distance from the NT in the order of 100 - 200 metres (d_2 in figure A.1) [200 m in the case of a high impedance cable (Z_c = 150 Ω) and 100 m in the case of a low impedance cable (Z_c = 75 Ω)]. It should be noted that the TE connections act as stubs on the cable thus reducing the NT receiver margin over that of a point-to-point configuration. A maximum number of 8 TEs with connections of 10 m in length should be accommodated.

The range of 10 to 14 μs for the round trip delay is composed as follows. The lower value of 10 μs is composed of two bits offset delay (see figure 3) and the negative phase deviation of -7 % (see subclause 9.2.3). In this case the TE is located directly at the NT. The higher value of 14 μs is calculated assuming the TE is located at the far end of passive bus. This value is composed of the offset delay between frames of two bits (10,4 μs), the round trip delay of the unloaded bus installation (2 μs), the additional delay due to the load of TEs (i. e. 0,7 μs) and the maximum delay of the TE transmitter according to subclause 9.2.3 (15 % = 0,8 μs).



TR: Terminating Resistor

NOTE: In principle, the NT may be located at any point along the passive bus. The electrical characteristics in this Recommendation, however, are based on the NT located at one end. The conditions related to other locations require confirmation.

Figure A.1: Short passive bus

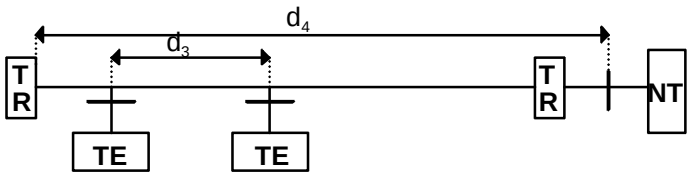
A.2.1.2 Extended passive bus (Figure A.2)

A configuration which may be used at an intermediate distance in the order of 100 to 1 000 metres is known as an extended passive bus. This configuration takes advantage of the fact that terminal connection points are restricted to a grouping at the far end of the cable from the NT. This places a restriction on the differential distance between TEs. The differential round trip delay is defined as that between zero-volt crossings of signals from different TEs and is restricted to 2 μs.

This differential round trip delay is composed of a TE differential delay of 22 % or 1,15 μs according to subclause 9.2.3, the round trip delay of the unloaded bus installation of 0,5 μs (line length 25 to 50 metres) and an additional delay due to the load of 4 TEs (0,35 μs).

The objective from this extended passive bus configuration is a total length of at least 500 metres (d_4 in figure A.2) and a differential distance between TE connection points of 25 to 50 metres (d_3 in figure A.2). (d_3 depends on the characteristics of the cable to be used.) However, an appropriate combination of the total length, the differential distance between TE connection points and the number of TEs connected to the cable may be determined by individual administrations.

NOTE: Round trip delay will normally be in the range of 10 to 26 μs. Where repeaters or amplifiers are utilized, 42 μs is the absolute maximum to ensure proper operation.



TR: Terminating Resistor

Figure A.2: Extended passive bus

A.2.2 Point-to-point (Figure A.3)

This configuration provides for one transmitter/receiver only at each end of the cable (see figure A.3). It is, therefore, necessary to determine the maximum permissible attenuation between the ends of the cable to establish the transmitter output level and the range of receiver input levels. In addition, it is necessary to establish the maximum round trip delay for any signal which shall be returned from one end to the other within a specified time period (limited by D-echo bits).

A general objective for the operational distance between TE and NT or NT1 and NT2 is 1 000 metres (d_1 in figure A.3). It is agreed to satisfy this general objective with a maximum cable attenuation of 6 dB at 96 kHz. The round trip delay is between 10 μs to 42 μs.

NOTE 1: Round trip delay will normally be in the range of 10 μs to 26 μs. Where repeaters or amplifiers are utilized, 42 μs is the absolute maximum to ensure proper operation.

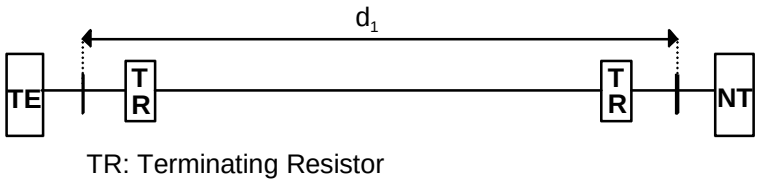


Figure A.3: Point-to-point

The lower value of 10 µs is derived in the same way as for the passive bus configuration. The upper value is composed of the following elements:

- bits due to frame offset (2 x 5,2 µs = 10,4 µs, see subclause 6.4.2.3);
- maximum 6 bits delay permitted due to the distance between NT and TE and the required processing time (6 x 5,2 µs = 31,2 µs);
- the fraction (+ 15 %) of a bit period due to phase deviation between TE input and output (see subclause 9.2.3, 0.15 x 5.2 ms = 0.8 µs).

It should be noted that an adaptive timing device at the receiver is required at the NT to meet these limits.

For the NT used for both point-to-point and passive bus configurations (see subclause 9.6.3.2), the tolerable round trip delay in passive bus wiring configurations is reduced to 13 µs due to the extra tolerance required for the adaptive timing. Using this type of wiring, it is also possible to provide point-to-multipoint mode of operation at layer 1.

NOTE 2: Point-to-multipoint operation can be accommodated using only point-to-point wiring. One suitable arrangement is an NT1 STAR illustrated in figure A.4. In such an implementation, bit streams from TEs should be buffered to provide for operation of the D-echo channel(s) to provide for contention resolution, but only layer 1 functionality is required. It is also possible to support passive bus wiring configurations on the ports of NT1 STARs. Support of this configuration does not affect the provisions of CCITT Recommendations I.430 [10], Q.921 or Q.931.

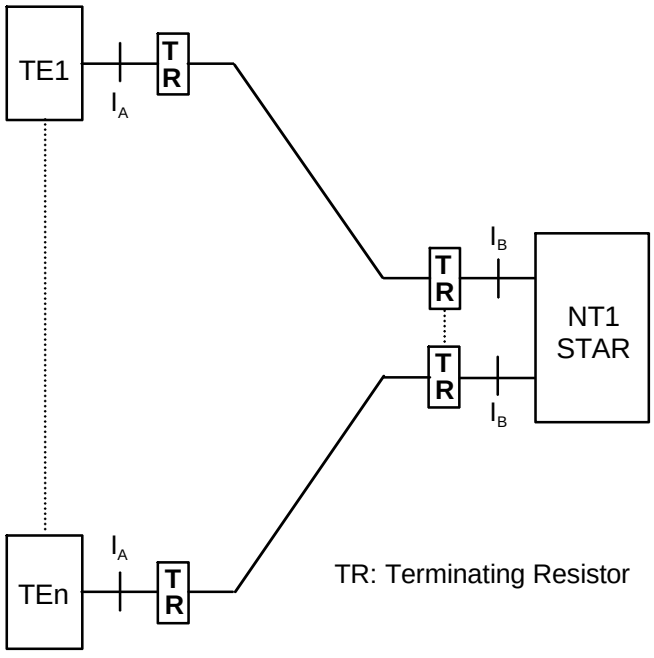
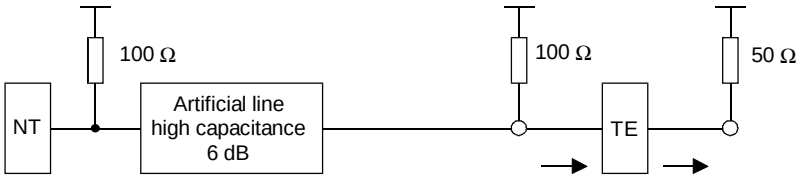


Figure A.4: NT1 STAR

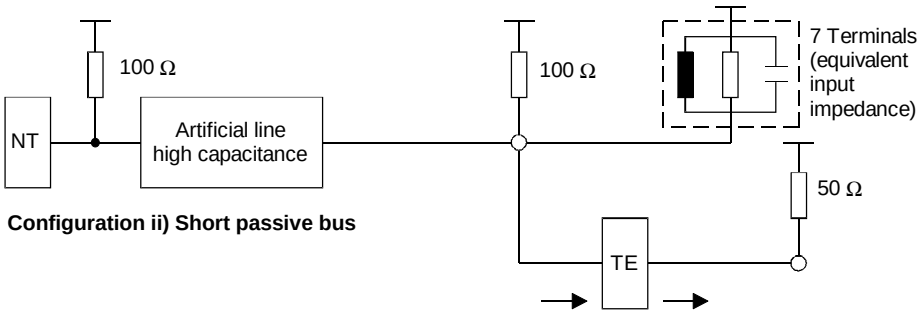
Annex B (normative): Test configurations

In clause 9, waveforms are shown for testing NT and TE equipment. This annex describes configurations, for testing TE equipment, which can be used to generate these waveforms (see figure B.1). Similar configurations can be used to test NT equipment.

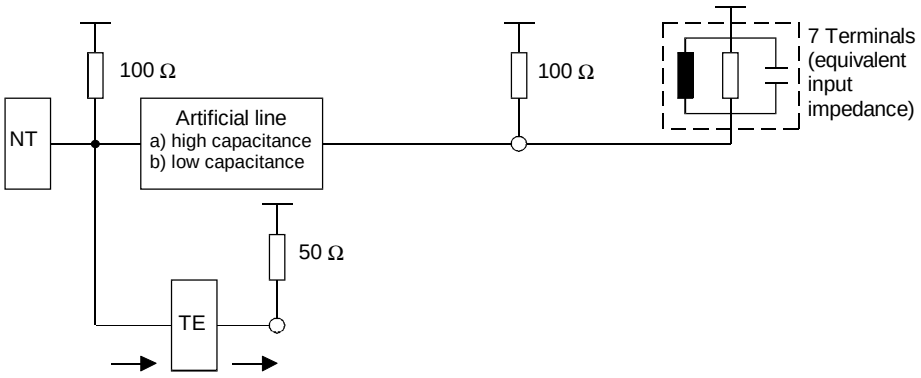
Table B.1 gives the parameters for the artificial lines reproduced in figure B.1. The artificial lines are used to derive the waveforms. For test configurations ii) and iii), the cable length used corresponds to a signal delay of 1 ms.



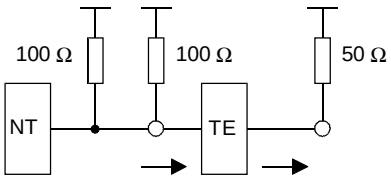
Configuration i) Point-to-point



Configuration ii) Short passive bus



Configuration iiia), iiib) Short passive bus



Configuration iv) Ideal test signal

Figure B.1: Test configurations

Table B.1: Parameters for the artificial lines

Parameters	High capacitance cable	Low capacitance cable
R (96 kHz)	160 Ω/km	160 Ω/km
C (1 kHz)	120 nF/km	30 nF/km
Zo (96 kHz)	75 Ω	150 Ω
Wire diameter	0,6 mm	0,6 mm

Annex C (normative): Test loopbacks defined for the basic UNI

C.1 Introduction

CCITT Recommendations in the I.600-Series specify an overall approach to be employed in maintaining the ISDN basic access. An integral part of that approach is the use of looping mechanisms in the failure confirmation and failure localization phases of network maintenance.

Detailed specifications of how such loopbacks are to be used may be found in the I.600-Series Recommendations. However, since the required loopbacks may impact the design of terminating pieces of equipment, a brief description of the loopbacks and their characteristics is presented in this annex.

C.2 Loopback mechanism definitions

This clause defines the terminology used in specifying the characteristics of loopbacks.

The loopback point is the location of the loopback.

The control point is the location from which activation/deactivation of the loopback is controlled.

NOTE 1: The generation of the test pattern used over the loopback may not be located at the control point.

The following three types of loopback mechanisms are defined:

a) Complete loopback - a complete loopback is a layer 1 mechanism which operates on the full bit stream. At the loopback point, the received bit stream shall be transmitted back towards the transmitting station without modification.

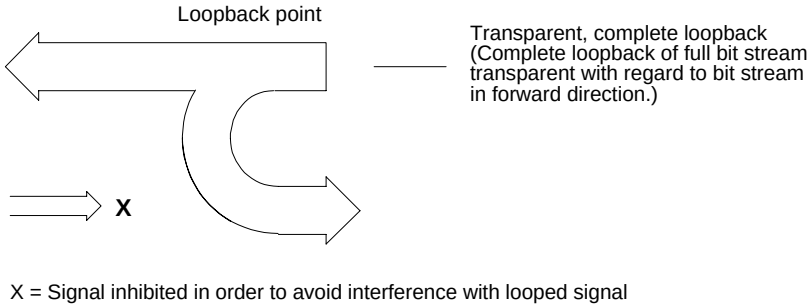
NOTE 2: The use of the term "complete loopback" is not related to implementation since such a loopback may be provided by means of active logic elements or controlled unbalance of a hybrid transformer, etc. At the control access point only the information channels may be available.

b) Partial loopback - a partial loopback is a layer 1 mechanism which operates on one or more specified channels multiplexed within the full bit stream. At the loopback point, the received bit stream associated with the specified channel(s) shall be transmitted back towards the transmitting station without modification.

c) Logical loopback - a logical loopback acts selectively on certain information within A channel or channels and may result in some specified modification of the looped information. Logical loopbacks may be defined at any layer of the OSI model and depend on the detailed maintenance procedures specified.

For each of the above three types of loopback mechanisms, the loopback may be further categorized as either transparent or non-transparent.

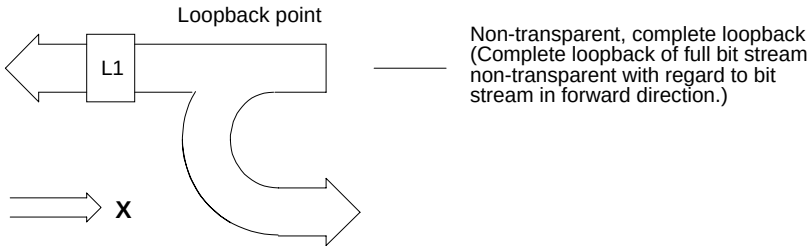
i) A transparent loopback is one in which the signal transmitted beyond the loopback point (the forward signal) when the loopback is activated, is the same as the received signal at the loopback point. See figure C.1.



X = Signal inhibited in order to avoid interference with looped signal

Figure C.1: Transparent loopback

ii) A non-transparent loopback is one in which the signal transmitted beyond the loopback point (the forward signal) when the loopback is activated is not the same as the received signal at the loopback point. The forward signal may be a defined signal or unspecified. See figure C.2.



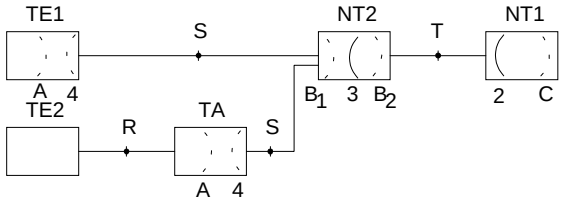
X = Signal inhibited in order to avoid interference with looped signal;
L1 = Device wich changes or inhibits the transferred signal.

Figure C.2: Non-transparent loopback

NOTE 3: Whether or not a transparent loopback is used, the loopback should not be affected by facilities connected beyond the point at which the loop is provided, e.g. by the presence of short circuits, open circuits or foreign voltages.

C.3 Test loopback reference configuration

Figure C.3 shows the possible locations of test loopbacks pertaining to the maintenance of the ISDN basic UNI. Recommended and desirable loopbacks are drawn in solid lines. Optional loopbacks are drawn with dashed lines. These optional loopbacks may not be provided by all equipments. The characteristics of each of these loopbacks are given in tables C.1 and C.2, respectively.



NOTE 1: Loopbacks B_1 and 3 are applicable to each individual interface at reference point S.

NOTE 2: Loopbacks A, B_1, B_2, C and 4 are optional. The definition of these loopbacks is outside the scope of this ETS.

Figure C.3: Location of loopbacks

C.4 Test loopback characteristics

Table C.1 presents the characteristics applicable to each recommended loopback.

The loopback 2 shall be implemented.

The loopback type indicates whether a complete, partial or logical loopback is required and whether the loopback should be transparent or non-transparent.

The loopback location is specified in a somewhat approximate manner, since the precise location may be implementation dependent.

The choice of loopback mechanism is dictated by the protocol layers available at the looping point and the addressing requirements. Thus, for instance, loopback 3 is controlled via layer 3 since selection of a particular S interface may be required.

Table C.1: Characteristics of recommended loopbacks

Loopback (see figure C.3)	Location	Channel(s) looped	Loopback type	Control point	Control mechanism	Implementation
2	In NT1, as near as possible to T reference point, towards the ET (note 1)	2B + D channels	Complete, transparent or non-transparent (note 2 and note 4)	Under control of local exchange	Layer 1 signals in transmission system	Mandatory
3	In NT2, as near as possible to S reference point, towards the ET	2B + D channels	Complete, transparent or non-transparent (note 2)	NT2	Local maintenance	Desirable (note 3)
				NT2	Layer 3 messages in D-channel or in band signalling in B-channel (note 2)	

NOTE 1: In the case of a combined NT1 and NT2 (i.e., an NT1/2), loopback 2 is located at the position within the NT1/2 which equates to the T reference point.
NOTE 2: Activation/deactivation of loopback 3 may be initiated by request from a remote maintenance server by layer 3 messages in the D channel or other signalling in the B channel. However, the generation of the test pattern over the loopback would be by the NT2.
NOTE 3: From a technical viewpoint, it is desirable (although not mandatory) that loopback 3 can always be implemented, therefore the design of protocols for loopback control should include the operation of loopback 3.
NOTE 4: In case a transparent loopback 2 is applied, the NT1 shall send INFO 4 frames toward the user with the D-echo channel bits set to ZERO.

Table C.2: Characteristics of optional loopbacks

Loopbacks (see Figure I-3/I.430)	Location	Channel(s) looped	Loopback type	Control point	Control mechanism	Implementation
4	Inside the TA or TE	B1, B2 (note)	Partial, transparent or non-transparent	NT2 local exchange, remote maintenance server or remote user	Layer 3	Optional

NOTE: The B_1- and B_2-channel loopbacks are controlled by separate control signals. However, both loopbacks may be applied at the same time.

NOTE: For conformance test purposes it is desirable that a complete loopback 4 as defined in table C.2 is provided by an item under test. The loop control mechanism is up to the manufacturer and should be declared to the test house.

Annex D (normative): Additional requirements applicable to the (explicit) S reference point

D.1 Introduction

This annex applies to the interface at the explicit S reference point, i. e. at the interface between a terminal and the Private Telecommunication Network eXchange (PTNX), see figure D.1.

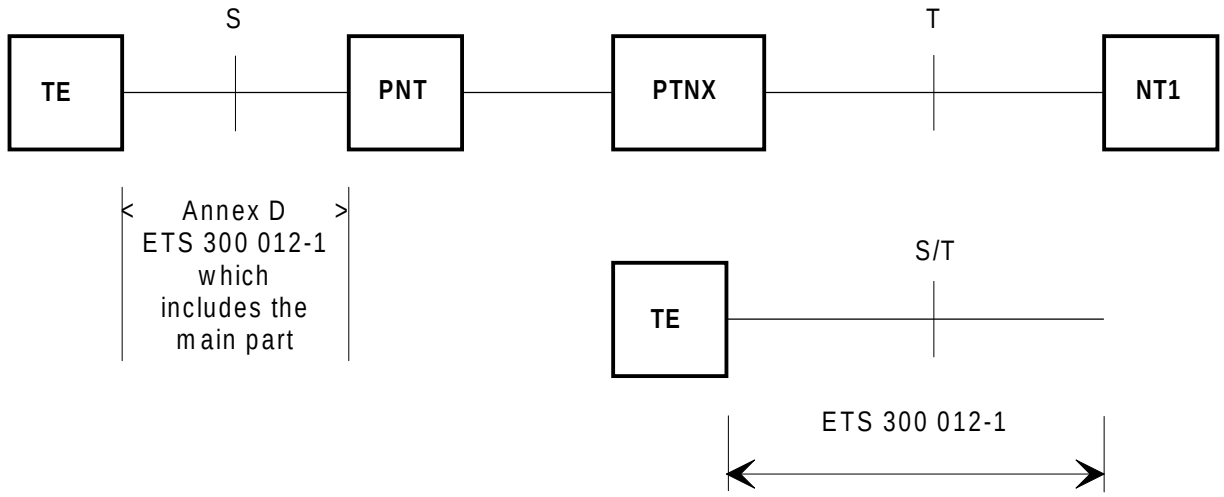


Figure D.1: Application of annex D

D.2 References

ENV41 004 [7]: "Reference Configuration for Calls, based on ISDN Connection Types, as provided by Private Telecommunication Network Exchange".

D.3 Definitions

D.3.1 Private Network Termination (PNT)

A remote unit of equipment which terminates a transmission system employed between the private telecommunication network exchange and the interface I_B and the S reference point.

D.3.2 Terminal Equipment (TE)

The definition of clause 3 applies with the exception that the NT2 functional grouping is not covered by this term within the context of this annex.

D.4 Conformance

All normative statements of the main body and annexes A to C are subject to conformance with the understanding as indicated by clause D.1 and subclauses D.3.1 and D.3.2.

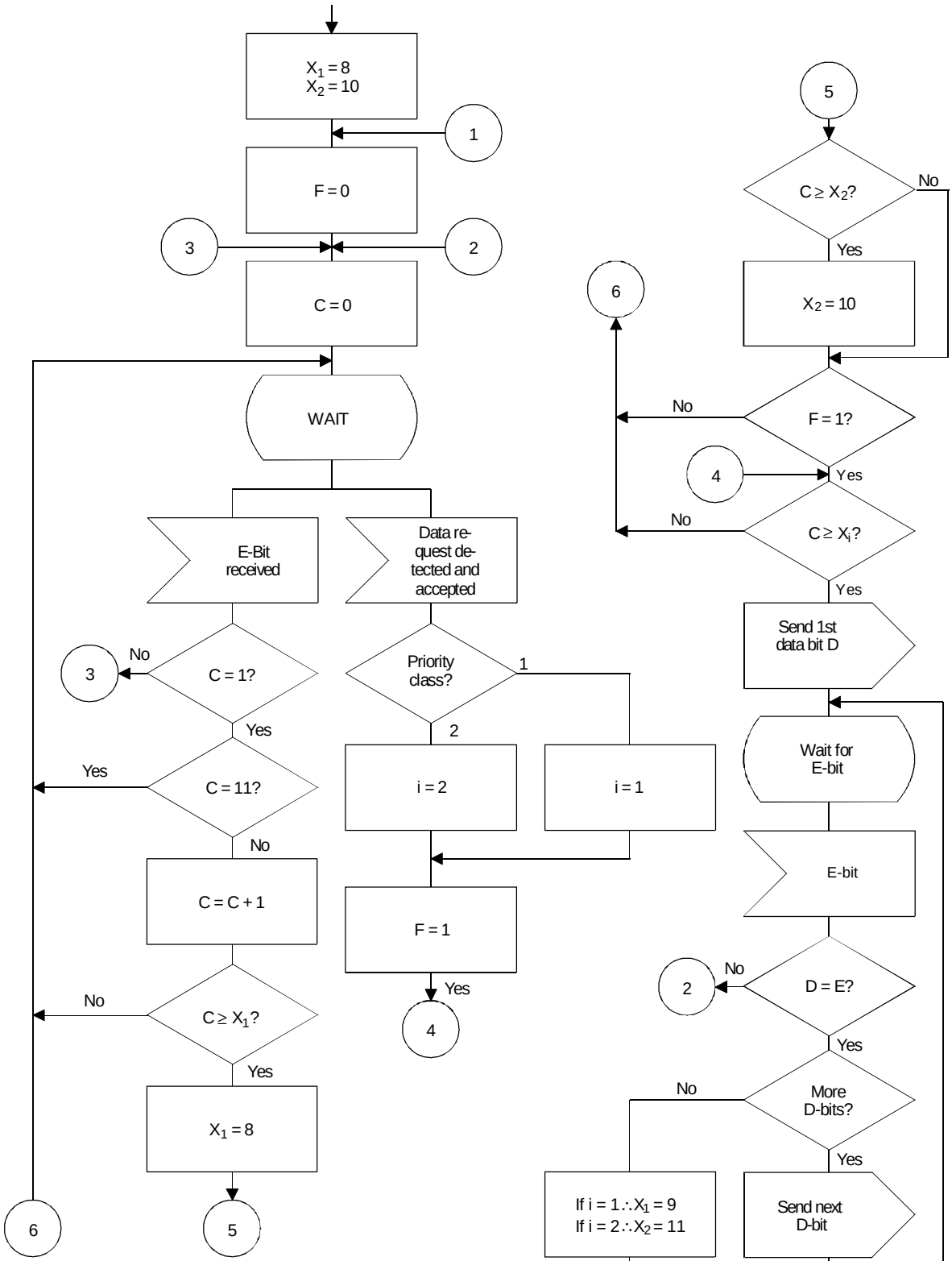
D.5 Requirements

Multiframing (to be stated whether there shall be a difference to subclause 8.3 as given in this ETS).

D.6 Provision of power

If reliable normal mode powering is provided by the PTNX to the interface the provision of restricted mode power is optional. The power source may have a connection to ground.

Annex E (informative): SDL representation of a possible implementation of the D-channel access



D D-channel bit
E D-echo-channel bit
F Flag indicating that frame is pending
C Number of consecutive ones detected on the D-echo-channel
X_1 Threshold for priority class 1
X_2 Threshold for priority class 2
i Priority class indicator

Annex F (informative): SDL representation of activation/deactivation procedures for TEs and NTs

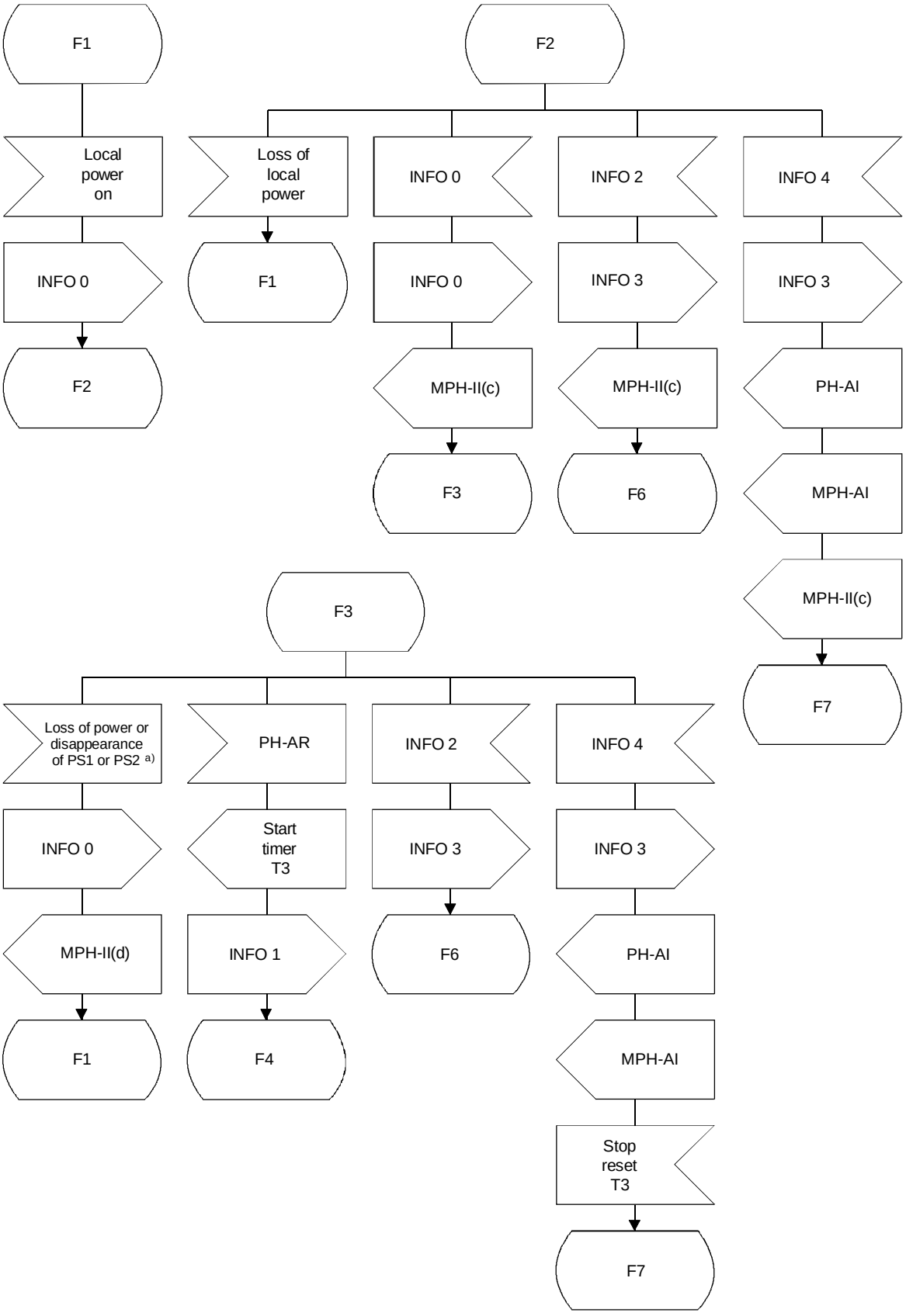
F.1 SDL representation of activation/deactivation procedures for TEs

In subclause 7.4 the procedure at various types of terminals is specified in form of a finite state matrices given in tables 5, 6 and 7.

When SDL representation and activation/deactivation tables are inconsistent, the tables shall apply.

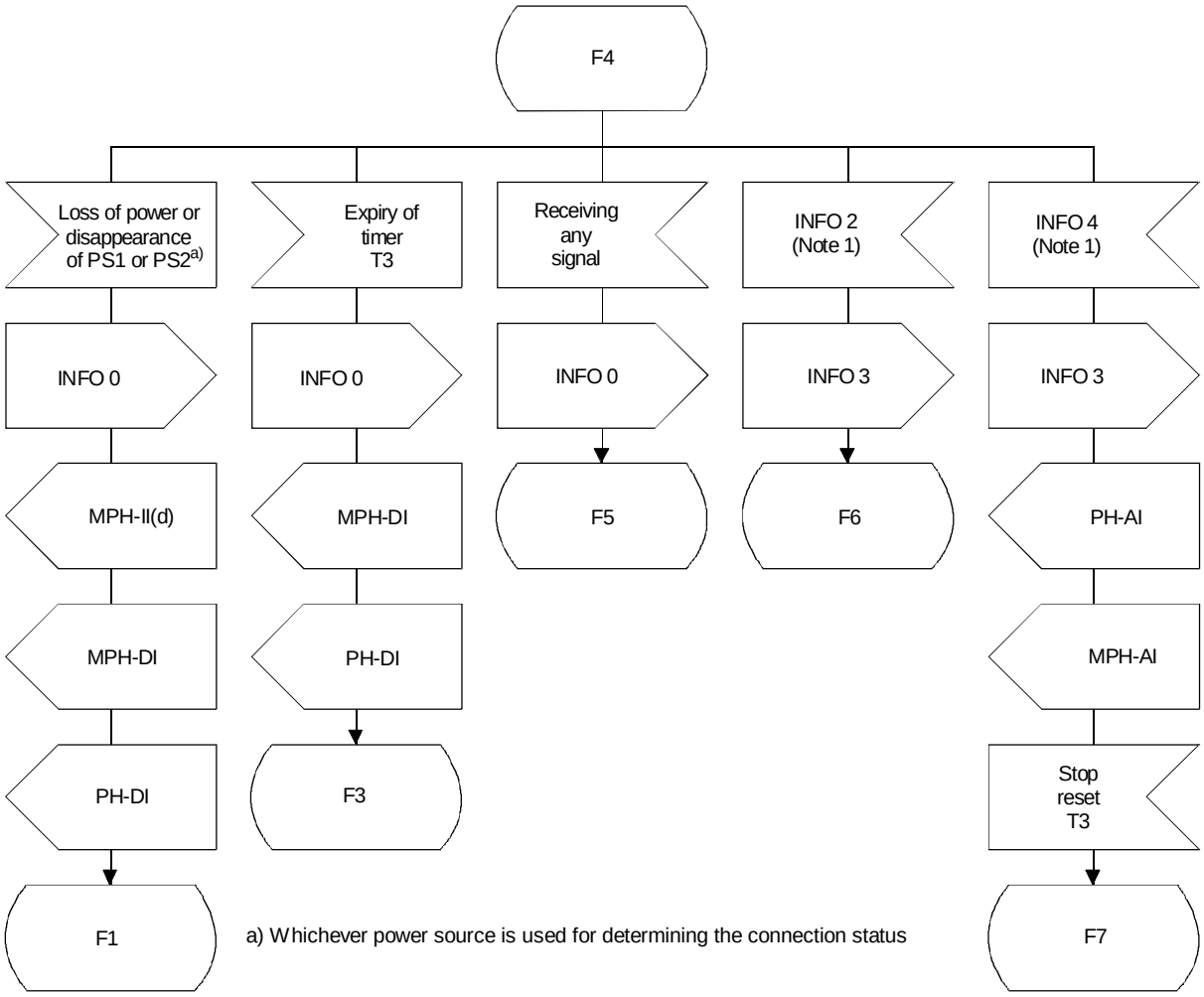
F.2 SDL representation of activation/deactivation procedures for NTs

SDL representation of activation/deactivation procedures for NTs (see table 8) is given in figure F.2.



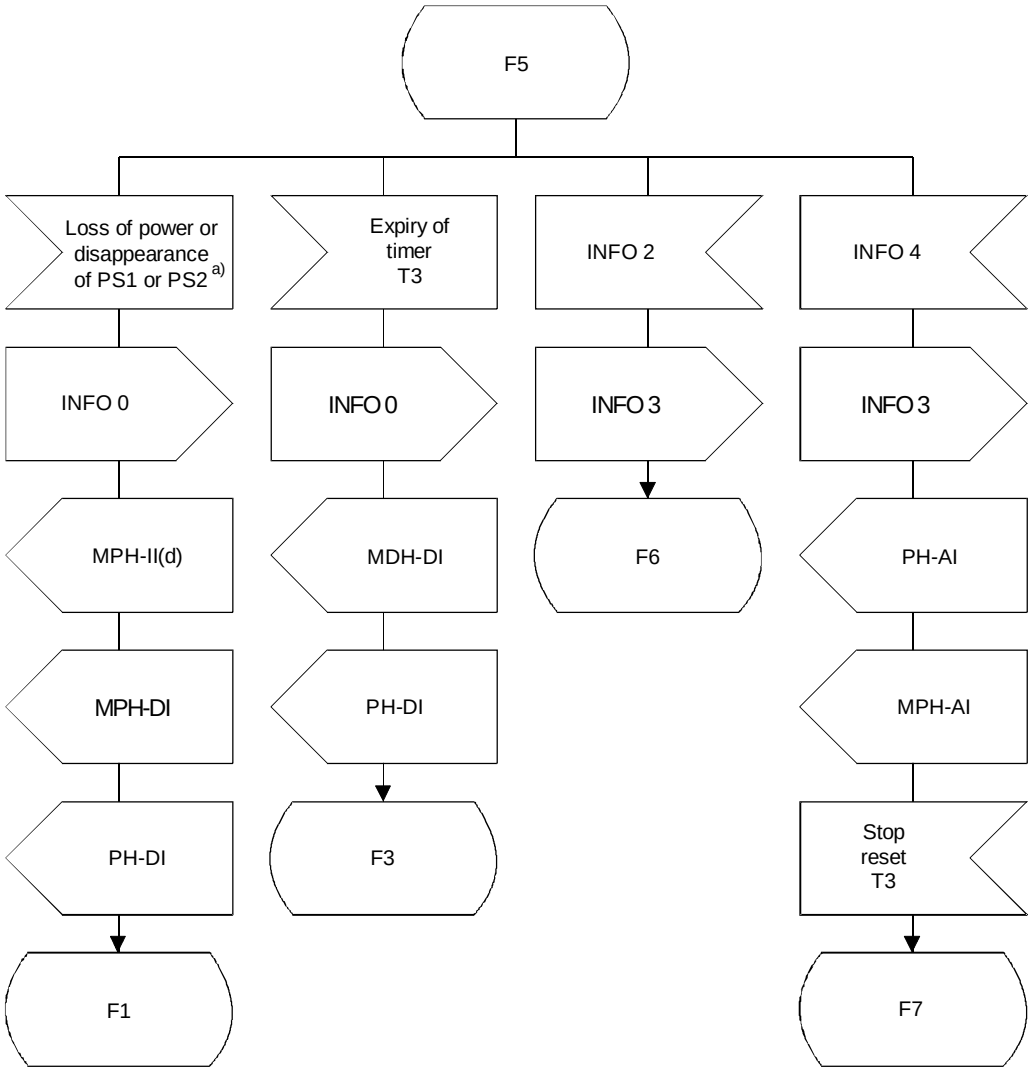
a) Whichever power source is used for determining the connection status.

Figure F.1: SDL representation of activation/deactivation procedures for TEs



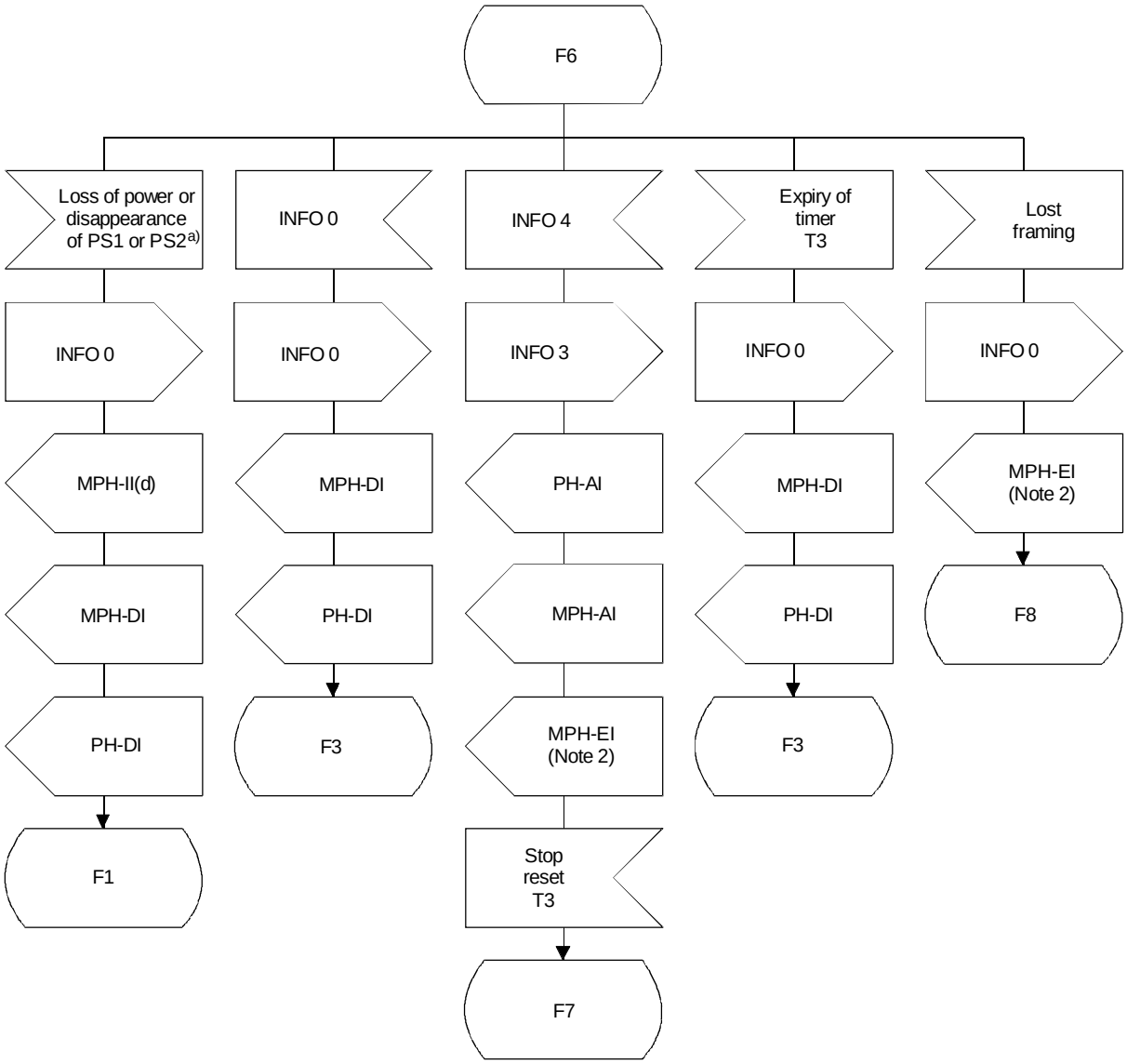
NOTE 1: If INFO 2 or INFO 4 is recognized within 5 ms after appearance of a signal, TEs shall go to F5

Figure F.1 (continued): SDL representation of activation/deactivation procedures for TEs



a) Whichever power source is used for dermining the connection status.

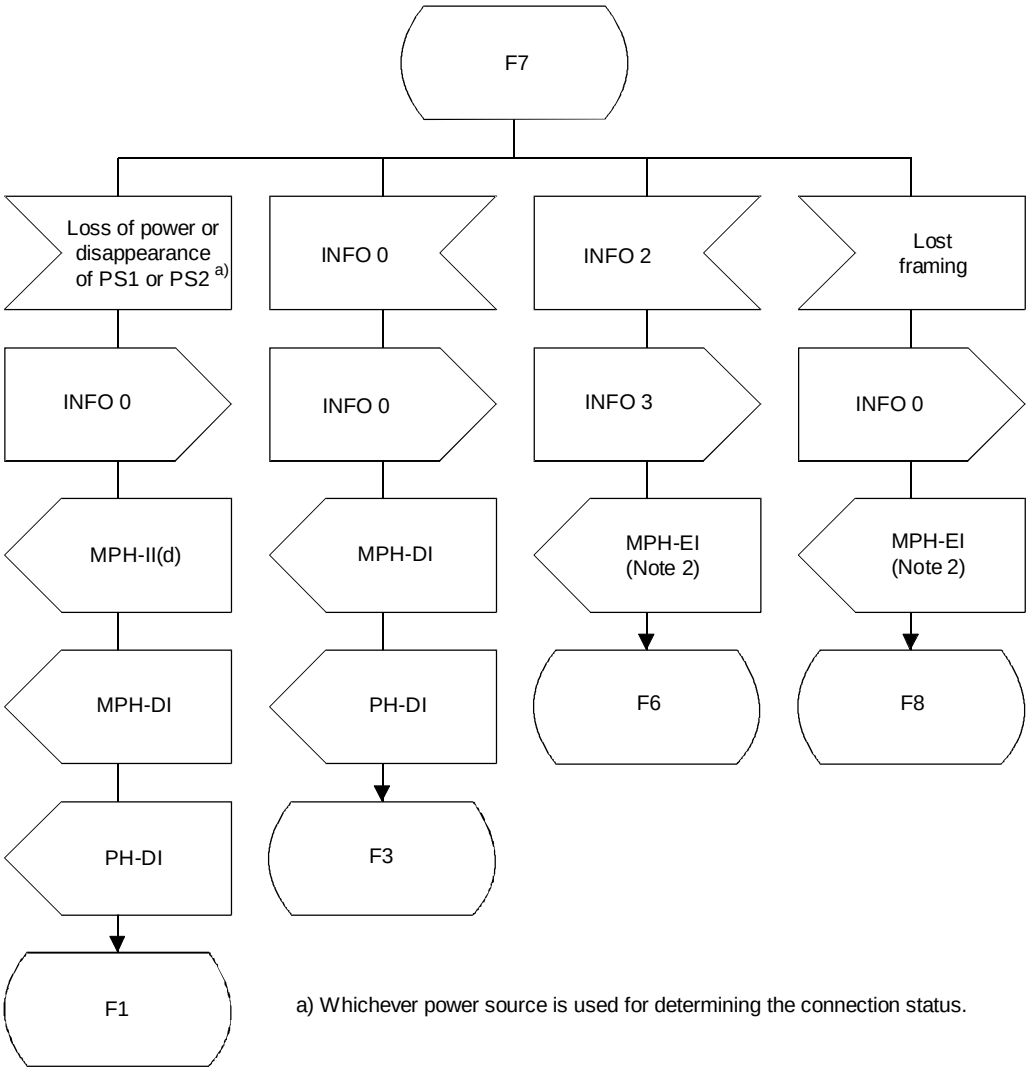
Figure F.1 (continued): SDL representation of activation/deactivation procedures for TEs



a) Whichever power source is used for dermining the connection status.

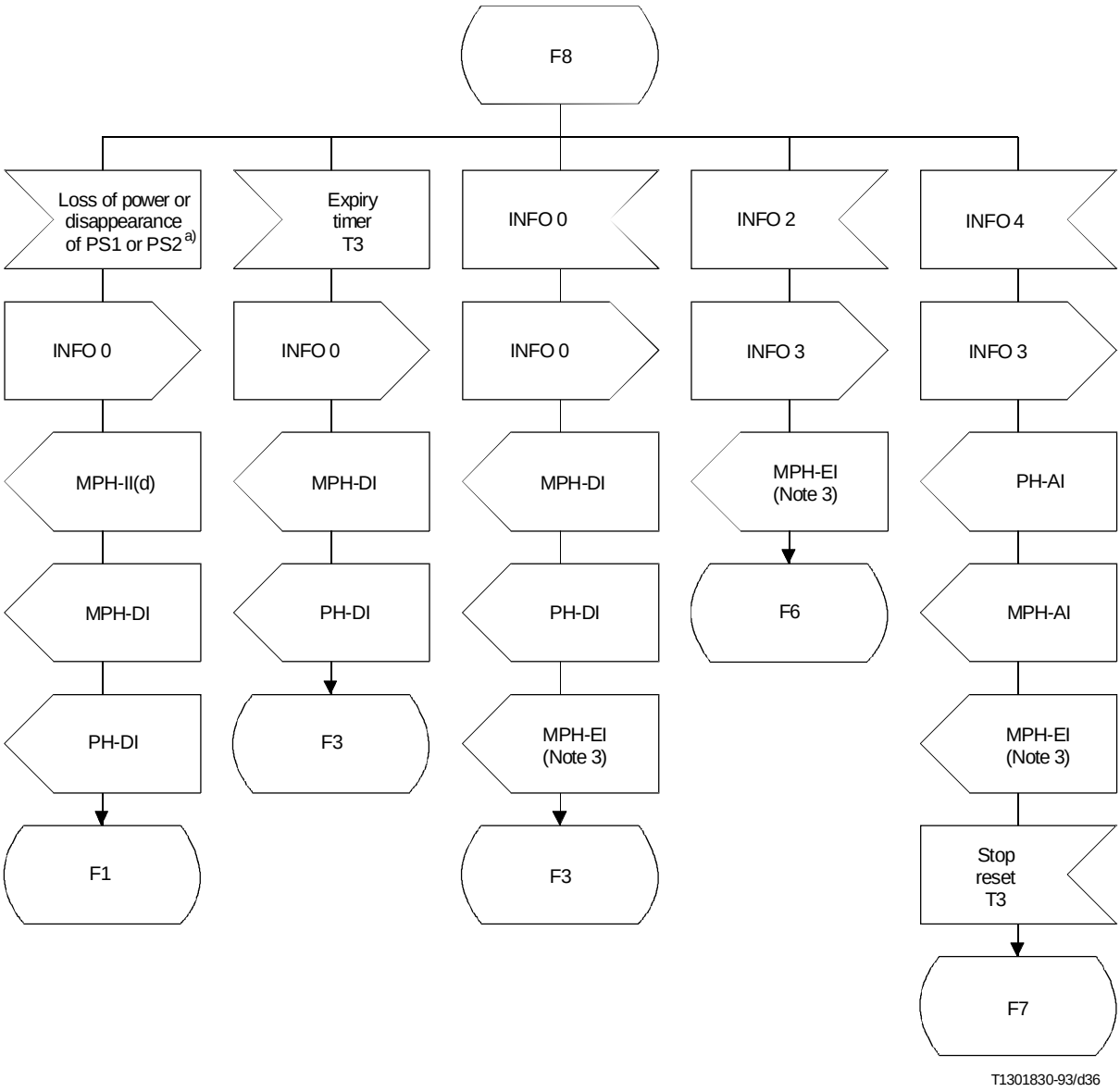
NOTE 2: This error indication reports the detection of an error.

Figure F.1 (continued): SDL representation of activation/deactivation procedures for TEs



NOTE 2: This error indication reports the detection of an error.

Figure F.1 (continued): SDL representation of activation/deactivation procedures for TEs

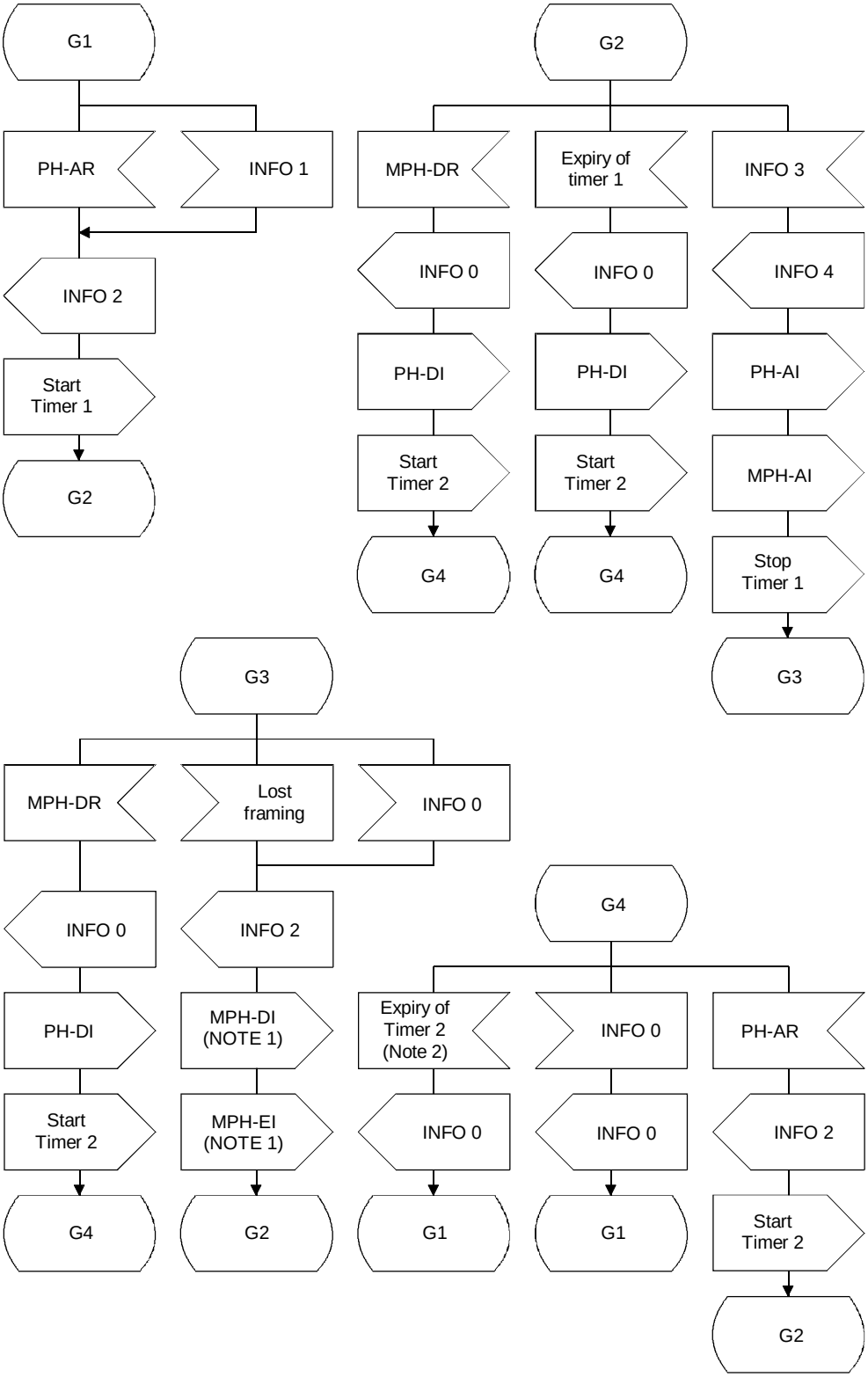


PH-AI	Primitive PH-ACTIVATE indication
MPH-AI	Primitive MPH-ACTIVATE indication
MPH-DI	Primitive MPH-DEACTIVATE indication
PH-DI	Primitive PH-Deactivate indication
MPH-EI	Primitive MPH-ERROR indication including a parameter indicating the cause
MPH-II(c)	Primitive MPH-INFORMATION indication (connected)
MPH-II(d)	Primitive MPH-INFORMATION indication (disconnected)
PH	Layer 1 $\longleftrightarrow$ layer 2
MPH	Layer 1 $\longleftrightarrow$ management entity

a) Whichever power source is used for determining the connection status.

NOTE 3: This error indication reports recovery from a previously reported error.

Figure F.1 (concluded): SDL representation of activation/deactivation procedures for TEs



NOTE 1: The notifications MPH-DI and MPH-EI need not be transferred to the management entity at the NT.

NOTE 2: The duration of timer T2 is network dependent (25 to 100 ms). This implies that a TE has to recognize INFO 0 and to react within 25 ms. If the NT is able to unambigously recognize INFO 1, then the value of timer T2 may be 0.

Figure F.2: SDL representation of activation/deactivation procedures for NTs

Annex G (informative): Multiframing mechanism

G.1 Multiframing

Multiframing provides a layer 1 signalling capability between the TEs and the NT in both directions through the use of extrA channels referred to as the S channel for the NT-to-TE direction and the Q channel for the TE-to-NT direction. This layer 1 signalling capability exists only between the TE and NT, i.e., there is no requirement in the NT for the transfer of signals between the TE-NT channels and the layer 1 signalling channel between the NT and the network.

The use of the Q and S channels should be the same in point-to-point as in point-to-multipoint configurations. There is no inherent collision detection mechanism provided for the Q channel, nor is there any addressing mechanism for the S channel. Procedures necessary to prevent or deal with collision and to indicate the desired TEs that are required for any application are not a part of this Recommendation.

The uses of the Q channels and S channels are optional. NTs that do not support these channels are not required to encode the F_A and M bits as required for the defined multiframing. TEs that do not use the Q-bit channel should set each Q bit to a ONE in each frame in which a ONE is received in the F_A-bit position of the NT-to-TE frame (i.e. echoing of the received $F_{A\ bit}$s).

G.1.1 General mechanism

a) *Q-bit Identification* : The Q bits (TE-to-NT) are defined to be the bits in the $F_{A\ bit}$ position of every fifth frame. The Q-bit positions in the TE-to-NT direction are identified by binary inversions of the F_A/N-bit pair (F_A = y ONE, N = y ZERO) in the NT-to-TE direction. The provision of this capability in NTs is optional. The provision for identification of the Q-bit positions in the NT-to-TE direction permits all TEs to synchronize transmission in Q-bit positions; thereby avoiding interference of $F_{A\ bit}$s from one TE with the Q bits of a second TE in passive bus configurations.

b) *Multiframe Identification* : A multiframe, which provides for structuring the Q bits into 4-bit characters (Q1 - Q4), is established by setting the M bit, in bit position 26 (see subclause 6.5.2.2) of the NT-to-TE frame, to ONE in every twentieth frame. This structure provides for 4-bit characters in a single channel, TE-to-NT. The provision of this capability in NTs is optional. Detection and use of the M bit by the TE is optional if the Q channel is not intended to be used.

G.1.2 Q-bit position identification algorithm

The Q-bit position identification algorithm is illustrated in table G.1. The TE synchronizes to the received $F_{A\ bit}$ inversions and transmits Q bits in every fifth frame, i.e., in frames in which $F_{A\ bit}$s (NT-to-TE direction) should be equal to ONE. The algorithm used by a TE to determine multiframe synchronization or loss of multiframe synchronization is not described in this Recommendation. However, a TE should echo the received Q-bit position identifier ($F_{A\ bit}$) into the TE-to-NT Q-bit position when multiframe synchronization is not established.

No special Q-bit identification derived from the received signal is required in the NT because the maximum round trip delay of NT-to-TE-to-NT is a small fraction of a frame, and, therefore, Q-bit identification is inherent in the NT.

Table G.1: Q-bit position identification and multi-frame structure

Frame number	NT-to-TE $F_{A\ bit}$ position	NT-to-TE M bit	TE-to-NT $F_{A\ bit}$ position (notes 1 and 2)
1	ONE	ONE	Q1
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	ZERO	Q2
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	ZERO	Q3
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	ZERO	Q4
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	ONE	Q1
2	ZERO	ZERO	ZERO
etc.			

NOTE 1: If the Q-bits are not used by a TE, the Q-bits should be set to ONE.

NOTE 2: Where multiframe identification is not provided with a ONE in an appropriate M bit, but where Q-bit positions are identified, Q-bits 1 through 4 are not distinguished.

G.1.3 TE multiframe identification

The first frame of the multiframe is identified by the M bit equal to a binary ONE. TEs that are not intended to use, nor to provide for the use of, the Q channel are not required to identify the multiframe. TEs that are intended to use, or to provide for the use of, the Q channel shall use the M bit equal to a binary ONE to identify the start of the multiframe.

The algorithm used by a TE to determine when synchronization or loss of synchronization of the multiframe is achieved is not described in this ETS; however, it should be noted that the transmission of multiframing from an NT is not mandatory.

G.2 S-channel structuring algorithm

The algorithm for structuring the S bits (NT-to-TE frame bit position 37 (see subclause 6.5.2.2, table 3)) into an S channel uses the same combination of the $F_{A\ bit}$ inversions and the M bit that is used to structure the Q-channel as described in subclause 8.3. The S-channel structure, shown in table G.2 provides for five subchannels, SC1 through SC5. Each subchannel SC*n* is comprised of the bits SC*n*1 through SC*n*4, which provide for the transfer of one 4-bit character per multiframe (5 ms).

TABLE G.2: S-Channel structure

Frame number	NT-to-TE $F_{A\ bit}$ position	NT-to-TE M bit	TE-to-NT S bit
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
3	ZERO	ZERO	SC31
4	ZERO	ZERO	SC41
5	ZERO	ZERO	SC51
6	ONE	ZERO	SC12
7	ZERO	ZERO	SC22
8	ZERO	ZERO	SC32
9	ZERO	ZERO	SC42
10	ZERO	ZERO	SC52
11	ONE	ZERO	SC13
12	ZERO	ZERO	SC23
13	ZERO	ZERO	SC33
14	ZERO	ZERO	SC43
15	ZERO	ZERO	SC53
16	ONE	ZERO	SC14
17	ZERO	ZERO	SC24
18	ZERO	ZERO	SC34
19	ZERO	ZERO	SC44
20	ZERO	ZERO	SC54
1	ONE	ONE	SC11
2	ZERO	ZERO	SC21
etc.			
NOTE: S-subchannels not used by the NT1 should be set to all ZEROs.			

Annex H (informative): Bibliography

- ITU-T Recommendation Q.921 (1993): "ISDN user-network interface-data link layer specification".

- ITU-T Recommendation Q.931 (03/93): "Digital Subscriber Signalling System No. 1 (DSS 1) - ISDN user-network interface layer 3 specification for basic call control".

History

Document history			
April 1992	First Edition		
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