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Foreword

This final draft second edition European Telecommunication Standard (ETS) was produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI) and is now submitted for the voting phase of the ETSI standards approval procedure.

This ETS aims to meet urgent requirements of network operators and equipment manufacturers who are designing equipment to operate with an Integrated Services Digital Network (ISDN) primary rate access User Network Interface (UNI).

This ETS is based upon CCITT Recommendation I.431 and provides modifications and further requirements to that document. It also is affected by CCITT Recommendations G.703, G.704 and G.706, and modifications to these CCITT Recommendations are provided within this ETS.

This ETS also takes into account requirements contained in ECMA Standard 104: "Physical layer at the primary rate access interface between data processing equipment and private switching networks (1985)", which are given in annex A.

This ETS consists of 3 parts as follows:

Part 1: "Layer 1 specification";

Part 2: "Conformance test specification for interface I_A and I_B";

Part 3: "Implementation Conformance Statement (ICS) and Implementation eXtra Information for Testing (IXIT) proforma specification for lnterface I_A and I_B".

Proposed transposition dates	
Date of latest announcement of this ETS (doa):	3 months after ETSI publication
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa

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1 Scope

This second edition European Telecommunication Standard (ETS) provides the test principles used to determine the compliance of an Implementation Under Test (IUT) for the requirements specified in ETS 300 011-1 [3].

It is outside the scope of this ETS to identify the specific tests required by an implementation where equipment has to meet attachment approval.

This ETS is applicable to interfaces I_A and I_B as appropriate. The field of applicability is reported at the beginning of each test.

2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references subsequent amendments to, or revisions of, any of these publications apply to this ETS only when incorporated in it by amendments or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation O.151 (1992): "Error performance measuring equipment operating at the primary rate and above".

[2] ETR 001: "Integrated Services Digital Network (ISDN); Customer access maintenance".

[3] ETS 300 011-1: "Integrated Services Digital Network (ISDN); Primary rate User Network Interface (UNI); Part 1: Layer 1 specification".

[4] ETS 300 233 (1994): "Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate".

[5] CCITT Recommendation X.200 (1994): "Information technology - Open Systems Interconnection - Basic reference model: The basic model".

[6] CCITT Recommendation O.162 (1992): "Equipment to perform in-service monitoring on 2 048, 8 448, 34 368 and 139 264 kbit/s signals".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this ETS, the following definitions apply:

Alternate Mark Inversion (AMI): Is a code where ONEs are represented by alternate positive and negative pulses, and ZEROs by spaces.

High-Density Bipolar 3 (HDB3): Is a modified AMI code. An exception occurs for blocks of 4 successive ZEROs. Each block of 4 successive ZEROs is replaced by OOOV or BOOV where B represents an inserted pulse conforming to the AMI and V represents an AMI violation. The choice of OOOV or BOOV is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no dc component is introduced.

Interface I_A: User side of the ISDN user-network interface for the primary rate access.

Interface I_B: Network side of the ISDN user-network interface for the primary rate access.

Network side: NT1, LT and ET functional groups in case of an interface at the T reference point; or relevant parts of the NT2 functional group in case of an interface at the S reference point.

Network option 1: The digital link between interface at the T and V reference point does not provide a CRC-4 processing, i.e. the CRC-4 is terminated in the TE and the ET. This digital link is called to be "without CRC processing" (see subclause 7.2.2.2 of ETS 300 011-1 [3]).

NOTE 1: This option is not provided by the public ISDN at the T reference point. However it might be used for PTNX interconnection using unstructured 2 048 kbit/s leased lines.

Network option 2: The digital link between interface at the T and V reference point provides CRC-4 processing in the NT1 and the ET according ETR 001 [2]. Therefore the combinations of CRC-4 error information and RAI indicate the fault condition; FC1 or FC4 (see subclause 7.2.2.1 of ETS 300 011-1 [3]).

NOTE 2: Option 3 of CCITT Recommendation I.604 with CRC-4 processing in NT1, LT and ET is not relevant for this ETS.

Network Termination (NT): An equipment providing interface I_B.

NOTE 3: This term is used in this ETS to indicate network-terminating aspects of NT1 and NT2 functional groups where these have an I_B interface.

Network Termination type 1 (NT1): This functional group includes functions broadly equivalent to layer 1 (physical) of the OSI reference model. These functions are associated with the proper physical and electromagnetic termination of the network. NT1 functions are:

- line transmission termination;
- layer 1 maintenance functions and performance monitoring;
- timing;
- layer 1 multiplexing;
- interface termination.

Network Termination type 2 (NT2): this functional group includes functions broadly equivalent to layer 1 and higher layers of the CCITT Recommendation X.200 [5] reference model. Private Telecommunication Network Exchange (PTNXs), local area networks and terminal controllers are examples of equipment or combinations of equipment that provide NT2 functions. NT2 functions include:

- layer 2 and layer 3 protocol handling;
- layer 2 and layer 3 multiplexing;
- switching;
- concentration;
- maintenance functions;
- interface termination and other layer 1 functions.

Private Telecommunication Network eXchange (PTNX): A nodal identity in a private telecommunication network which provides autonomous and automatic switching and call handling functions used for the provision of telecommunication services which are based on the definitions for those of the public ISDN.

Private Network Termination (PNT): A remote unit of equipment which terminates a transmission system employed between the PTNX and the interface I_B and the S reference point.

Simulator: (terminal or network) device generating a stimulus signal conforming to this ETS to bring the IUT into the required operational state and monitoring the receive signal from the IUT. It can either be a simulator for the user side or the network side of the interface.

Terminal Adapter (TA): An equipment with interface I_A and one or more auxiliary interfaces that allow non-ISDN terminals to be served by an ISDN user-network interface.

Terminal Equipment (TE): An equipment providing an interface I_A.

NOTE 4: This term is used in this ETS to indicate terminal-terminating layer 1 aspects of TE1, TA and NT2 functional groups, where these have an I_A interface.

NOTE 5: In annex A of ETS 300 011-1 [3], this definition applies with the exception that the NT2 functional grouping is not covered.

Terminal Equipment type 1 (TE1): This functional group includes functions belonging to the functional group TE, and with an interface that complies with the ISDN user-network interface standard.

User side: Terminal terminating layer 1 aspects of TE1, TA and NT2 functional groups.

3.2 Symbols

For the purposes of this ETS, the following symbols apply:

ONE	binary "1"
ZERO	binary "0"

3.3 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

AIS	Alarm Indication Signal
CRC	Cyclic Redundancy Check
dc	direct current
ET	Exchange Termination
HDB3	High-Density Bi-polar 3 (line code)
HDLC	High level Data Link Control
ICS	Implementation Conformance Statement
IUT	Implementation Under Test
NOF	Normal Operational Frames
NT	Network Termination
PRBS	Pseudo-Random Binary Sequence
PTN	Private Telecommunications Network
PTNX	Private Telecommunications Network Exchange
RAI	Remote Alarm Indication
Rx	Interface signal receiver of IUT or simulator
SMF	Sub-MultiFrame
TA	Terminal Adapter
TE	Terminal Equipment
Tx	Interface signal transmitter of IUT or simulator

4 Conformance tests

4.1 General information

Detailed test equipment accuracy and the specification tolerance of the test devices is not a subject of this ETS. Where such details are provided then those test details are considered as being an "informative" addition to the test description.

The test configurations given do not imply a specific realization of test equipment, nor arrangement, nor the use of specific test devices for conformance testing. However, any test configuration used shall provide those test conditions specified under "system state", "stimulus" and "monitor" for each individual test.

In the case of a multi-access implementation under test supporting interface I_A, unless otherwise stated, only one access at a time shall receive the stimulus. All other accesses shall receive "no signal" (state F3).

4.2 Additional information to support the test

It is assumed that, at least one of the following facilities is provided by IUT:

1) a transparent loopback of at least one timeslot towards the interface;

2) the ability to transmit a 2^{11}-1 Pseudo-Random Binary Sequence (PRBS) in a timeslot.

When the IUT does not provide these facilities the equipment supplier may provide:

a) a test equipment using the same chip set and interface components as in the IUT and able to provide a transparent loopback of at least one timeslot towards the interface; or

b) a test equipment using the same chip set and interface components as in the IUT and able to provide a 2^{11}-1 PRBS in a timeslot.

4.3 Connection of the simulator to the IUT

For testing the electrical characteristics of the IUT, the simulator, or its relevant part, shall be connected directly to the interconnecting points for the interface wiring at the IUT unless otherwise stated. For the tests given in subclauses 5.3 (except 5.3.1.1) and 5.5, a cord connected at an IUT shall be removed since a cord is regarded as integral part of the interface wiring.

All other tests may be performed with interface wiring complying with the requirements given in ETS 300 011-1 [3], subclause 4.3.

5 Conformance tests specification

5.1 Functional characteristics tests

These tests are designed to test conformance to the functional characteristics of the layer 1 of primary rate interface.

5.1.1 Frame structure

These tests check the frame composition.

5.1.1.1 Number of bits per timeslot

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

5.1.1.2 Number of timeslots per frame

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

5.1.1.3 Generation of frame alignment word

Test applicable for I_A and I_B interfaces.

Purpose: To check the correct generation of frame alignment word, multiframe alignment word, CRC bits C_1 to C_4.

Test configuration:

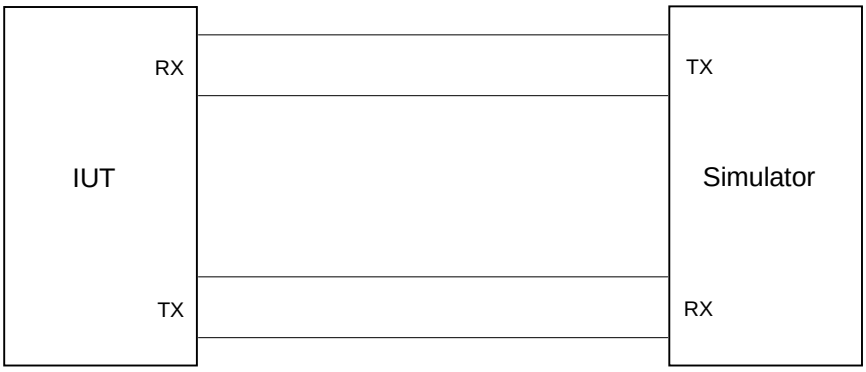


Figure 1: Test of frame alignment word

System state for I_A: Any state F1 to F5.

System state for I_B: State G1, G2, G3, G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: Correct frame alignment word pattern.

Results: No detection of incorrect frame alignment word, multiframe alignment word, and no received sub-multiframes in error within 1 second measured in any state. For IUT with CRC-DISABLE function activated (as defined in subclause A.2.3 of ETS 300 011-1 [3]) bit 1 of timeslot 0 shall always be ONE.

During this test the E bit is not considered.

5.1.1.4 S_a bits

Test applicable for I_A and I_B interfaces.

Purpose: To check the S_a bits contained in timeslot 0 of the frame not containing the frame alignment signal:

- bits 4 and 8 are reserved for international use are not defined;
- bits 5, 6 and 7 are specified in ETS 300 233 [4] for use in the access digital section.

Since no specific functions are defined for the S_a bits, no specific test is prescribed for the generation of these S_a bits. The immunity of the receiving side to the S_a bits is implicitly tested with the test described in subclauses 5.2.1 and 5.2.2.

5.1.2 Timeslot assignment

This requirement cannot be verified via layer 1 procedures.

Test to be performed at higher protocol layers.

5.1.3 Test of signals sent by IUT

These tests check the different signals sent by the IUT.

5.1.3.1 HDB3 coding and normal operational frame

Test applicable for I_A and I_B interfaces.

Purpose: To check the coding, decoding, and the binary organization of Normal Operational Frame (NOF).

Test configuration:

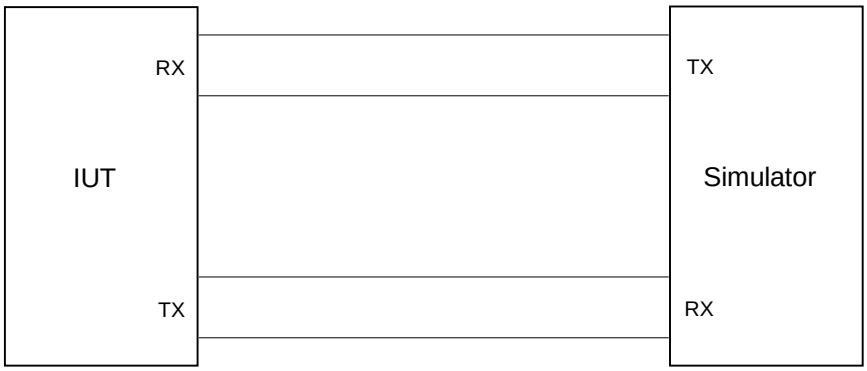


Figure 2: Test of HDB3 coding and NOF

System state for I_A: State F1. Application of one of the facilities defined in subclause 4.2 is required. The IUT shall be tested with loopback 4 activated according to annex B of ETS 300 011-1 [3].

System state for I_B: State G1.

Stimulus: NOF sent continuously from the Simulator with valid timeslot 0 including active CRC and without CRC error. Pseudo-random pattern 2^{15}-1 shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s).

Monitor: The correct coding and the frame structure of the signal sent from the IUT.

Results: The signal received shall be encoded according to the HDB3 coding rule of ETS 300 011-1 [3]. The frame shall comprise valid timeslot 0 with A bit set to 0, E bit set to 1 and including correct CRC without CRC blocks in error. For IUT with CRC-DISABLE function activated (as defined in subclause A.2.3 of ETS 300 011-1 [3]) bit 1 of timeslot 0 shall always be ONE.

5.1.3.2 Remote alarm indication

Test applicable for I_A and I_B interfaces.

This test is combined with test described in subclauses 5.2.1 and 5.2.2.

5.1.3.3 Alarm indication signal

Test applicable for I_B interface.

Purpose: To check the correct generation of Alarm Indication Signal (AIS).

This test is combined with test described in subclauses 5.2.1 and 5.2.2.

5.1.3.4 CRC error information

Test applicable for I_A and I_B interfaces.

Purpose: To check the detection of CRC blocks in error and the correct report with E bit.

This test is combined with test described in 5.2.6.

5.1.3.5 Remote alarm indication and continuous CRC error indication

Test applicable for I_B interface.

Purpose: To check the correct generation of remote Alarm Indication and continuous CRC error information (RAI and E bit set to ZERO).

This test is combined with test described subclauses 5.2.1 and 5.2.2.

5.1.4 Received and transmitted line code

5.1.4.1 Received line code

Test applicable for I_A and I_B interfaces.

Purpose: To test the line coding of the received frames.

This test is included in test 5.2.6 (CRC4 processing).

5.1.4.2 Transmitted line code

Test applicable for I_A and I_B interfaces.

Purpose: To test the line coding of the transmitted frames.

This test is included in test 5.1.3.1 Normal Operational Frame (NOF).

5.1.5 Timing considerations

5.1.5.1 AIS recognition

Test applicable for I_A interface.

Purpose: To check the ability of IUT to recognize AIS.

Test configuration:

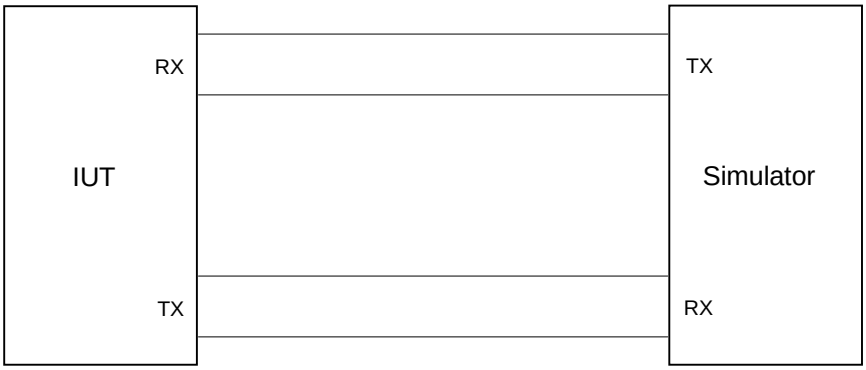


Figure 3: Test of AIS recognition

System state: State F4.

Stimulus: AIS signal with clock frequency 2 048 kbit/s ± 50 ppm.

It is not possible to distinguish between states F3 and F4 using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Monitor: The frames transmitted by IUT.

Results: IUT shall remain in state F4, therefore no change of error indication shall occur.

IUT having more than one access shall not synchronize its internal reference clock to the incoming signal frequency.

5.1.5.2 Synchronization

Test applicable for I_A interface.

Purpose: The ability of IUT to synchronize its timing on the signal received from the network.

Test configuration:

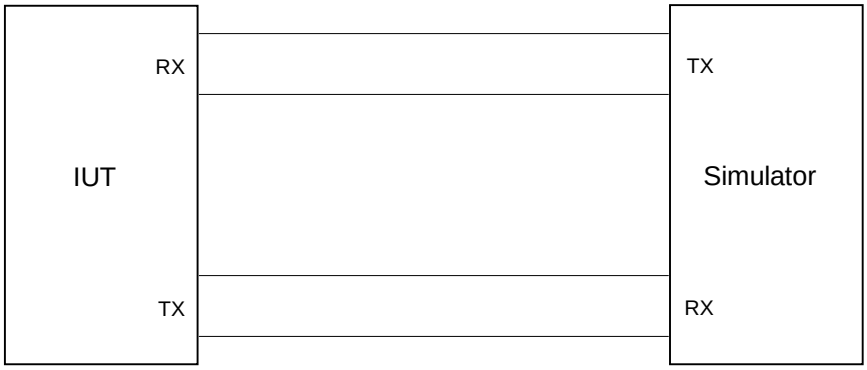


Figure 4: Test of synchronization

System state: State F1.

Stimulus: Normal operational frames with clock frequency variation from the nominal value.

For IUT to be connected to T reference point the corresponding bit rate shall be in the range 2 048 kbit/s ± 1 ppm.

For IUT to be connected to S reference point the corresponding bit rate shall be in the range 2 048 kbit/s ± 32 ppm.

For interface at IUT for PTNX interconnection the corresponding bit rate shall be in the range 2 048 kbit/s ± 32 ppm.

For implementation with free running clock frequency accuracy better than ± 1 ppm, as declared by the equipment supplier the stimulus shall be in the range ± 1 ppm.

In case of multi-access IUT, this test has to be performed on each access declared to be capable to extract synchronization from the network, while all other accesses are in state F3 or F4.

The stimulating signal is provided to a timing synchronizing input of IUT. The frequency of the output signal at each access has to follow the input signal frequency.

Monitor: The frames transmitted by IUT.

Results: 1) The IUT shall remain in state F1.

2) The frequency of the outgoing signal at each access has to follow the frequency of the stimulating input signal.

NOTE: The speed of the variation of the output frequency depends on the Q factor of the reference clock recovery timing of the IUT.

5.2 Interface procedures tests

Definition of test sequences:

FAS: Frame with correct FAS (Frame Alignment Signal), correct bits C_1 to C_4 and correct MFAS (CRC Multi Frame Alignment Signal) in timeslot 0.

/FAS: Frame with not correct FAS (Frame Alignment Signal), correct bits C_1 to C_4 and correct MFAS in timeslot 0.

BIT 2: Bit 2 of timeslot 0 not containing the frame alignment signal.

FRAME A: Two consecutive frames having FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0 and no contiguous group of seven bits which simulates the Frame Alignment Signal in timeslots 1 to 31.

FRAME B: Two consecutive frames having FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0, simulated BIT 2 = 1 in the first timeslot 31 and simulated FAS (no corresponding MFAS) in the second timeslot 31.

FRAME C: Two consecutive frames having /FAS in the first timeslot 0, BIT 2 = 1 in the second timeslot 0, simulated BIT 2 = 1 in the first timeslot 31 and simulated FAS (no corresponding MFAS) in the second timeslot 31.

SMF A: Sub-multiframe having correct generation of C_1 to C_4 bits.

SMF B: Sub-multiframe having incorrect generation of C_1 to C_4 bits.

MF A: Multiframe having correct FAS, BIT 2 = 1, MFAS and correct C_1 to C_4 bits.

MF B: Multiframe having correct FAS, BIT 2 = 1, but incorrect MFAS and correct C_1 to C_4 bits.

n: # indicates that the sequence defined in the previous line may be repeated before entering the next sub-sequence. If the parameter "n" is defined this sequence shall be repeated at least "n" times.

Additional information regarding interface procedure tests for interface I_B:

- when monitoring interface I_B it has to be recognized that a time delay period independent of actual response times of interface receivers/transmitters may be introduced (e.g. delays attributable to the implementation of transmission systems between the NT and ET, where a line transmission termination is present or where coding, decoding and processing occurs etc.). Therefore it is to be expected that test state transitions may show a delay when monitored.

- separate test response descriptions for interfaces I_A and I_B are provided. Indication of state transition for I_B is given only where stimulus is repeated (indicated by a #). The expected signal response to a repeated stimulus may however still display a time delay.

5.2.1 States-matrix at the IUT network side

Test applicable for I_B interface.

Purpose: The tests defined in this subclause intend to check the different stable states at the IUT side and the possible transitions between them. These tests are performed by simulating the opposite side (and simulating internal fault in the IUT for interface I_B), monitoring the IUT at the interface and verifying appropriate state transition.

Test configuration:

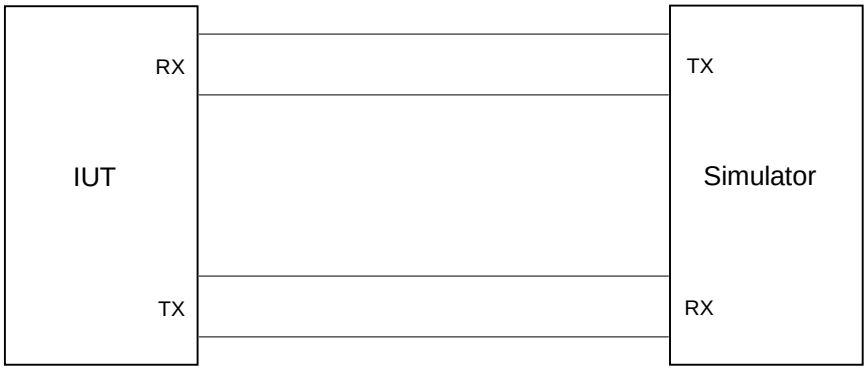


Figure 5: State-matrix test at the network side

System state: Any state G0 to G5.

It is not possible to distinguish between states G1 and G3 using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Stimulus: For each initial state, each possible new event indicated in table 6 of ETS 300 011-1 [3] shall be performed.

Stimulus shall be maintained for a time period sufficient to allow the expected state transition.

S_a bits shall be set to binary ONE.

Monitor: The status indication provided by the IUT and the signal transmitted towards the interface.

The final state shall be checked 1 second after the stimulus has been transmitted.

Results: New state, transmitted signal and primitives sent to the higher layers according to table 6 of ETS 300 011-1 [3].

5.2.2 States-matrix at the IUT user side

Test applicable for I_A interface.

Purpose: The tests defined in this subclause intend to check the different stable states at the IUT side and the possible transitions between them. These tests are performed by simulating the opposite side, monitoring the IUT at the interface and verifying appropriate state transition.

Test configuration:

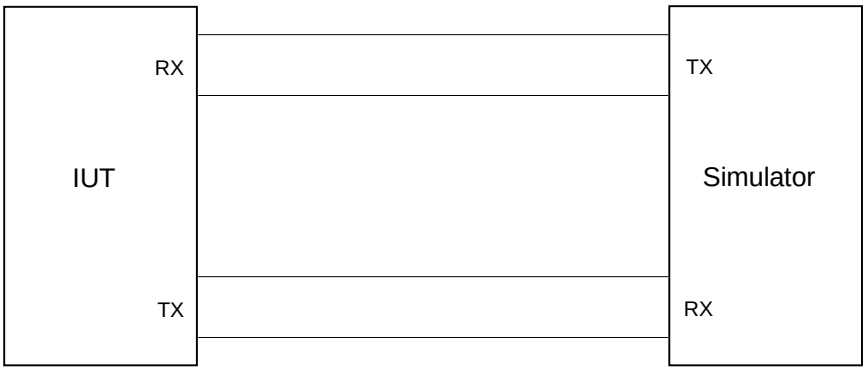


Figure 6: State-matrix test at the user side

System state: Any state F0 to F5.

It is not possible to distinguish between states F1, F2 and F5 or between states F3 and F4, using only layer 1 information at the interface.

IUT suppliers shall provide information how IUT presents status indication (i.e. detected defect conditions corresponding to MPH error indication or recovery from defect condition).

Stimulus: For each initial state, each possible new event indicated.

Stimulus shall be maintained for a time period sufficient to allow the expected state transition.

S_a bits in signals having a frame structure shall contain PRBS pattern.

The test shall be made with both signals:

- AIS_2 Sequence of 512 bits composed of 510 ONEs and 2 binary ZEROs. This sequence to check correct AIS recognition according to CCITT Recommendation O.162 [6].

- AIS_3 Sequence of 512 bits composed of 509 ONEs and 3 binary ZEROs. This sequence to check incorrect AIS recognition according to CCITT Recommendation O.162 [6].

Monitor: The status indication provided by the IUT and the signal transmitted towards the interface.

The final state shall be checked 1 second after the stimulus has been transmitted.

Results: IUT shall react on receipt of AIS_3 with state F3.
IUT shall react on receipt of AIS_2 with state F4.
New state, transmitted signal and primitives sent to the higher layers according to table 5 of ETS 300 011-1 [3].

5.2.3 Interframe (layer 2) time fill

Test applicable for I_A and I_B interfaces.

Purpose: To test the pattern on the D Channel when the IUT does not send frames.

Test configuration:

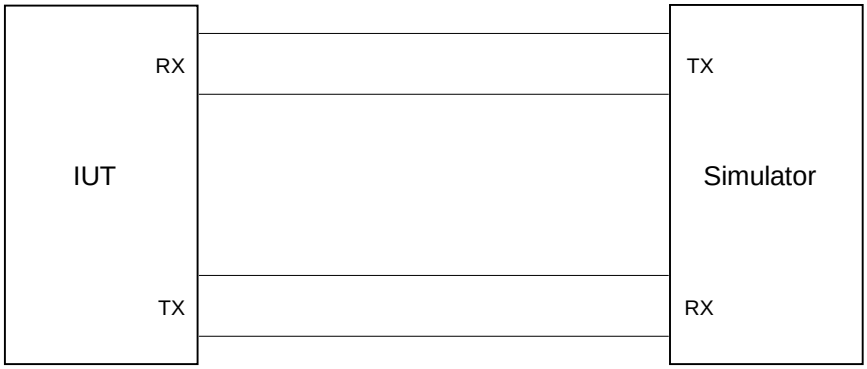


Figure 7: Test of interframe time fill

System state for I_A: State F1.

System state for I_B: State G1.

Stimulus: Normal operational frames with contiguous HDLC flags in the D-channel from the simulator.

Monitor: Pattern on the D Channel (timeslot 16).

Results: Contiguous HDLC flags.

NOTE: An HDLC flag is defined as an octet with a binary pattern 01111110. Therefore contiguous HDLC flags are defined as the consecutive transmission of 8 bit flags. There is no requirement to map the HDLC flag into an octet transmitted in timeslot 16 of one frame.

5.2.4 Frame alignment (without the test of CRC procedure)

Test applicable for I_A and I_B interfaces.

Purpose: To test that IUT correctly executes the frame alignment procedure.

Test configuration:

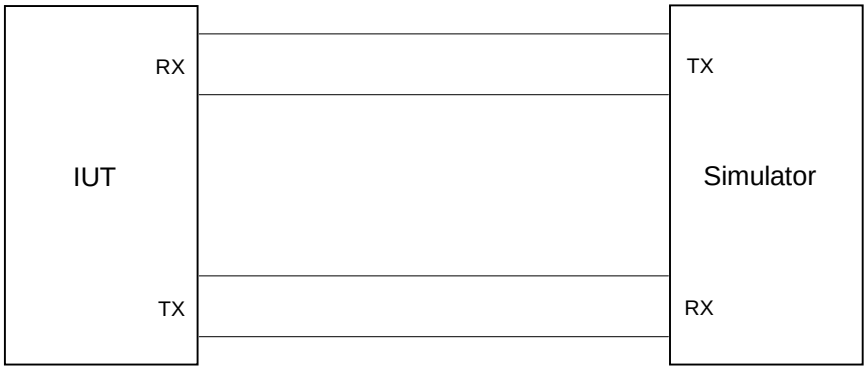


Figure 8: Test of frame alignment procedure

System state: Various states.

Stimulus: Consecutive correct and bad frame sequences (but including correct multiframe alignment signal and correct bits C_1 to C_4) from the simulator, i.e. bit 2 to 8 of timeslot 0 containing the frame alignment signal and bit 2 of timeslot 0 not containing the frame alignment signal, as given below.

The test signal shall not contain any other contiguous group of seven bits which simulates the Frame Alignment Signal.

Monitor: Output signal from the IUT.

Table 1: Result of frame alignment test

Stimulus	Monitor	Comment
BIT 2 = 1, FAS (see note 1) #	NOF	Frame alignment tests.
BIT 2 = 1, /FAS	NOF	
BIT 2 = 1, FAS #	NOF	
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS BIT 2 = 1, FAS #	NOF NOF	
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS BIT 2 = 1, FAS, BIT 2 = 1, FAS #	RAI NOF	
BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS BIT 2 = 1, FAS, BIT 2 = 1, /FAS #	RAI RAI	
BIT 2 = 1, FAS BIT 2 = 0, FAS #	RAI RAI	
BIT 2 = 1, FAS #	NOF	
BIT 2 = 0, FAS, BIT 2 = 1, FAS, BIT 2 = 1, FAS #	NOF	
BIT 2 = 0, FAS, BIT 2 = 0, FAS, BIT 2 = 1, FAS #	NOF	
BIT 2 = 0, FAS, BIT 2 = 0, FAS, BIT 2 = 0, FAS #	RAI or NOF (see note 2)	
BIT 2 = 1, FAS #	NOF	
BIT 2 = 1 FRAME B #	NOF	Correct frame alignment.
6 X FRAME C	RAI -> NOF	Loss of frame alignment and frame alignment with simulated frame alignment word.
FRAME B #	NOF	
4 ms to 8 ms	RAI and back to NOF will occur (if Multiframe Alignment is operating properly), (see note 3). No further RAI shall occur within a time period of 20 ms.	No multiframe alignment on the simulated frame alignment word.
NOTE 1: This stimulus shall be repeated in order to allow clock synchronization of the IUT, the time taken to synchronize may be dependant on the implementation. NOTE 2: RAI or NOF depending on the implementation options described in ETS 300 011-1 [3]. NOTE 3: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.		

5.2.5 CRC multiframe alignment

Test applicable for I_A and I_B interfaces.

Purpose: To test the IUT correctly executes the CRC multiframe alignment.

Test configuration:

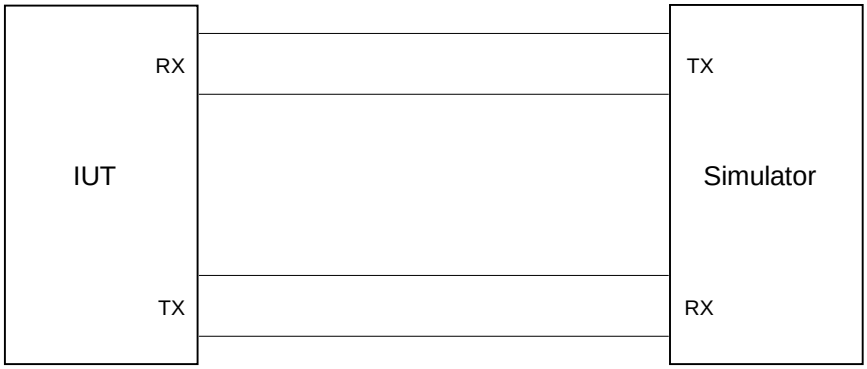


Figure 9: Test of multiframe frame alignment procedure

System state: Various states.

Stimulus: Consecutive correct and bad CRC multiframe alignment signals from the simulator, i.e. bit 1 in frames not containing the frame alignment signal as given below.

Monitor: Output signal from the IUT as given below.

Table 2: Results of multiframe alignment test

Stimulus	**Monitor**	**Comment**
FRAME B # /FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /Fas, BIT 2 = 1 MF A 4 X MF B MF A	(see note) NOF RAI NOF RAI NOF	Initial condition. No multiframe alignment.
37 X MF B	NOF, transition to RAI and back to NOF	
MF A, MF B, MF A, MF B, MF A, MF B MF B # 251	NOF NOF Stable NOF	2 MFAS within 8 ms in the limit of 100 ms. No RAI 500 ms after a loss of multiframe alignment.
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1 MF B	RAI NOF	Initial condition. Correct basic frame alignment but not multiframe.
# 250 MF B	 RAI	No multiframe alignment within 500 ms.
MF A, 4 X MF B MF A, 2 X MF B, MF A MF A, 2 X MF B, 2 X MF A MF B, MF A #	RAI Undefined condition NOF NOF	 Multiframe alignment reached.
NOTE: This stimulus shall be repeated in order to allow clock synchronization of the IUT, the time taken to synchronize may be dependant on the implementation.		

5.2.6 CRC processing

Test applicable for I_A and I_B interfaces.

Purpose: To test the correct execution of CRC calculation, comparison with the received bits C_1 to C_4 and generation of the CRC error report with bit E.

Test configuration:

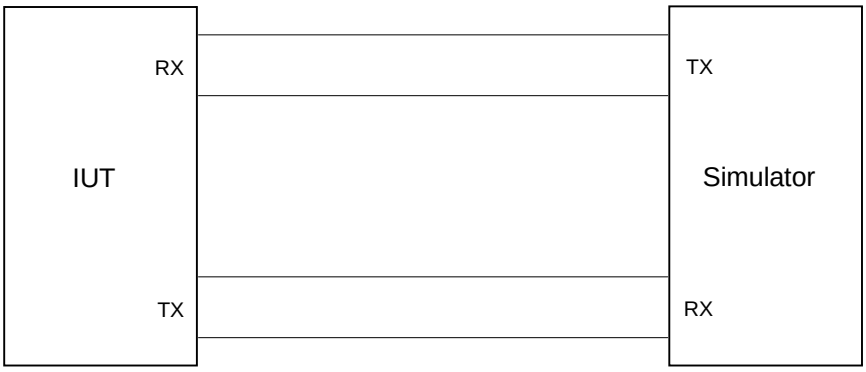


Figure 10: Test of CRC processing

System state for I_A: State F1.

System state for I_B: State G1.

Stimulus: SMF A and SMF B as given below.

Monitor: Output signal, i.e. E bits as given below.

Results: As listed in table 3.

A CRC error report, indicated by an E bit set to ZERO, shall be received within one second after the generation of a SMF in error. Definition of a SMF in error is given in ETS 300 011-1 [3], subclause 5.5.4.

Table 3: Results of CRC processing test

Stimulus	**Monitor**		
	I_A	I_B option 1 (see note 2)	I_B option 2 (see note 2)
SMF A # Repeat more than 1 second	No E bit set to zero	=	=
SMF B SMF A #	One E bit set to zero No E bit set to zero	= =	= =
SMF B, SMF B SMF A # Repeat more than 1 second	Two contiguous E bits set to ZERO No E bit set to zero	=	=
914 X SMF B 86 X SMF A 914 X SMF B SMF A # Repeat more than 1 second	914 contiguous E bits set to zero 914 contiguous E bits set to zero No E bit set to zero	= = =	= = =
915 X SMF B 85 X SMF A 915 X SMF B SMF A #	Temporarily RAI (see note 3)	 = (see note 1) =	 = (see note 1) =
/FAS, BIT 2 = 1, /FAS, BIT 2 = 1, /FAS, BIT 2 = 1 #	RAI, no E bit set to zero RAI, no E bit set to zero	= =	E bit set to 0 plus RAI E bit set to 0 plus RAI

NOTE 1: Due to possible delay temporary RAI may not be detected at I_B.
NOTE 2: Monitor for I_B option 1 and option 2 is considered to be the same as for I_A case (=) unless otherwise stated.
NOTE 3: The vertical bar indicates that the given monitor result shall appear at least once during application of the stimulus.

5.3 Electrical characteristics tests

5.3.1 Specifications at the output ports

5.3.1.1 Bit rate when unsynchronized

Test applicable for I_A and I_B interface.

Purpose: To measure the bit rate when the IUT (Implementation Under Test) is not synchronized.

Test configuration:

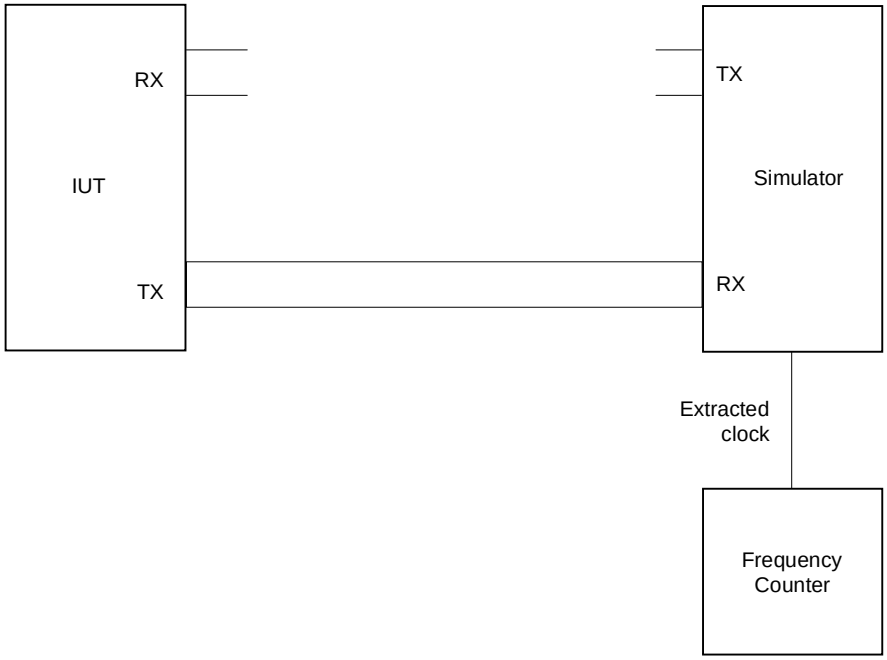


Figure 11: Measurement of bit rate when IUT is unsynchronized

System state for I_A: State F3, IUT transmitting RAI.

System state for I_B: State G4, IUT transmitting AIS.

Stimulus: No signal from the simulator to the input supplying timing.

I_A case: Signal having an amplitude 20 dB below nominal level according to the criterion of LOS in subclause 6.1, ETS 300 011-1 [3].

I_B case: interruption of the signal at any point between NT1 and ET or at the interface I_A of a PTNX supplying timing.

Monitor: Measure bit rate with frequency counter, as extracted by the timing recovery circuit of the network simulator.

The measurement overall accuracy shall be better than 1 % of the bit rate tolerance.

Results: I_A interface - For IUT as defined in subclause 5.8 of ETS 300 011-1 [3], foreseen to act as a master, the corresponding bit rate shall be in the range 2 048 kbit/s ± 32 ppm, in all other cases the corresponding bit rate shall be in the range 2 048 kbit/s ± 50 ppm.
I_B interface, T reference point - The corresponding bit rate shall be in the range 2 048 kbit/s ± 50 ppm.
I_B interface, S reference point - The corresponding bit rate shall be in the range 2 048 kbit/s ± 32 ppm (as defined in subclause 5.8 of ETS 300 011-1 [3]).

5.3.1.2 Pulse shape and amplitude of a mark (pulse)

Test applicable for I_A and I_B interfaces.

Purpose: To check the conformance of the shape of all mark pulses, irrespective of the polarity, transmitted by IUT.

Test configuration:

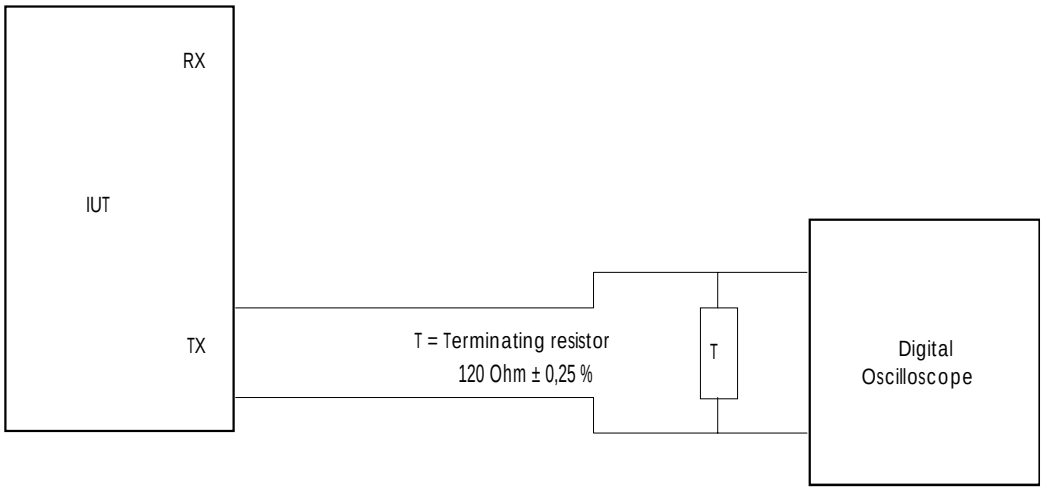


Figure 12: Measurement of pulse shape and amplitude

System state for I_A: Any state F1 to F5.

System state for I_B: Any state G1 to G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: The marks transmitted by IUT.

Results: Both positive and negative pulse shall be within the mask of figure 8 of ETS 300 011-1 [3], assuming V = 100 %, to be 3 V.

NOTE 1: The measurement overall accuracy should be better than 1 % of the nominal amplitude of a mark (i.e. 3V).

NOTE 2: All the measurements should be performed using a digital oscilloscope in dc mode.

NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependant on the energy of the positive and the negative pulses.

5.3.1.3 Peak voltage of a space (no pulse)

Test applicable for I_A and I_B interfaces.

Purpose: To check the absence of any voltage higher than 10 % of the nominal peak value of a pulse during the transmission of a space (no pulse).

Test configuration:

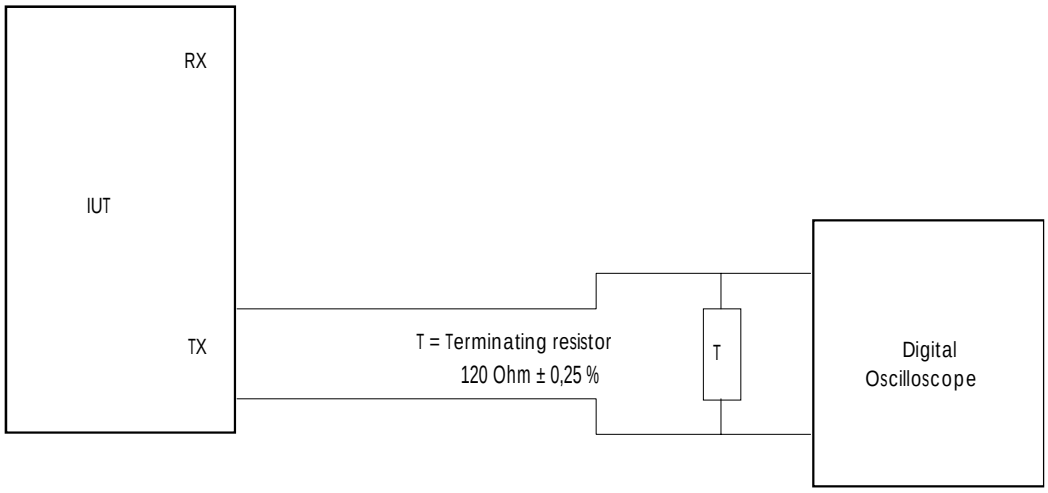


Figure 13: Measurement of voltage of a space

System state for I_A: Any state F1 to F5.

System state for I_B: Any state G1 to G5.

Stimulus: Relevant signals defined to force IUT to enter the appropriate state.

Monitor: The spaces transmitted by IUT.

Results: The bit interval corresponding to a transmission of a space shall not present voltages higher than ± 0,3 V.

NOTE 1: The measurement overall accuracy should be better than 1 % of the nominal amplitude of a mark (i.e. 3V).

NOTE 2: All the measurements should be performed using a digital oscilloscope in dc mode.

NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

5.3.1.4 Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval

Test applicable for I_A and I_B interfaces.

Purpose: To check the balance between the amplitude of positive and negative pulses (measured at the centre of the pulse interval).

Test configuration:

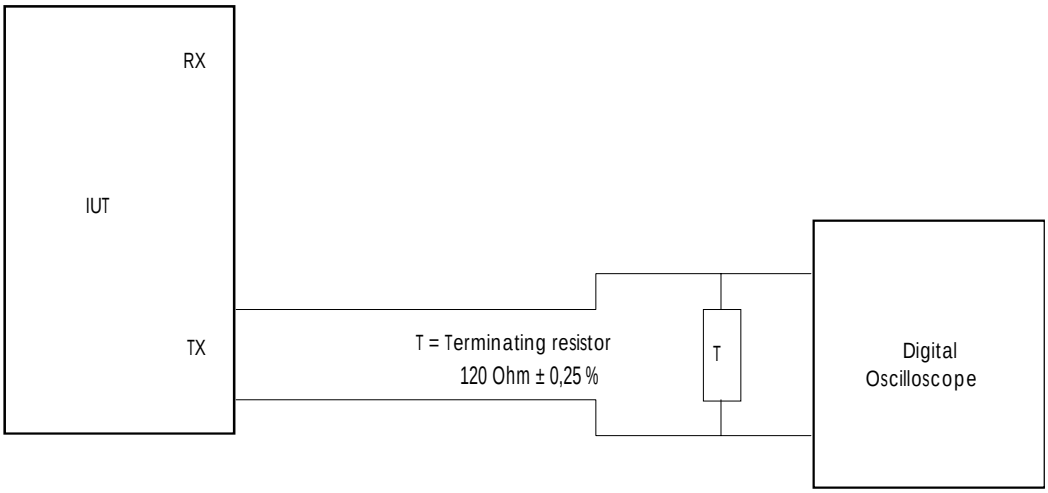


Figure 14: Measurement of ratio of the amplitudes of positive and negative pulses

System state for I_A: Any state F1 to F5.

System state for I_B: Any state G1 to G5.

Stimulus: Relevant signal defined to force IUT to enter the appropriate state.

Monitor: The amplitude of positive and negative pulses (measured at the centre of the pulse interval).

To determine the centre of a pulse:

- Determine the level equal to half the nominal pulse amplitude (i.e. 1,5 V), where the width of the actual pulse shall be measured;
- A point equal to half the value of the measured width of the pulse is the centre of the pulse.

Results: The ratio between the amplitudes shall be within the range from 0,95 to 1,05.

NOTE 1: The measurement overall accuracy should be better than 0,25 % of the nominal ratio.

NOTE 2: All the measurements should be performed using a digital oscilloscope in dc mode.

NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

5.3.1.5 Ratio of the widths of positive and negative pulses at the nominal half amplitude

Test applicable for I_A and I_B interfaces.

Purpose: To check the balance between the time duration of pulses of different polarity (measured at the half of the nominal pulse amplitude).

Test configuration:

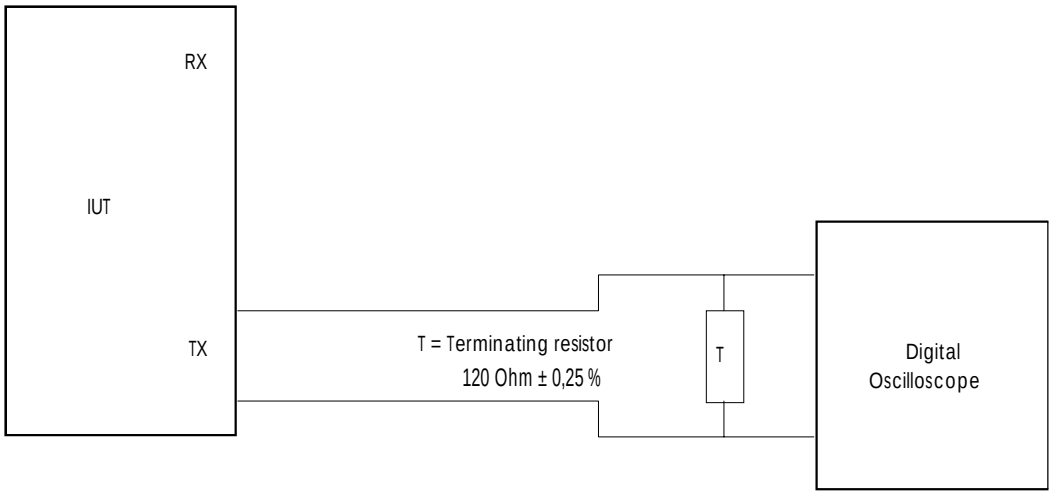


Figure 15: Measurement of ratio of the widths of positive and negative pulses

System state for I_A: Any state F1 to F5.

System state for I_B: Any state G1 to G5.

Stimulus: Relevant signal defined to force IUT to enter the appropriate state.

Monitor: The time duration of positive and negative pulses measured at the nominal half of the pulse amplitude (i.e. 1,5 V).

Results: The ratio between the time durations shall be within the range from 0,95 to 1,05.

NOTE 1: The measurement overall accuracy should be better than 1 % of the nominal ratio.

NOTE 2: All the measurements should be performed using a digital oscilloscope in dc mode.

NOTE 3: Fixed zero level approach should be chosen taking into account the transformerless implementation of the interface. Such an implementation might not be able to establish a floating zero level which is dependent on the energy of the positive and the negative pulses.

5.3.1.6 Return loss at the output port

Test applicable for I_A and I_B interfaces.

Purpose: To measure the return loss of the receiving section of IUT.

Test configuration:

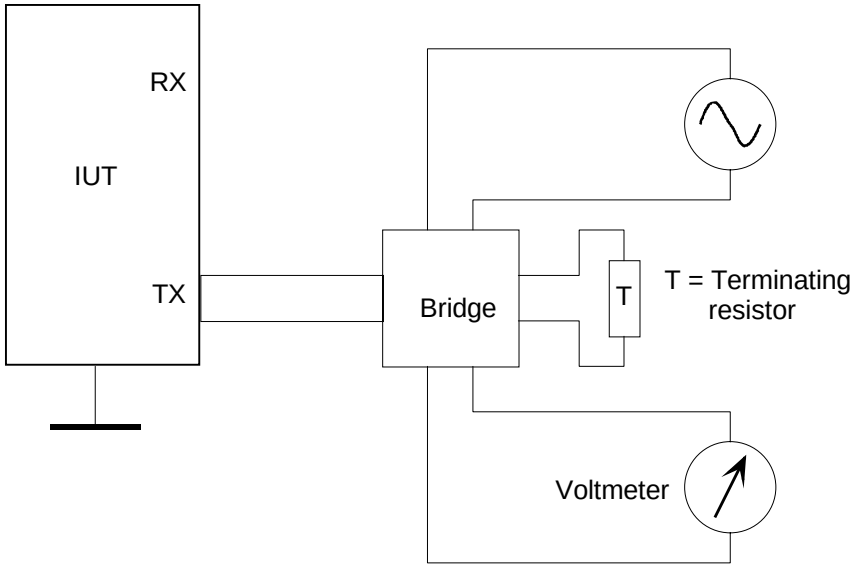


Figure 16: Measurement of output return loss

System state: Powered.

Stimulus: Sinusoidal signal of 3 V peak at the input port, and frequency variable between 51 kHz and 3 072 kHz.

Monitor: Voltage measured across the bridge, representing a terminating resistor of 120 Ω, using a selective voltmeter with bandwidth less than 1 kHz.

Results: The measured return loss shall comply with table 4:

Table 4:

Frequency range	Return loss
51 kHz to 102 kHz	6 dB
102 kHz to 3 072 kHz	8 dB

NOTE: The characteristics of the generator and of the voltmeter may be different depending on the implementation of the bridge. However, the total error of the test set-up should be less than 0,5 dB in the range between 10 and 20 dB. When connected to a 120 Ω ± 0,25 % resistor the measured return loss of the bridge should be 20 dB higher than the specified limits for the IUT.

5.3.1.7 Impedance towards ground of the transmitter

Test applicable for I_A and I_B interfaces.

Purpose: To check IUT transmitter output impedance towards ground.

Test configuration:

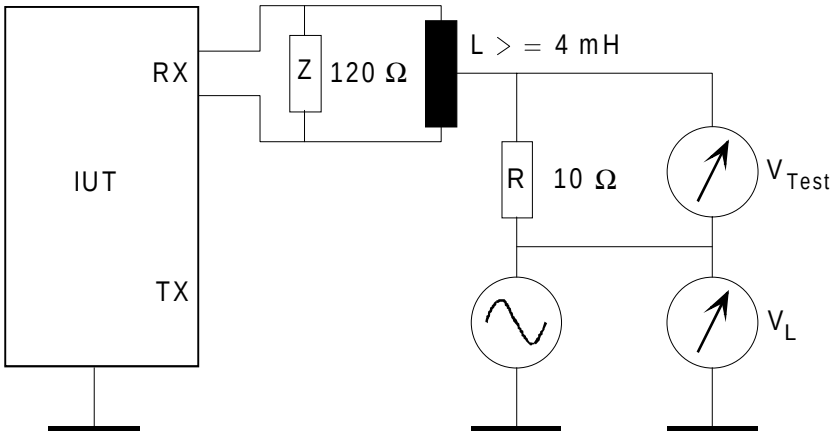


Figure 17: Measurement of impedance towards ground of the receiver

System state for I_A: State F3.

System state for I_B: State G5.

Stimulus: Sinusoidal test signal voltage V_L shall be 2 V_{rms}.

The test signal shall be applied at any frequency chosen in the range 10 Hz - 1 MHz.

Monitor: Voltage of V_{Test}.

NOTE: Frequency selective level measuring equipments should be used. wideband measuring equipment is not suitable for devices measuring V_{Test} and V_L.

Results: 10 Hz ≤ f ≤ 500 kHz: Voltage V_{Test} ≤ 20 mV_{rms}.
500 kHz ≤ f ≤ 1 MHz: Voltage V_{Test} ≤ 20 mV_{rms} at 500 kHz increasing with a slope of 6 dB/octave.

5.3.2 Specifications at the input ports

5.3.2.1 Receiver sensitivity and input port immunity against reflections

Test applicable for I_A and I_B interfaces.

Purpose: To check the input port immunity against an interfering signal combined with the input signal with a cable attenuation of maximum 6 dB.

Test configuration:

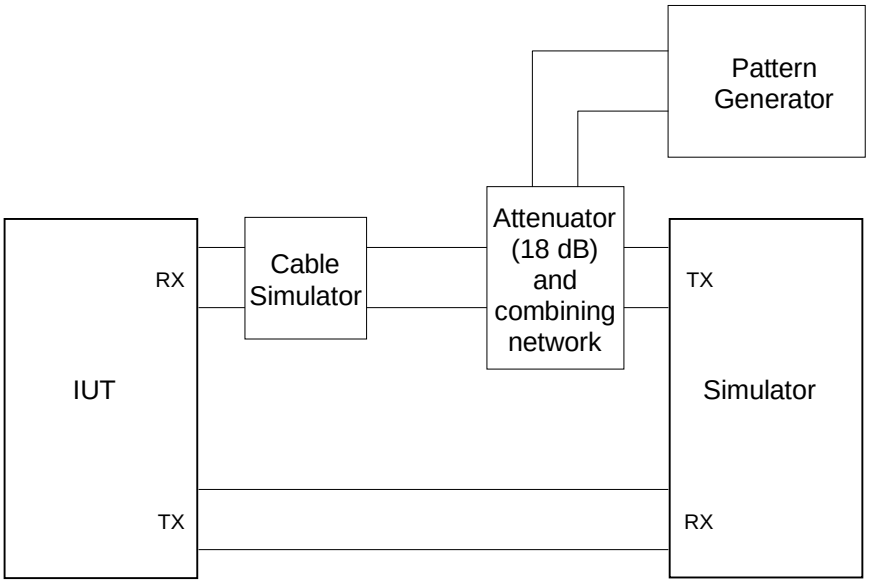


Figure 18: Measurement of receiver sensitivity

The output signal of the network simulator shall conform to a pulse shape as defined in figure 8 of ETS 300 011-1 [3] when sending normal operational frames. The binary content of the timeslots 1 to 31 shall comply with the 2^{15}-1 PRBS as defined in CCITT Recommendation O.151 [1].

Due to the lack of definition of the return loss for transmitters in the previous version of this ETS, the simulator output shall provide maximum reflection (i.e. low output impedance to simulate simple transmitter implementations).

The interfering signal shall conform to a pulse shape as defined in figure 8 of ETS 300 011-1 [3], encoded HDB3. Its binary content shall comply with the 2^{15}-1 PRBS as defined in CCITT Recommendation O.151 [1]. The bit rate shall be within the limits specified ETS 300 011-1 [3] (± 50 ppm) and shall not be synchronized to the output signal of the simulator.

The interfering signal shall be combined with the main signal in a combining network having an impedance of 120 Ω, with zero loss in the main path and an attenuation of the interference path of 18 dB.

The conformance of IUT shall be verified in the following two test conditions:

a) without cable simulator. The amplitude of the signal transmitted by the simulator shall be 3,3 V (nominal amplitude plus 10 %);

b) with cable simulator having 6 dB attenuation measured at 1 024 kHz and following a $\sqrt{f}$ law. The amplitude of the signal transmitted by the simulator shall be 2,7 V (nominal amplitude minus 10 %).

System state for I_A: State F1.

System state for I_B: State G1.

Stimulus: NOFs with a 2^{15}-1 PRBS pattern in timeslots 1 to 31.

A 2^{15}-1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s).

The test shall be repeated with the wires at the IUT input reversed.

Monitor: Monitor the CRC error information report transmitted by IUT.

Results: No E bit set to 0 shall be received for a time period of at least one minute.

NOTE 1: The $\sqrt{f}$ law of a cable simulator should apply in a frequency range 100 kHz to 10 MHz.

NOTE 2: This test relies on the correct operation of the CRC error information report by IUT.

5.3.2.2 Return loss at the input port

Test applicable for I_A and I_B interfaces.

Purpose: To measure the return loss of the receiving section of IUT.

Test configuration:

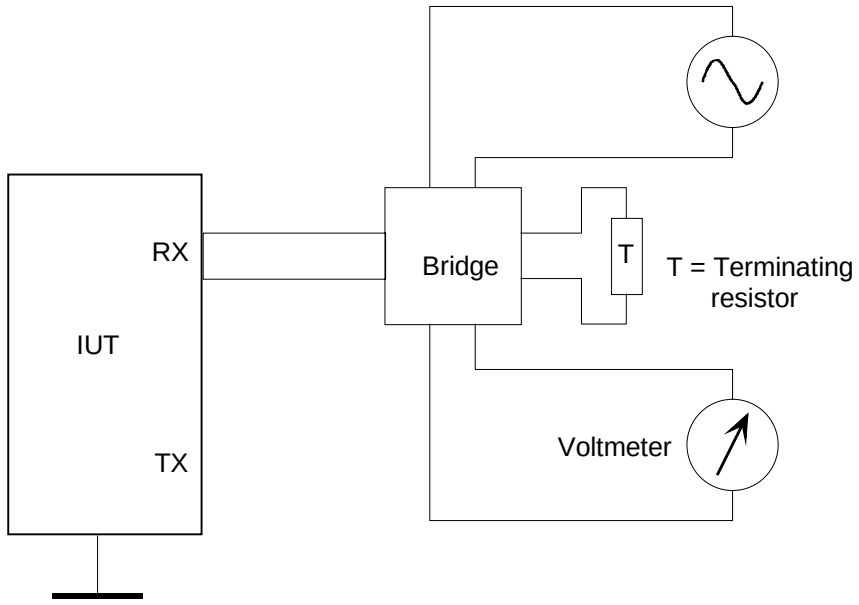


Figure 19: Measurement of input return loss

System state: Powered.

Stimulus: Sinusoidal signal of 3 V peak at the input port, and frequency variable between 51 kHz and 3 072 kHz.

Monitor: Voltage measured across the bridge, representing a terminating resistor of 120 Ω, using a selective voltmeter with bandwidth less than 1 kHz.

Results: The measured return loss shall comply with table 5:

Table 5:

Frequency range	Return loss
51 kHz to 102 kHz	12 dB
102 kHz to 2 048 kHz	18 dB
2 048 kHz to 3 072 kHz	14 dB

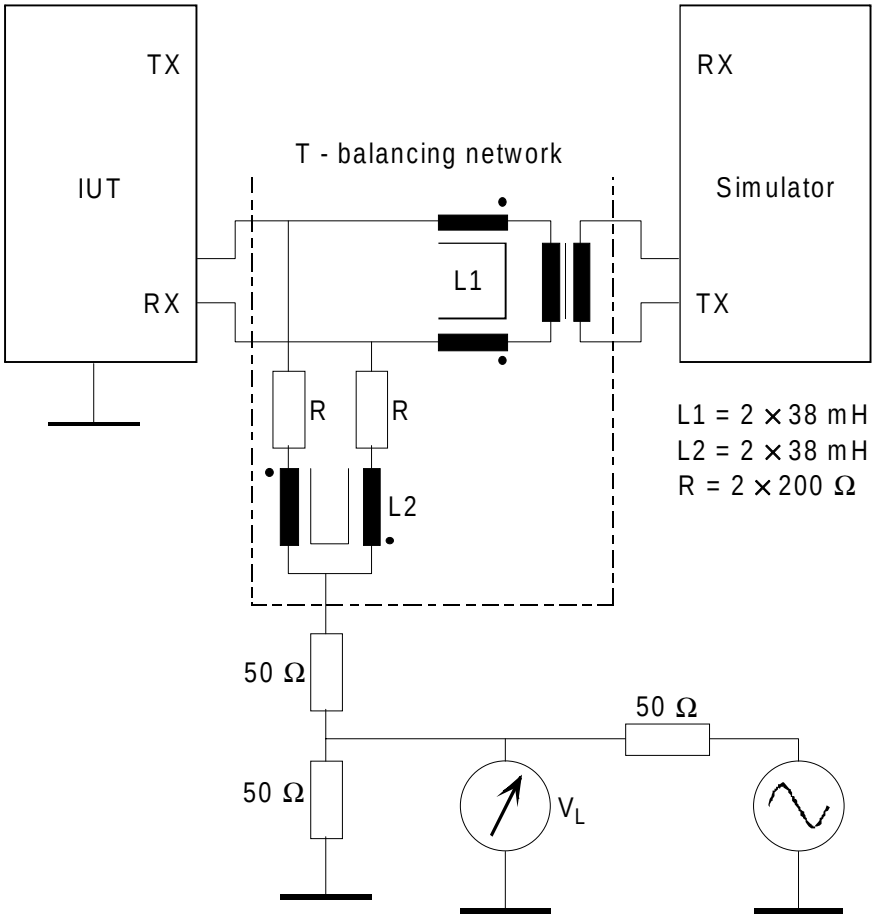
NOTE: The characteristics of the generator and of the voltmeter may be different depending on the implementation of the bridge. However, the total error of the test set-up should be less than 0,5 dB in the range between 10 and 20 dB. When connected to a 120 Ω ± 0,25 % resistor the measured return loss of the bridge should be 20 dB higher than the specified limits for the IUT.

5.3.2.3 Tolerable longitudinal voltage

Test applicable for I_A and I_B interfaces.

Purpose: To check minimum tolerance to longitudinal voltage at input ports.

Test configuration:



NOTE: The transformer has been added to provide earth decoupling between the IUT and the simulator.

Figure 20: Measurement of tolerable longitudinal voltage

System state for I_A: State F1.

System state for I_B: State G1.

Stimulus: NOFs with a 2^{15}-1 PRBS pattern in timeslots 1 to 31. A 2^{15}-1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s).

A longitudinal sinusoidal voltage V_L of 2Vrms shall be applied for 2 seconds at any frequency chosen in the range 10 Hz - 30 MHz.

Monitor: Frames transmitted by IUT.

Results: IUT shall remain in state F1 (G1 for interface I_B), no CRC error information report shall be detected by the simulator.

5.3.2.4 Impedance towards ground of the receiver

Test applicable for I_A and I_B interfaces.

Purpose: To check IUT receiver input impedance towards ground.

Test configuration:

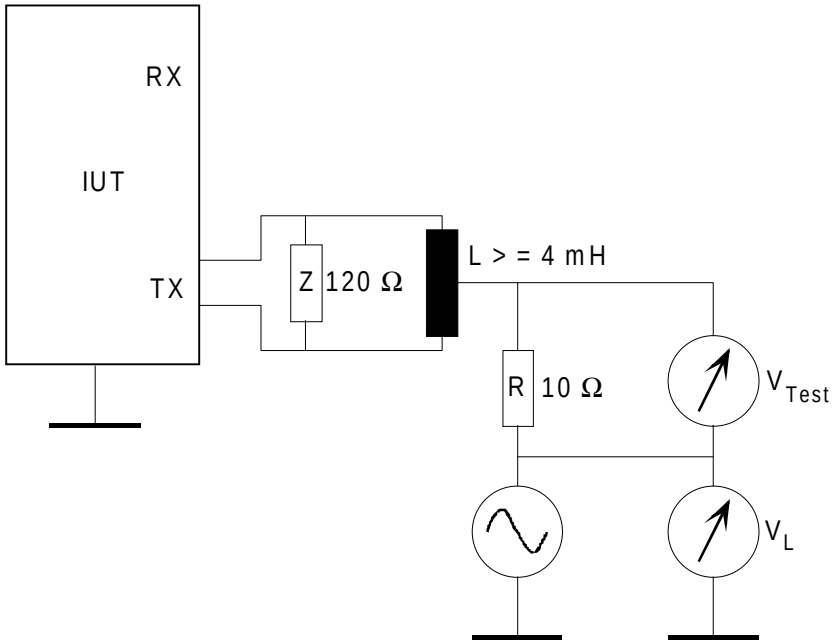


Figure 21: Measurement of impedance towards ground of the transmitter

System state for I_A: State F3.

System state for I_B: State G5.

Stimulus: Sinusoidal test signal voltage V_L shall be 2 Vrms.

The test signal shall be applied at any frequency chosen in the range 10 Hz - 1 MHz.

Monitor: Voltage of V_{Test}.

Results: 10 Hz ≤ f ≤ 500 kHz: Voltage $V_{Test} \leq 20\ mV_{rms}$.
500 kHz ≤ f ≤ 1 MHz: Voltage $V_{Test} \leq 20\ mV_{rms}$ at 500 kHz increasing with a slope of 6 dB/octave.

5.4 Jitter

5.4.1 Minimum tolerance to jitter and wander at inputs

Test applicable for I_A and I_B interfaces

Purpose: To check the ability of IUT to tolerate on the 2 048kbit/s incoming signal a sinusoidal jitter/wander in accordance with subclauses 8.4.2 and 8.4.4 of ETS 300 011-1 [3].

Test configuration:

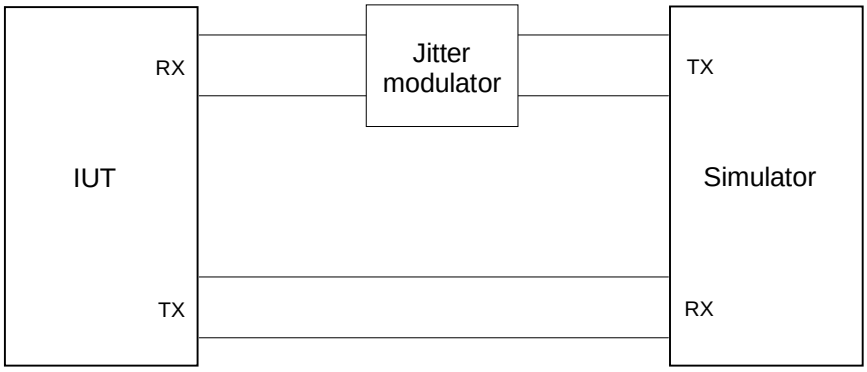


Figure 22: Measurement of jitter and wander tolerance

System state for I_A: State F1.

System state for I_B: State G1.

Stimulus: NOFs with jitter/wander according to table 1, subclause 5.4.2 and with a 2^{15}-1 PRBS pattern in timeslots 1 to 31. A 2^{15}-1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s). This signal shall be applied with following two conditions:

a) without cable simulator. The amplitude of the signal transmitted by the simulator shall be 3,3 V (nominal amplitude plus 10 %);

b) with cable simulator having 6 dB attenuation measured at 1 024 kHz and following a $\sqrt{f}$ law. The amplitude of the signal transmitted by the simulator shall be 2,7 V (nominal amplitude minus 10 %).

Other inputs in state F3 (G3 for interface I_B).

This test has to be performed for the following frequencies:

- for IUT to be connected to T reference point, simulator providing the nominal frequency plus 1 ppm and minus 1 ppm;
- for IUT to be connected to S reference point, simulator providing the nominal frequency plus 32 ppm and minus 32 ppm;
- for interface at IUT for PTNX interconnection, simulator providing the nominal frequency plus 32 ppm and minus 32 ppm.

For implementation with free running clock frequency accuracy better than ± 1 ppm, as declared by the equipment supplier the stimulus shall be in the range ± 1 ppm.

Points A1-f2 and A2-f4 shall be measured. For the range between A0-f0 to A1-f1 the jitter behaviour can be determined from the Q factor.

For I_A interface multi-access IUT case:

- on each access declared to be capable of extracting synchronization from the network this test shall be performed by imposing a maximum wander of 20,5 UI while all other accesses are in state F3 or F4;

- on each pair of accesses declared to be capable of extracting synchronization from the network, when evaluating the effect of wander, the amount of phase difference (i.e. 20,5 UI) shall be given to each access, but with opposite phase, i.e. the maximum relative phase difference is 41 UI.

For an access not declared to be capable of extracting synchronization from the network, the test shall be made in conjunction with an access capable of extracting synchronization. When evaluating the effect of wander, the amount of phase difference (i.e. 20,5 UI) shall be given to each access, but with opposite phase, i.e. the maximum relative phase difference is 41 UI.

Monitor: The frames transmitted by IUT.

Results: IUT shall remain in state F1 (G1 for interface I_B), no CRC error information report shall be detected by the simulator.

IUT declared suitable for leased lines applications shall tolerate a jitter A1 of 1,5 UI with corresponding f2 of 2,4 kHz (see subclause 8.4.2 of ETS 300 011-1 [3]).

NOTE: This test relies on the correct operation of the CRC error information report by IUT.

5.4.2 Output jitter

5.4.2.1 Output jitter with jitter at the input supplying timing

Test applicable for I_A interface.

Purpose: To measure the jitter generated from IUT in the presence of input jitter when IUT is synchronized by the simulator.

Test configuration:

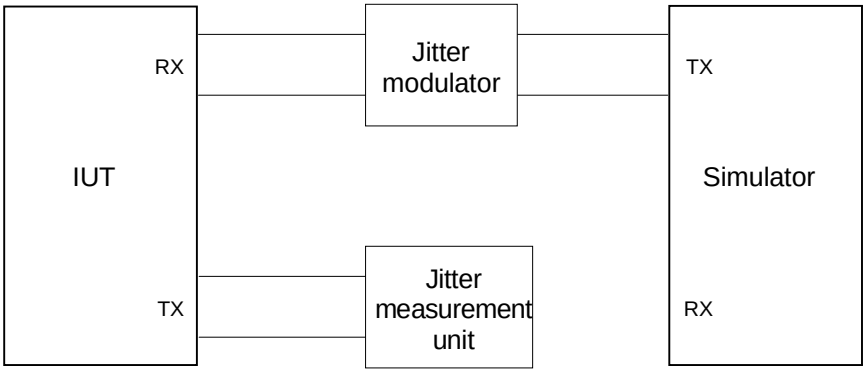


Figure 23: Measurement of output jitter

The jitter measurement shall be done using equipment that has an external timing reference to the jitter measurement set which has no phase variation energy in the jitter region under test.

System state: State F1.

Stimulus: Normal operational frames with jitter according to subclause 8.4.3 of ETS 300 011-1 [3], provided to the synchronizing input and with a 2^{15}-1 PRBS pattern in timeslots 1 to 31. A 2^{15}-1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s). This signal shall be applied with following two conditions:

a) without cable simulator. The amplitude of the signal transmitted by the simulator shall be 3,3 V (nominal amplitude plus 10 %);

b) with cable simulator having 6 dB attenuation measured at 1 024 kHz and following a $\sqrt{f}$ law. The amplitude of the signal transmitted by the simulator shall be 2,7 V (nominal amplitude minus 10 %).

Interface at IUT for PTNX interconnection shall tolerate a jitter A1 of 1,5 UI with corresponding f2 of 2,4 kHz (see ETS 300 011-1 [3], subclause 8.4.2.2).

a) For IUT to be connected to T reference point only.

This test shall be performed for three different cases:

- simulator providing the nominal frequency;
- simulator providing the nominal frequency plus 1 ppm;
- simulator providing the nominal frequency minus 1 ppm.

b) For IUT to be connected to S reference point and for IUT used for PTNX interconnections.

This test shall be performed for three different cases:

- simulator providing the nominal frequency;
- simulator providing the nominal frequency plus 32 ppm;
- simulator providing the nominal frequency minus 32 ppm.

For interface at IUT for PTNX interconnection, having implementation with free running clock frequency accuracy better than ± 1 ppm, as declared by the equipment supplier, the stimulus shall be in the range ± 1 ppm.

Monitor: The jitter extracted from the signal transmitted by the IUT measured at all outputs.

Results: The peak to peak jitter shall comply with table 6:

Table 6:

Measurement filter bandwidth		**Output jitter**
Lower cut off (high pass)	Upper cut off (low pass)	UI peak-to-peak (maximum)
20 Hz (see note 1)	100 kHz	1,1 UI (see note 3)
400 Hz (see note 2)	100 kHz	0,11 UI
NOTE 1: In case of multi-access IUT the lower cut off frequency shall be 4 Hz. NOTE 2 In case of multi-access IUT the lower cut off frequency shall be 40 Hz. NOTE 3: Interface at IUT for PTNX interconnection shall not exceed 1,6 UI when measured with a lower cut off (high pass) at 4 Hz high pass (see subclause 8.4.3 of ETS 300 011-1 [3]).		

5.4.2.2 Output jitter at network side

Test applicable for I_B interface.

Purpose: To measure the jitter generated from the IUT.

Test configuration:

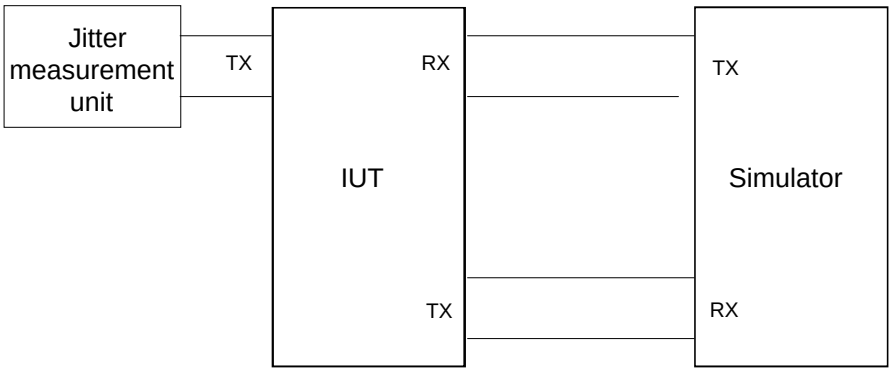


Figure 24: Measurement of output jitter at the network side of the NT

The jitter measurement shall be done using equipment that has an external timing reference to the jitter measurement set which has no phase variation energy in the jitter region under test.

System state: State G1.

Stimulus: a) For test at interface at T reference point:

Normal operational frames without jitter provided by the simulator (e.g. connected at V3 reference point to the digital section) and with a 2^{15}-1 PRBS pattern in timeslots 1 to 31. A 2^{15}-1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s). This signal shall be applied with following two conditions:

- without cable simulator. The amplitude of the signal transmitted by the simulator shall be 3,3 V (nominal amplitude plus 10 %);
- with cable simulator having 6 dB attenuation measured at 1 024 kHz and following a $\sqrt{f}$ law. The amplitude of the signal transmitted by the simulator shall be 2,7 V (nominal amplitude minus 10).

This test shall be performed for three cases:

- simulator providing the nominal frequency;
- simulator providing the nominal frequency plus 1 ppm;
- simulator providing the nominal frequency minus 1 ppm.

b) For test at interface at S reference point:

NOFs with jitter according to table 1, subclause 5.4.2, provided to the synchronizing input of IUT (i.e. I_A interface at T reference point) and with a 2^{15} - 1 PRBS pattern in timeslots 1 to 31. A 2^{15} - 1 PRBS shall fill continuously all the frame except timeslot 0 (net bit rate 1 984 kbit/s).

This test shall be performed for three cases:

- simulator providing the nominal frequency;
- simulator providing the nominal frequency plus 32 ppm;
- simulator providing the nominal frequency minus 32 ppm.

Monitor: The jitter extracted from the signal transmitted by the IUT.

Results: The peak to peak jitter shall comply with table 7:

Table 7:

Measurement filter bandwidth		**Output jitter**
Lower cut off (high pass)	Upper cut off (low pass)	UI peak-to-peak
20 Hz	100 kHz	≤ 1,0 UI
18 kHz	100 kHz	≤ 0,2 UI

5.5 Power feeding

5.5.1 Provision of power and feeding voltage

Test applicable for I_A interface.

Purpose: To test the provision of power by the IUT.

Test configuration:

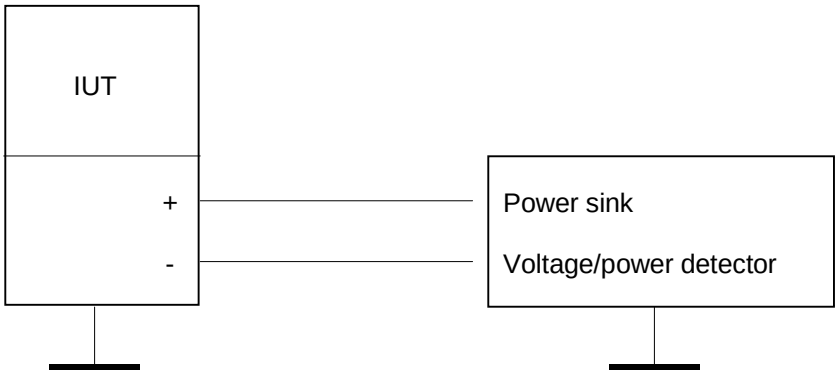


Figure 25: Measurement of provided power and feeding voltage

System state: Any state F1 to F6.

Stimulus: Power on at IUT; test power sink connected to power interface.

Result: Open circuit voltage: Within the range of - 20 V to - 57 V. The voltage, when power up to 10 W is drawn by the power sink shall be in the range of - 20 V to - 57 V.

If one of the wires is connected to ground, then the polarity of the other wire relative to ground shall be negative.

5.5.2 Protection against short circuit

Test applicable for I_A interface.

Purpose: To verify the ability of the power source to withstand a short circuit condition.

Test configuration:

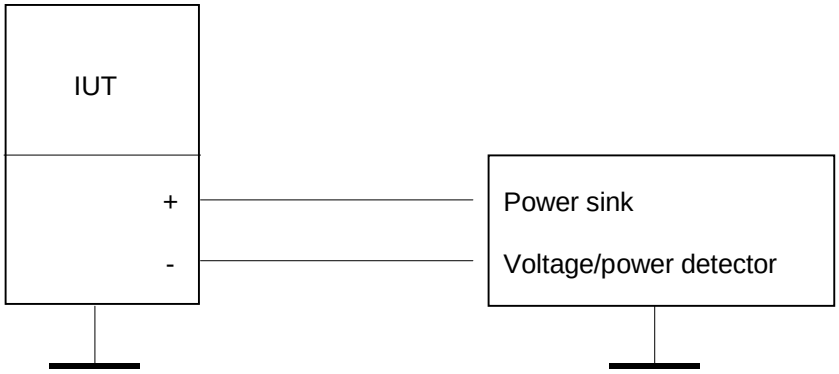


Figure 26: Test of protection against short circuit

System state: Any state F1 to F5.

Stimulus: 1) Load equal to 10 W.

2) Short circuit (five minutes).

3) Load equal to 10 W.

4) Wait one minute.

Result: Output voltage after step 4) shall be in the range -20 V to -57 V.

NOTE: The replacement of a broken fuse is permissible.

5.5.3 Protection against overload

Test applicable for I_A interface.

Purpose: To verify the ability of the power source to withstand an overload condition.

Test configuration:

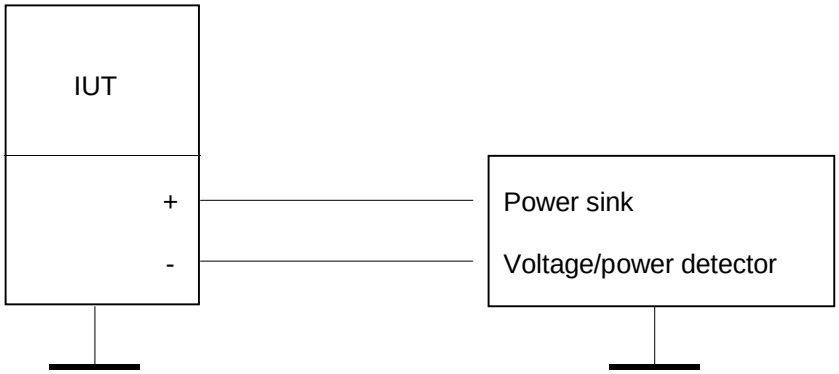


Figure 27: Test of overload conditions

System state: Any state F1 to F5.

Stimulus: 1) Load equal to 10 W, measure the voltage.

2) Increase the load for five minutes to 15 W calculated with the voltage measured in step 1.

3) Load as in step 1 for 1 minute.

4) Load equal to 10 W.

Result: Output voltage after step 4 shall be in the range -20 V to -57 V.

5.5.4 Power consumption and interchange of wires

Test applicable for I_B interface.

Purpose: To verify that the power consumption is within the specified limits and that no damage shall occur in case of interchange of the power feeding wires.

Test configuration:

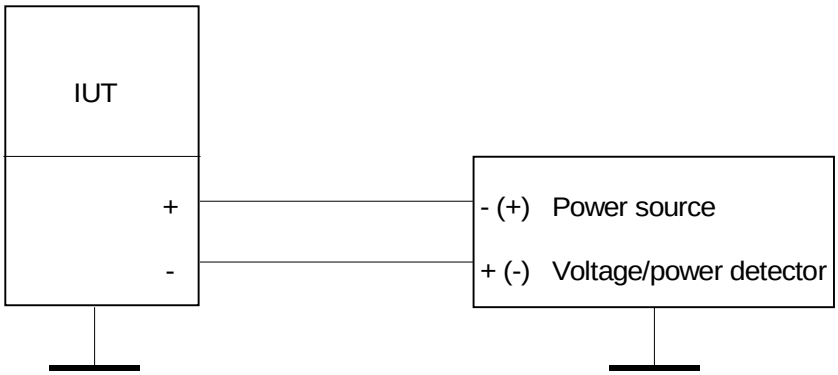


Figure 28: Measurement of power consumption

System state: Any state G1 to G5.

Stimulus: 1) Feeding voltage - 20 V to - 57 V (1 minute).

2) Feeding voltage + 20 V to + 57 V (5 minutes).

3) Feeding voltage - 20 V to - 57 V.

Result: The power drawn by IUT shall not exceed 10 W. IUT shall be able to operate correctly when fed in steps 1 and 3.

History

Document history			
April 1996	First Edition		
November 1996	Public Enquiry	PE 117:	1996-11-04 to 1997-02-28
December 1997	Vote	V 9809:	1997-12-30 to 1998-02-27