



## **Surface Mount Technology (SMT) Requirements for Embedded Communication Modules For Machine To Machine Communications**

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Reference

DGS/SMT-001

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Keywords

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**ETSI**

650 Route des Lucioles  
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C  
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## Foreword

This Group Specification (GS) has been produced by ETSI Industry Specification Group (ISG) Surface Mount Technique (SMT).

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## Modal verbs terminology

In the present document "**shall**", "**shall not**", "**should**", "**should not**", "**may**", "**may not**", "**need**", "**need not**", "**will**", "**will not**", "**can**" and "**cannot**" are to be interpreted as described in clause 3.2 of the [ETSI Drafting Rules](#) (Verbal forms for the expression of provisions).

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## Introduction

The goal of the present document is to specify a form factor for Surface Mount Technology (SMT) based communication modules for devices supporting services across multiple vertical markets and not one specific market segment.

The present document reflects the current state for M2M and connected device design and attempts to address future needs.

---

# 1 Scope

This present document proposes mechanical and electrical requirements for wireless module implementations. This includes the SMT pad layout and common interface assignments for essential pads including some general electrical characteristics. Certain aspects such as z-height, shielding geometry and weight are not defined by the present document.

The SMT module pad configurations defined in the present document are primarily intended to allocate specific pad functionalities that need to be routed on the host device to the respective pads on the SMT module. Although many interfaces may be defined in the various pad configurations, it does not necessarily imply that all interfaces need to be supported at the same time. The assigned allocations are intended to enable the module supplier and host device integrator to design compatible circuits with aligned pad assignments as specified.

---

# 2 References

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references only the cited version applies. For non-specific references, the latest version of the referenced document (including any amendments) applies.

Referenced documents which are not found to be publicly available in the expected location might be found at <http://docbox.etsi.org/Reference>.

NOTE: While any hyperlinks included in this clause were valid at the time of publication, ETSI cannot guarantee their long term validity.

## 2.1 Normative references

The following referenced documents are necessary for the application of the present document.

- [1] ISO/IEC 7816-3: " Identification cards -- Integrated circuit cards -- Part 3: Cards with contacts -- Electrical interface and transmission protocols".
- [2] ETSI TS 102 221: "Smart Cards; UICC-Terminal interface; Physical and logical characteristics".
- [3] USB 2.0 Specification (April 2000): "Universal Serial Bus Specification, Revision 2.0".

NOTE: Available from [http://www.usb.org/developers/docs/usb20\\_docs](http://www.usb.org/developers/docs/usb20_docs).

- [4] USB 2.0 Specification: "HSIC - High-Speed Inter-Chip USB Electrical Specification", Version 1.0 (September 23, 2007), plus HSIC ECN Disconnect Supplement to High-Speed Inter-Chip Specification Revision 0.94 (September 20, 2012).
- [5] USB 3.1 Specification (July 2013): "Universal Serial Bus 3.1 Specification".

NOTE: Available from <http://www.usb.org/developers/docs/>.

- [6] PCI-SIG: "PCI Express M.2 Specification", Revision 1.0, December 12, 2013.

NOTE: Available from [https://www.pcisig.com/specifications/pciexpress/M.2\\_Specification/](https://www.pcisig.com/specifications/pciexpress/M.2_Specification/).

- [7] mipi alliance: "M-PHY® Specification", version 2.0, April 4, 2012.

NOTE: Available from: <http://mipi.org/specifications/physical-layer>.

- [8] ETSI TS 124 008: "Digital cellular telecommunications system (Phase 2+); Universal Mobile Telecommunications System (UMTS); LTE; Mobile radio interface Layer 3 specification; Core network protocols; Stage 3 (3GPP TS 24.008 Release 12)".

- [9] mipi alliance: "Serial Low-power Inter-chip Media Bus (SLIMbus®) Specification".
- NOTE: Available from <http://mipi.org/specifications/serial-low-power-inter-chip-media-bus-slimbusm-specification>.
- [10] IEEE 1149.1: "IEEE Standard for Test Access Port and Boundary-Scan Architecture". (Joint Test Action Group, or JTAG).
- [11] SD Card Association: "SD Specifications Part 1 - Physical Layer - Simplified Specification" Version 3.01, 2010.
- [12] SD Card Association: "SD Specifications Part 1 - Physical Layer - Simplified Specification" Version 4.10, 2013.
- [13] ISO 11898-1:2003: "Road vehicles -- Controller area network (CAN) -- Part 1: Data link layer and physical signalling".
- NOTE: Available from [http://www.iso.org/iso/iso\\_catalogue/catalogue\\_tc/catalogue\\_detail.htm?csnumber=33422](http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=33422).

## 2.2 Informative references

The following referenced documents are not necessary for the application of the present document but they assist in its understanding.

Not applicable.

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# 3 Definitions and abbreviations

## 3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

**AT command:** command language with a series of short text strings which combine together to output complete commands for different operations such as hanging up, dialling and changing connection parameters for modems

**General Purpose Pad (GPP):** pad on the physical form factor that is not assigned a specific function

NOTE: Module manufacturers have the choice of assigning an I/O interface to a general purpose pad, or support additional General Purpose I/O on a general purpose pad, or leave a general purpose pad unconnected.

**General Purpose I/O (GPIO):** digital interface that can be set to electrical "0" or "1" by the module (output) or the host (input) with a use not defined by the present document

**ground slug pad:** pad dedicated to electrical ground for the module

**host device:** any device that embeds a M2M module

**Machine-to-Machine communications:** transfer of information between M2M Devices

**M2M Device:** physical equipment with communication capabilities that does not necessarily have a Human-Machine interface

**MIPI:** alliance of companies which establishes standards for hardware and software interfaces in mobile devices

**module:** complete WWAN radio devices that for the purposes of the present document connect to the integrated device through a surface mount soldered connection

NOTE: A module may or may not include an integral antenna system or SIM/USIM interface.

**M-PHY:** specification which provides a serial interface technology with high bandwidth capabilities particularly developed for mobile applications to obtain low pin count combined with very good power efficiency



**pad:** physical contact on the module or host

**pad layout:** 2 dimensional configuration of the mechanical pad placement

**pitch:** distance between common points on two adjacent pads on a common row

**shielding geometry:** implementation of material to shield or isolate a portion or portions of the module

**Surface Mount Technology (SMT):** method for manufacturing electronic circuits in which the components are mounted directly onto the surface of printed circuit boards

**z-height:** height of the module in a 3 dimensional realm

## 3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

ADCI	A/D Converter input
API	Application Programming Interface
AT	Attention
CAN	Controller Area Network
CLK	Clock
CTS	Clear To Send
DACO	D/A Converter output
DCD	Data Carrier Detect
DPR	Dynamic Power Reduction
DSR	Data Set Ready
DTR	Data Terminal Ready
ETSI	European Telecommunication Standards Institute
GND	Ground (electrical)
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input/Output
GPP	General Purpose Pad
GPS	Global Positioning System
GS	Group Specification
HS	High-Speed
HSIC	High-Speed Inter-Chip
I2C	Inter Integrated Circuit (interface)
I2S	Inter-IC Sound
IOH	High Output Current
IOL	Low Output Current
ISG	Industry Specification Group
JTAG	Joint Test Action Group (IEEE 1149.1 [10])
LED	Light Emitting Iode
LGA	Land Grid Array
LLI	Low Latency Interface (MIPI)
LTE	Long Term Evolution
M2M	Machine to Machine Communications
MBIM	Mobile Broadband Interface Model
NFC	Near Field Communications
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect - express
PCM	Pulse Code Modulation
PWM	Pulse Width Modulation
RF	Radio Frequency
RF_AUX	Antenna for auxiliary
RFU	Reserved for Future Use
RTC	Real Time Clock
RTS	Ready To Send
RX	Receive

SAR	Specific Absorption Rates
SDIO	Secure Digital Input Output
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
SPU	Standard or Proprietary Use
SSIC	SuperSpeed Inter-Chip
TX	Transmit
UART	Universal Asynchronous Receiver-Transmitter
UICC	Universal Integrated Circuit Card
UIM	User Identity Module
USB	Universal Serial Bus
VCC	Voltage Common Collector
VIH	High Input Voltage
VIL	Low Input Voltage
VOH	High Output Voltage
VOL	Low Output Voltage
VREF	Voltage Reference
WAN	Wide Area Network
WLAN	Wireless Local Area Network
WS	Word Select
WWAN	Wireless Wide Area Network

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## 4 Physical Form Factor Specifications

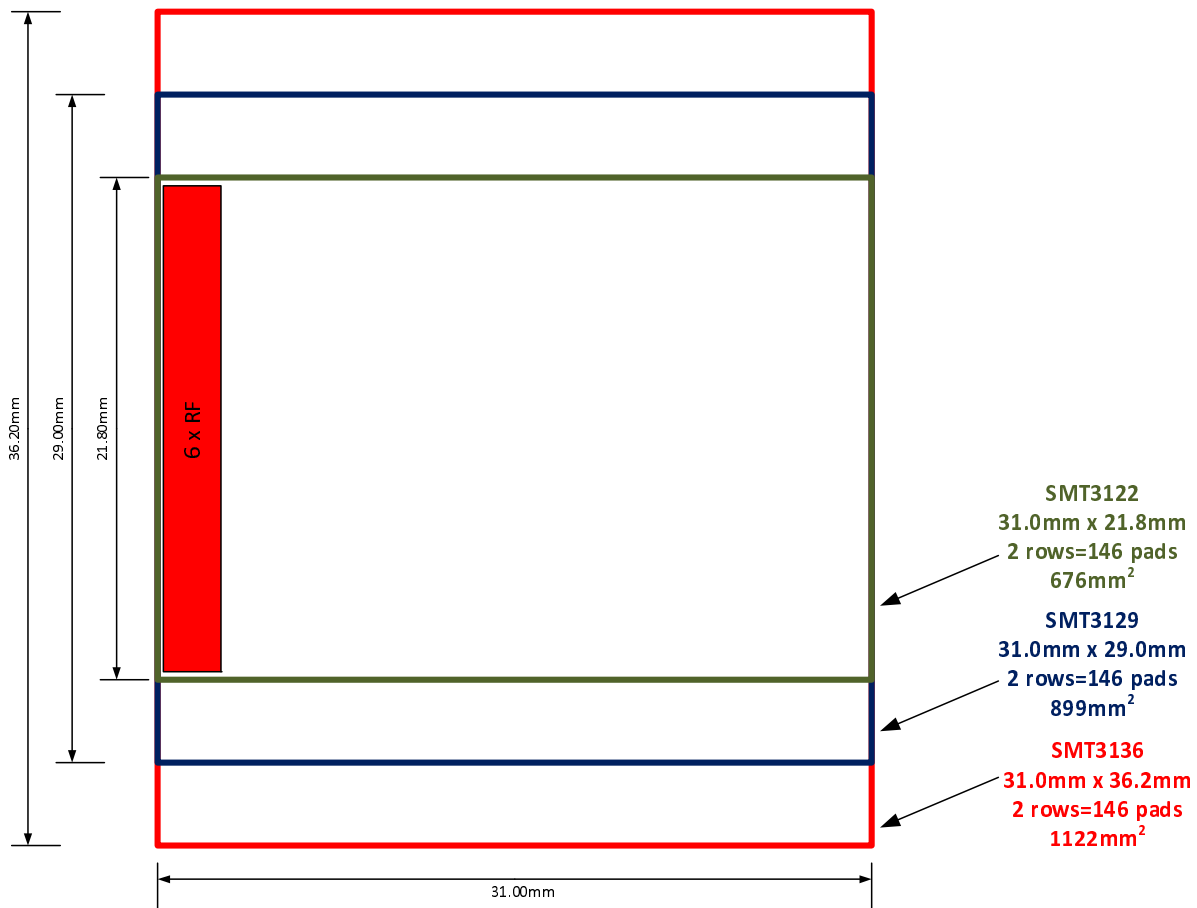
This clause defines the multiple physical form factors in terms of dimensions and pad assignments. Every design is complimentary to each other and can exist in a common footprint environment. All footprints share the same RF pad placement to optimize the reuse of designs. The naming convention SMTwwhh (ww=width, hh=height both in millimetres) provides the mapping to the specific physical layouts.

The SMT modules defined by the present document are LGA designs with all components mounted on a single side, and LGA pads mounted on the opposite side.

For any module design the recommendation is for all interface pads of a module to be soldered to the host PCB regardless of whether the pad is intended to be used electrically in the integrated design. The present document is based on the LGA methods, however, this does not explicitly exclude the use of other methods.

### 4.1 SMT Module Layouts

This clause covers all modules defined in the present document for mechanical pad placement and association with specific electrical interfaces defined in clause 5. Figure 1 shows the overview of the family of modules included in the present document.



**Figure 1: SMT modules SMT3136, SMT3129, and SMT3122 are shown with a common RF edge**

The mechanical drawings for the module layout are as viewed from the top of the module down through the module also known as an X-Ray view. The host PCB layouts are a direct view of the PCB. The overhang at the edges of the module is stated below.

Each module in the present document shares the common properties of signal pads with a size of 1 mm × 0,7 mm spaced on a 1,2 mm pitch. The size of ground slug pads is defined in the mechanical drawings for each module. The mechanical tolerances for module pad placement allow for a variance of +/- 0,02 mm from the dimensions defined. The present document indicates a minimum 0,35 mm overhang from any outside pad to the outer edge of the module. Host PCB designs should take into consideration any overhang variance.

#### 4.1.1 SMT3136 Module Mechanical Properties

Figures 2, 3 and 4 specify the overall dimensions of the SMT3136 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146 as shown in figures 2, 3 and 4.

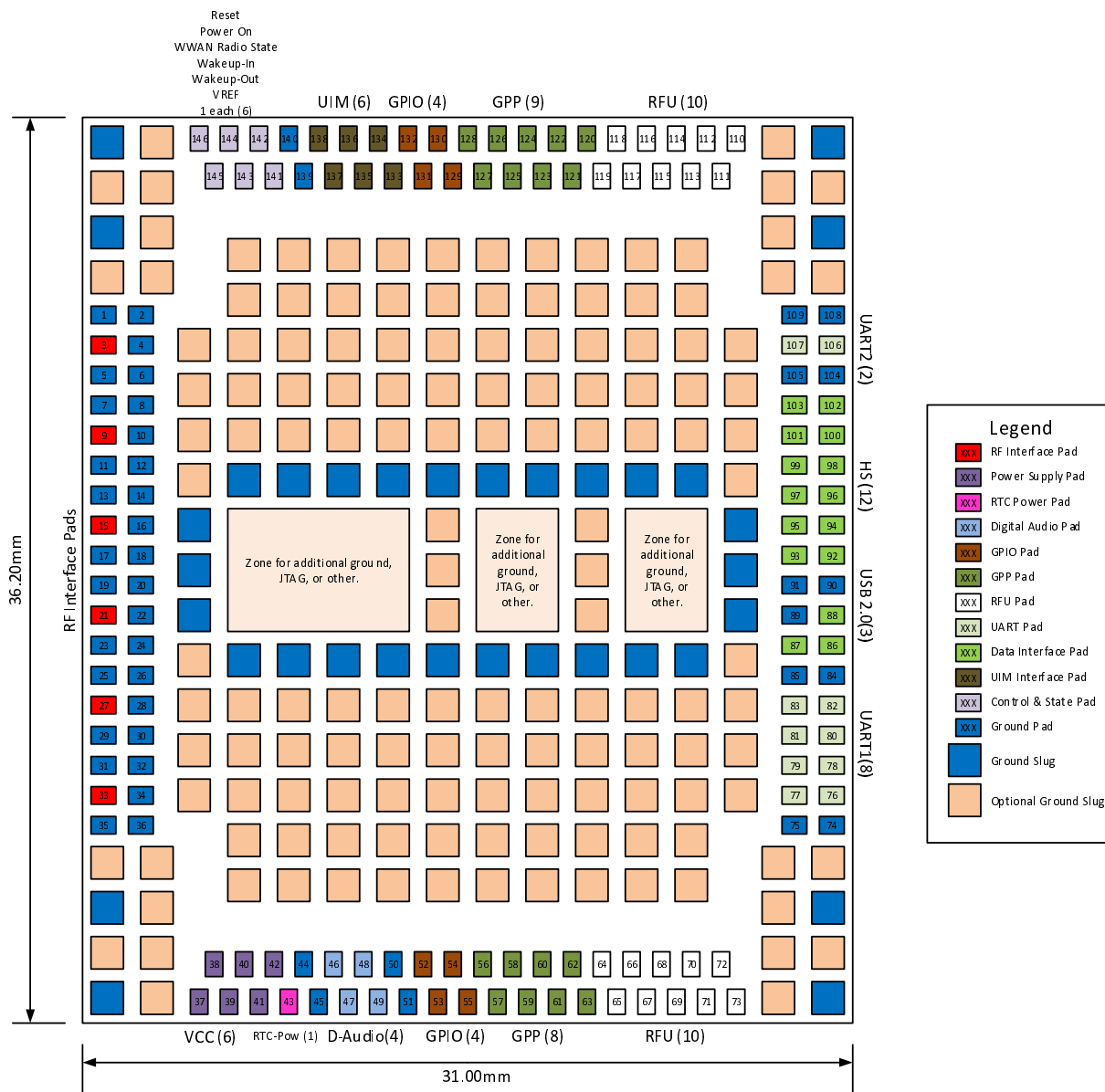
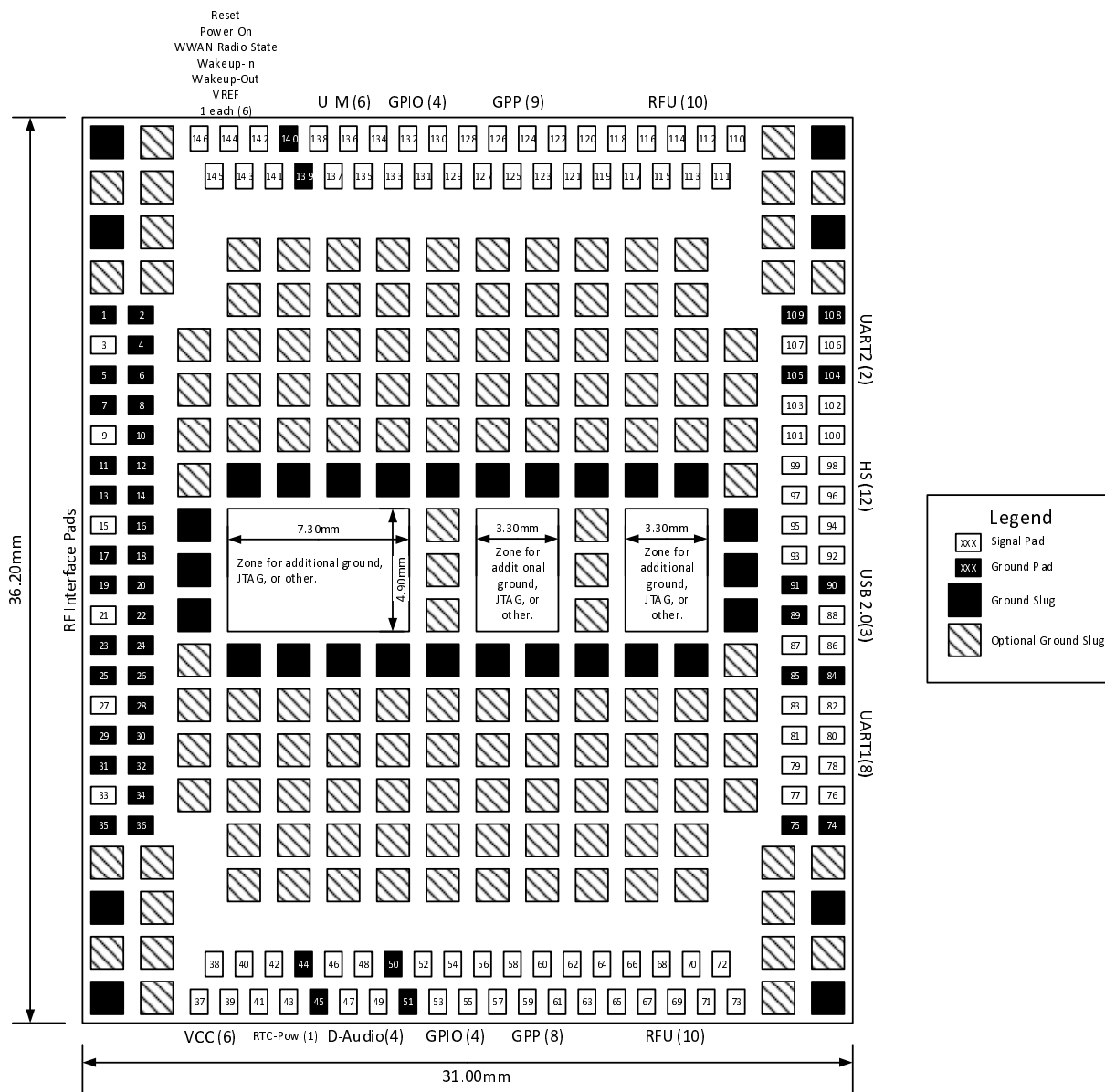


Figure 2: SMT3136 physical form factor (1 122 mm<sup>2</sup>), dimensions, pad numbering and placement



**Figure 3: SMT3136 black and white physical form factor (1 122 mm<sup>2</sup>), dimensions, pad numbering and placement**

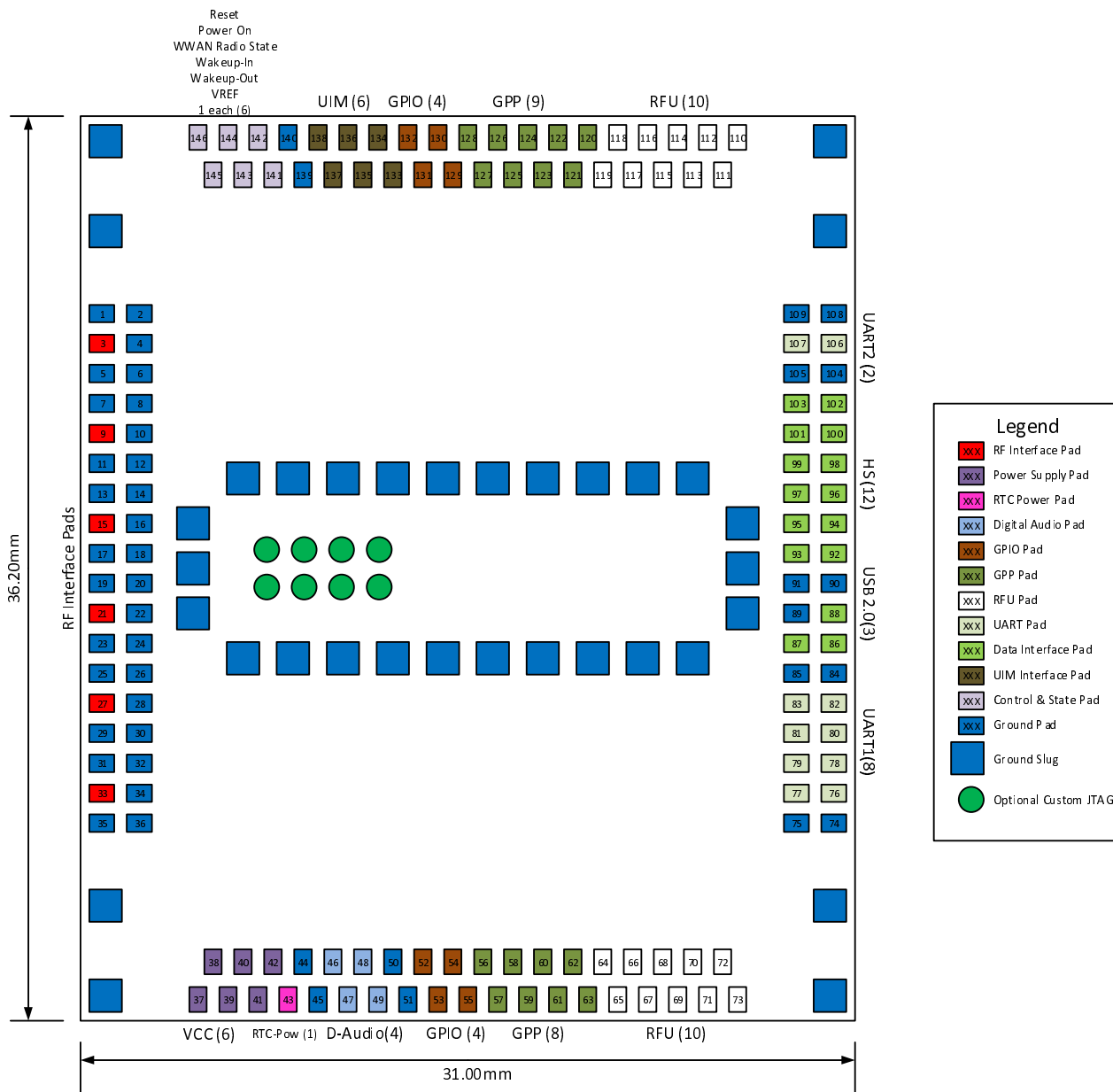


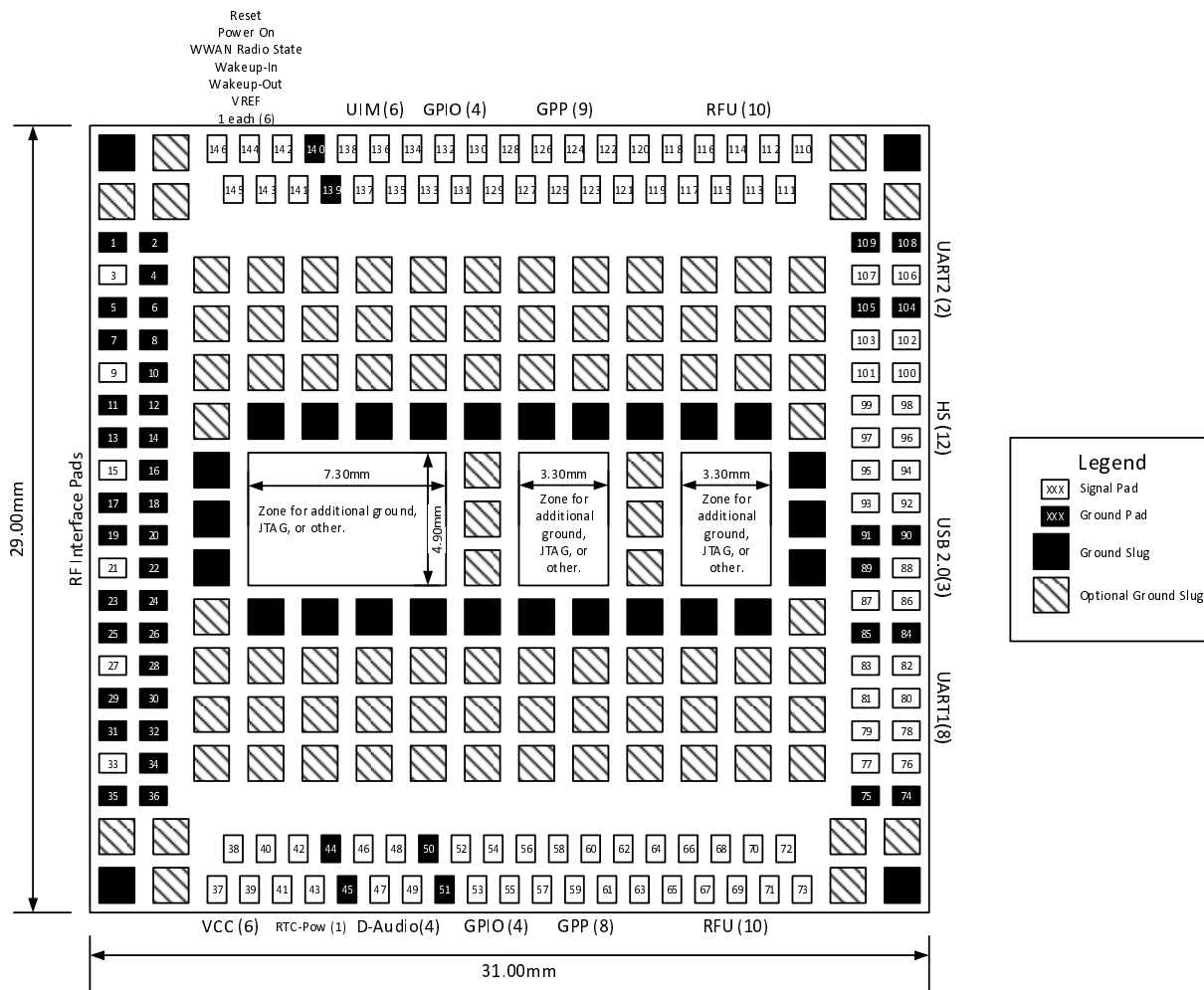
Figure 4: SMT3136 typical physical implementation (1 122 mm<sup>2</sup>), dimensions, pad numbering and placement

### 4.1.2 SMT3129 Module Mechanical properties

Figures 5, 6 and 7 specify the overall dimensions of the SMT3129 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146 as shown in figures 5, 6 and 7.



Figure 5: SMT3129 physical form factor (899 mm<sup>2</sup>), dimensions, pad numbering and placement



**Figure 6: SMT3129 black and white physical form factor (899 mm<sup>2</sup>), dimensions, pad numbering and placement**



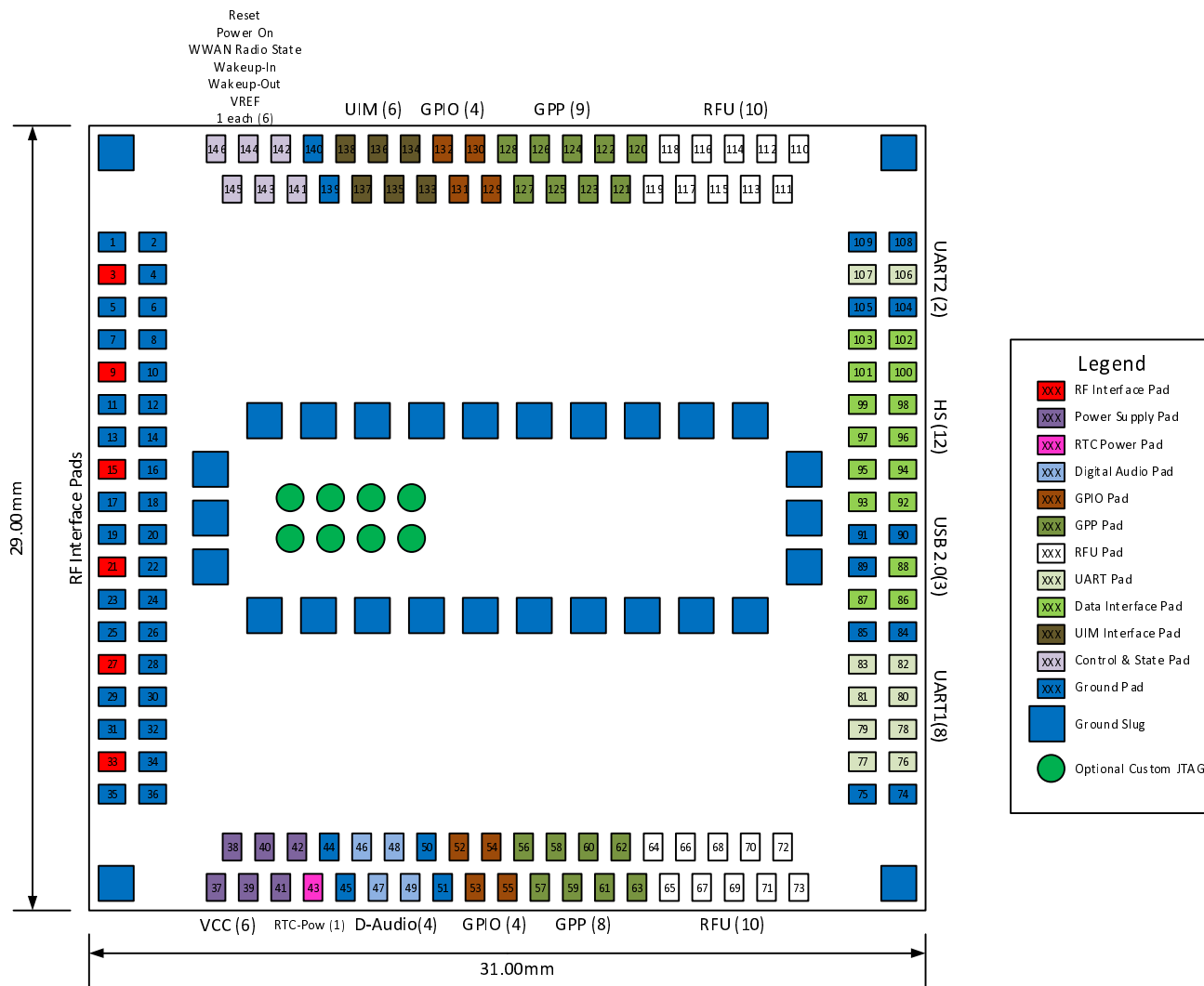


Figure 7: SMT3129 typical physical implementation (899 mm<sup>2</sup>), dimensions, pad numbering and placement

### 4.1.3 SMT3122 Module Mechanical properties

Figures 8, 9 and 10 specify the overall dimensions of the SMT3122 module form factor in millimetres. The form factor provides 146 pads which are numbered 1 through 146 as shown in figures 8, 9 and 10.

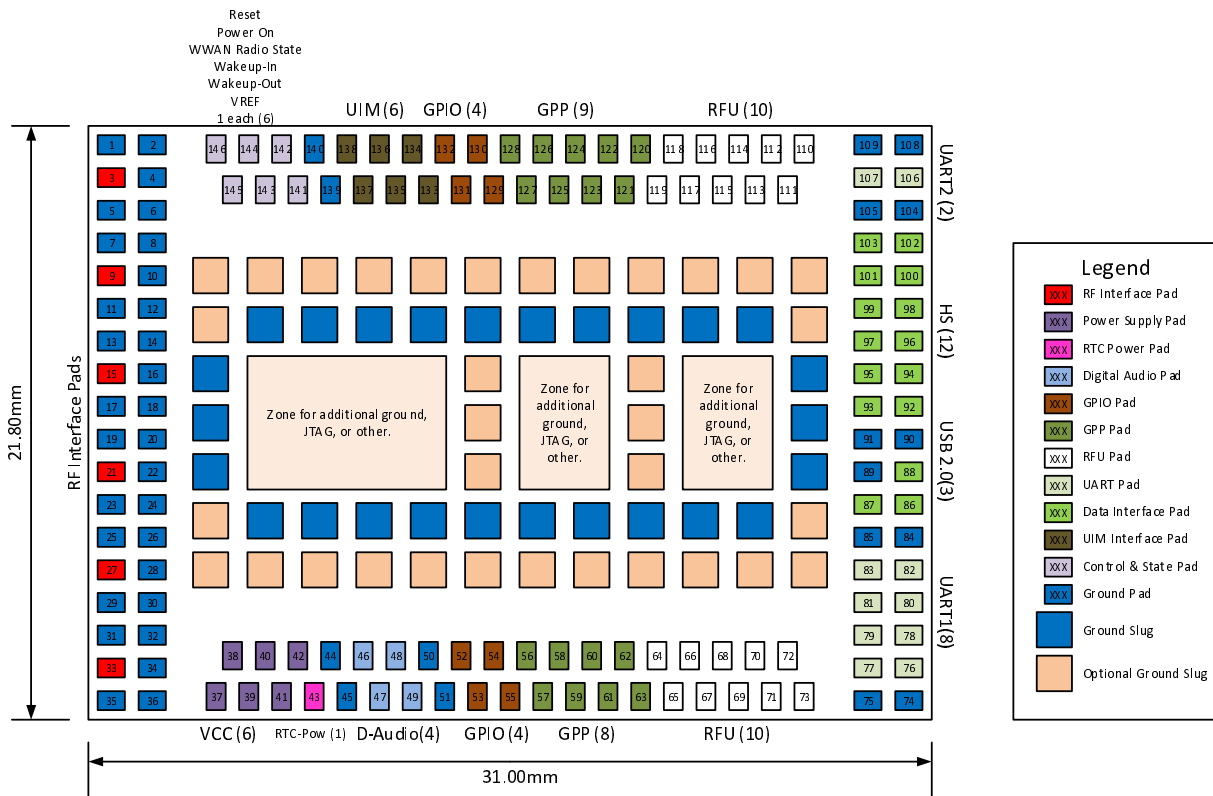


Figure 8: SMT3122 physical form factor (676 mm<sup>2</sup>), dimensions, pad numbering and placement

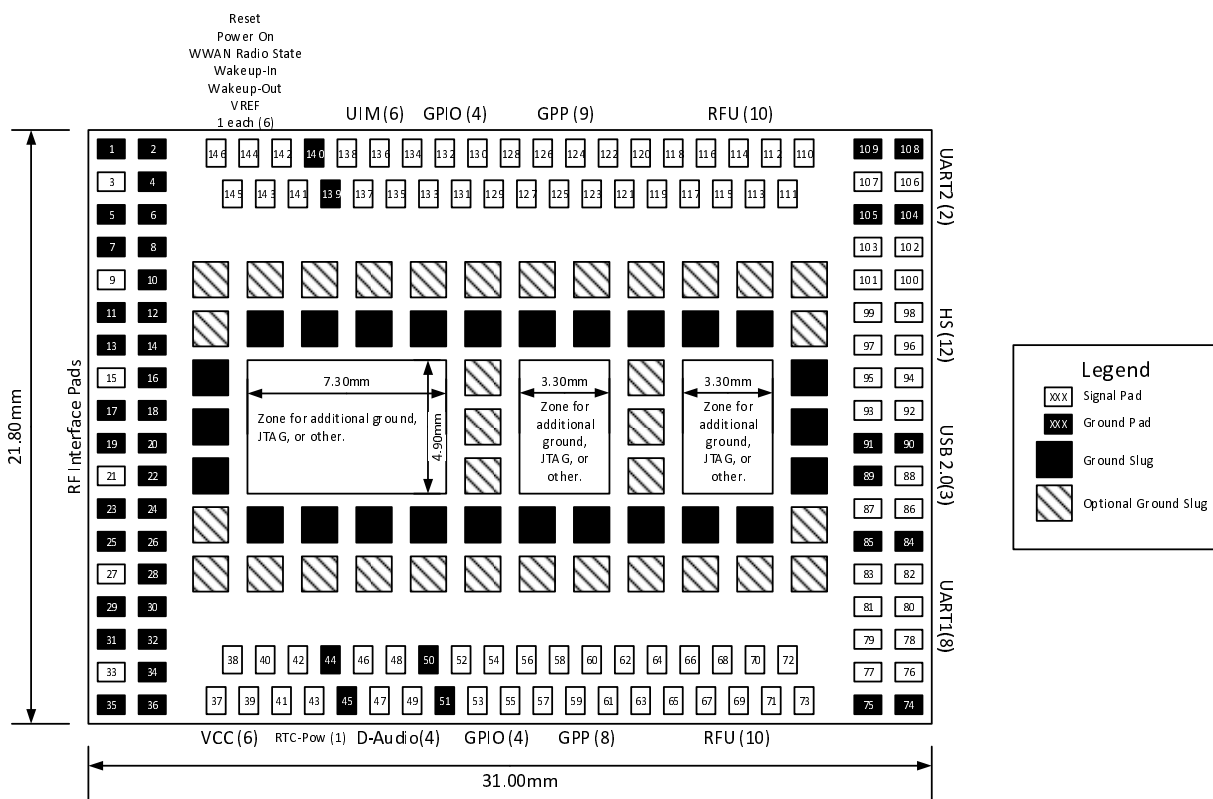


Figure 9: SMT3122 black and white physical form factor (676 mm<sup>2</sup>), dimensions, pad numbering and placement

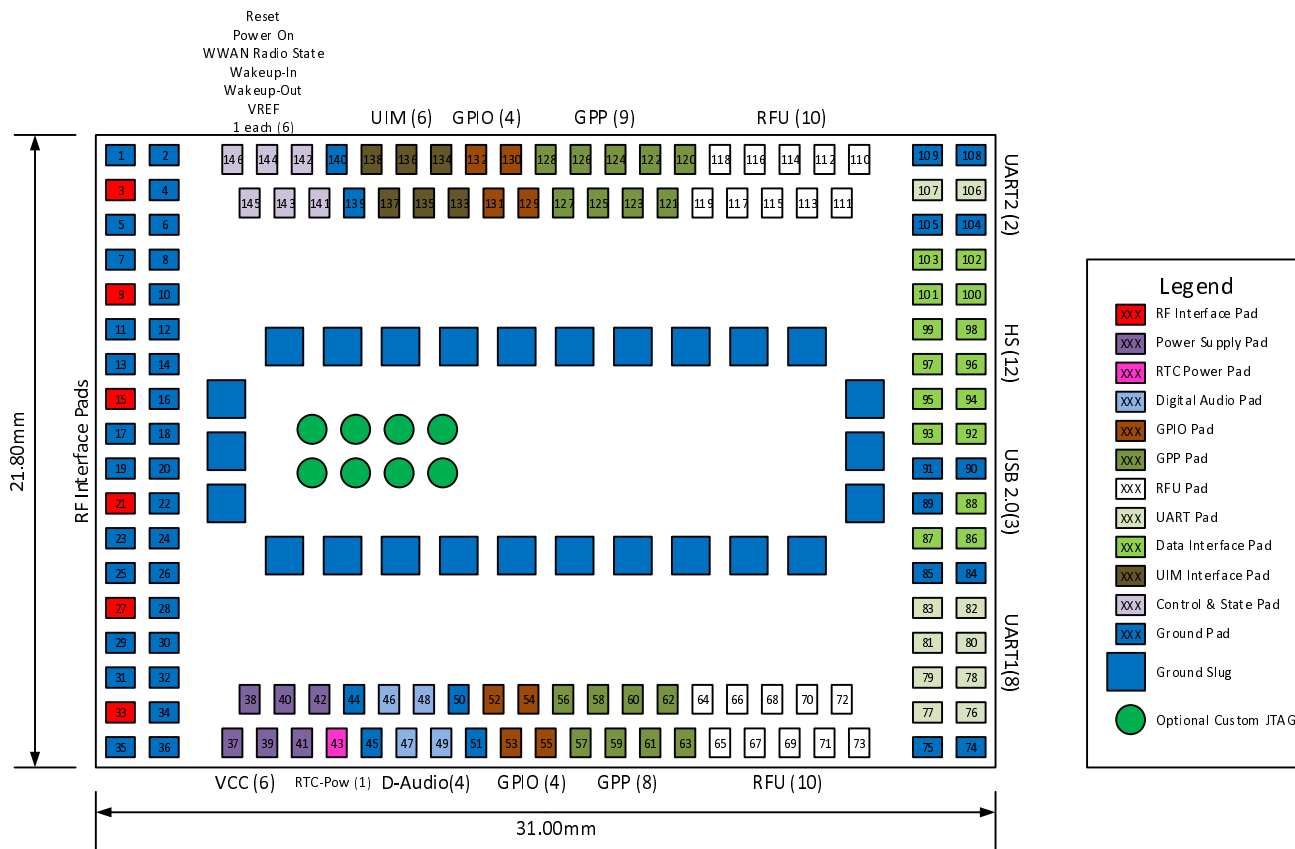


Figure 10: SMT3122 typical physical implementation (676 mm<sup>2</sup>), dimensions, pad numbering, and placement

## 4.2 Pad Size and Spacing

Figures 11, 12 and 13 show the dimensions of the pads, the distance between pads and the distance between the pads and the edge of the module. The module is symmetric with respect to the placement of the pads on each side. All measurements are in mm.

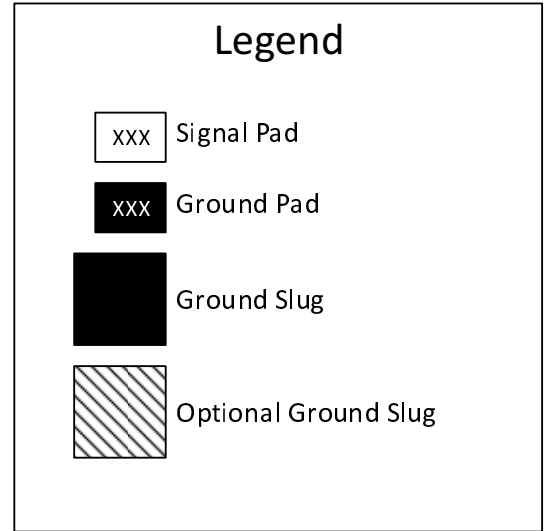
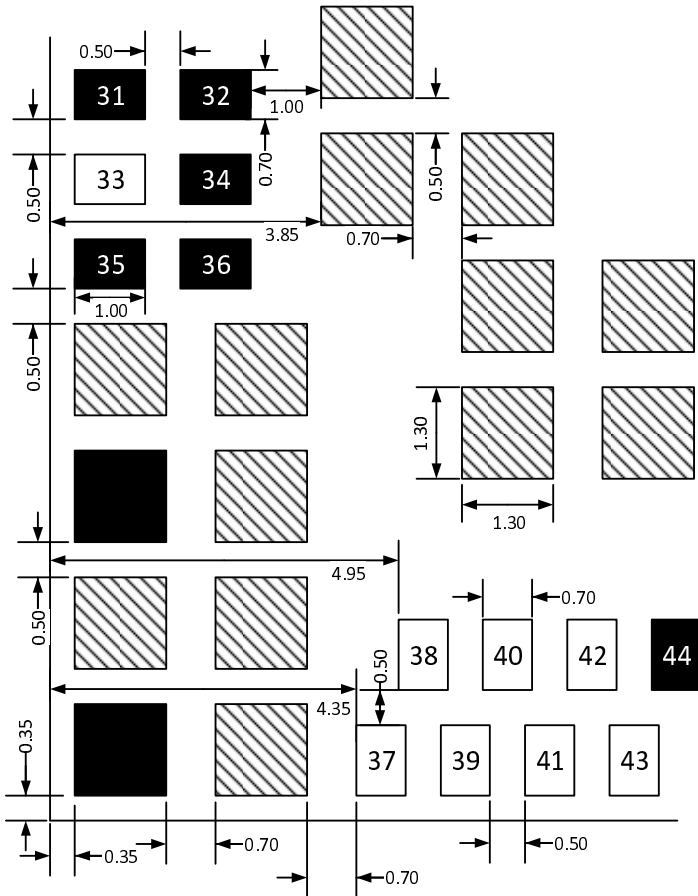


Figure 11: SMT 3136 Pad Size and Spacing

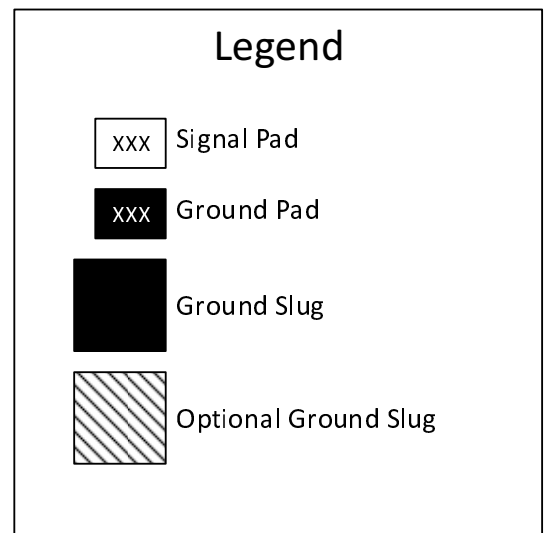
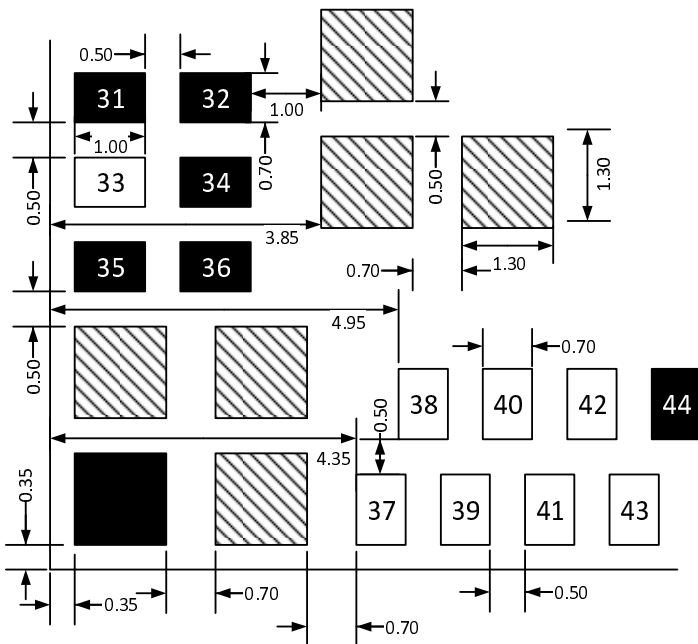


Figure 12: SMT 3129 Pad Size and Spacing

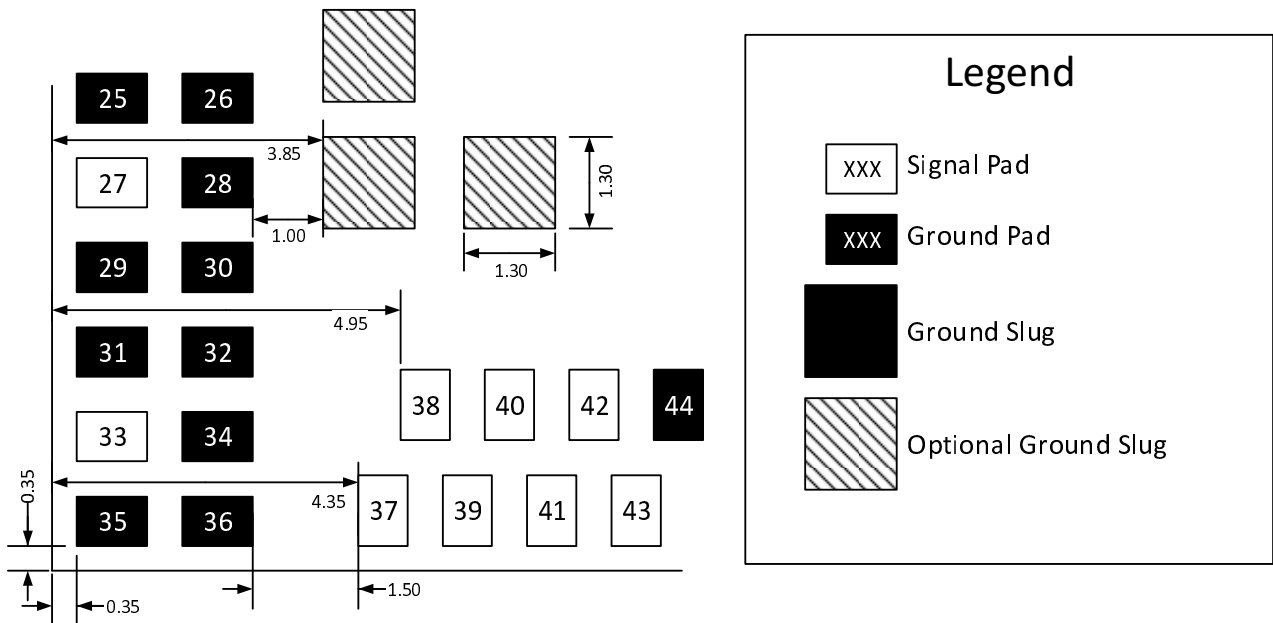


Figure 13: SMT 3122 Pad Size and Spacing

### 4.3 Pad Assignments

This clause specifies which interfaces are assigned to which pads. Each module in the present document leverages the same pad numbering assignment. The electrical characteristics of these interfaces are described in clause 5 of the present document.

Table 1: Common Pad Assignments

No. (see note 1)	Name	Description	Clause (see note 2)
1	GND	Ground	Clause 5.6.2
2	GND	Ground	Clause 5.6.2
3	RF_3	Antenna for diversity	Clause 5.1.1.3
4	GND	Ground	Clause 5.6.2
5	GND	Ground	Clause 5.6.2
6	GND	Ground	Clause 5.6.2
7	GND	Ground	Clause 5.6.2
8	GND	Ground	Clause 5.6.2
9	RF_GNSS	Antenna for a GNSS receiver	Clause 5.1.1.5
10	GND	Ground	Clause 5.6.2
11	GND	Ground	Clause 5.6.2
12	GND	Ground	Clause 5.6.2
13	GND	Ground	Clause 5.6.2
14	GND	Ground	Clause 5.6.2
15	RF_1	Main antenna	Clause 5.1.1.1
16	GND	Ground	Clause 5.6.2
17	GND	Ground	Clause 5.6.2
18	GND	Ground	Clause 5.6.2
19	GND	Ground	Clause 5.6.2
20	GND	Ground	Clause 5.6.2
21	RF_2	Antenna for diversity	Clause 5.1.1.2
22	GND	Ground	Clause 5.6.2
23	GND	Ground	Clause 5.6.2
24	GND	Ground	Clause 5.6.2
25	GND	Ground	Clause 5.6.2
26	GND	Ground	Clause 5.7.2
27	RF_AUX	Antenna for auxiliary RF(ex: Bluetooth)	Clause 5.1.1.6
28	GND	Ground	Clause 5.6.2
29	GND	Ground	Clause 5.6.2
30	GND	Ground	Clause 5.6.2
31	GND	Ground	Clause 5.6.2
32	GND	Ground	Clause 5.6.2
33	RF_4	Antenna for diversity	Clause 5.1.1.4
34	GND	Ground	Clause 5.6.2
35	GND	Ground	Clause 5.6.2
36	GND	Ground	Clause 5.6.2
37	VCC1	Power	Clause 5.6.1.1
38	VCC2	Power	Clause 5.6.1.1
39	VCC3	Power	Clause 5.6.1.1
40	VCC4	Power	Clause 5.6.1.1
41	VCC5	Power	Clause 5.6.1.1
42	VCC6	Power	Clause 5.6.1.1
43	RTC_POWER	Power Input for Real Time Clock	Clause 5.6.1.2
44	GND	Ground	Clause 5.6.2
45	GND	Ground	Clause 5.6.2
46	PCM_SYNC/I2S_WS/SLIM_CLK/GPIO46	PCM/I2S/SLIMBus/GPIO	Clauses 5.5 and 5.4.1
47	PCM_DIN/I2S_DIN/SLIM_DATA/GPIO47	PCM/I2S/SLIMBus/GPIO	Clauses 5.5 and 5.4.1
48	PCM_DOUT/I2S_DOUT/GPIO48	PCM/I2S/GPIO	Clauses 5.5 and 5.4.1
49	PCM_CLK/I2S_CLK/GPIO49	PCM/I2S/GPIO	Clauses 5.5 and 5.4.1
50	GND	Ground	Clause 5.6.2
51	GND	Ground	Clause 5.6.2
52	GPIO01	General Purpose Input / Output 1	Clause 5.6.1
53	GPIO02	General Purpose Input / Output 2	Clause 5.6.1
54	GPIO03	General Purpose Input / Output 3	Clause 5.6.1
55	GPIO04	General Purpose Input / Output 4	Clause 5.6.1
56	GPP01	General Purpose Pad 1	Clause 5.6.2
57	GPP02	General Purpose Pad 2	Clause 5.6.2

No. (see note 1)	Name	Description	Clause (see note 2)
58	GPP03	General Purpose Pad 3	Clause 5.6.2
59	GPP04	General Purpose Pad 4	Clause 5.6.2
60	GPP05	General Purpose Pad 5	Clause 5.6.2
61	GPP06	General Purpose Pad 6	Clause 5.6.2
62	GPP07	General Purpose Pad 7	Clause 5.6.2
63	GPP08	General Purpose Pad 8	Clause 5.6.2
64	RFU	Reserved for Future Use	Clause 5.8
65	RFU	Reserved for Future Use	Clause 5.8
66	RFU	Reserved for Future Use	Clause 5.8
67	RFU	Reserved for Future Use	Clause 5.8
68	RFU	Reserved for Future Use	Clause 5.8
69	RFU	Reserved for Future Use	Clause 5.8
70	RFU	Reserved for Future Use	Clause 5.8
71	RFU	Reserved for Future Use	Clause 5.8
72	RFU	Reserved for Future Use	Clause 5.8
73	RFU	Reserved for Future Use	Clause 5.8
74	GND	Ground	Clause 5.6.2
75	GND	Ground	Clause 5.6.2
76	UART1_DTR (UART 1)	Data Terminal(Host)Ready-UART 1	Clause 5.2.1.8
77	UART1_RING (UART 1)	UART Ring Indicator-UART 1	Clause 5.2.1.7
78	UART1_DCD (UART 1)	Data Carrier Detect-UART 1	Clause 5.2.1.6
79	UART1_DSR (UART 1)	Data Set Ready on module-UART 1	Clause 5.2.1.5
80	UART1_CTS (UART 1)	Clear To Send for UART 1	Clause 5.2.1.4
81	UART1_RTS (UART 1)	Request To Send for UART 1	Clause 5.2.1.3
82	UART1_RX (UART 1)	Receive for UART 1	Clause 5.2.1.2
83	UART1_TX (UART 1)	Transmit for UART 1	Clause 5.2.1.1
84	GND	Ground	Clause 5.6.2
85	GND	Ground	Clause 5.6.2
86	USB_Dp	USB Data Positive	Clause 5.2.2.1
87	VBUS/GPIO87	USB Detect / GPIO	Clauses 5.2.2.3 and 5.5.1
88	USB_Dn	USB Data Negative	Clause 5.2.2.2
89	GND	Ground	Clause 5.6.2
90	GND	Ground	Clause 5.6.2
91	GND	Ground	Clause 5.6.2
92	USB3_SSTXn/PCle_Tn/MPHY_TX1_Dn	USB 3.0/PCle/MIPI M-PHY	Clauses 5.2.4.2, 5.2.5.4 and 5.2.6.2
93	PCle_CLKREQ/MPHY_SB1	PCle/MIPI M-PHY	Clauses 5.2.5.8 and 5.2.6.9
94	USB3_SSTXp/PCle_Tp/MPHY_TX1_Dp	USB 3.0/PCle/MIPI M-PHY	Clauses 5.2.4.1, 5.2.5.3 and 5.2.6.1
95	PCle_WAKE/MPHY_SB2	MIPI M-PHY/PCle	Clauses 5.2.5.9 and 5.2.6.10
96	USB3_SSRXn/PCle_Rn/MPHY_RX1_Dn	USB 3.0/ PCle/MIPI M-PHY	Clauses 5.2.4.4, 5.2.5.2 and 5.2.6.4
97	PCle_RST/MPHY_SB3	PCle/MIPI M-PHY	Clauses 5.2.5.7 and 5.2.6.11
98	USB3_SSRXp/PCle_Rp/MPHY_RX1_Dp	USB 3.0/ PCle/MIPI M-PHY	Clauses 5.2.4.3, 5.2.5.1 and 5.2.6.3
99	USB_STROBE/MPHY_SB4	HSIC USB/MIPI M-PHY	Clauses 5.2.3.1 and 5.2.6.12
100	USB_DATA/MPHY_TX2_Dn	HSIC USB/MIPI M-PHY	Clauses 5.2.3.2 and 5.2.6.6
101	MPHY_TX2_Dp	MIPI M-PHY	Clause 5.2.6.5
102	PCle_REFCLKn/MPHY_RX2_Dn	PCle/MIPI M-PHY	Clauses 5.2.5.6 and 5.2.6.8
103	PCle_REFCLKp/MPHY_RX2_Dp	PCle/MIPI M-PHY	Clause 5.2.5.5 and 5.2.6.7
104	GND	Ground	Clause 5.6.2
105	GND	Ground	Clause 5.6.2
106	UART2_RX (UART 2)	Receive for UART 2	Clause 5.2.1.2
107	UART2_TX (UART 2)	Transmit for UART 2	Clause 5.2.1.1
108	GND	Ground	Clause 5.6.2
109	GND	Ground	Clause 5.6.2

No. (see note 1)	Name	Description	Clause (see note 2)
110	RFU	Reserved for Future Use	Clause 5.8
111	RFU	Reserved for Future Use	Clause 5.8
112	RFU	Reserved for Future Use	Clause 5.8
113	RFU	Reserved for Future Use	Clause 5.8
114	RFU	Reserved for Future Use	Clause 5.8
115	RFU	Reserved for Future Use	Clause 5.8
116	RFU	Reserved for Future Use	Clause 5.8
117	RFU	Reserved for Future Use	Clause 5.8
118	RFU	Reserved for Future Use	Clause 5.8
119	RFU	Reserved for Future Use	Clause 5.8
120	GPP09	General Purpose Pad 9	Clause 5.4.2
121	GPP10	General Purpose Pad 10	Clause 5.4.2
122	GPP11	General Purpose Pad 11	Clause 5.4.2
123	GPP12	General Purpose Pad 12	Clause 5.4.2
124	GPP13	General Purpose Pad 13	Clause 5.4.2
125	GPP14	General Purpose Pad 14	Clause 5.4.2
126	GPP15	General Purpose Pad 15	Clause 5.4.2
127	GPP16	General Purpose Pad 16	Clause 5.4.2
128	GPP17	General Purpose Pad 17	Clause 5.4.2
129	GPIO05	General Purpose Input / Output 5	Clause 5.4.1
130	GPIO06	General Purpose Input / Output 6	Clause 5.4.1
131	GPIO07	General Purpose Input / Output 7	Clause 5.4.1
132	GPIO08	General Purpose Input / Output 8	Clause 5.4.1
133	UIM_VCC	Power source for external UIM	Clause 5.1.2.1
134	UIM_DATA	Data in/out	Clause 5.1.2.2
135	UIM_CLK	Clock signal	Clause 5.1.2.3
136	UIM_RESET	Reset signal	Clause 5.1.2.4
137	UIM_DETECT	UIM Detect signal	Clause 5.1.2.5
138	UIM_SPU	Standard or Proprietary Use	Clause 5.1.2.6
139	GND	Ground	Clause 5.6.2
140	GND	Ground	Clause 5.6.2
141	WWAN_STATE	Wireless WAN Radio State	Clause 5.3.1
142	POWER_ON	Power On the module	Clause 5.3.2
143	WAKEUP_OUT/GPIO143	Module wakes up host OR GPIO	Clauses 5.3.3 and 5.4.1
144	WAKEUP_IN/GPIO144	Host wakes up module OR GPIO	Clauses 5.3.4 and 5.4.1
145	RESET	Reset the module	Clause 5.3.5
146	VREF	Reference Logic Voltage	Clause 5.3.6

NOTE 1: Number referring to the numbering in corresponding module figure.  
NOTE 2: This column refers to the clause that defines the electrical characteristics of the interface provided by this pad.

## 5 Electrical Specifications

This clause defines the I/O interfaces that may be supported by the SMT module and their electrical characteristics.

Where clause 4 assigns any of the specified interfaces to specific pads, modules may leave these pads unimplemented inside the module. Host devices using this module with unimplemented interfaces may then either connect these unused pads to ground or leave them floating. This is to avoid possible interference conditions where a particular host device was designed for a particular interface to be present.



Table 2: Electrical Interfaces and Interface Families

Interface Family	Interface	Signal	Description	I/O	
RF Interfaces		RF_1	Used in a system with 1 or more antennae	I/O	
		RF_2	Used in a system with 2 or more antennae	I/O	
		RF_3	Used in a system with 3 or more antennae	I/O	
		RF_4	Used in a system with 4 or more antennae	I/O	
		RF_GNSS	Antenna for GNSS	I	
		RF_AUX	Antenna for additional peripheral	I/O	
User Identity Module		UIM_VCC	Power source for external UIM	O	
		UIM_DATA	Data in/out	I/O	
		UIM_CLK	Clock signal	O	
		UIM_RESET	Reset signal	O	
		UIM_DETECT	UIM detect signal	I	
		UIM_SPU	Standard or Proprietary Use	-	
Data Interfaces	UART	UART_RTS	Module ready to send	O	
		UART_TX	Module sending data	O	
		UART_RX	Module receiving data	I	
		UART_CTS	Clear to send	I	
		UART_DSR	Data ready on module	O	
		UART_DCD	Carrier detect	O	
		UART_RING	Ring indication	O	
		UART_DTR	Host ready	I	
	USB 2.0	USB_Dp	USB 2.0 Data positive	I/O	
		USB_Dn	USB 2.0 Data negative	I/O	
		VBUS	USB 2.0 Signal detect	I	
	HSIC USB	USB_STROBE	USB 2.0 HSIC Strobe	I/O	
		USB_DATA	USB 2.0 HSIC Data	I/O	
	USB 3.0	USB3_SSTXp	USB 3.0 SuperSpeed send positive	I/O	
		USB3_SSTXn	USB 3.0 SuperSpeed send negative	I/O	
		USB3_SSRXp	USB 3.0 SuperSpeed receive positive	I/O	
		USB3_SSRXn	USB 3.0 SuperSpeed receive negative	I/O	
	PCIe	PCIe_Rp	PCIe Receive positive	I	
		PCIe_Rn	PCIe Receive negative	I	
		PCIe_Tp	PCIe Transmit positive	O	
		PCIe_Tn	PCIe Transmit negative	O	
		PCIe_REFCLKp	Reference clock positive	I	
		PCIe_REFCLKn	Reference clock negative	I	
		PCIe_RST	PCIe Reset	I	
		PCIe_CLKREQ	PCIe Clock request	I/O	
		PCIe_WAKE	PCIe Wake	I/O	
		MIPI M-PHY	MPHY-TX1-Dp	Transmit lane 1 - data positive	O
	MPHY_TX1-Dn		Transmit lane 1 - data negative	O	
	MPHY_RX1-Dp		Receive lane 1 - data positive	I	
	MPHY_RX1-Dn		Receive lane 1 - data negative	I	
	MPHY_TX2-Dp		Transmit lane 2 - data positive	O	
	MPHY_TX2-Dn		Transmit lane 2 - data negative	O	
	MPHY_RX2-Dp		Receive lane 2 - data positive	I	
	MPHY_RX2-Dn		Receive lane 2 -data negative	I	
	MPHY_SB1		MIPI M-PHY Sideband #1	I/O	
	MPHY_SB2		MIPI M-PHY Sideband #2	I/O	
	MPHY_SB3		MIPI M-PHY Sideband #3	I/O	
	MPHY_SB4		MIPI M-PHY Sideband #4	I/O	
	Module Control and State Interfaces		WWAN_STATE	WWAN radio state	O
			POWER_ON	Power on	I
WAKEUP_OUT		Module wakes up host	O		
WAKEUP_IN		Host wakes up module	I		
RESET		Reset module	I		
Power and Ground	VREF	Voltage Reference Output	O		
	VCC	Main Power	I		
	GROUND	Ground	I		
	RTC_POWER	Power for an internal Real Time Clock	I		
General Purpose	GPIO	Digital I/O	I/O		
	GPP	General Purpose Pad	I/O		

Interface Family	Interface	Signal	Description	I/O
Digital Audio	PCM	PCM_SYNC	Synchronization signal	O
		PCM_DIN	Data In	I
		PCM_DOUT	Data Out	O
		PCM_CLK	Clock	O
	I2S	I2S_WS	I2S Word Select	I/O
		I2S_DIN	I2S Data In	I
		I2S_DOUT	I2S Data Out	O
		I2S_CLK	I2S Clock	I/O
	SLIMBus	SLIM_CLK	SLIMBus Clock Line	I/O
		SLIM_DATA	SLIMBus Data Line	I/O
RFU	RFU	RFU	Reserved For Future Use	-
Test and Debug	JTAG	JTAG	Defined by manufacturer	-

## 5.1 RF and UIM

### 5.1.1 RF Interfaces

The electrical characteristics of the RF interfaces are:

#### 5.1.1.1 RF\_1

An antenna pad to be used in a system that uses 1 or more antennae.

The nominal RF impedance shall be 50 Ohms.

#### 5.1.1.2 RF\_2

An antenna pad to be used in a system that uses 2 or more antennae.

The nominal RF impedance shall be 50 Ohms.

#### 5.1.1.3 RF\_3

An antenna pad to be used in a system that uses 3 or more antennae.

The nominal RF impedance shall be 50 Ohms.

#### 5.1.1.4 RF\_4

An antenna pad to be used in a system that uses 4 antennae.

The nominal RF impedance shall be 50 Ohms.

#### 5.1.1.5 RF\_GNSS

An antenna pad to be used for GNSS. This signal is typically an input signal only.

The nominal RF impedance shall be 50 Ohms.

#### 5.1.1.6 RF\_AUX

An antenna pad for an additional peripheral.

The nominal RF impedance shall be 50 Ohms.

## 5.1.2 User Identity Module

If an external UIM is used in the design then the module shall provide the following interfaces to support an external User Interface Module compliant with [1]. For further reference also see [2].

### 5.1.2.1 UIM\_VCC

A power source output to an external UIM.

### 5.1.2.2 UIM\_DATA

Data in/out for an external UIM.

### 5.1.2.3 UIM\_CLK

An output clock signal to an external UIM.

### 5.1.2.4 UIM\_RESET

An output reset signal to an external UIM.

### 5.1.2.5 UIM\_DETECT

An input signal used to detect an external UIM.

### 5.1.2.6 UIM\_SPU

The module may provide this interface for forward looking standard or proprietary use.

ETSI ISG SMT has defined that this pad will be used for UICC-CLF (NFC communications) when the standards support the use case. The pad would be connected to UICC contact C6 when used.

## 5.2 Data Interfaces

Data interfaces are those interfaces that enable the exchange of data between the module and the host. Module control functions (for example AT Commands, MBIM or other APIs) are typically included over one or more data interfaces. Physical form factors defined in clause 4 may provide dedicated pad locations for some data interfaces while other data interfaces may be allocated to shared pad locations.

### 5.2.1 Universal Asynchronous Receiver-Transmitter

The Universal Asynchronous Receiver-Transmitter (UART) interface has the following electrical characteristics:

- A 2-wire UART consists of the UART\_TX and UART\_RX interfaces.
- A 4-wire UART consists of the UART\_RTS, UART\_CTS, UART\_TX and UART\_RX interfaces.
- An 8-wire UART consists of all interfaces defined in this clause.

#### 5.2.1.1 UART\_TX

This is a module output for transmitting data (Tx). This signal maps to the UART Rx interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 2-wire, 4-wire, or 8-wire UART interface.

### 5.2.1.2 UART\_RX

This is a module input for receiving data (Rx). This signal maps to the UART Tx interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 2-wire, 4-wire, or 8-wire UART interface.

### 5.2.1.3 UART\_RTS

This is a module output for the Ready To Send (RTS) signal used for host flow control. This signal maps out to the UART CTS interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 4-wire or 8-wire UART interface.

### 5.2.1.4 UART\_CTS

This is a module input for the Clear To Send (CTS) signal. This signal originates from the UART RTS interface of the host. The voltage logic on this interface utilizes VREF. This interface is required on any 4-wire or 8-wire UART interface.

### 5.2.1.5 UART\_DSR

Data Set Ready on module. This is an output from the module. This interface is only included on an 8-wire UART interface.

### 5.2.1.6 UART\_DCD

Data Carrier Detect. This is an output from the module. This interface is only included on an 8-wire UART interface.

### 5.2.1.7 UART\_RING

UART Ring indication is an output from the module. This interface is only included on an 8-wire UART interface. It may serve a similar function as the WAKEUP\_OUT interface to alert the host upon an event occurrence within the module such as an incoming call received, SMS received, etc. This is an active low signal.

### 5.2.1.8 UART\_DTR

Data Terminal Ready (also known as host ready) is an input to the module. This interface is only included on an 8-wire UART interface.

## 5.2.2 Universal Serial Bus 2.0

The USB 2.0 interface provides data transfer, communication, debugging and communication to and from external peripherals and host devices. For the electrical characteristics of the USB 2.0 interface please refer to [3].

### 5.2.2.1 USB\_Dp

USB 2.0 Data positive.

### 5.2.2.2 USB\_Dn

USB 2.0 Data negative.

### 5.2.2.3 VBUS

The VBUS is a USB 2.0 Signal detection and is an input to the module to detect that the host is present. If the USB 2.0 interface is utilized the implementation of this pad is optional. If this pad is not used for the purpose described in this clause this pad may instead be used as a GPIO interface.

## 5.2.3 Universal Serial Bus 2.0 High-Speed Inter-Chip

For the electric characteristics of the Universal Serial Bus 2.0 High-Speed Inter-Chip (USB 2.0 HSIC) please refer to [4].

### 5.2.3.1 USB\_STROBE

USB 2.0 HSIC Strobe.

### 5.2.3.2 USB\_DATA

USB 2.0 HSIC Data.

## 5.2.4 Universal Serial Bus 3.0 SuperSpeed Interfaces

For the electric characteristics of the Universal Serial Bus 3.0 (USB 3.0) SuperSpeed interface please refer to [5].

### 5.2.4.1 USB3\_SSTXp

USB 3.0 SuperSpeed send positive is an output from the module.

### 5.2.4.2 USB3\_SSTXn

USB 3.0 SuperSpeed send negative is an output from the module.

### 5.2.4.3 USB3\_SSRXp

USB 3.0 SuperSpeed receive positive is an input to the module.

### 5.2.4.4 USB3\_SSRXn

USB 3.0 SuperSpeed receive negative is an input to the module.

## 5.2.5 Peripheral Component Interconnect Express

For the electric characteristics of the Peripheral Component Interconnect Express (PCIe) please refer to [6].

### 5.2.5.1 PCIe\_Rp

PCIe Receive positive.

### 5.2.5.2 PCIe\_Rn

PCIe Receive negative.

### 5.2.5.3 PCIe\_Tp

PCIe Transmit positive.

### 5.2.5.4 PCIe\_Tn

PCIe Transmit negative.

### 5.2.5.5 PCIe\_REFCLKp

Reference clock positive.

### 5.2.5.6 PCIe\_REFCLKn

Reference clock negative.

### 5.2.5.7 PCIe\_RST

PCIe Reset.

### 5.2.5.8 PCIe\_CLKREQ

PCIe Clock request.

### 5.2.5.9 PCIe\_WAKE

PCIe Wake.

## 5.2.6 MIPI M-PHY

For the electric characteristics of the MIPI M-PHY interface please refer to [7].

The MIPI Low Latency Interface (LLI), SuperSpeed Inter-Chip (SSIC) interface or Mobile PCIe can be provided over the MIPI M-PHY interface. Two transmit and two receive lanes and four sidebands are provided for implementing any of these protocols.

### 5.2.6.1 MPHY\_TX1-Dp

Transmit lane 0 - data positive.

### 5.2.6.2 MPHY\_TX1-Dn

Transmit lane 0 - data negative.

### 5.2.6.3 MPHY\_RX1-Dp

Receive lane 0 - data positive.

### 5.2.6.4 MPHY\_RX1-Dn

Receive lane 0 - data negative.

#### 5.2.6.5 MPHY\_TX2-Dp

Transmit lane 1 - data positive.

#### 5.2.6.6 MPHY\_TX2-Dn

Transmit lane 1 - data negative.

#### 5.2.6.7 MPHY\_RX2-Dp

Receive lane 1 - data positive.

#### 5.2.6.8 MPHY\_RX2-Dn

Receive lane 1 - data negative.

#### 5.2.6.9 MPHY\_SB1

MIPI M-PHY Sideband #1.

#### 5.2.6.10 MPHY\_SB2

MIPI M-PHY Sideband #2.

#### 5.2.6.11 MPHY\_SB3

MIPI M-PHY Sideband #3.

#### 5.2.6.12 MPHY\_SB4

MIPI M-PHY Sideband #4.

### 5.3 Module Control and State Functions

Module control and state function interfaces support various core operating functions of the module. For details of the electrical specification for each interface in this sub-clause see clause 5.6.4 where electrical details of digital logic levels for different voltage platforms are defined.

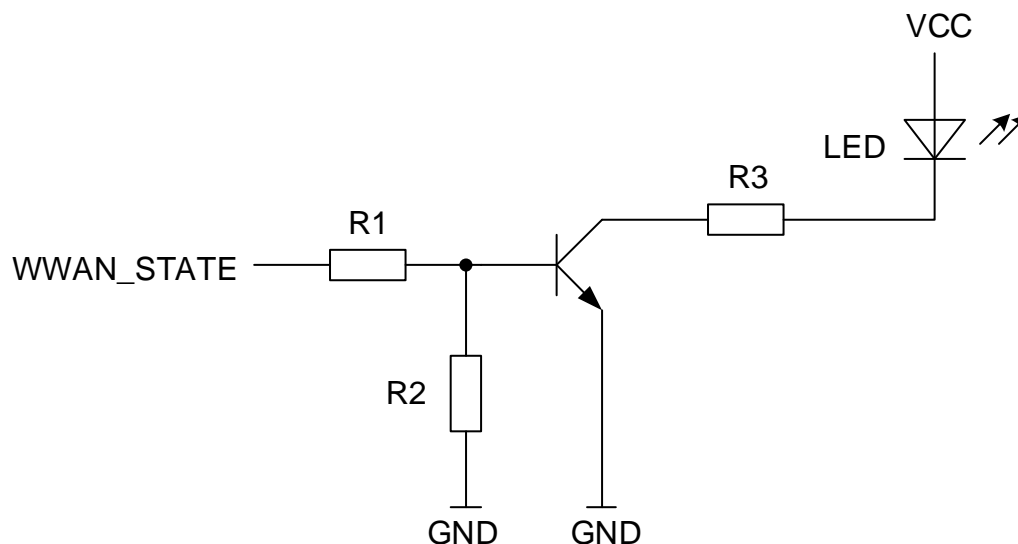
#### 5.3.1 WWAN\_STATE

The WWAN\_STATE pad may support an LED signal to provide radio state indications to users. The signal is active high and intended to drive a system-mounted LED indicator.

OFF - Radio is incapable of transmitting. This state is indicated when the radio is not powered or when the radio is disabled by software.

ON - Radio is capable of transmitting. The signal should remain ON even if the radio is not actually transmitting. For example, the signal remains ON during temporary radio disablements performed by the module of its own volition to do scanning, switching radios/bands, power management, etc. If the module is in a state where it is possible that radio can begin transmitting without the system user performing any action, this signal should remain ON.

A recommended external hardware circuit for an LED is shown in figure 14.



**Figure 14: A recommended external hardware LED circuit**

The present document also allows user programmable states for this signal for more exotic state methods as described in clause B.4 of Annex B.

### 5.3.2 POWER\_ON

The POWER\_ON pad is an input signal used to control whether the module is in the Module Enabled or Module Disabled state.

There are three possible states the module can be in:

- Module Off - VCC is not present.
- Module Enabled - VCC is supplied and the module is enabled.
- Module Disabled - VCC is supplied and the module is disabled.

The state transitions are defined as follows:

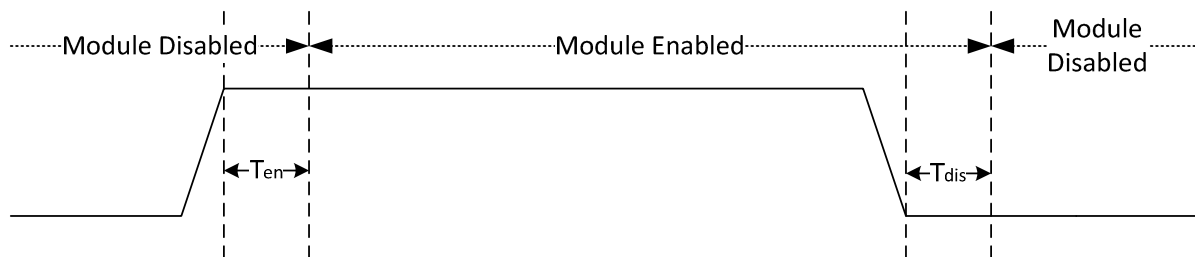
- When voltage is applied to VCC the module shall enter the Module Disabled state.
- An input to the POWER\_ON pad shall trigger the transition from the Module Disabled to the Module Enabled state.
- An input to the POWER\_ON pad shall trigger the transition from the Module Enabled to the Module Disabled state.

Example implementations for the input to the POWER\_ON pad are described here:

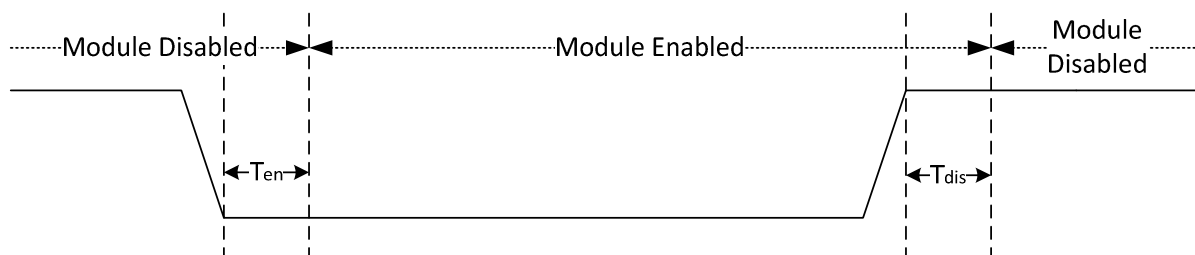
- The POWER\_ON signal can be Active High ( $V_{IH}$  for  $V_{REF}$ ) or Active Low ( $V_{IL}$  for  $V_{REF}$ ) and behave either as a State Request (Active represents Enabled, Non-Active represents Disabled) or a Change of State Request (Enabled to Disabled or Disabled to Enabled).

Here are some examples of possible designs using the POWER\_ON interface.

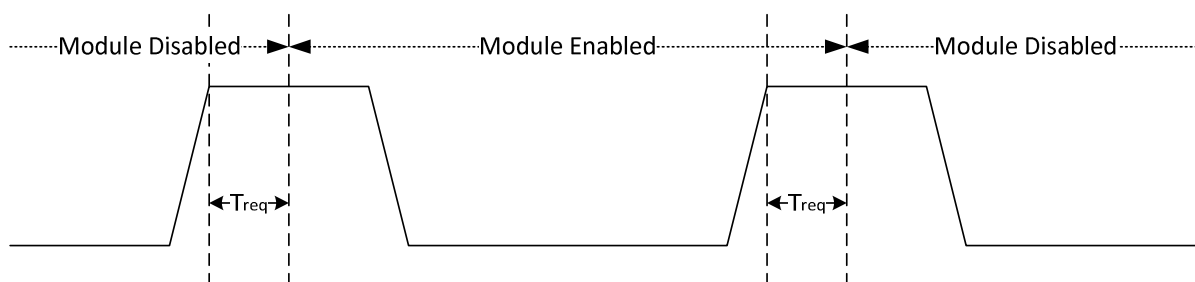




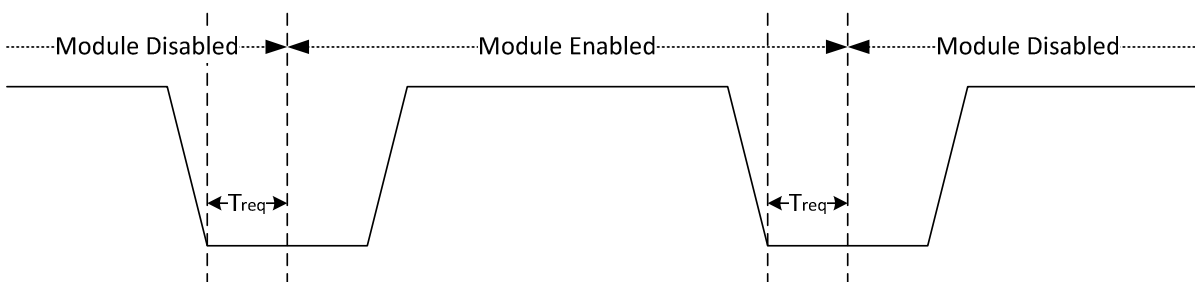
**Figure 15: State Request, Active High,  $T_{en}$  = Enable Timer,  $T_{dis}$  = Disable Timer**



**Figure 16: State Request, Active Low,  $T_{en}$  = Enable Timer,  $T_{dis}$  = Disable Timer**



**Figure 17: Change of State Request, Active High (Initial State = Disabled),  $T_{req}$  = Request Timer**



**Figure 18: Change of State Request, Active Low (Initial State = Enabled),  $T_{req}$  = Request Timer**

Host side implementation for the POWER\_ON interface is to be defined by the Module provider (including timing diagrams, operation sequencing, etc.) as the actual implementation is module specific.

**NOTE:** For 3GPP compliant modules it is required that the module is kept ON for at least 2 seconds after a command to power down the module has been issued to ensure that there is time for the module to shut down properly. The shutdown behaviour towards the SIM and network shall comply with 3GPP requirements, please refer to [8].

### 5.3.3 WAKEUP\_OUT

The WAKEUP\_OUT pad is an output signal which allows the module to alert the host of a trigger event within the module. When the module intends to wake up the host this interface shall be set high.

If the defined pad for the module is not used for the WAKEUP\_OUT function then it may be used as a GPIO.

This interface should conform to the VREF Digital Logic Levels for most modules.

### 5.3.4 WAKEUP\_IN

The WAKEUP\_IN pad is an input signal which allows the host device to wake up the module from a state such as a low power mode. When the host intends to wake up the module this interface shall be set high.

If the defined pad for the module is not used for the WAKEUP\_IN function then it may be used as a GPIO.

This interface should conform to the VREF Digital Logic Levels for most modules.

### 5.3.5 RESET

An input to the RESET pad will immediately place the module in a Power On reset condition.

When this interface is set to low for a minimum period of time the module will reset.

Care should be taken not to activate this pad unless there is a critical failure and all other methods of regaining control and/or communication with the module have failed.

See clause B.5 of Annex B for recommended implementation guidelines for the RESET pad.

### 5.3.6 VREF

VREF is a reference voltage output supplied from the module to provide a logic reference for digital interfaces. See clause 5.6.3 Reference Voltage and Digital Logic Levels.

## 5.4 General Purpose

Where clause 4 does not assign the interface to specific pads, implementations may provide the interface over General Purpose Pads (GPP) or General Purpose I/O (GPIO) pads.

### 5.4.1 General Purpose Input/Output (GPIO)

The General Purpose Input/Output pad is a digital I/O which control and usage shall be defined by the module developer.

This interface should conform to the VREF Digital Logic Levels.

### 5.4.2 General Purpose Pad (GPP)

The General Purpose Pads are pads that have variable use cases. See Annex A.

## 5.5 Digital Audio

The present document allows multiple digital audio formats to be supported. Any unused Digital Audio pads may be used as a GPIO interface.

### 5.5.1 Pulse Code Modulation

The module may support a Pulse Code Modulation interface to communicate narrowband, monotonic audio (typically voice) to external peripherals.

### 5.5.1.1 PCM\_SYNC

PCM synchronization signal, an output.

### 5.5.1.2 PCM\_DIN

PCM data in, an input.

### 5.5.1.3 PCM\_DOUT

PCM data out, an output.

### 5.5.1.4 PCM\_CLK

PCM clock signal, an output.

## 5.5.2 Integrated Inter Chip Sound

The module may support an Integrated Inter Chip Sound interface for digital audio.

### 5.5.2.1 I2S\_WS

I2S Word Select. This interface is an input if the I2S pads are used as a digital audio input in conjunction with I2S\_DIN. This interface is an output if the I2S pads are used as a digital audio output in conjunction with I2S\_DOUT.

### 5.5.2.2 I2S\_DIN

I2S data input if I2S is used as a digital audio input.

### 5.5.2.3 I2S\_DOUT

I2S data output if I2S is used as a digital audio output.

### 5.5.2.4 I2S\_CLK

I2S Serial Clock. This interface is an input if the I2S pads are used as a digital audio input in conjunction with I2S\_DIN. This interface is an output if the I2S pads are used as a digital audio output in conjunction with I2S\_DOUT.

## 5.5.3 SLIMBus

The module may support a SLIMBus interface for digital audio. For the electrical characteristics of the SLIMBus interface please refer to [9].

### 5.5.3.1 SLIM\_CLK

SLIMBus Clock Line.

### 5.5.3.2 SLIM\_DATA

SLIMBus Data Line.

## 5.6 Power, Ground, and Digital Logic Levels

The present document has defined six VCC pads to enable high continuous current if required.

### 5.6.1 Power Supply

#### 5.6.1.1 VCC Pads 1 ~ 6

VCC is a 3,8 Volt raw power supply input to the module.

For modules designed to operate on a raw voltage of 3,8 Volts all designs shall be able to operate on a power supply that meets the following requirements. Module designs may exceed these specifications.

**Table 3: VCC**

Name	Min	Typ	Max
VCC	3,4 V	3,8 V	4,2 V

The present document assumes a maximum current of 1 A per 1 mm<sup>2</sup> of VCC pad surface area.

The present document is intended to support multiple technologies and configurations, therefore to specify current draw for the power supply is beyond the scope of the present document.

#### 5.6.1.2 RTC\_POWER

This pad is intended to provide an external power supply input for the internal clock so that it may be maintained when VCC is not present at the module.

**Table 4: RTC\_POWER**

Name	Min	Typ	Max
RTC_POWER	2,0 V	3,0 V	3,25 V

### 5.6.2 Ground

All ground pins on the module are designed to be connected to ground on the host implementation.

### 5.6.3 Reference Voltage and Digital Logic Levels

#### 5.6.3.1 VREF

VREF is a reference voltage output supplied from the module to provide a logic reference for the following interfaces:

- UART1 and UART2 - see clause 5.2.1.
- WWAN Radio State - see clause 5.3.1.
- POWER\_ON - see clause 5.3.2
- Wakeup Out - see clause 5.3.3.
- Wake-up In - see clause 5.3.4.
- RESET - see clause 5.3.5.
- GPIO (unless otherwise indicated) - see clause 5.4.1.

This clause describes the electrical characteristics utilized based upon the VREF from the module.

**Table 5: Electrical characteristics—Generic Voltage Reference I/O**

Parameter	Description	Minimum	Typical	Maximum	Unit	Condition
V <sub>IL</sub>	Low-level input voltage	-0,3	0	0,30*VREF	V	
V <sub>IH</sub>	High-level input voltage	0,70*VREF	VREF	VREF + 0,3	V	V <sub>IH</sub> Maximum shall be a minimum level supported.
V <sub>OL</sub>	Low-level output voltage	0	0	0,45	V	I <sub>OL</sub> varies by pad definition
V <sub>OH</sub>	High-level output voltage	VREF - 0,45	VREF	VREF	V	I <sub>OH</sub> varies by pad definition
I <sub>OH</sub>	High-level output current			1 to 8	mA	Maximum varies by pad definition
I <sub>OL</sub>	Low-level output current			-1 to -8	mA	

**Table 6: Electrical characteristics - An example of a 1,8 V type (1V8) digital I/O**

Parameter	Description	Minimum	Typical	Maximum	Unit	Condition
V <sub>IL</sub>	Low-level input voltage	-0,3 V	0 V	0,54 V	V	
V <sub>IH</sub>	High-level input voltage	1,26 V	1,8 V	2,1 V	V	
V <sub>OL</sub>	Low-level output voltage	0,0 V	0,0 V	0,45 V	V	I <sub>OL</sub> varies by pad definition
V <sub>OH</sub>	High-level output voltage	1,35 V	1,8 V	1,8 V	V	I <sub>OH</sub> varies by pad definition
I <sub>OH</sub>	High-level output current			1 to 8 mA	mA	Maximum varies by pad definition
I <sub>OL</sub>	Low-level output current			-1 to -8 mA	mA	

## 5.7 Test and Debug Interface

For the electrical characteristics of the IEEE 1149.1 (Joint Test Action Group, or JTAG) interface for testing and debugging please refer to [10].

Implementation and location of the JTAG interface are optional.

## 5.8 Reserved for Future Use (RFU)

It is expected that the Reserved for Future Use pads shall be physically present but not connected internally to the surface mount module. These pads are reserved for definition in future revisions of the present document. Non-standard use of these pads may result in incompatibilities in solutions aligned with the future revisions.

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## Annex A (informative): Interfaces that may be provided over General Purpose I/O (GPIO) or General Purpose Pads (GPP)

Where clause 4 and 5 do not assign an interface to specific pads implementations may provide the interface over General Purpose I/O (GPIO) or General Purpose Pads (GPP) pads.

---

### A.1 Additional Interfaces

The interfaces defined in this clause are considered to be important for select module implementations. They may be implemented on pads designated as either GPIO or GPP on the module. Alternately a pad designated as GPP may be used to provide additional GPIO functions.

#### A.1.1 Module State Functions

The electrical characteristics of interfaces to signal the state of various module aspects is the following:

Interface	Description	I/O	Electrical characteristics
RF_DISABLE	Radio Enable/Disable	I	
GPS_STATE	GPS radio state	O	
PER1_STATE	Peripheral radio state	O	
TX_ON	Module transmitting	O	
READY	Module ready for I/O	O	

##### A.1.1.1 RF\_DISABLE

The Radio Enable/Disable interface can be used to enable and disable the transmitting capabilities of the module and properly deregister the module from the network without powering the module down. One application for this interface is to support "flight mode" for consumer electronics.

##### A.1.1.2 GNSS\_STATE

The GPS State pad can be used as an indication to the host device of whether the module has obtained a valid GPS fix or not.

##### A.1.1.3 PER1\_STATE

The PER1 State pad can be used as an indication to the host device of whether the module has a valid registration on the peripheral radio interface or not.

##### A.1.1.4 TX\_ON

The TX ON pad can be used as an indication to the host device of whether the module is actively transmitting over the cellular network or not.

##### A.1.1.5 READY

The READY pad can be used as an indication to the host device of whether the module is in a state when it is ready to start receiving commands from the host device.

## A.1.2 Analog Interfaces

The module may support analog interfaces other than RF such as analog audio (clause A.1.2.1) and an analog-digital converter (clause A.1.2.2). If these interfaces are supported, care should be taken with their placement on the module so as to avoid interference with digital interfaces. The electrical characteristics of an analog audio interface are as follows:

Interface	Description	I/O	Electrical characteristics
MICp	Microphone positive	I	Module defined
MICn	Microphone negative	I	
SPKp	Speaker positive	O	
SPKn	Speaker negative	O	
ADCI	A/D Converter input	I	
DACO	D/A Converter output	O	

### A.1.2.1 Analog Audio

The module may provide an analog audio interface for providing speaker and microphone access for devices are unable to support a digital audio interface.

### A.1.2.2 A/D Converter

The module may support an A/D converter for taking raw analog input data and converting it into digital logic levels. Care should be taken to ensure that the allowable input voltage range on this interface is clearly specified.

### A.1.2.3 D/A Converter

The module may support a D/A converter for taking digital logic level input data and converting it into an analog output.

## A.1.3 Host interface select

The module may provide an interface to allow the host to select a data interface if the module supports several such interfaces. This is a logical interface representing a binary number: an  $n$  line interface allows the host to choose between  $2^n$  interfaces:

Interface	Description	I/O	Electrical characteristics
HOST_IO_SEL1	$n$ -bit binary logic signal	I	Module defined
HOST_IO_SEL2		I	
...		...	
HOST_IO_SEL $n$		I	

## A.1.4 Antenna control

The module may support an interface for antenna control. Such an interface would typically have up to 4 lines:

Interface	Description	I/O	Electrical characteristics
RF_CTRL1	Generic interface for antenna control		Undefined
RF_CTRL2			
RF_CTRL3			
RF_CTRL4			

## A.1.5 Real Time Clock

The module may provide an interface for the host to provide a 32 kHz clock signal to the module or an interface for the host to provide power for the real time clock of the module:

Interface	Description	I/O	Electrical characteristics
RTC_IN	Real time clock in	I	Module defined

## A.1.6 Pulse Width Modulation

The module may provide a Pulse Width Modulation (PWM) interface to modulate acoustic and visual signals.

## A.1.7 Timer Interface

The module may provide a timer interface.

## A.1.8 Interrupt

The module may provide an interrupt interface.

## A.1.9 Dynamic Power Reduction

The module may provide a Dynamic Power Reduction (DPR) interface to allow hardware control for Specific Absorption Rates (SAR) adherence.

Interface	Description	I/O	Electrical characteristics
DPR	Dynamic Power Reduction	I	Module defined

## A.1.10 Virtual GPIO (vGPIO)

The module may provide a virtual GPIO (vGPIO) interface to increase the number of supported GPIO signals.

Interface	Description	I/O	Electrical characteristics
VGPI0_DIN	vGPIO Data In	I	Module defined (Under standardization efforts in MIPI)
VGPI0_DOUT	vGPIO Data Out	O	
VGPI0_CLK	vGPIO Clock	I/O	

---

## A.2 Peripheral Interfaces

Peripheral interfaces are interfaces that support the exchange of data and control information between the module and peripheral devices.

### A.2.1 Secure Digital Input Output Interface

Secure Digital Input Output (SDIO) is mostly used for storage or WLAN but can be also used for high speed data exchange in general. A device can be an SDIO master or slave. The electrical characteristics of the SDIO interface are as follows:



Interface	Description	I/O	Electrical characteristics
SDIO_CLK	SDIO clock signal	I/O	Please refer to [11]. On an SDIO slave the SDIO_CLK and SDIO_CMD interfaces are inputs (I). On an SDIO master the SDIO_CLK and SDIO_CMD interfaces are outputs (O).
SDIO_CMD	SDIO command	I/O	
SDIO_DATA1	Data line	I/O	
SDIO_DATA2	Data line	I/O	
SDIO_DATA3	Data line	I/O	
SDIO_DATA4	Data line	I/O	

## A.2.2 Inter Integrated Circuit Interface

The module may provide an Inter Integrated Circuit (I2C) interface to control off-board peripherals such as an accelerometer, camera or touch screen display.

Interface	Description	I/O	Electrical characteristics
I2C_CLK	I2C clock signal		Module defined
I2C_DATA	I2C data interface	I/O	

Note that if I2C is supported, the module will act as master to the peripheral.

## A.2.3 Serial Peripheral Interface

The module may provide a Serial Peripheral Interface (SPI), for connecting external display equipment or to control off-board devices such as ZigBee and Bluetooth:

Interface	Description	I/O	Electrical characteristics
SPI_CLK	SPI clock signal	O	Module defined
SPI_MOSI	SPI master out slave in	O	
SPI_MISO	SPI master in slave out	I	
SPI_SS	SPI slave select	O	

Note that the module may act as a master or slave to the peripheral.

## A.2.4 Controller Area Network Bus

The module may support a Controller Area Network (CAN) Bus interface, which is mostly used for automotive applications: For the electrical characteristics of the CANBUS interface please refer to [**Error! Reference source not found.**].

Interface	Description	I/O	Electrical characteristics
CAN_RX	CAN Bus receive data	I	
CAN_TX	CAN Bus send data	O	

---

## Annex B (informative): Design guidelines and recommendations

### B.1 Recommendations from ETSI ISG SMT on how to use the present document

The reader of the present document will find many well known interfaces and functionalities targeted to cover the majority of use cases for embedded wireless modules. The reader will also discover that not every pad or function is fully characterized thus leaving room for custom flexibility and future functionalities through the use of unassigned general purpose pads and pads reserved for future use.

When a host device manufacturer elects to build to and order modules according to the present document it is necessary to agree with target module suppliers which aspects of the specification are required, optional or not required for the products being ordered.

Module suppliers may select which interfaces, capabilities, and configuration they intend to supply based on the speculation of market demand. There is no guarantee of interoperability across different modules adherent to the present document. The present document makes no attempt to define the software control interface to the module.

For interfaces that are not fully specified in other fora, some electrical and functional behaviour may be specified in the present document. If it is not specified in other fora or the present document, then the module OEM can define it as is needed.

The present document assumes an LGA footprint is used for mechanical mounting purposes however, this does not explicitly exclude the use of other methods.

---

### B.2 Host PCB Pad Layouts

This clause provides possible printed circuit board (PCB) pad layouts for modules defined in the present document. The mechanical drawings for the host PCB footprints are as they would be seen looking downward toward the PCB. The recommended mechanical tolerances for PCB pad placement should allow for a variance of  $\pm 0,02$  mm from the dimensions defined. The present document indicates a minimum 0,35 mm overhang from any module outside pad to the outer edge of the module. Host PCB designs are recommended to take into consideration any overhang variance.

#### B.2.1 SMT3136 Module PCB Pad Layout

Figure 19 specifies host PCB pads for the SMT3136 module form factor. The form factor provides 146 pins which are numbered 1 through 146.

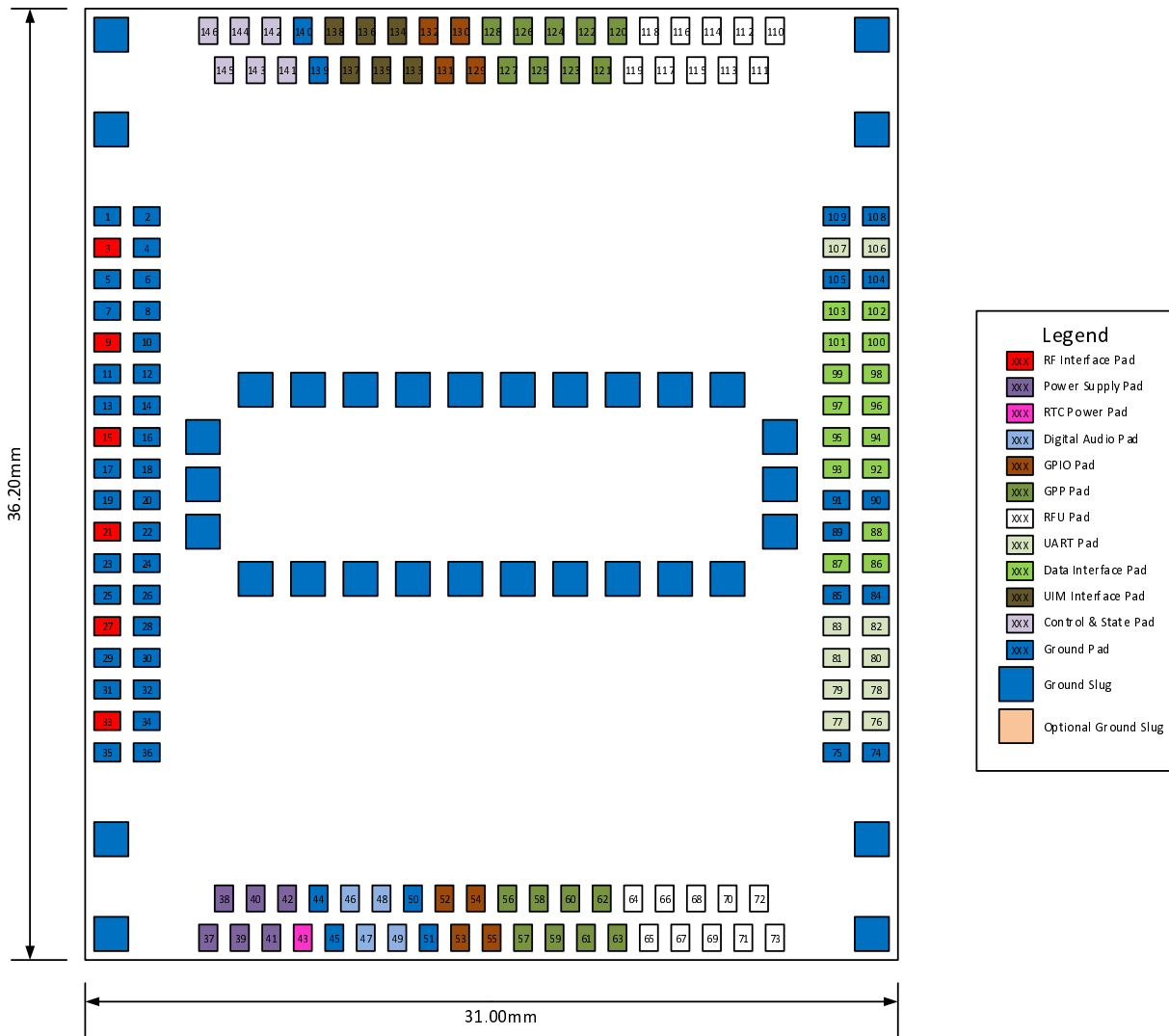


Figure 19: SMT3136 Module PCB Pad Layout

## B.2.2 SMT3129 Module PCB Pad Layout

Figure 20 specifies host PCB pads for the SMT3129 module form factor. The form factor provides 146 pins which are numbered 1 through 146.

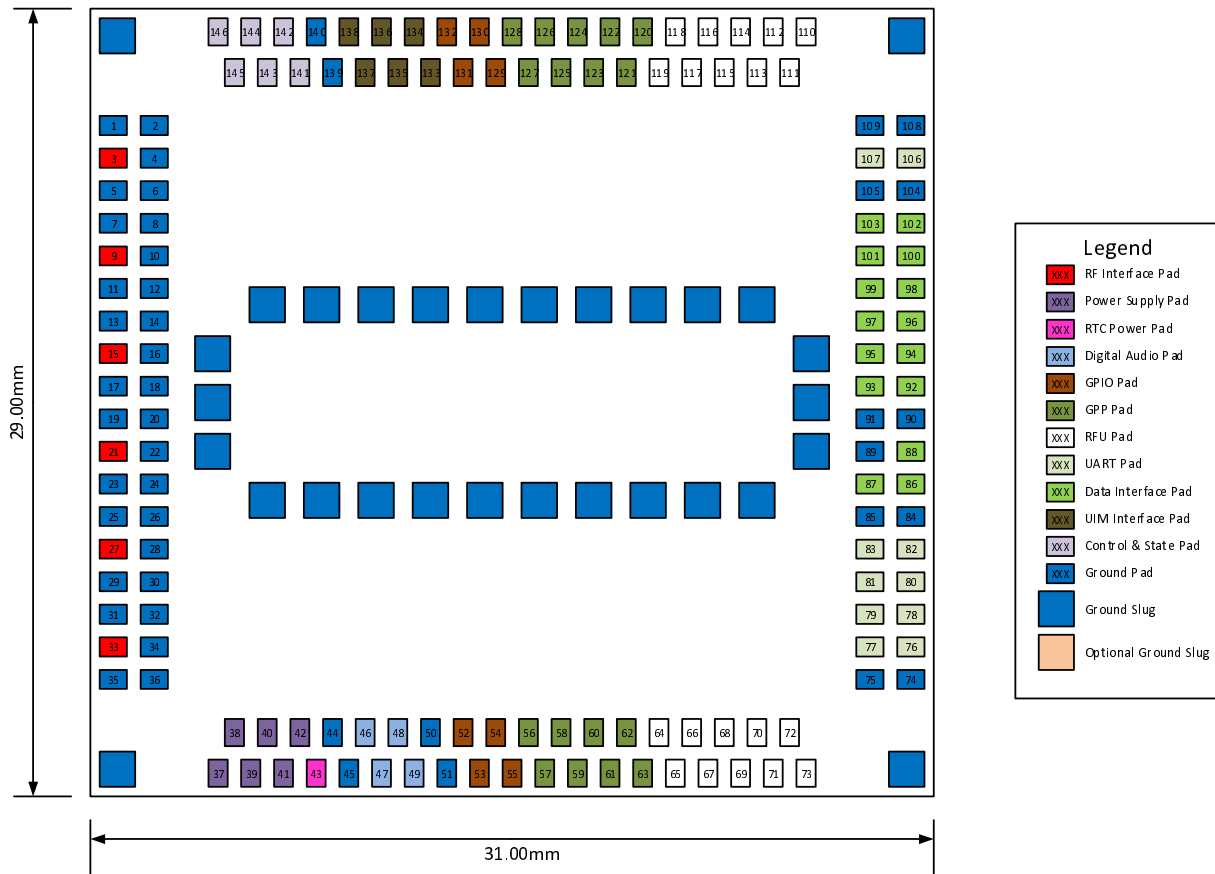


Figure 20: SMT3129 Module PCB Pad Layout

### B.2.3 SMT3122 Module PCB Pad Layout

Figure 21 specifies host PCB pads for the SMT3122 module form factor. The form factor provides 146 pins which are numbered 1 through 146.

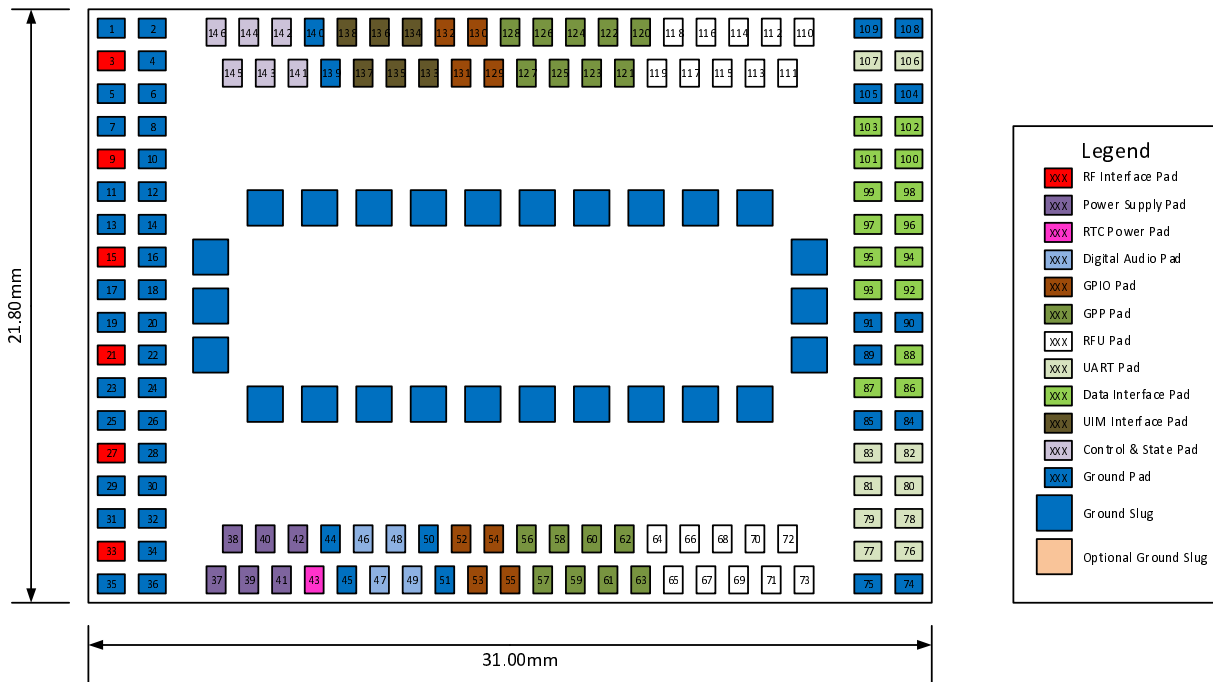


Figure 21: SMT3122 Module PCB Pad Layout

### B.2.4 SMT3136, SMT3129 and SMT3122 Common PCB Pad Layout

Figure 22 specifies host PCB pads for a board which can accommodate the SMT3136, SMT3129 and SMT3122 module form factors on a common PCB.

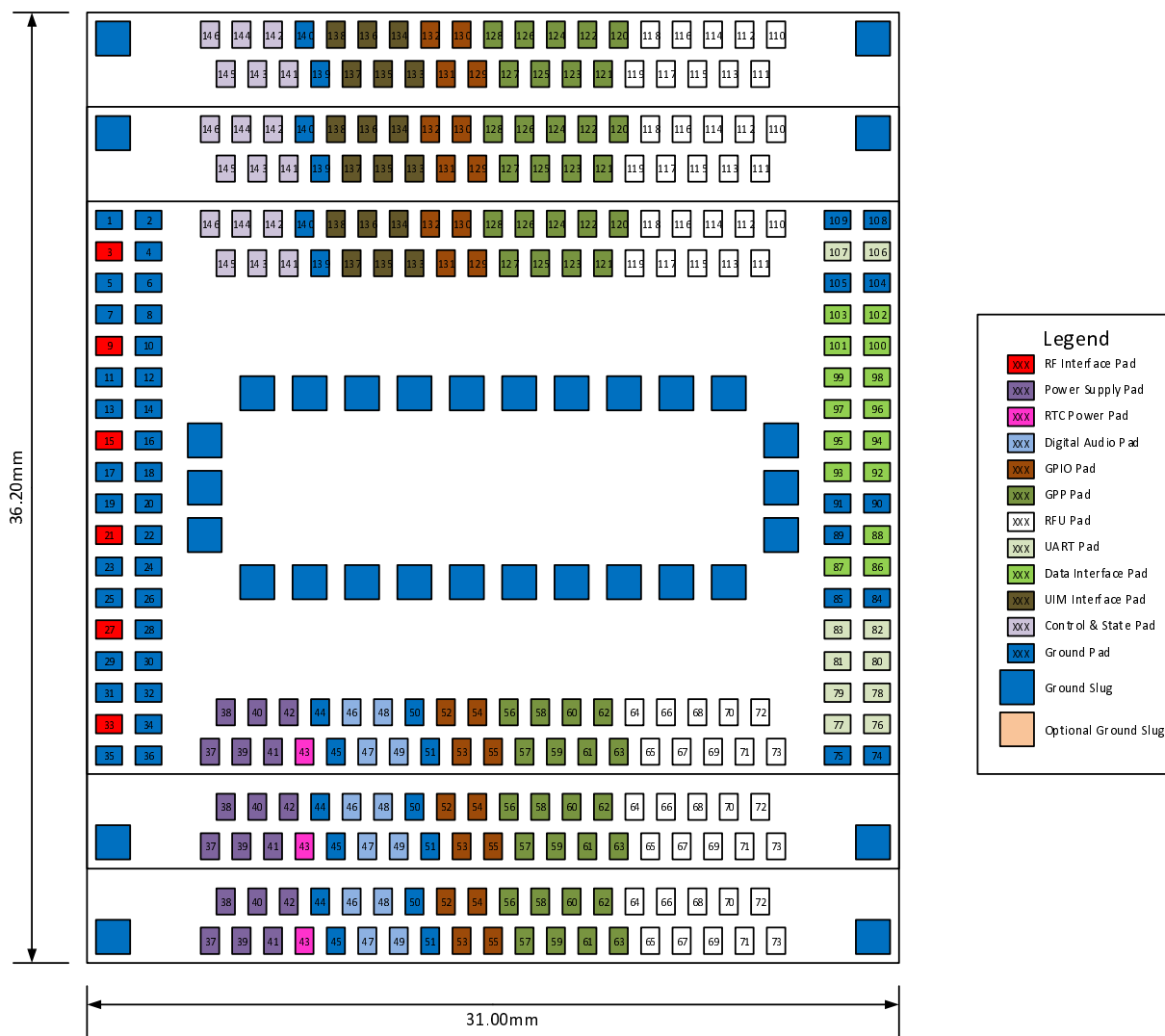


Figure 22: SMT3136, SMT3129, and SMT3122 Common PCB Pad Layout

### B.3 Reserved for Future Use (RFU) Pads on Host PCB

It is expected that the Reserved for Future Use pads should be physically connected for mechanical stability, but not electrically connected to anything on the host PCB. These pads are reserved for definition in future revisions of the present document. Non-standard use of these pads may result in incompatibilities in solutions aligned with the future revisions.

### B.4 Advanced Indicator Protocols for WWAN\_STATE

More advanced indicator protocols are allowed. Advanced features might include use of blinking or intermittent ON states which can be used to indicate radio operations such as scanning, associating, or data transfer activity. The implementation of blinking states may also be useful in reducing LED power consumption.

An example of a more advanced protocol:

Signal Off	Module off
Signal Fast blinking	network searching, not registered, turning off
Signal Slow blinking	Registered full service, In call
Signal On	No defined states

---

## B.5 Recommendations for RESET Implementation

The minimum timing to hold the RESET pad low for a hardware reset is recommended at 50 ms with a typical time of 100 ms.

In good design it is recommended that the host provides a high impedance (~100 k Ohm) external pull-up resistor connected to the high digital reference voltage to avoid an accidental low state on the pad.

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## Annex C (informative): Bibliography

GSM Association - "Embedded Mobile Surface Mount Technology, Technical Requirements" Version 1.0 September 29th, 2011.



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## History

<b>Document history</b>		
V1.1.1	October 2014	Publication