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Open Radio equipment Interface (ORI);
ORI Interface Specification;
Part 1: Low Layers
(Release 1)

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Foreword

This Group Specification (GS) has been produced by ETSI Industry Specification (ISG) Open Radio equipment Interface (ORI).

The present document is part 1 of a multi-part deliverable covering the ORI Interface Specification, as identified below:

Part 1: "Low Layers (Release 1)";

Part 2: "Control and Management (Release 1)".

1 Scope

The present document defines low layer protocols aspects of the Open Radio equipment Interface (ORI). Low layer protocols are those terminating the ORI Link (a bi-directional interface in-between two directly-connected ORI ports, on two ORI nodes).

The Layer 1/2 protocols of CPRI Specification [1] have been used as a baseline for which further requirements for protocols up to and including the Layer 2 have been defined.

See the associated specification "Requirements for Open Radio equipment Interface" [2] for more information on how the Low Layer protocols relate to other aspects of the ORI interface.

2 References

References are either specific (identified by date of publication and/or edition number or version number) or non-specific. For specific references, only the cited version applies. For non-specific references, the latest version of the reference document (including any amendments) applies.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

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2.1 Normative references

The following referenced documents are necessary for the application of the present document.

[1] "Common Public Radio Interface (CPRI); Interface Specification V4.1 (2009-02-18)".

NOTE: Available at http://www.cpri.info/spec.html.

[2] ETSI GS ORI 001: "Open Radio equipment Interface (ORI); Requirements for Open Radio equipment Interface (ORI); (Release 1)".

[3] SFF INF-8074i: "SFP (Small Formfactor Pluggable) 1 Gbs Transceiver", Revision 1.0, May 12, 2001".

NOTE: Available at http://www.sffcommittee.com.

[4] SFF SFF-8431: "SFP+", Revision 4.1, 6th of July 2009".

NOTE: Available at http://www.sffcommittee.com.

[5] ETSI TS 125 104: "Universal Mobile Telecommunications System (UMTS); Base Station (BS) radio transmission and reception (FDD) (3GPP TS 25.104)".

[6] ETSI TS 125 215: "Universal Mobile Telecommunications System (UMTS); Physical layer; Measurements (FDD) (3GPP TS 25.215)".

[7] ETSI TS 125 133: "Universal Mobile Telecommunications System (UMTS); Requirements for support of radio resource management (FDD) (3GPP TS 25.133)".

[8] ETSI TS 136 104: "LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); Base Station (BS) radio transmission and reception (3GPP TS 36.104)".

2.2 Informative references

The following referenced documents are not necessary for the application of the present document but they assist the user with regard to a particular subject area.

[i.1] ETSI GS ORI 002-2: "Open Radio Equipment Interface (ORI); ORI Interface Specification; Part 2: Control and Management (Release 1)".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the terms and definitions given in GS ORI 001 [2] and the following apply:

NOTE: For any terms used in the present document that are not defined either here or directly in the clause in which they are used, refer to CPRI specification [1].

Active link: See clause 3.1 in [2].

Antenna Carrier (AxC): See section 2.1 in [1].

AxC container: See section 2.1 in [1].

AxC container block: See section 2.1 in [1].

AxC group: See section 2.1 in [1].

Master Port: See section 2.1 in [1].

ORI Port: See clause 3.1 in [2].

ORI-specific negotiation: subset of negotiations between master port and slave port that are defined in section 4.5.3.5 of [1] to be "vendor-specific", but for which behaviour is explicitly defined within the ORI specification

ORI vendor-specific negotiation: subset of negotiations between master port and slave port that are defined in section 4.5.3.5 of [1] to be "vendor-specific", and not defined within the ORI specification to be "ORI-specific negotiations"

Passive Link: See clause 3.1 of [2].

RE antenna port: for Rx and Tx antenna ports, this corresponds to the Tx and Rx BS antenna connector as defined as Test Port A in [5] for UTRA-FDD, and [8] for E-UTRA

Slave Port: See section 2.1 in [1].

Stuffing bits: See section 2.1 in [1].

Stuffing samples: See section 2.1 in [1].

Subchannel: See section 4.2.7.4 in [1].

Uplink Automatic Gain Control (UL AGC): function that controls the gain of the RE UL signal path of an UTRA UL AxC with the target to keep the RMS level of the UL IQ signal at the ORI port at a target value (see clause 7.1.2)

3.2 Symbols

For the purposes of the present document, the following symbols apply:

AxC Antenna-carrier
V_{RMS} Target RMS level

3.3 Abbreviations

For the purposes of the present document, the following abbreviations apply:

3GPP	3rd Generation partner Project
AGC	Automatic Gain Control
BS	Base Station
C&M	Control and Management
CPRI	Common Public Radio Interface
dec	Decimal
DL	DownLink
E-UTRA	Evolved UMTS Terrestrial Radio Access
FDD	Frequency Division Duplex
HFN	Hyper-Frame Number
IQ	In-phase data and Quadrature data
L1	Layer 1
L2	Layer 2
LSB	Least Significant Bit
MAC	Media Access Control
MSB	Most Significant Bit
ORI	Open Radio equipment Interface
RE	Radio Equipment
REC	Radio Equipment Control
RMS	Root Mean Square
RTWP	Received Total Wideband Power
Rx	Receiver
SFP	Small Form-factor Pluggable
Tx	Transmitter
UL	UpLink
UTRA	UMTS Terrestrial Radio Access

4 ORI Low Layers specification compliance

The RE/REC compliant to the ORI Low Layers specification shall:

- be fully compliant to CPRI Specification, as defined in section 5.2 of [1];
- support mandatory requirements defined within ORI that are defined as options within CPRI Specification;
- support mandatory requirements defined within ORI that do not refer to functionality in CPRI Specifications.

5 Layer 1 configuration

5.1 General

Requirements for the L1 characteristics are defined below. For each of the defined characteristics, the level of support shall be declared for each port of the RE/REC.

Line bit rate

At least one of the CPRI line bit rate options specified in [1], section 4.2.1 shall be supported by the RE and REC, with the exception of 614,4 Mbit/s line bit rate.

Physical Interface

At least one of the following interfaces shall be supported:

- Optical interface parameters defined in clause 5.2.
- Electrical interface parameters defined in clause 5.3.

5.2 Optical interface

Connector type

At least one of the following connector types shall be supported by the RE and REC: LC-type, SC-type.

Simplex/Duplex operation mode

At least one of the following operation modes shall be supported by the RE and REC: Simplex (one fibre per direction), Duplex (one fibre for both transmission and reception).

Optical Fiber Type

The ORI recommendation for optical cabling follows section 4.2.4.1. of [1].

Wave length

The wave lengths to be supported by RE and REC are not specified.

Optical output power

Optical output power to be supported by RE and REC is not specified.

Sensitivity

The optical sensitivity to be supported by RE and REC is not specified.

Signal condition capabilities

The maximum fibre length and attenuation to be supported by RE and REC are not specified.

5.3 Electrical interface

Electrical Connector type

At least one of the following connector types shall be supported by the RE and REC:

- SFP [3], SFP+ [4], those defined in section 4.2.3.2 of the CPRI Specification [1].

Electrical Cable Type

The Electrical Cable Type for the ORI link follows section 4.2.3.1 in the CPRI Specification [1].

Electrical Interface Characteristics

No specific Electrical Interface Characteristics are specified by ORI. It is recommended to follow section 6.2 of the CPRI Specification [1].

6 Control plane

6.1 Mapping to CPRI protocol structure

ORI compliant nodes shall apply the usage of subchannels defined in CPRI control words (see [1]), as described in Table 6.1.1:

Table 6.1.1: Subchannel allocation within ORI

Subchannel Ns	Area	Usage
0 to 15	CPRI reserved control words	Refer to CPRI [1] for usage.
16 to 40	Vendor specific area	This area is open for vendor specific use; general ORI rules for vendor specific extensions apply (see [2]).
41 to 52	ORI reserved area	This area shall be reserved for specification by ORI. See clause 6.3 for further definition.
53 to 63	Fast C&M channel	This area carries the ORI C&M messaging (for active links only). (min. 10,56 Mbit/s @ 1 228,8 Mbit/s link speed).

NOTE: As the minimum CPRI link rate supported by ORI is 1 228,8 Mbit/s, control words have a minimum width of 16 bits.

The listed allocation leads to the map of CPRI control words, which shall be mapped for active links as described in Figure 6.1.1.

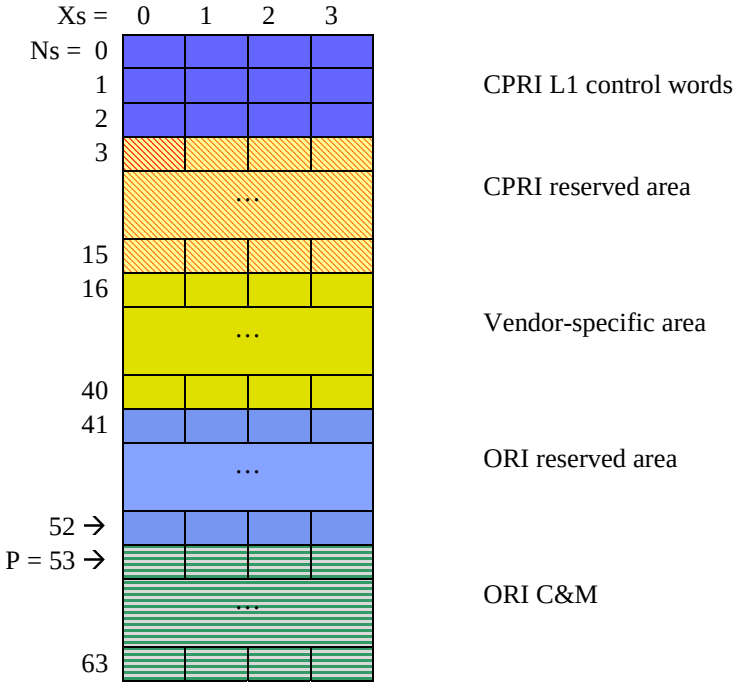

Figure 6.1.1: Control word mapping to subchannel allocation

6.2 C&M resource allocation

The Fast C&M channel, as described in [1] shall be supported by REC and RE for both Downlink and Uplink C&M communication.

The C&M pointer p is defined at byte Z.194.0 in [1].

The master port shall set byte Z.194.0 with p= 53 [dec] for active links, and p = 0 for passive links.

6.3 ORI reserved area

The Control Words in the "ORI reserved area" shall be reserved for specification within ETSI ORI, and shall not be used for other purposes.

The control words within the ORI reserved area shall be allocated as described in Table 6.3.1.

Control words not defined in table 6.3.1 are reserved for future definition, shall be set to 0 in this Release of the specification, and shall not be interpreted by the receiving ORI node.

Table 6.3.1: Control word definition within ORI reserved field

Subchannel index Ns	Allocation	Data content	Comment
52	PORT_ID	See clause 6.3.1	
50 and 51	RTWP measurement report	See clause 6.3.2	

6.3.1 PORT_ID

The PORT_ID uniquely identifies an ORI port of an ORI node (RE or REC). It is defined as follows:

<PORT_ID> = <MAC address><ORI port number><reserved byte>

MAC address: Ethernet MAC address of the node (size: 6 bytes)

ORI port number: one byte indicating the port number (from 1 to 255) per node. The port number 0 shall not be used but is reserved for possible future purposes (e.g. testing); therefore up to 255 ports per node can be addressed.

Reserved byte: The transmitter shall send zero for the reserved byte and the receiver shall not interpret this byte.

The size of the PORT_ID is 8 bytes in total such that the information completely fills two bytes (Y = 0, Y = 1) of the subchannel. For line rates higher than 1,228 Gbps, the additional bytes (Y > 1) of the subchannel shall be treated as reserved.

The exact bitwise mapping of the PORT_ID shall be as shown in Table 6.3.1.1.

Table 6.3.1.1: Allocation of PORT_ID within subchannel

Byte number	Bit number	Z.52.Y	Z.116.Y	Z.180.Y	Z.244.Y
Y = 0	B = 0	LSB of reserved byte	LSB of MAC byte#0	LSB of MAC byte#2	LSB of MAC byte#4
	:	:	:	:	:
	:	:	:	:	:
	B = 7	MSB of reserved byte	MSB of MAC byte#0	MSB of MAC byte#2	MSB of MAC byte#4
Y = 1	B = 8	LSB of Port number	LSB of MAC byte#1	LSB of MAC byte#3	LSB of MAC byte#5
	:	:	:	:	:
	:	:	:	:	:
	B = 15	MSB of Port number	MSB of MAC byte#1	MSB of MAC byte#3	MSB of MAC byte#5

The PORT_ID shall be sent in each hyperframe upon achieving L1/L2 synchronization of the ORI link.

An example for topology detection based on the PORT_ID is given in clause A.1.

6.3.2 UTRA RTWP measurement report

For UTRA-FDD operation, the Received Total Wideband Power (RTWP) shall be measured and reported from RE to REC as defined below:

1) RTWP measurement definition:

   The received total wide band power, including noise generated in the receiver, within the bandwidth defined by the receiver pulse shaping filter. The reference point for the measurement shall be the RE (Rx) antenna port. In case of receiver diversity the value shall be reported per AxC from the RE. It is the responsibility of the REC to use these reported values to create the RTWP measurement defined by TS 125 215 [6].

2) RTWP measurement period in the RE:

   The RTWP measurement period shall be 2 ms.

3) RTWP measurement accuracy minimum performance requirement:

   The RTWP measurement performed by RE and reported to REC shall have an accuracy such that the measurement reported to the REC allows the REC to meet the RTWP minimum performance requirements defined in TS 125 133 [7] corresponding to the Base Station class supported by the RE.

4) RTWP measurement reporting:

   - Reporting conditions:

     The Received Total Wideband Power measurement shall be reported per AxC. Reporting of a real value is required for all AxCs of type "UTRA-FDD" that are configured and reporting shall be performed autonomously by the RE. An RTWP reported value shall be reported from the RE every 2 ms.

NOTE: An AxC is configured by higher layers as defined in [i.1].

   - Mapping of RTWP measured values to RTWP reported values:

     The RTWP measured value is adjusted according to the value of "UL feeder adjustment" prior to reporting, as defined and indicated to the RE in [i.1].

     In table 6.3.2.1 the mapping of the RTWP measured value (after feeder adjustment) to the RTWP reported value is defined. The reporting range for Received total wideband power (RTWP) is from -112 dBm to -50 dBm.

     The range in the signalling may be larger than the guaranteed accuracy range. The reported value shall be expressed in 0,1 dB steps.

Table 6.3.2.1: RTWP reported value mapping

Reported value	RTWP Measured value after feeder adjustment	Unit
0x0000	RTWP < -112,0	dBm
0x0001	-112,0 ≤ RTWP < -111,9	dBm
0x0002	-111,9 ≤ RTWP < -111,8	dBm
…	…	…
0x026B	-50,2 ≤ RTWP < -50,1	dBm
0x026C	-50,1 ≤ RTWP < -50,0	dBm
0x026D	-50,0 ≤ RTWP	dBm

5) Signal format at the RTWP measurement report:

   The RTWP measurement report shall be transmitted to REC in the ORI reserved area of the Control word. The RTWP measurement reported values for all AxCs shall be transported in the area of hyperframe number 0, 30, 60, 90, 120 (HFN#0, 30, 60, 90, 120). For the mapping of the RTWP reported value to ORI subchannel, a unique AxC RTWP group shall be defined for each AxC for which RTWP reporting is required. The mapping of AxC to AxC RTWP group is defined in [i.1].

Based on the frame structure described in [1], Table 6.3.2.2 describes the required mapping of AxC RTWP groups to the subchannels 50 and 51, and corresponding values of Xs. Only the AxC RTWP groups contained within byte numbers Y = 0 and Y = 1 are described, i.e. AxC RTWP groups 1 to 8 only.

The AxC RTWP group corresponding to other Y values is described in Table 6.3.2.3, where the value ***n*** is an integer value ranging from 1 to 8, corresponding to AxC RTWP groups values 1 to 8. For AxC RTWP group values higher than 8, the AxC RTWP group value generated from a given value of ***n*** shall be mapped to the same subchannel and Xs value as that of the AxC RTWP group ***n*** in the Table 6.3.2.2, i.e. for Y = 2,3, the AxC RTWP group 9 shall map to subchannel 50 and Xs = 0.

Table 6.3.2.2: Allocation of RTWP reported value to subchannel and Xs value for Y = 0,1 (HFN#0)

Subchannel number Ns	Xs = 0	Xs = 1	Xs = 2	Xs = 3
50	1st AxC RTWP group	2nd AxC RTWP group	3rd AxC RTWP group	4th AxC RTWP group
51	5th AxC RTWP group	6th AxC RTWP group	7th AxC RTWP group	8th AxC RTWP group

Table 6.3.2.3: Allocation of RTWP reported value to subchannel and Xs value for Y > 1 (HFN#0)

BYTE number, Y	AxC RTWP group
0, 1	***n***-th AxC RTWP group
…	
i, ***i*** +1	(***i****4 + ***n***)-th AxC RTWP group
…	
($N_{bitrate}$ -1)*2, ($N_{bitrate}$ -1)*2+1	((($N_{bitrate}$ **- 1**)*2)*4 + ***n***)-th AxC RTWP group

$\mathbf{N}_{bitrate}$ is the number calculated from the bitrate as $\mathbf{N}_{bitrate}$ = (line bitrate) / 1 228,8 (Mbit/s).

Figure 6.3.2.1 shows the corresponding bit assignment for AxC RTWP groups 1 to 8 where the variable B refers to the bit counter as defined in CPRI [1].

For AxC RTWP groups 9 to 16, the bit counter B ranges from 31 (MSB) to 16 (LSB).

For AxC RTWP groups 17 to 24, the bit counter B ranges from 47 (MSB) to 32 (LSB), and so on.

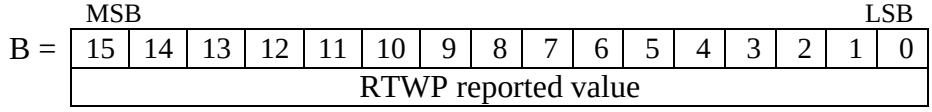

Figure 6.3.2.1: Bit allocation at RTWP reported value for AxC RTWP groups 1 to 8

6.4 ORI low layer reset

Upon receiving a valid reset in Z.130.0 as defined in the CPRI Specification [1] the RE shall perform an equivalent to a power-up reset of the RE. The ORI Low Layer Reset may be used when there is no functional Control and Maintenance channel established to reset the RE.

6.5 Data link layer for Fast C&M channel

The Data Link Layer for Fast C&M shall be as defined in section 4.4 of [1].

7 User plane

7.1 Mapping and format of IQ data

The ORI user plane may be configured to transport IQ sampled data of AxCs for E-UTRA, UTRA-FDD, or both E-UTRA and UTRA-FDD simultaneously. The RE and REC shall support at least the following configuration of the user plane for the respective scenarios. The parameters are defined in [1].

NOTE: Section 4.2.7.2 of [1] is the basis on which the requirements below have been derived, and further definition of parameters and terms is found in that specification.

7.1.1 E-UTRA

- CPRI mapping method 3 ("backward compatible") shall be used as defined in section 4.2.7.2.7 of [1] and applying the values according to Table 7.1.1.1 that correspond to the different E-UTRA channel bandwidths supported. E-UTRA channel bandwidths are also listed in TS 136 104 [8].
- No AxC grouping (i.e. N_A=1).
- No stuffing samples, i.e. N_V = 0 (N_C = S) for all sampling rates - except 1,92 MHz - as shown in Table 7.1.1.1.
- All S AxC containers of the same AxC Container Block mapped in "packed position". Further mapping is specified in [i.1].
- 2's complement code numbers for I and Q data in UL and DL (MSB = sign bit).
- DL and UL sample width M = M' = 15.
- For DL, the maximum transmission power (dBm) per AxC at the RE (Tx) antenna port shall be defined as 100 % when the effective voltage amplitude value V_{RMS} (= sqrt (I^2+Q^2)) = 3 277 [dec].
- For UL, the reception power per AxC at the RE (Rx) antenna port is defined as Pr(= reference sensitivity +67,1 dB) when the effective voltage amplitude value V_{RMS} (= sqrt (I^2+Q^2)) = 16 383 [dec].
- The content of stuffing bits/samples is not specified in ORI specifications.

Table 7.1.1.1: Number N_V of stuffing samples for N_A =1 (E-UTRA)

E-UTRA channel bandwidth [MHz]	f_S [MHz]	N_A	S	K	N_C	$N_V = N_C \cdot K - N_A \cdot S$
1,4	1,92	1	1	2	1	1
3	3,84	1	1	1	1	0
5	7,68	1	2	1	2	0
10	15,36	1	4	1	4	0
15	23,04	1	6	1	6	0
20	30,72	1	8	1	8	0

7.1.2 UTRA-FDD

- The mapping shall be according to [1], section 4.2.7.2.
- 2's complement code numbers for I and Q data in UL and DL (MSB = sign bit).
- Downlink (DL) sample width M = 15.
- The maximum transmission power per AxC at the RE (Tx) antenna port shall be defined as 100% when the effective voltage amplitude value V_{RMS} (= sqrt (I^2+Q^2)) = 3 277 [dec].
- Downlink Oversampling Ratio n = 1.

- Downlink Mapping of AxC Container within one Basic Frame: Option 1 (packed position). Further mapping is specified in [i.1].
- Uplink (UL) sample width M' = 7.
- Uplink Oversampling Ratio n = 2.
- IQ data shall express the linear value of voltage amplitude. The RE shall clip the IQ sample data to the limit of the interface format when the linear value would otherwise exceed the range of the interface format.
- Uplink Mapping of AxC Container within one Basic Frame: Option 2 (flexible position) with 2 reserved bits following each UTRA-FDD UL AxC Container – in order to allow the same effective positioning of AxC Containers in UL as in DL (see note). Further mapping is specified in [i.1].

NOTE: 1 UL AxC(M' = 7) + 2 reserved bits is in total the same number of bits (30 bits) as 1 DL AxC(M = 15).

- **UL AGC**: The following UL AGC configuration shall be supported:
  - Target RMS level (V_{RMS}):
    - This is configured in the RE via C&M, as defined in [i.1].
    - Value range for V_{RMS} (= sqrt (I^2+Q^2)) = 6 to 32[dec], in steps of 1[dec].
  - Settling Time:

    Time interval for the RMS level to settle to the configured target RMS level for any RX input power step with a maximum residual error of 1dB.
    - value range: 66,7 µs x 2^N with N = 0, …, 12

      The N value to be used is configured in the RE via C&M. Capability concerning supported N values are signalled from the RE via C&M. This is further defined in [i.1].
    - settling time accuracy: ±20 %
  - The maximum power error in AGC settlement for any Rx input power change: ±1 dB.

An optional mode for in-band reporting of AGC values shall be specified in Release 2 of the ORI specification.

7.1.3 E-UTRA and UTRA-FDD combined

Details of both E-UTRA and UTRA-FDD shall apply at the same time.

8 ORI start-up sequence

8.1 General

The start-up sequence shall follow section 4.5 of [1] with the following additions and/or exceptions.

8.2 Optical interface

For optical interface, the additional actions shall be followed:

In CPRI State A:

Master port: the output shall be off.

Slave port: the output shall be off.

In CPRI State B:

Master port: the optical output shall be switched "from off to on" upon entering state B of the start-up sequence.

Slave port: the optical output shall be off until the slave port has detected optical light from the master port on the other side of the link and has reached synchronization state HFNSYNC in State B.

In CPRI States C through G:

Master port: the output shall be on.

Slave port: the output shall be on.

8.3 CPRI Transition 6 in ORI

Trigger:

All of the ORI specific negotiations and vendor specific negotiation have been successfully completed.

Note that, if neither ORI specific negotiation nor vendor specific negotiation is defined, the transition 4 (state D to E) directly causes the transition 6.

NOTE: The definition of any vendor specific negotiation is not specified in the ORI specifications.

Actions:

The "layer 1 start-up timer" is cleared.

8.4 Layer 1 start-up timer value

The L1 start-up timer is defined in section 4.5.2 of the CPRI Specification [1]. The master port and the slave port shall use the following value as the L1 start-up timer expiry value, with the exception when "vendor specific" negotiation is involved and for which case the timer value can be extended accordingly.

Master port: 9,9 seconds to 10,1 seconds.

Slave port: 9,9 seconds to 10,1 seconds.

NOTE: If ORI vendor specific negotiation in state E is involved, this value has to be reconsidered.

8.5 CPRI State B duration in ORI

In state B, the slave port shall attempt to reach synchronisation state HFNSYNC for at least the duration of 10 minutes.

Annex A (informative): Example for topology detection based on PORT_ID

PORT_IDs are sent via a L1 control word upon achieving L1/L2 synchronization on a CPRI link (see clause 6.3.1). Figure A.1.1 shows the PORT_IDs of an exemplary topology (that exceeds topologies supported by ORI Release 1).

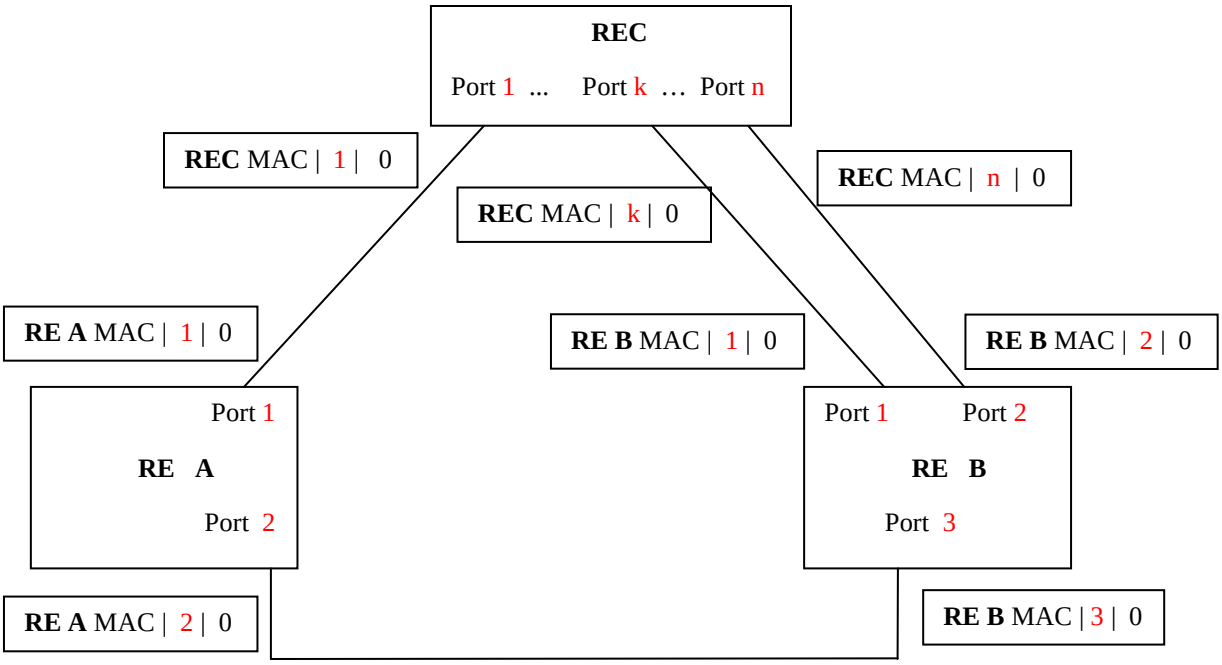

Figure A.1.1: Topology example

In topologies supported by ORI Release 1, a REC is directly connected to all REs. Therefore, the REC can derive the complete topology directly from the L1 control word containing the PORT_ID.

In future releases of ORI, also more complicated topologies might be supported, e.g. chains of REs. The REC can derive neighbour relations based on L3 PORT_ID reports as exemplarily shown in Table A.1.1.

Table A.1.1: PORT_ID reports for the example given in Figure A.1.1

Node	Transmitted PORT_ID	Received PORT_ID
Known in REC:	REC MAC | 1 | 0	RE A MAC | 1 | 0
	…	…
	REC MAC | k | 0	RE B MAC | 1 | 0
	…	…
	REC MAC | n | 0	RE B MAC | 2 | 0
Reported by RE A:	RE A MAC | 1 | 0	REC MAC | 1 | 0
	RE A MAC | 2 | 0	RE B MAC | 3 | 0
Reported by RE B:	RE B MAC | 1 | 0	REC MAC | k | 0
	RE B MAC | 2 | 0	REC MAC | n | 0
	RE B MAC | 3 | 0	RE A MAC | 2 | 0

History

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