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on metallic local lines**

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Foreword

This ETSI Technical Report (ETR) was produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

ETRs are informative documents resulting from ETSI studies which are not appropriate for European Telecommunication Standard (ETS) or Interim European Telecommunication Standard (I-ETS) status. An ETR may be used to publish material which is either of an informative nature, relating to the use or the application of ETSs or I-ETSs, or which is immature and not yet suitable for formal adoption as an ETS or an I-ETS.

This ETR describes a transmission technique called High bit rate Digital Subscriber Line (HDSL), as a means for the transportation of several types of applications.

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1 Scope

This ETSI Technical Report (ETR) describes a transmission technique called High bit rate Digital Subscriber Line (HDSL), as a means for the transportation of several types of applications. The ETR defines the requirements for the individual HDSL transmission system, the transmission performance, the HDSL maintenance requirements and procedures and the mapping of information from the dedicated applications.

An individual HDSL transceiver system is a two wire bi-directional transceiver for metallic wires using the echo cancellation method. Two systems may be utilized, one transporting a bit rate of 784 kbit/s over each of three pairs used in parallel and a second with an increased bit rate of 1 168 kbit/s and two pairs in parallel only.

This ETR defines the common circuitry for combining and controlling two or three HDSL transceiver systems, depending on the bit rate of the transceiver system used, for the support of applications with a 2 048 kbit/s hierarchy. The common circuitry and the necessary number of HDSL transceiver systems form the HDSL core, which is independent from the different applications defined in this ETR.

The applications of are determined by the functionality of the mapping and interface part some of which are defined as follows:

- ISDN primary rate access digital section in accordance with ETS 300 233 [4];
- ONP leased line access D2048U based on ETS 300 246 [5] and ETS 300 247 [6];
- ONP leased line access D2048S based on ETS 300 418 [8] and ETS 300 419 [9];
- TU 12 or VC12 access for the SDH.

The HDSL core may be used for applications that are not restrictive to the access portion of the network but this is outside the scope of this ETR.

NOTE: If further applications are identified in future this ETR may be enhanced to define the relevant interface and mapping requirements as far as these do not violate the specification of the HDSL core.

Special applications of the HDSL core or part of the HDSL core can be:

- fractional installation, which provides reduced access capability only by a reduced number of HDSL transceivers, to cater for an inexpensive system if the total capacity of 30 x 64 kbit/s is not needed. The bit rate at the application interface will be 2 048 kbit/s also in this application, but only part of the time slots in the ITU-T Recommendation G.704 [19] frame may be occupied;
- partial operation, which is the persistent operation of the operable HDSL transceiver systems when others become inoperable;
- fractional payload, e.g. H0-channel;
- n x 64 kbit/s services.

There may also be other applications possible with the HDSL core, e.g. for the transport of bit rates lower than 2 048 kbit/s.

This ETR does not specify all the requirements for the implementation of NTU, LTU or REG. It serves only to describe the functionality needed.

2 References

This ETR incorporates by dated and undated reference, provisions from other publications. These references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETR only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- [1] ETR 080 (1993): "Transmission and Multiplexing (TM); Integrated Services Digital Network (ISDN) basic rate access; Digital transmission system on metallic local lines".
- [2] ETS 300 011 (1992): "Integrated Services Digital Network (ISDN); Primary rate user-network interface; Layer 1 specification and test principles".
- [3] ETS 300 019: "Equipment Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment".
- [4] ETS 300 233 (1994): "Integrated Services Digital Network (ISDN); Access digital section for ISDN primary rate".
- [5] ETS 300 246 (1993): "Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased line (D2048U); Network interface presentation".
- [6] ETS 300 247 (1993): "Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased line (D2048U) Connection characteristics".
- [7] ETS 300 386: "Equipment Engineering (EE); Public telecommunication network equipment Electro-Magnetic Compatibility (EMC) requirements".
- [8] ETS 300 418: "Business Telecommunications (BTC); 2 048 kbit/s digital unstructured and structured leased lines (D2048U and D2048S); Network interface presentation".
- [9] ETS 300 419: "Business Telecommunications (BTC); 2 048 kbit/s digital structured leased line (D2048S); Connection characteristics".
- [10] EN 41003: "Particular safety requirements for equipment to be connected to telecommunication networks".
- [11] EN 60950: "Safety of information technology equipment, including electrical business equipment".
- [12] ITU-T Recommendation G.823 (1993): "The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy".
- [13] ITU-T Recommendation G.826 (1993): "Error performance parameters and objectives for international, constant bit rate digital paths at or above the primary rate".
- [14] ITU-T Recommendation I.431: "Primary rate user-network interface - Layer 1 specification".
- [15] CCITT Blue Book - Fascicle I.3: "Terms and definitions. Abbreviations and acronyms. Recommendations on means of expression (Series B) and General telecommunications statistics (Series C)".

- [16] ITU-T Recommendation K.17 (1990): "Tests on power-fed repeaters using solid-state devices in order to check the arrangements for protection from external interference".
- [17] ITU-T Recommendation K.20 (1994): "Resistibility of telecommunication switching equipment to overvoltages and overcurrents".
- [18] ITU-T Recommendation K.21 (1988): Resistibility of subscribers' terminals to overvoltages and overcurrents".
- [19] ITU-T Recommendation G.704: "Synchronous frame structures used at primary and secondary hierarchical levels".

3 Abbreviations

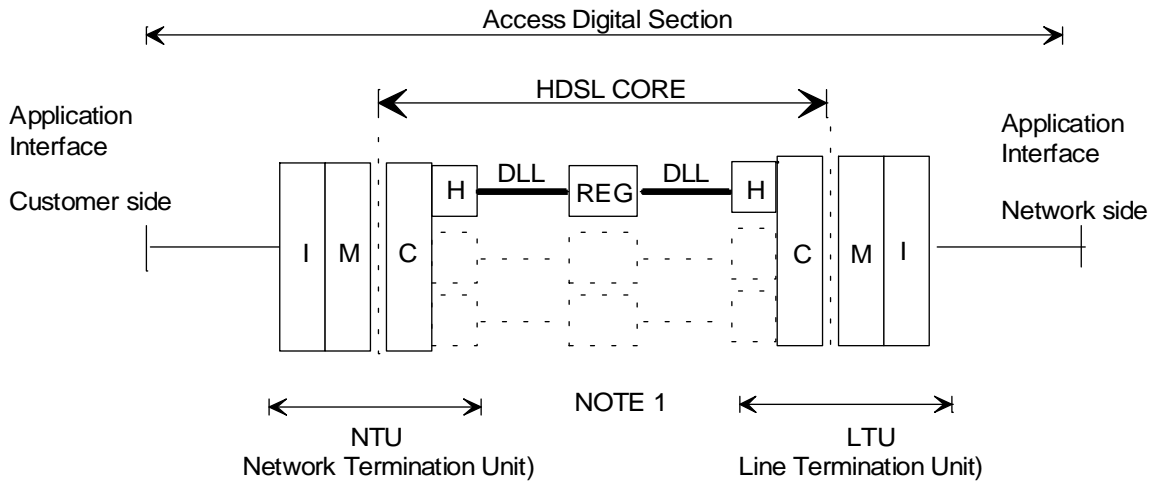
For the purposes of this ETR, the following abbreviations apply:

BERTS	Bit Error Ratio Test Set
BT	Bridged Tap, an unterminated twisted pair section bridged across the line
DLL	Digital Local Line
EOC	Embedded Operations Channel
IUT	Item Under Test
LCL	Longitudinal Conversion Loss
LFA	Loss of Frame Alignment
LOS	Loss of Signal
LTU	Line Termination Unit
NEXT	Near End CrossTalk
NTU	Network Termination Unit
O&M	Operation and Maintenance
PRBS	Pseudo-Random Bit Sequence
PSL	Power Sum Loss
REG	Regenerator
REG-C	NTU side of the regenerator
REG-R	LTU side of the regenerator
TMN	Telecommunication Management Network

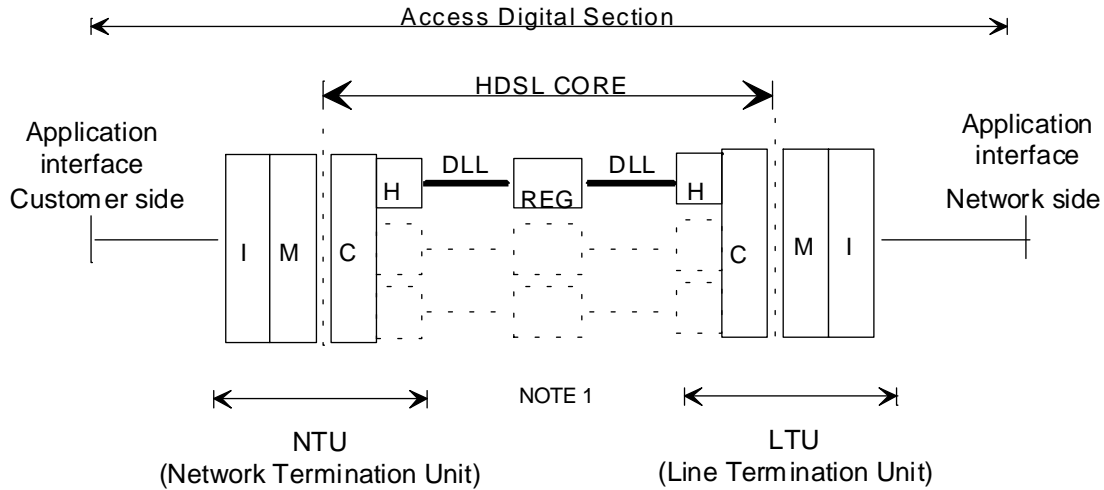
4 Reference configuration and functional description

An access digital section which uses HDSL technology can be considered as a number of functional blocks, see figure 1. Depending upon the HDSL transceiver (H) transmission rate, a fully equipped HDSL core consists of two 1 168 kbit/s or three 784 kbit/s HDSL transceiver pairs connected by Digital Local Lines (DLLs) (and optional Regenerators (REGs)), which are linked by some common circuitry (C). The HDSL core is application independent. Operation with a non fully equipped HDSL core is also permitted. An application is defined by the interface (I) and mapping & maintenance (M) functionalities.

The functionalities at the exchange side constitute the Line Termination Unit (LTU) and act as master to the (slave) customer side functionalities, which collectively form the Network Termination Unit (NTU) and the REGs where applicable.



Description of functional blocks:
 C = Common circuitry
 H = HDSL transceiver
 I = Interface
 M = Mapping and Maintenance
 REG = Regenerator

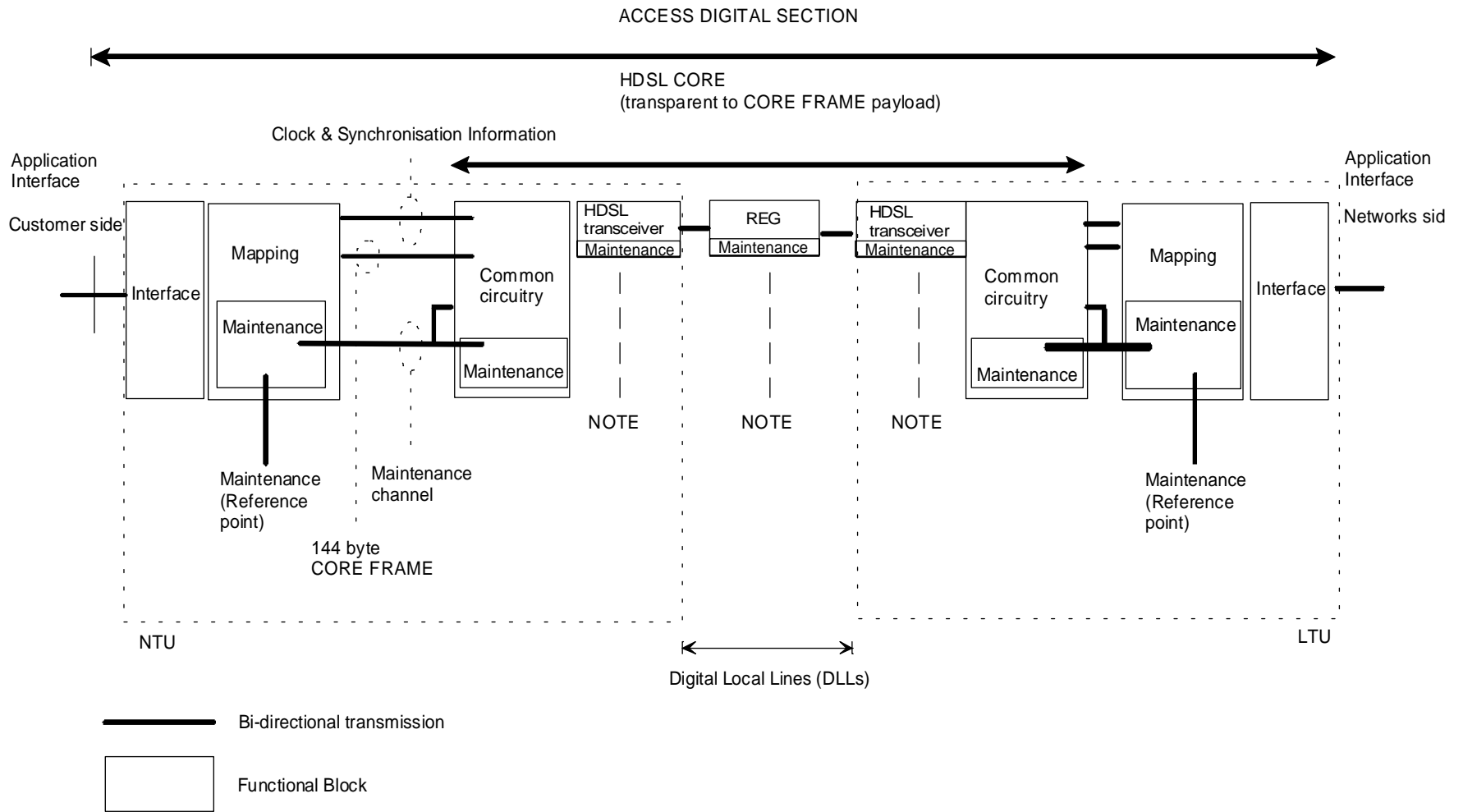


NOTE: A fully equipped HDSL CORE consists of two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 1: Access Digital Section employing HDSL technology (simplified configuration)

It should be noted that throughout this ETR, reference is made to the terms REG-C, REG-R and individual HDSL transmission systems. REG-R identifies functionalities located at the LTU side of the regenerator, REG-C identifies functionalities located at the NTU side of the regenerator, and an individual transmission system can be considered to consist of H + DLL (with optional REG) + H functional groups.

Figure 2 describes the maintenance and other communication functionalities more clearly.



NOTE: A fully equipped HDSL CORE consists of two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 2: Access digital section employing HDSL technology (detailed configuration)

The information transmitted between the NTU side (slave side) and LTU side (master side) is handled as follows:

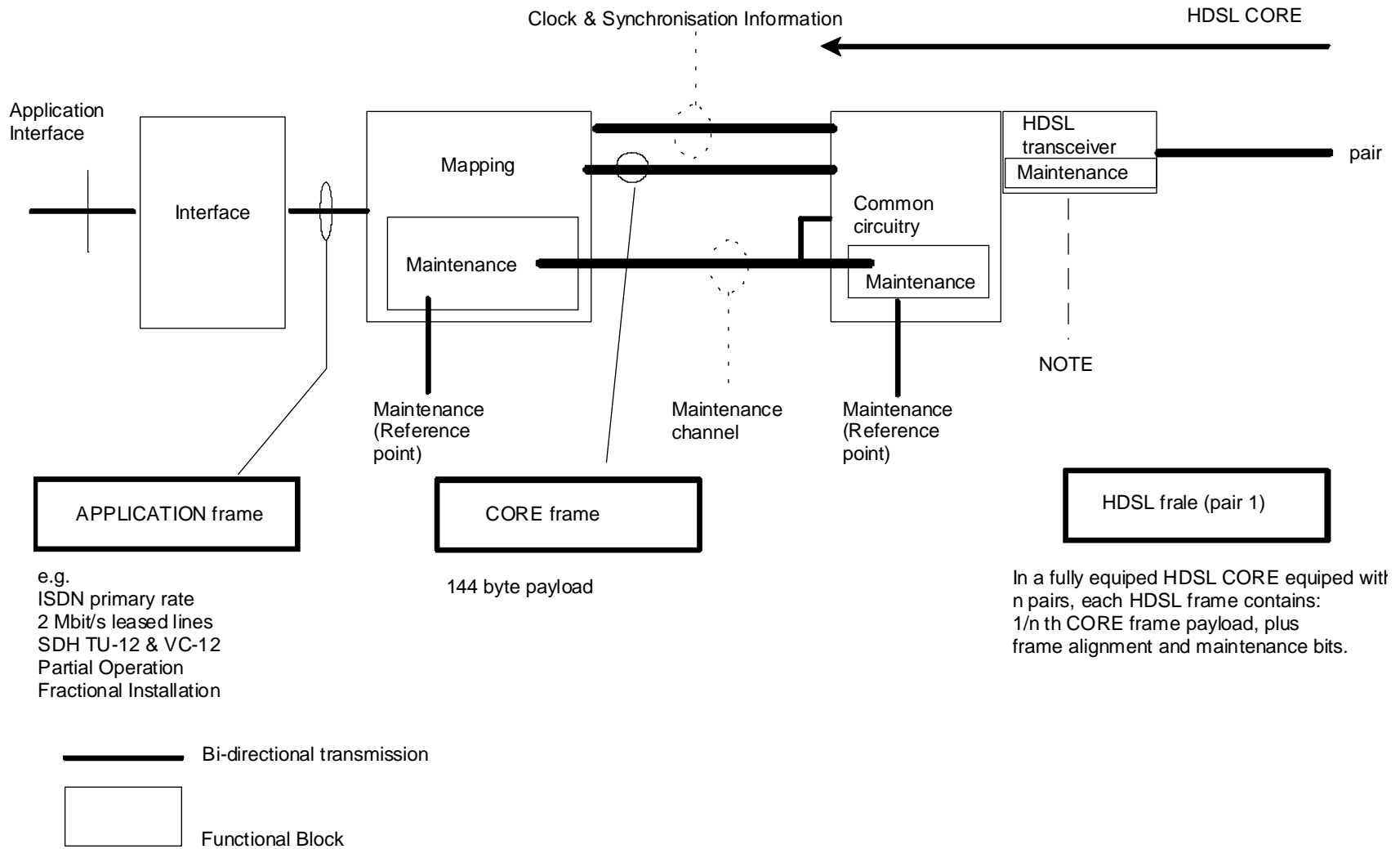
At the application interface (I), the data flow is grouped in application frames (e.g. 32 time slot ISDN primary rate frames, as specified in ETS 300 011 [2]).

The mapping function (part of the M functional block) then takes the application frame and inserts it into a 144 byte core frame. (In some applications not all data bytes will contain valid information and may be set to idle patterns.)

The core frame is then given to the common circuitry (C) where it is combined with any necessary alignment bits, maintenance bits and overhead bits, in order to be sent transparently in HDSL frames over the DLLs. The use of REGs is optional.

At the receiving side, data within the HDSL frames is multiplexed by the common circuitry to again form the core frame which is passed to the mapping function where it is mapped into the application frame and transmitted over the application interface (I).

An overview of the different framing procedures can be found in figure 3.



NOTE: A fully equipped HDSL CORE consists of two or three H, REG, DLL combinations depending on HDSL transceiver data transmission rate. REGs are optional.

Figure 3: An overview of framing procedures

In addition, there may be maintenance and/or power feeding functions associated with the HDSL core for the support of failure identification, localisation and HDSL start-up control, however, the presentation of this information at the maintenance reference point is outside the scope of this ETR.

The specification of the HDSL core is aimed at interoperability of two equipments from different vendors.

5 HDSL core specification

5.1 Functions

The functions listed below are necessary for the correct operation of the HDSL core.

Functions related to the HDSL core	LTU	NTU/ REG
Transparent transport of core frames (144 bytes)	↔	
Stuffing and destuffing	↔	
CRC-6 procedures and transmission error detection	↔	
Error reporting	↔	
Failure detection	↔	
Failure reporting	↔	
Bit timing	↔	
Frame alignment	↔	
HDSL transceiver autonomous start-up control	→	
Loopback control and co-ordination	→	
Mapping of core frames into HDSL frames	↔	
Control of maintenance channel	↔	
Synchronisation and co-ordination of HDSL transceivers	→	
Identification of pairs	↔	
Correction of pair identification		(note)

NOTE: Correction of pairs is a function of the NTU.

Functions related to power feeding	LTU	NTU/ REG
Remote power feeding (optional)	→	
Wetting current (optional)	→	

5.1.1 Transparent transport of core frames

This function provides for the bi-directional transmission of the core frames with 144 bytes over two or three parallel HDSL transceiver systems connected by separate pairs.

5.1.2 Stuffing and destuffing

This function provides for the synchronization of the application data clock to the HDSL transceiver system clock, by means of adding zero or two stuffing quats per HDSL frame.

5.1.3 CRC-6 procedures and transmission error detection

This function provides per HDSL frame for error performance monitoring of the HDSL transceiver systems.

5.1.4 Error reporting

This function provides for the reporting of errors detected by means of CRC-6 procedure.

5.1.5 Failure detection

This function provides for the detection of failures in the HDSL transceiver system.

5.1.6 Failure reporting

This function provides for the reporting of failures detected in the HDSL transceiver systems by means of messages in the maintenance channel realized, i.e. by HDSL frame overhead bits.

5.1.7 Bit timing

This function provides bit (signal element) timing to enable the HDSL transceiver systems to recover information from the aggregate bit stream.

5.1.8 Frame alignment

This function provides information to enable the HDSL transceiver systems to recover the HDSL frame and the HDSL frame overhead.

5.1.9 HDSL transceiver autonomous start-up control

This function provides for the recovering of the operational state after first powering or break down of the HDSL transceiver systems.

5.1.10 Loopback control and co-ordination

This function provides for the activation and release of loopbacks in the LTU, the REG and the NTU.

5.1.11 Mapping between core frames and HDSL frames

This function provides for the mapping between the 144 bytes core frame and the HDSL frame(s).

5.1.12 Control of the maintenance channel

This function provides for the control of the maintenance channel formed by the HDSL frame overhead bits.

5.1.13 Synchronisation and co-ordination of HDSL transceivers

This function provides for the synchronization of the HDSL transceiver systems, the equalization of different signal delays on the pairs and the correct sequence of the signals coming from the separate pairs.

5.1.14 Identification of pairs

This function provides for the marking of the pairs at the LTU/NTU by means of two or three Z bits per pair to enable the correct identification of the pairs.

5.1.15 Correction of pair identification

This function provides for the realignment of the identification of pairs if an unintentional interchange of pairs has occurred and was detected by the NTU.

5.1.16 Remote power feeding

This optional function provides for remote power feeding of either the NTU if no REG is provided- or the REG from the LTU via the pairs.

5.1.17 Wetting current

This optional function provides for feeding of a low current on the pairs to prevent corrosion of contacts.

5.2 Transmission medium

5.2.1 Description

The transmission medium over which the digital transmission system is expected to operate is the local line distribution network.

A local line distribution network employs cables of pairs to provide services to customers.

In a local line distribution network, customers are connected to the local exchange via local lines.

A metallic local line is able to simultaneously carry bi-directional digital information in the appropriate HDSL format.

To simplify the provision of HDSL, a digital transmission system needs to be capable of satisfactory operation over the majority of metallic local lines without requirement of any special conditioning. In order to permit the use of HDSL transmission systems on the maximum possible number of local lines, the restrictions imposed by HDSL requirements are kept to the minimum necessary to guarantee acceptable operation.

5.2.2 Minimum digital local line (DLL) requirements for HDSL applications

- No loading coils.
- Only twisted pair or quad cable.
- No additional shielding necessary.
- When bridged taps are present, the maximum number shall be limited to 2 and each length to 500 m.

5.2.3 DLL physical characteristics

A DLL is constructed of one or more cable sections that are spliced or interconnected together.

The distribution or main cable is structured as follows:

- cascade of cable sections of different diameters and lengths;
- up to two Bridged Taps (BTs) may exist at various points in installation and distribution cables.

A general description of the DLL physical model is shown in figure 4 and typical examples of cable characteristics based on ETR 080 [1] are given in table 1.

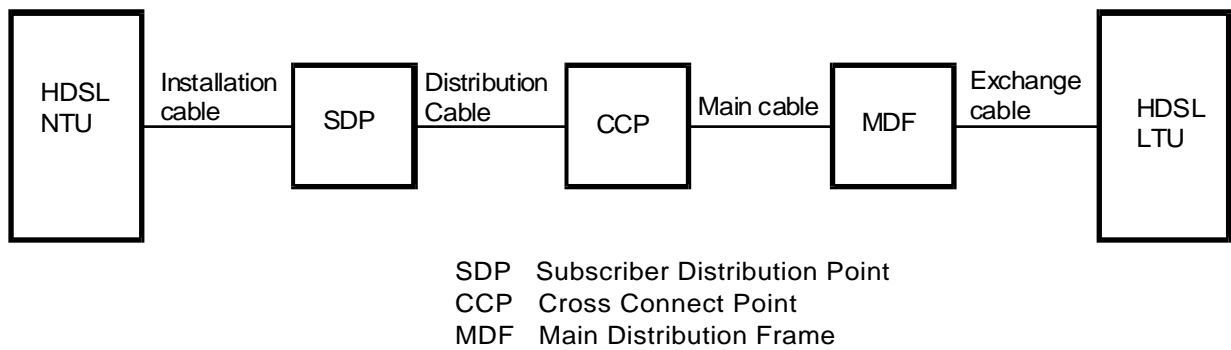


Figure 4: DLL physical model

Table 1: Cable characteristics

	Exchange cable	Main cable	Distribution cable	Installation cable
Wire diameter (mm)	0,5, 0,6, 0,32, 0,4	0,3 - 1,4	0,3 - 1,4	0,4, 0,5, 0,6, 0,8, 0,9, 0,63
Structure	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ (B) or TP (L)	SQ or TP or UP
Maximum number of pairs	1 200	2 400 (0,4 mm) 4 800 (0,32 mm)	600 (0,4 mm)	2 (aerial) 600 (in house)
Installation		underground in ducts	underground or aerial	aerial (drop) in ducts (in house)
Capacitance (nF/km at 800 Hz)	55 ... 120	25 ... 60	25 ... 60	35 ... 120
Wire insulation	PVC, FRPE	PE, paper pulp	paper, PE, Cell PE	PE, PVC
TP:	Twisted Pairs	PE:	Polyethylene	
SQ:	Star Quads	PVC:	Polyvinylchloride	
UP:	Untwisted Pairs	Pulp:	Pulp of paper	
L:	Layer Cell	PE:	Cellular Foam Polyethylene	
B:	Bundles (units)	FRPE:	Fire Resistant PE	
NOTE:	This table is intended to describe the cables presently installed in the local loop. Not all of the above cable types are suitable for HDSL systems.			

5.2.4 DLL electrical characteristics

The transmitted signal will suffer from impairments due to crosstalk, impulsive noise and the non-linear variation with frequency of DLL characteristics. These impairments are described in more detail in the following subclauses.

5.2.4.1 Principal characteristics

The principal electrical characteristics varying nonlinearly with frequency are:

- insertion loss;
- group delay;
- characteristic impedance, comprising real and imaginary parts.

The maximum value for insertion loss specified for HDSL transmission systems is defined in clause 7, for both two and three pairs systems.

NOTE: The term group delay is defined in the CCITT Blue Book - Fascicle I.3 [15].

5.2.4.2 Differences in physical transmission characteristics between pairs in the DLL

Between the LTU and NTU the characteristics of the pairs may differ. This difference may be in wire diameter, insulation type, length, number and length of bridged taps and exposure to impairments. These differences in transmission characteristics may change with time.

The common circuitry shall compensate for any differences in the transmission time due to these pair differences, (see clause 6).

It is recommended that the difference of total signal delay between each of the two or three pairs is limited to a maximum of $D2 = 50 \mu\text{s}$ at 150 kHz, corresponding to about $(D2/5 \mu\text{s})$ km difference in line length between LTU and NTU.

5.2.4.3 Crosstalk characteristics

Crosstalk noise in general results due to finite coupling loss between pairs sharing the same cable, especially those pairs that are physically adjacent. Finite coupling loss between pairs causes a vestige of the signal flowing on one DLL (disturber DLL) to be coupled into a adjacent DLL (disturbed DLL). This vestige is known as crosstalk noise.

Near End CrossTalk (NEXT) is assumed to be the dominant type of crosstalk.

Intersystem NEXT results when pairs carrying different digital transmission systems interfere with each other.

Intrasystem NEXT or self-NEXT results when all pairs interfering with each other in a cable are carrying the same digital transmission system. Intrasystem NEXT noise coupled into a disturbed DLL from a number of DLL disturbers can be represented as being due to an equivalent single disturber DLL with a coupling loss versus frequency characteristics known as Power Sum Loss. Values for 1 % NEXT loss vary from 40 dB to 70 dB at 150 kHz depending upon the cable type, number of disturbers and environment.

For testing HDSL systems the NEXT is represented by an artificial noise as defined in clause 7.

5.2.4.4 Unbalance about earth

The DLL will have finite balance about earth. Unbalance about earth is described in terms of Longitudinal Conversion Loss (LCL). The expected worst case value is 42,5 dB at 150 kHz decreasing with frequency by 5 dB/decade.

5.2.4.5 Impulse noise

The DLL will have impulse noise resulting from other systems sharing the same cables as well as from other sources. The requirement for tolerance to impulsive noise is described in detail in clause 7.

5.2.4.6 Micro interruptions

A micro interruption is a temporary line interruption due to external mechanical action on the copper wires constituting the transmission path, for example, at a cable splice. Splices can be hand-made wire-to-wire junctions, and during cable life oxidation phenomena and mechanical vibrations can induce micro interruptions at these critical points.

The effect of a micro interruption on the transmission system can be a failure of the digital transmission link, together with a failure of the power feeding (if provided) for the duration of the micro interruption.

The objective is that in the presence of a micro interruption of specified maximum length the system should not reset, and the system should automatically reactivate with a complete start-up procedure if a reset occurs due to a longer micro interruption. The requirements for tolerance to micro interruptions, together with guidelines for a laboratory susceptibility test set are given in clause 7.

5.3 Transmission method

5.3.1 General

The transmission system provides for duplex transmission on 2-wire metallic local lines. Duplex transmission shall be achieved through the use of an Echo Cancellation Hybrid (ECH). With the echo cancellation method, illustrated in figure 5, the Echo Canceller (EC) produces a replica of the echo of the transmitted signal that is subtracted from the total received signal. The echo is the result of imperfect balance of the hybrid and impedance discontinuities, caused e.g. by splicing different kind of cables.

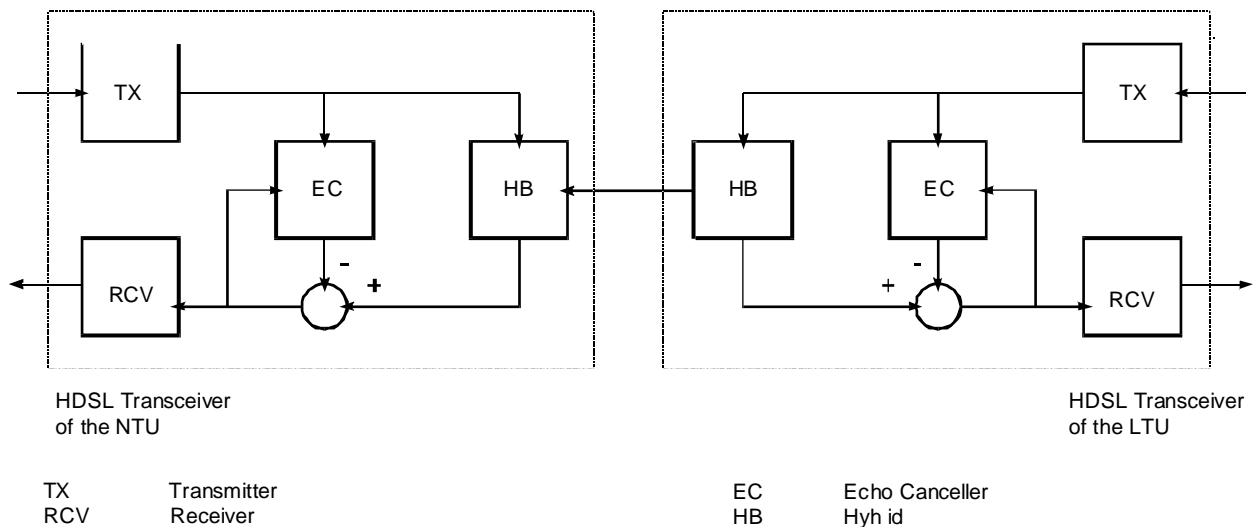


Figure 5: Functional diagram of echo cancellation method

5.3.2 Transmission on three pairs

Transmission on three DLLs is provided by three parallel HDSL transceivers, each operating at 784 kbit/s and using 2B1Q line code.

5.3.3 Transmission on two pairs

Transmission on two DLLs is provided by two parallel HDSL transceivers, each operating at 1 168 kbit/s and using 2B1Q line code.

5.3.4 Transmission on one or four pairs

The transmission of the complete core frame on one or four pairs is not excluded, but is not at present treated here.

5.3.5 Line code

The line code shall be 2B1Q (two binary, one quaternary).

Before transmission the bit stream in each HDSL transceiver of figure 1, except the synchronization word which has a fixed pattern, shall be grouped into pairs of bits which are converted to quaternary symbols (quats) as specified in table 2.

Table 2: 2B1Q coding

First bit (sign)	Second bit (Magnitude)	Quaternary Symbol
1	0	+ 3
1	1	+ 1
0	1	- 1
0	0	- 3

At the receiver, each quaternary symbol is converted to a pair of bits reversing table 2.

5.3.6 Line baud rate

The baud rate of the HDSL transceiver shall be:

- 392 kbaud \pm 32 ppm for a three pairs system; and
- 584 kbaud \pm 32 ppm for a two pairs system.

5.4 Frame structure

5.4.1 Core frame

Inside the mapping functional block, as indicated in the reference configuration figure 3, the application dependant frame containing the payload is inserted into a 500 μ s long core frame containing 144 bytes as shown in figure 6 a). Different mapping options depending on the special applications exist, as shown in figures 6 b) to 6 d). The details of the mapping procedures for the different applications are described in clause 7. The core frames with 144 bytes/500 μ s form a continuous bit stream with a bit rate of 2 304 kbit/s which are split on a byte per byte basis into parallel HDSL frames which are transmitted in each one of the HDSL transceiver systems.

5.4.2 2B1Q HDSL frame

This subclause describes the proposed HDSL frame structure in the binary format before scrambling and encoding. This structure is valid during normal operation after symbol timing synchronization, frame alignment and after all internal transceiver coefficients have been stabilized sufficiently to permit a reliable transport of the signals through the HDSL transceiver systems.

- The nominal HDSL frame length is 6 ms.
- The mean length of the HDSL frame for the three pairs system is 2 352 quats (equivalent to 4 704 bits) in 6 ms. Each individual frame contains either 0 or 2 stuffing quats which gives a real length of 2 351 quats in 6 - 1/392 ms or 2 353 quats in 6 + 1/392 ms.
- The mean length of the HDSL frame for the two pairs system is 3 504 quats (equivalent to 7 008 bits) in 6 ms. Each individual frame contains either 0 or 2 stuffing quats which gives a real length of 3 503 quats in 6 - 1/584 ms or 3 505 quats in 6 + 1/584 ms.
- The bit assignment in each HDSL frame in each direction of transmission for all pairs is shown in tables 3 and 4.
- The HDSL transceiver systems shall each independently accommodate differences in the bit timing of the two directions of transmission or of the application data and the HDSL transceiver system by including none or two stuffing quats at the end of the HDSL frame.

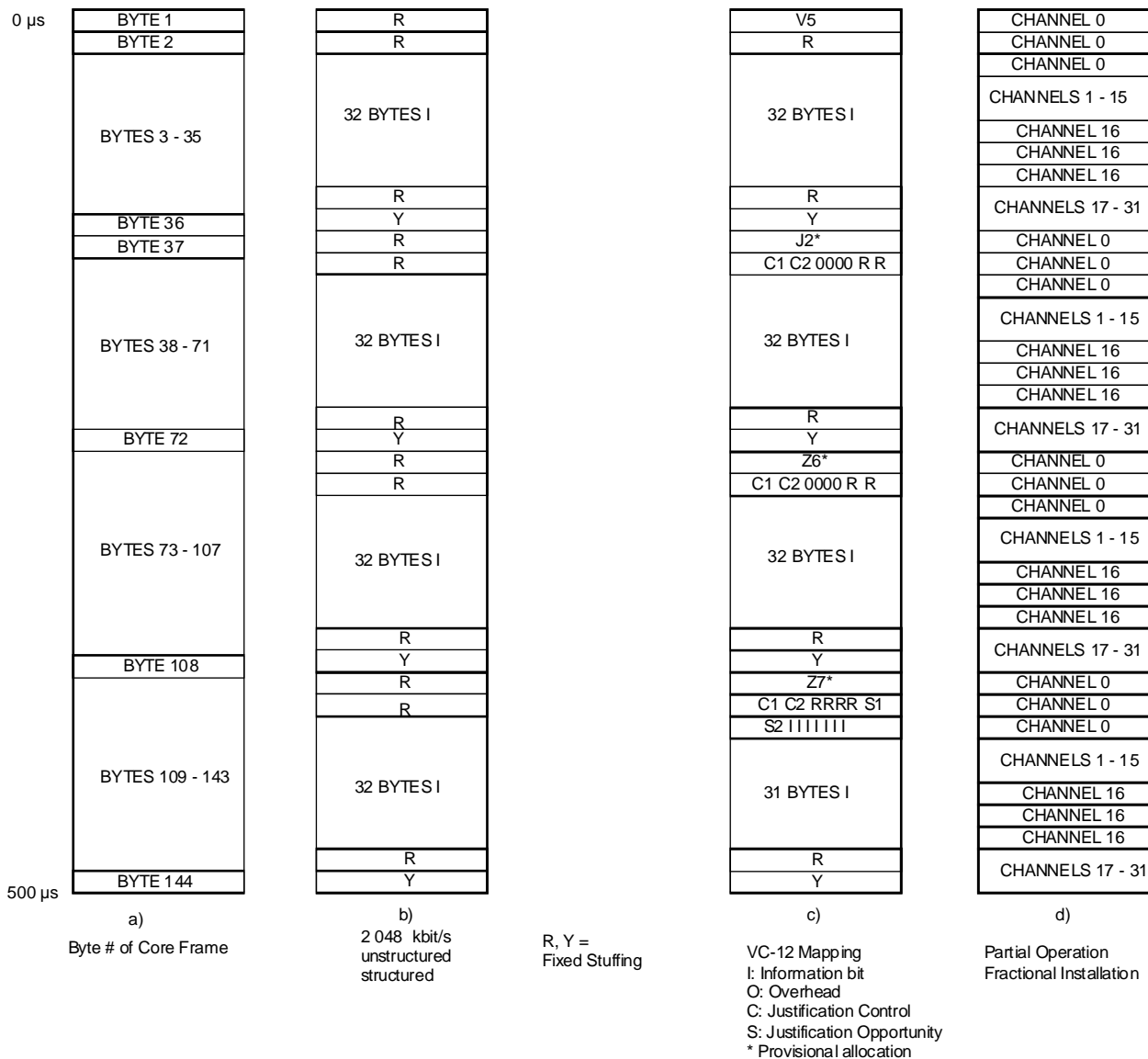


Figure 6: Core frame mapping options

Table 3: HDSL frame structure for the three pairs system

Time	Frame Bit #	HOH Bit#	Abrv. Name	Full Name	Notes
0 ms	1 - 14	1 - 14	SW 1 - 14	Synch word	Double Barker Code
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17-1180	————	B01 - B12	Payload block 1-12	HDSL payload including Z _{m1} -Z _{m12}
	1 181	17	eoc01	eoc address	
	1 182	18	eoc02	eoc address	
	1 183	19	eoc03	eoc data/opcode	
	1 184	20	eoc04	eoc odd/even byte	
	1 185	21	crc 1	cyclic redundancy check	CRC-6
	1 186	22	crc 2	cyclic redundancy check	CRC-6
	1 187	23	ps1	NTU power status bit 1	NTU → LTU only
	1 188	24	ps2	NTU power status bit 2	NTU → LTU only
	1 189	25	bpv	bipolar violation	
	1 190	26	eoc05	eoc unspecified	
	1 191 - 2 354	————	B13-B24	Payload blocks 13 - 24	HDSL payload including Z _{m13} -Z _{m24}
	2 355	27	eoc06	eoc message bit 1	
	2 356	28	eoc07	eoc message bit 2	
	2 357	29	eoc08	eoc message bit 3	
	2 358	30	eoc09	eoc message bit 4	
	2 359	31	crc3	cyclic redundancy check	CRC-6
	2 360	32	crc4	cyclic redundancy check	CRC-6
	2 361	33	hrp	regenerator present	LTU ← REG → NTU
	2 362	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	2 363	35	rcbe	regenerator central block error	LTU ← REG → NTU
	2 364	36	rega	regenerator alarm	LTU ← REG → NTU
	2 365 - 3 528	————	B25-B36	Payload blocks 25-36	HDSL payload including Z _{m25} -Z _{m36}

(continued)

Table 3 (concluded): HDSL frame structure for the three pairs system

Time	Frame Bit #	HOH Bit#	Abrv. Name	Full Name	Notes
	3 529	37	eoc10	eoc message bit 5	
	3 530	38	eoc11	eoc message bit 6	
	3 531	39	eoc12	eoc message bit 7	
	3 532	40	eoc13	eoc message bit 8	
	3 533	41	crc5	cyclic redundancy check	CRC-6
	3 534	42	crc6	cyclic redundancy check	CRC-6
	3 535	43	rta	remote terminal alarm	NTU →LTU only
	3 536	44	indc/indr	ready to receive	indc=LTU/REG-C→NTU indr=NTU/REG-R→LTU
	3 537	45	uib	unspecified indicator bit	
	3 538	46	uib	unspecified indicator bit	
6 - 1/392 ms	3 539 - 4 702	————	B37-B48	Payload blocks 37-48	HDSL Payload including Z _m 37 - Z _m 48
	4 703	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	4 704	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	4 705	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/392 ms	4 706	50	stq2m	stuff quat 2 magnitude	Frame stuffing

Table 4: HDSL frame structure for the two pairs system

Time	Frame Bit #	HOH Bit#	Abrv. Name	Full Name	Notes
0 ms	1 - 14	1 - 14	SW 1-14	Synch word	Double Barker Code
	15	15	losd	loss of input signal at the far end application interface	
	16	16	febe	far end block error	
	17 - 1756	————	B01-B12	Payload block 1-12	HDSL payload including Z _{m1} -Z _{m12}
	1 757	17	eoc01	eoc address	
	1 758	18	eoc02	eoc address	
	1 759	19	eoc03	eoc data/opcode	
	1 760	20	eoc04	eoc odd/even byte	
	1 761	21	crc 1	cyclic redundancy check	CRC-6
	1 762	22	crc 2	cyclic redundancy check	CRC-6
	1 763	23	ps1	NTU power status bit 1	NTU → LTU only
	1 764	24	ps2	NTU power status bit 2	NTU → LTU only
	1 765	25	bpv	bipolar violation	
	1 766	26	eoc05	eoc unspecified	
	1 767-3 506	————	B13-B24	Payload blocks 13-24	HDSL payload including Z _{m13} -Z _{m24}
	3 507	27	eoc06	eoc message bit 1	
	3 508	28	eoc07	eoc message bit 2	
	3 509	29	eoc08	eoc message bit 3	
	3 510	30	eoc09	eoc message bit 4	
	3 511	31	crc3	cyclic redundancy check	CRC-6
	3 512	32	crc4	cyclic redundancy check	CRC-6
	3 513	33	hrp	regenerator present	LTU ← REG → NTU
	3 514	34	rrbe	regenerator remote block error	LTU ← REG → NTU
	3 515	35	rcbe	regenerator central block error	LTU ← REG → NTU
	3 516	36	rega	regenerator alarm	LTU ← REG → NTU

(continued)

Table 4 (concluded): HDSL frame structure for the two pairs system

Time	Frame Bit #	HOH Bit#	Abrv. Name	Full Name	Notes
	3 517-5 256	————	B25-B36	Payload blocks 25 - 36	HDSL payload including Z _{m25} -Z _{m36}
	5 257	37	eoc10	eoc message bit 5	
	5 258	38	eoc11	eoc message bit 6	
	5 259	39	eoc12	eoc message bit 7	
	5 260	40	eoc13	eoc message bit 8	
	5 261	41	crc5	cyclic redundancy check	CRC-6
	5 262	42	crc6	cyclic redundancy check	CRC-6
	5 263	43	rta	remote terminal alarm	NTU → LTU only
	5 264	44	indc/indr	ready to receive	indc=LTU/REG-C → NTU indr=NTU/REG-R → LTU
	5 265	45	uib	unspecified indicator bit	
	5 266	46	uib	unspecified indicator bit	
6 - 1/584 ms	5 267-7 006	————	B37-B48	Payload blocks 37 - 48	HDSL payload including Z _{m37} - Z _{m48}
	7 007	47	stq1s	stuff quat 1 sign	Frame stuffing
6 ms nominal	7 008	48	stq1m	stuff quat 1 magnitude	Frame stuffing
	7 009	49	stq2s	stuff quat 2 sign	Frame stuffing
6 + 1/584 ms	7 010	50	stq2m	stuff quat 2 magnitude	Frame stuffing

- In the LTU the clock rate of the different HDSL frames shall be derived from the same source. The location of the synchronisation word, i.e. the start of the HDSL frames in the different pairs shall be synchronised to each other. The maximum delay between the start of the frames shall be less than one symbol period, measured at the line side of each HDSL transceiver.
- The insertion of stuffing quats, if necessary shall be identical for all pairs.

5.4.2.1 2B1Q HDSL frame structure

5.4.2.1.1 Frame structure on the three pairs system

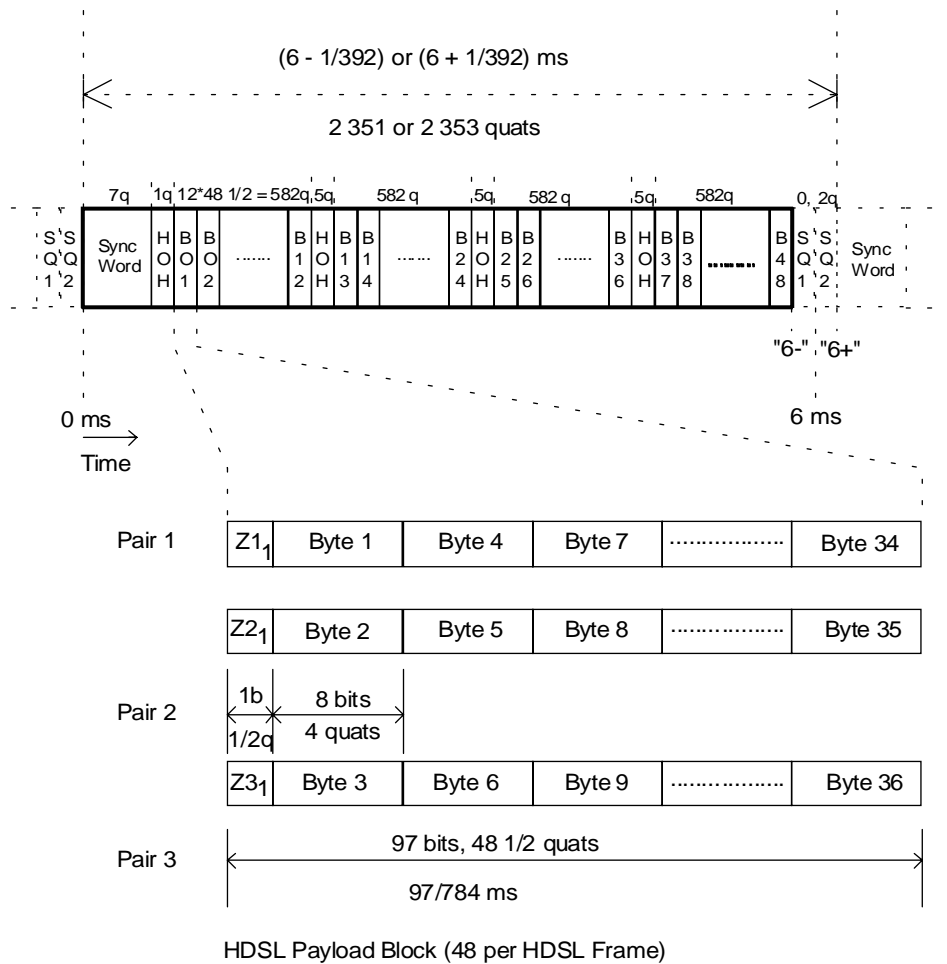
Figure 7 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and twelve blocks of HDSL payload, each consisting of 48,5 quats, equivalent to 97 bits, containing one overhead-bit Z_{mn} and twelve bytes of the core frame. The Z_{mn}-bits (m = 1..3 indicates one of the three pairs; n = 1..48 is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which forty eight bits per frame of each HDSL transceiver system at a capacity of 8 kbit/s are available.

The first eight Z-bits (Z_{m1}...Z_{m8}) are reserved for core applications. Bits Z_{m1}...Z_{m3} are used for pair identification (see subclause 5.6.7), whereas Z_{m4}...Z_{m8} are reserved for future use and are presently set to ONE.

The Z-bits no. 9...48 (Z_{m9}...Z_{m48}) are application dependant and are transparently transported through the HDSL core. The use of these bits is described in clause 7 for the application specific requirements.

The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and twelve HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 Z-bits and 576 bytes of the core frame.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together, this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 2 353 quats, which equals $6 + 1/392$ ms for the nominal HDSL clock frequency, or 2 351 quats corresponding to $6 - 1/392$ ms and the average will tend to 2 352 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the synch word in the following frame and to adjust the demultiplexing of the data stream.



SYMBOL

NAME, FUNCTION

SYMBOL	NAME, FUNCTION
B01 to B48	HDSL system payload blocks
Byte n	Byte n from core frame
(n = 1...144)	
HOH	HDSL overhead (sw, eoc, crc, etc.)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Synch Word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/392 ms, 6+1/392 ms
Zm _n	Additional overhead bits (Z-bits)
(n = 1... 48)	Indicating number of payload block
(m = 1... 3)	Indicating corresponding pair

Figure 7: Frame structure on the three pairs system

5.4.2.1.2 Frame structure on the two pairs system

Figure 8 illustrates the HDSL frame structure composed of quaternary symbols (quats) and the mapping of the core frame bytes to it. The frame is subdivided into four groups. The first group of the frame starts with the seven symbols long synchronization word followed by one HDSL overhead quat and twelve blocks of HDSL payload, each consisting of 72,5 quats, equivalent to 145 bits, containing one overhead-bit Z_{mn} and eighteen bytes of the core frame. The Z_{mn} -bits ($m = 1,2$ indicates one of the two pairs; $n = 1..48$ is the running number of the HDSL payload block in the frame) provide an additional overhead channel, for which 48 bits per frame of each HDSL transceiver system at a capacity of 8 kbit/s are available.

The first eight Z-bits ($Z_{m1}...Z_{m8}$) are reserved for core applications. Bits Z_{m1} , Z_{m2} are used for pair identification (see subclause 5.6.7), whereas $Z_{m3}...Z_{m8}$ are reserved for future use and are presently set to ONE.

The Z-bits no. 9...48 ($Z_{m9}...Z_{m48}$) are application dependent and are transparently transported through the HDSL core. The use of these bits is described in clause 7 for the application specific requirements.

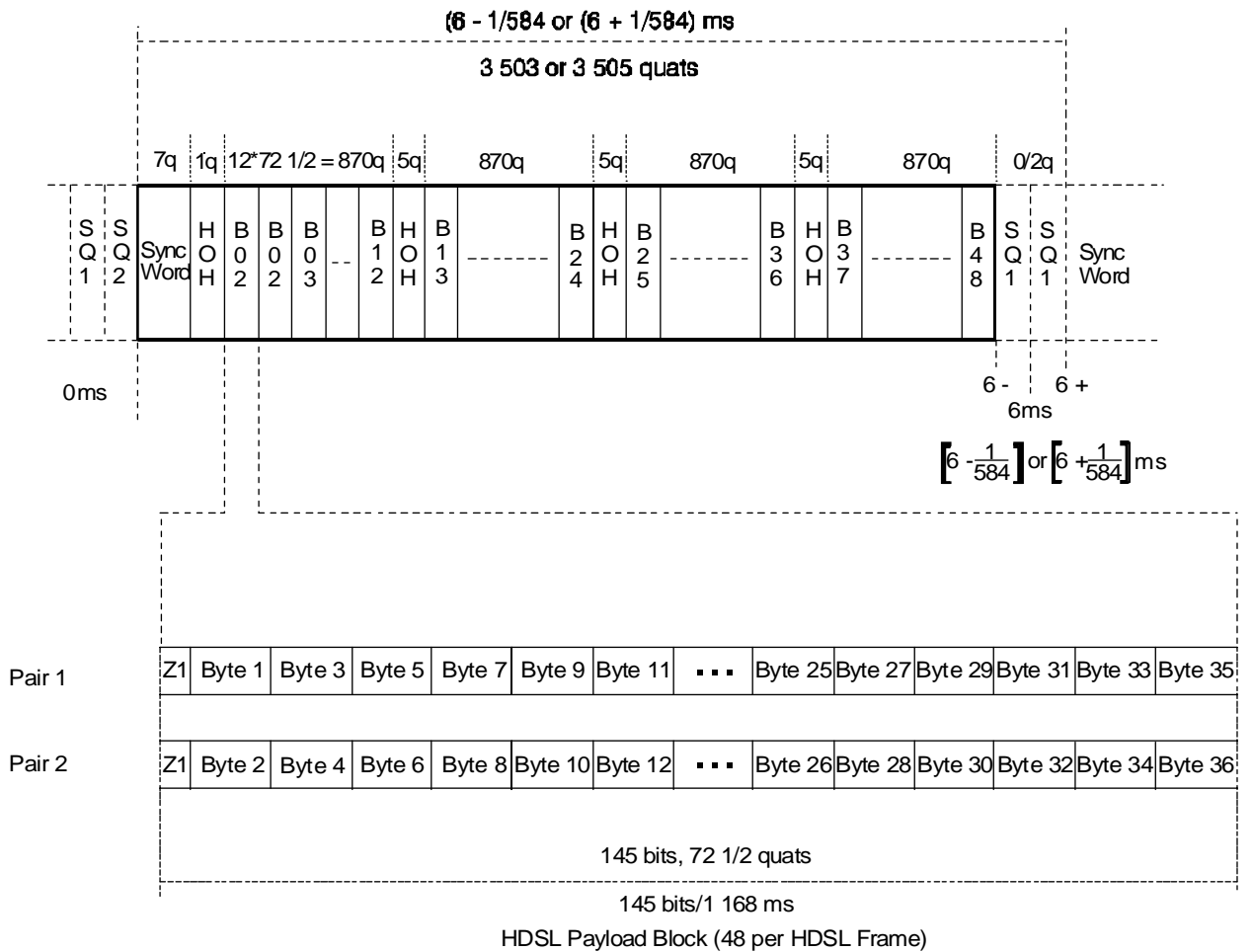
The three groups following the first group have an equal structure. Each consists of five HDSL overhead quats and twelve HDSL payload blocks as described above. So one frame contains a synchronization word, 16 HDSL overhead quats, 48 Z-bits and 864 bytes of the core frame.

At the end of the frame the possibility of 2 stuffing quats is foreseen. These quats are used always together, this means either none or two stuffing quats are inserted, depending on the relation of the timing. The length of the HDSL frame is either 3 505 quats, which equals $6 + 1/584$ ms for the nominal HDSL clock frequency, or 3 503 quats corresponding to $6 - 1/584$ ms and the average will tend to 3 504 quats or 6 ms. The receiver is able to evaluate the length of an incoming frame by detection of the synch word in the following frame and to adjust the demultiplexing of the data stream.

5.4.2.2 Frame bit assignments

In tables 3 and 4 the bit sequence of the HDSL frame prior to scrambling at the transmit and after descrambling at the receive side is presented. While the frame structures are identical in both directions of transmission, the functional assignments of individual bits in the direction LTU-to-NTU or NTU-to-LTU are different. Unused bits in either direction are set to ONE. For example the proposed NTU power status bits are defined only in the frame transmitted towards the LTU and the corresponding bit positions in the reverse direction have no assignment. The bit assignments are identical in each of the pairs.

The following gives a short description of the currently defined overhead bits.



SYMBOL

NAME, FUNCTION

SYMBOL	NAME, FUNCTION
B01 to B48	HDSL system payload blocks
Byte n	Byte n from core frame
(n = 1...144)	
HOH	HDSL overhead (sw, eoc, crc,...)
quat	Quaternary symbol
SQ1, SQ2	Stuff quats
Synch Word	7-symbol Barker codes, "double Barker" → 14 bits
"6-", "6+"	6 - 1/584 ms, 6+1/584 ms
Zm _n	Additional overhead bits (Z-bits)
(n = 1... 48)	Indicating number of payload block
(m = 1... 2)	Indicating corresponding pair

Figure 8: Frame structure on the two pairs system

- *Synch word:*

The synchronization words (Synch words) enable the HDSL receivers to acquire quat and bit timing so that the incoming signals can be decoded into their original binary forms. The synchronisation words shall be seven-quat Barker code sequences as shown in table 5. The same patterns are used in both directions on all pairs.

Table 5: Seven-quat Barker code synchronization word patterns

Quat #	pattern
01	+ 3
02	+ 3
03	+ 3
04	- 3
05	- 3
06	+ 3
07	- 3

The coding in table 5 will preserve the 2,64 V peak symbol levels for the synch words on the line with the double assignment of the Barker code bits to the quats. Only the HDSL deframer utilizes this special quaternary-to-binary coding. All other quats use the normal 2B1Q coding as described in subclause 5.3.5.

The same binary value shall be assigned to both the sign and magnitude bits of quat numbers 1 through 7 of the HDSL frame. In other words, each number of the pairs sw_{1s} and sw_{1m} through sw_{7s} and sw_{7m} , shall have the same binary value (ONE or ZERO) as its mate. This double assignment of the code word binary values is referred to as a "Double Barker Code".

The quaternary-to-binary conversion used to generate the bit stream that is examined for purposes of finding HDSL frame synchronization shall use the decoding as shown in table 6.

- *losd-bit (loss of signal)*

If there is no signal from the application interface, the losd-bit shall be set to ZERO in the next frame towards the far end. Under normal conditions, this bit shall be set to ONE.

- *febe-bit (far end block error)*

The febe-bit shall be set to ZERO in the following frame towards the far end, when the local receiver detects a crc error in the HDSL frame. When there is no febe bit value ready (due to different frame lengths in the two directions) or no failure has been detected in the previous frame, the febe bit shall be set to ONE.

Table 6: Quaternary-to-binary decoding used by HDSL de-framer

Quat Symbol	First bit (Sign)	Second bit (Magnitude)	Notes
+ 3	1	1	valid synch word quat
+ 1	-	-	not used for synch
- 1	-	-	not used for synch
- 3	0	0	valid synch word quat
NOTE: This decoding scheme is different to the scheme given in table 2.			

- *eoc-bits (embedded operations channel)*

13 bits (eoc 01...eoc13) are provided as a separate maintenance channel. For a description of codes and the used procedures in this channel see subclause 5.5.

- *crc-bits*

The HDSL frame shall have six bits assigned to a Cyclic Redundancy Check (CRC) code on both directions for each pair.

The CRC code block is calculated for the previous HDSL frame in the given direction except for the fourteen sync word bits, the six crc-bits and any stuff quat bits.

The six crc-bits transmitted in the (N+1)th frame shall be determined as follows:

- 1) All bits of the N-th frame except the fourteen sync word bits, the six crc-bits and any stuffing bits, for a total of m bits (m equals to 4682 for the three pair system and 6986 for the two pair system), are used, in order of occurrence, to construct a polynomial in "X" such that the bit "0" of the (N)-th frame is the coefficient of the term X^{m-1} and bit m-1 of the (N)th frame is the coefficient of the term X^0 .
- 2) The polynomial is multiplied by the factor X^6 , and the result is divided, modulo 2, by the generator polynomial $X^6 \oplus x \oplus 1$. The coefficients of the remainder polynomial are used, in order of occurrence, as the ordered set of check bits, crc_1 through crc_6 , for the (N+1)-th frame. The ordering is such that the coefficient of the term X^5 in the remainder polynomial is check bit crc_1 and the coefficient of the term X^0 in the remainder polynomial is check bit crc_6 .
- 3) The check bits, crc_1 through crc_6 , contained in a frame are those associated with the content of the preceding frame. When there is no immediately preceding frame, the check bits may be assigned any value.

- *ps1-, ps2-bit (power supply bits)*

The power supply bits ps1 and ps2 are used to indicate the status of the primary and secondary power supply in the NTU. The power status bit function definitions are shown in table 7.

Table 7: Coding of power status

NTU power status	ps1, ps2	
All power normal	1	1
Secondary power out	1	0
Primary power out	0	1
Power Loss	0	0

On loss of power at the NTU, there shall be enough power left to communicate three "Power Loss" messages towards the LTU.

- *bpv-bit (bipolar violation)*

Whenever during one HDSL frame period, a line coding violation is detected at the application interface, the bpv-bit is set to ZERO in the following frame towards the far end. Under normal conditions, this bit shall be set to ONE.

- *hrp-bit (HDSL regenerator present)*

If a regenerator is present, the hrp-bit shall be set to ZERO by the regenerator in both directions towards the NTU and the LTU. The NTU and the LTU set the hrp bit to ONE in the outgoing frames.

- *rrbe-bit (regenerator remote block error)*

The rrbe-bit shall be set to ZERO by the regenerator towards the LTU and NTU in the next outgoing frame, when a CRC error has been detected by the receiver located at the LTU-side in the regenerator. If no failure has been detected, this bit shall be set to ONE.

- *rcbe-bit (regenerator central block error)*

The rcbe-bit shall be set to ZERO by the regenerator towards the LTU and NTU in the next outgoing frame, when a CRC error has been detected by the receiver located at the NTU-side in the regenerator. If no failure has been detected, this bit shall be set to ONE.

- *rta-bit (remote terminal alarm)*

The rta-bit is set to ZERO by the NTU to signal internal alarm conditions to the LTU. The LTU, after detecting the rta-bit, may read the status register of the NTU and evaluate the reason for the failure condition. With no alarm pending in the NTU, the rta-bit is set to ONE.

- *rega-bit (internal alarm in the regenerator)*

The rega-bit is set by the REG to signal internal alarm conditions. The LTU, after detecting the rega-bit, may read the status register of the REG and evaluate the reason for the failure condition. With no alarm pending in the REG, the rega-bit is set to ONE.

- *uib-bits (unspecified indicator bits)*

These bits are reserved for future use. They shall be set to ONE.

- *stq (stuffing quats)*

(stq_{1m}, stq_{1s}, stq_{2m}, stq_{2s})

These quats are always used together. Either none or two stuffing quats are inserted, depending on the relation of the timing between the two transmit directions. The coding of the sync word (+3+3+3-3-3+3-3) results in an average +3 DC-offset per frame. Normally stuffing occurs every other frame allowing a DC-compensation of two sync words. Setting the two stuffing quats continuously to -3, would allow to balance the +6 DC-content of two transmitted HDSL-frames. Therefore, if used, the two stuffing quats shall be set to the quaternary symbols -3.

- *indc- and indr-bit (ready to receive indicator at the LTU, REG and NTU resp.)*

These bits are set to ZERO by the respective HDSL transceiver to indicate to the distant HDSL transceiver that it is ready to receive data, in all other conditions the indc-and indr-bit will be set to ONE.

NOTE: The indc- and indr-bit in the HDSL frame overhead is different and not to be confused with the indicator INDC and INDR used inside the HDSL transceivers during the start-up procedure.

5.4.3 Scrambling method

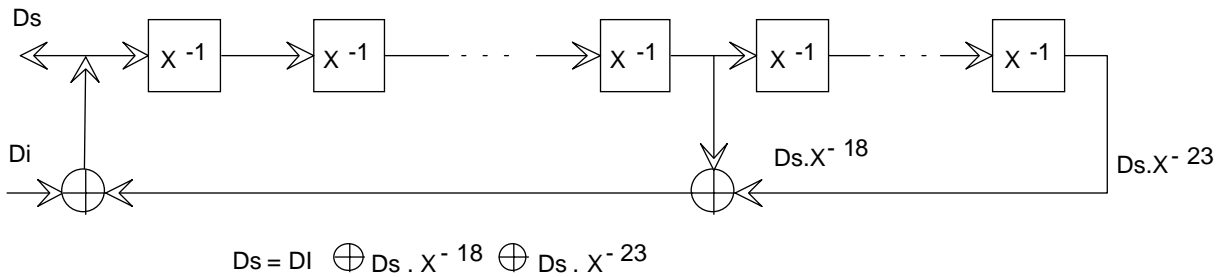
The HDSL transceiver systems use the same self synchronizing scrambling procedure as the 2B1Q transmission system for ISDN BA as defined in annex A of ETR 080 [1]. The data stream with exception of the 14 bits of the sync word and the stuffing bits is scrambled by means of a 23rd-order polynomial prior to encoding:

- for the direction NTU→LTU the polynomial shall be $x^{23} \oplus x^{18} \oplus 1$, where the sign \oplus stands for modulo 2 summation;
- for the direction LTU→NTU the polynomial shall be $x^{23} \oplus x^5 \oplus 1$;

- the binary data stream is recovered in the receiver by applying the same polynomial to the scrambled data. Figure 9 illustrates block diagrams for the scramblers and descramblers.

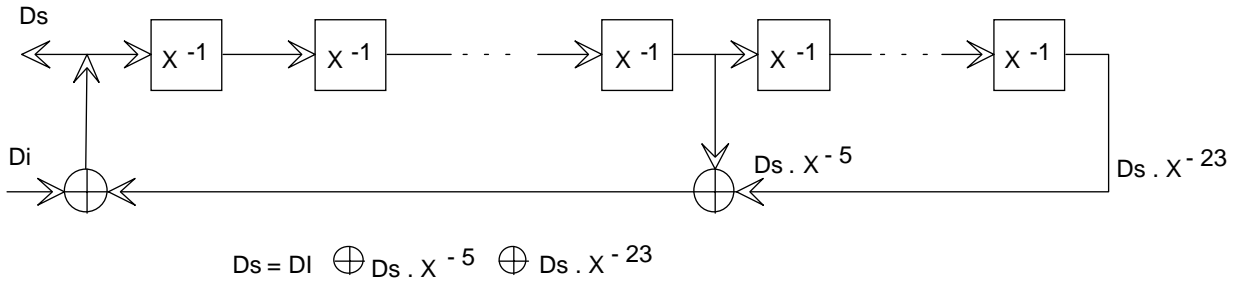
NTU (REG-R)

Transmit Scrambler (NTU to LTU)



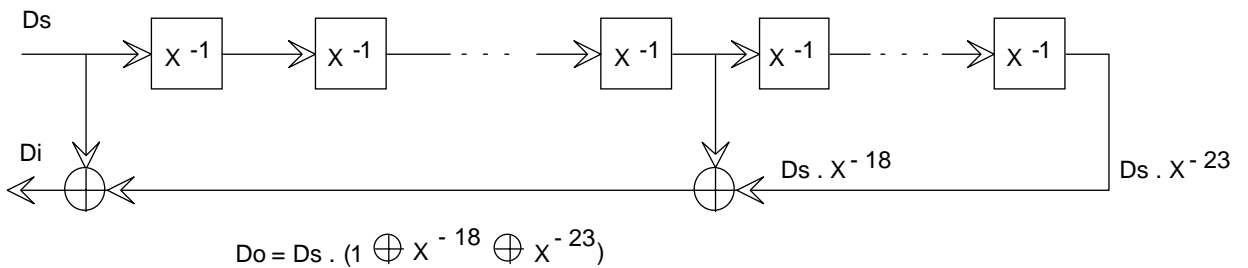
LTU (REG-C)

Transmit Scrambler (LTU to NTU)



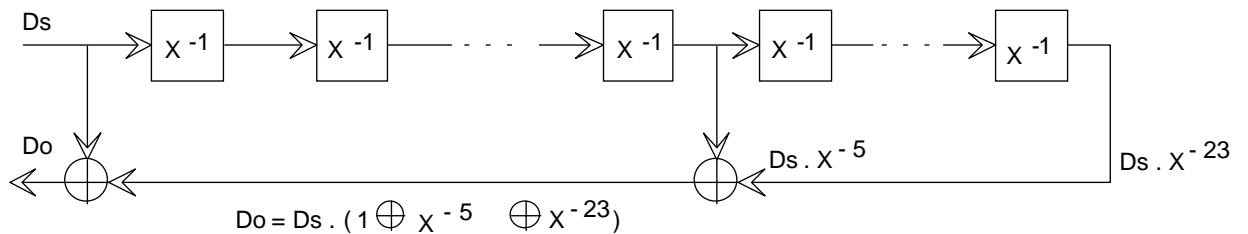
LTU (REG-C)

Transmit Descrambler (NTU to LTU)



NTU (REG-R)

Receive Descrambler (LTU to NTU)



D_s = scrambled (s) data
 D_i = unscrambled input (i) data
 D_o = unscrambled output (o) data
 X^{-n} = delay of bit periods

\oplus = logical exclusive or
 \circ = multiplication

Figure 9: Scramblers and descramblers

5.5 HDSL embedded operations channel (eoc)

This subclause specifies the requirements for the embedded operations channel. 13 of the available 50 HDSL overhead bits (HOH) as shown in tables 3 and 4 are used for the eoc-application and present a complete eoc-frame synchronised to the corresponding HDSL frame. The structure of each single eoc-frame is as shown in table 8 and discussed next.

Table 8: HDSL eoc frame structure

Bit Position	# of Bits	Description	Remarks
1,2	2	Address	Can address 4 locations
3	1	Data (ZERO)/ message (ONE) indicator	
4	1	Odd (ONE)/even (ZERO) byte	Multibyte Transmission
5	1	Unused	
6-13 (note)	8	Information field	256 Opcodes, 8 bits Data
NOTE: eoc-bit 6 contains the MSB and eoc-bit 13 the LSB of the opcode/data as described in in tables 9 to 11.			

- 1) The address field:
 - the first two bits (eoc 01 & eoc 02) allow for unique addressing of four network elements. This ETR specifies requirements for only three locations, NTU, REG and LTU;
 - the LTU address is "11" and can be considered as the eoc-master;
 - the NTU and REG (if present) addresses are "00" and "10" (eoc01, eoc02) respectively, and can be considered as the addresses of the slaves;
 - the address in a return echo should be set to that of the responding unit.
- 2) The data/message indicator bit:
 - the data/message indicator bit shall be set to ONE when the information field contains the operation code for an HDSL eoc message;
 - the data/message indicator bit shall be set to ZERO when the information field contains data, either binary or ASCII.
- 3) Odd/even byte:
 - the "odd byte"/"even byte" field is used as follows: The first byte of data to be either read or written, it is set to ONE to indicate "odd byte";
 - the next byte is set to ZERO to indicate even byte and so on, alternately;
 - this field is used to speed up data read and write by eliminating the need for intermediate codes to indicate to the far end that the previous byte was successfully received.
- 4) Unused bit:
 - set to ONE.
- 5) Information field:
 - up to 256 different messages or 8 bits of binary or ASCII data may be encoded in the information field.

5.5.1 Functions of the HDSL eoc

The LTU, as the master, sends commands to the slaved NTU/REG to perform certain functions. Some of these functions require the slave to activate changes in the circuitry (e.g. to either loopback or send crc bits that are corrupted). Other functions can be invoked to read from and write to data registers located in the slave.

Some of these commands are "latching", meaning that a subsequent command will be required to release from this state. Thus multiple HDSL eoc-initiated actions can be in effect simultaneously. A separate command "Return To Normal" together with the appropriate address shall be used to unlatch all latched states in the REG or the NTU. If no message is pending for both the NTU and the REG (idle state), the "Return To Normal" message shall be sent by the LTU together with the NTU-address "00". If no opcode has to be sent during a latched state the LTU may send the "Hold State" message.

The NTU, if not properly addressed, shall insert the "Hold State" message with the NTU-address "00" in the direction NTU → LTU. Normally if the REG has been addressed and its eoc-unit is working properly, this NTU message will be overwritten in the REG. In the case, the eoc unit in the REG is unable to react (due to improper function), receiving the "Hold State" message from the NTU indicates to the LTU, that the REG is not working properly, although the messages are transported over the whole link down to the NTU.

The regenerator REG is transparent to all messages in the direction LTU → NTU, including messages addressing the regenerator itself. In the direction NTU → LTU the regenerator is transparent as long as no messages addressing the regenerator, are received. In this case, any message from the NTU in the direction NTU → LTU is overwritten, depending on the action required by the eoc message for the regenerator.

The complete set of commands is listed in table 9 and described in subclause 5.5.5.

5.5.2 HDSL eoc acknowledgement protocol

The LTU is the master of the HDSL eoc and always issues the commands. The slave responds to properly addressed messages by acknowledging to the master that the message was received correctly. Thus, the HDSL eoc protocol operates in a Command/Response mode with the master issuing the command and the slave responding.

Any message to be sent by the LTU shall be inserted in parallel over all HDSL transceiver pairs. In the slave (NTU/REG) the evaluation and the acknowledgement is carried out separately for each HDSL transceiver system (subsystem), i.e. every subsystem echoes the received eoc message independent of the code on the other subsystems.

This subsystem oriented handling of the eoc-protocol allows for a regenerator implementation based on independent modules for each pair. This general principle is also provided in the NTU, i.e. messages which require an action on a single pair (e.g. all eoc-functions, read noise margin) are executed only on those pairs, where the message has been received correctly.

Global messages, not addressing functions of a single pair (e.g. loopback of application frame at NTU, read status register NTU, write configuration register NTU) shall also be sent over all pairs in parallel by the LTU.

The NTU, after receiving three consecutive valid messages on at least one single pair, enters the corresponding state and performs the appropriate action. The individual echoing of the received message is maintained however on each subsystem as described above. The eoc unit in the NTU has to take care, that a delayed evaluation of a valid code in one pair due to different BER on the different subsystems does not lead to a restart of an action already in progress.

Three types of responses are allowed from the slave, and thus there are three protocol states allowed on the HDSL eoc. At any time the HDSL eoc will be in one of the three protocol states, and can switch from one state to another during a message.

The three protocol states are:

- 1) message/Echo-response protocol state;
- 2) message/Data-Response protocol state;
- 3) message/Unable To Comply (UTC)-response protocol state.

5.5.2.1 Message/echo response protocol state

To acknowledge a properly addressed message from the LTU, the slave (NTU or REG) responds to a received HDSL eoc message by returning identical HDSL eoc frames back to the LTU. This response procedure is termed "echoing" the HDSL eoc message. The combination of the LTU sending the HDSL eoc frame and the slave echoing the frame back comprises the message/echo-response protocol state.

To assure the validity of the message, the slave needs to receive three identical, and consecutive HDSL eoc frames before activating the requested function. In this way, the transmitted HDSL eoc messages received by the slave can be assumed to be correct with high probability.

For the LTU to confirm correct reception of the message by the slave, the message is repeated until the LTU receives three identical and consecutive echoes. This serves as an implicit acknowledgement to the LTU that the slave has correctly received the transmitted message and is acting on it. This completes the Command/Response protocol mode.

In summary, the HDSL eoc protocol requires that the LTU transmits a message continuously until it receives three identical and consecutive echoes of the HDSL eoc frame originally transmitted.

The LTU cannot start sending a new message to the slave until the previous message on the HDSL eoc is acknowledged and the Command Response protocol for that message is completed. This "one message outstanding" rule automatically eliminates HDSL eoc contention problems that may occur between NTU and REG.

An HDSL core divides the payload between two or three pairs. The rules stated previously, requiring three consecutive identical receptions of a message or an acknowledgement, apply to a single pair. That is, the message or acknowledgement needs to be received three times consecutively, and identically over the same pair.

5.5.2.2 Command/response mode of operation for HDSL eoc

The following requirements apply:

- 1) only one message, under the control of the LTU, shall be outstanding (not yet acknowledged and confirmed) on the HDSL eoc at any time;
- 2) in order to cause the desired action in the slave, the LTU shall continue to send the message until it receives at least three identical consecutive HDSL eoc frames from the slave over one pair. This shall constitute an acknowledgement to the LTU that the slave received the transmitted message correctly;
- 3) for non-latching conditions the LTU shall after the receipt of the three valid echos continuously send the activating message or, alternatively, it shall switch to sending the Hold State message;
- 4) the slave shall initiate action when, and only when, three identical, consecutive, and properly addressed HDSL eoc frames, that contain a message recognised by the slave, have been received over at least one pair;
- 5) the slave shall respond to all properly addressed received messages. The response shall be an echo of the received HDSL eoc frame towards the LTU;
- 6) any reply or echoed HDSL eoc frame shall be sent in the next available returning HDSL eoc frame;

- 7) the loopback (in the NTU/REG) and request/notify corrupted crc commands shall be latching, permitting multiple HDSL eoc-initiated actions to be in effect simultaneously;
- 8) to unlatch all latched conditions, the message, "Return to Normal" shall be transmitted by the LTU. When the slave correctly receives the Return to Normal message from the LTU (3 times identically and consecutively), it shall unlatch all currently latched conditions initiated by prior HDSL eoc messages;
- 9) the slave shall not send autonomous messages.

5.5.2.3 Unable-to-comply mode of operation

When the slave does not support a properly addressed message that it has received three times identically and consecutively over the active pair, the slave responds with the UTC HDSL eoc response message instead of a third identical and consecutive echo. The slave shall then switch over to the message/UTC-response protocol state.

The slave also enters the message/UTC-response control state, if a message has been received that is not applicable in the current status of the command/response mode of operation, e.g. if a "Next Byte" message is detected without having received a "Read-data-register" opcode.

An error in transmission could corrupt the UTC response. This would make the LTU conclude that it was a proper message and was acknowledged. To reduce the probability of this happening, the UTC code is selected to have a Hamming distance of at least two from all other codes except the idle code.

Thus, the following requirements apply:

- a) if the NTU/REG does not support the message in a properly addressed HDSL eoc frame, it shall return the UTC message with its own address rather than echo on the third and all subsequent consecutive reception of that same correctly addressed HDSL eoc frame;
- b) the sending by the NTU/REG and the subsequent receipt by the LTU of three identical, consecutive, properly addressed UTC messages shall constitute notification to the LTU that the NTU/REG does not support the requested function, at which time the LTU may abandon its attempt.

The LTU may, of course, abandon the attempt at any time before the UTC is received (for example, if the "Return to Normal" or "Hold State" message is sent by the LTU);

- c) the NTU/REG exits the UTC mode of operation only after receiving three consecutive "Return To Normal" messages from the LTU.

5.5.3 The HDSL eoc data read/write mode

For data transmission, bit three and bit four are used in combination. Bit three will be set to data (ZERO) only when data (rather than an opcode) are transmitted. Bit four makes multi-byte data transmission more efficient. It will denote whether the data byte being transmitted is an "odd byte" or "even byte". As described in the next subclause, with this procedure there is a Message/Echo Response state to access the register, and following that one byte of data can be transferred for each Message/Data Response state. The LTU can either write data into the NTU/REG memory, or read data from the NTU/REG.

5.5.3.1 Data read protocol

If the LTU is reading data from the NTU/REG it will send an appropriate read opcode message to the NTU/REG that specifies the register to be read. After receiving three identical and consecutive acknowledgements, the LTU will request for the first byte to be sent from the NTU/REG by sending "Next Byte" messages with bit four set to ONE indicating a request for an "odd" byte. The NTU/REG will respond to these "Next Byte" messages by echoing them until it has received three such messages consecutively and identically. Beginning with the third such reception, the NTU/REG will respond by sending the first byte of the register in an HDSL eoc data frame with bit four set to ONE to indicate "odd byte". (A data frame

that contains data in the information fields is distinguished from a frame containing an opcode by setting bit three to ZERO.) The LTU continues to send the "Next Byte" message byte with bit four set to "odd byte", and the NTU/REG continues to respond with a data frame containing the first byte of data and bit four equal to "odd byte", until the LTU has received three consecutive and identical data frames with bit four set to "odd byte".

If there is more data to be read, the LTU requests the second byte of data by sending "Next Byte" messages with bit four set to ZERO ("even byte"). The NTU/REG echoes all messages received until three such "Next Byte" messages have been received, and on the third consecutive and identical "Next Byte" message, the NTU/REG starts sending data frames containing the second byte of the register with bit four set to ZERO. The LTU continues to send the "Next Byte" message with bit four set to "even byte", and the NTU/REG continues to respond with a data frame containing the second byte with bit four set to "even byte", until the LTU has received three consecutive and identical data frames with bit four set to "even byte". Note that once the NTU/REG is in the Data Read mode, to continue reading data, the only message that the LTU is allowed to send is the "Next Byte" message with bit four toggling.

If the LTU wants to end the Data Read mode (either normally or abnormally), it shall send the "Hold State" or "Return to Normal" message depending upon if the LTU wants to retain any latched state or not. If the NTU/REG receives any other message, three times consecutively, and identically, it should go into a UTC mode.

The process continues for the third and all subsequent bytes with the value of bit four toggling from "odd byte" to "even byte" or vice versa, on each succeeding byte. Each time bit four is toggled, the NTU/REG echoes for two correct frames, and starts sending the data frame on the third reception. The process ends only when all data in the register have been read. If the LTU continues to send the "Next Byte" message, with the fourth bit toggled, then the NTU/REG will send an "End of Data" message. It is assumed that the LTU knows how many bytes of data to expect, but this is a safety measure to end the process. Thus, each time a data byte is received satisfactorily by the LTU, the LTU will send a "Next Byte" code with the "odd/even" byte set appropriately until it is satisfied that it has received all the bytes, or, until it has received three identical and consecutive "End of Data" messages with bit three set to ONE indicating opcode. Thus, it is possible to accommodate data of many bytes.

The Data Read mode ends, and the NTU/REG releases the register, when the LTU switches over to a known state with the "Hold State" message or "Return To Normal" message depending on whether it wants the latched conditions held or not.

5.5.3.2 HDSL eoc data read mode requirements

The protocol state sequence for the data read mode is as follows:

1) *message/echo-response protocol state*

- a) The HDSL eoc shall enter the Data Read mode of operation when the LTU sends a "Read Data" message for a specific register.
- b) The response to this message shall be the echo response.

2) *message/data-response protocol state*

- a) Upon receiving three identical and consecutive echo responses that match the register-specific Data Read message, the LTU shall send the "Next Byte" message. At this time, bit three shall be set to ONE to indicate an opcode message, and bit four shall be set to ONE to indicate "Odd Byte".
- b) On receiving the "Next Byte" message, the NTU/REG shall echo the message until it receives it three times consecutively and identically. On the third identical and consecutive reception, the NTU/REG response shall change from the echo response to an HDSL eoc data frame containing the data byte requested. For this frame, bit three shall be set to ZERO to indicate that the information field contains data, and bit four shall be set to ONE.

- c) If the data requested by the LTU is retrieved from a one byte register, when the LTU has received three identical and consecutive HDSL eoc data frames containing the data byte, the "Return to Normal" message or "Hold State" message shall end the Data Read mode.
- d) If the data requested by the LTU is contained in a register two or more bytes long, the LTU shall initiate additional HDSL eoc protocol states. It shall continue sending the "Next Byte" message with bit three set to ONE, but bit four will be toggled between ZERO and ONE as each byte of data is successfully received (three identical, consecutive echos). Each time there is a change in bit four the NTU/REG shall start echoing the message, while remaining in the Data Read mode. On the third identical and consecutive reception, the NTU/REG shall switch to sending a data frame with the next byte of data in the information field.

3) *message/echo-response protocol state*

- a) When the LTU has completed its requirements for reading data, it shall start sending the "Hold State" message or "Return to Normal" message to end the Data Read mode.

5.5.3.3 Data write protocol

If the LTU wants to write data into the NTU/REG's memory, it will send a "Write Data" opcode message to the NTU/REG that identifies the required register to be written to. When the NTU/REG acknowledges with an echo message, three times identically and consecutively, the LTU will send the first byte of data. The NTU/REG will acknowledge the receipt of the byte with an echo of the message. After the LTU is satisfied with three identical and consecutive correct echo responses, it will start sending the next byte of data. Each time the LTU receives three identical and consecutive correct data echo responses, it will switch to sending the next byte of data. It will also toggle the "odd/even" bit accordingly. There is no need for sending "Next Byte" messages in the write mode. The LTU will end the write mode with the "End of Data" message indicating to the NTU/REG to release the register and to end the data write mode.

The contents of the addressed register in the NTU/REG are overwritten only, if the number of transmitted bytes equals the size of the addressed register and if the Data Write Mode has been properly finished by sending the "End of data" message by the LTU.

In any other case, i.e. if the number of transmitted bytes is higher or lower than defined or if the Data Write Mode is not properly finished, the NTU/REG enters the UTC mode and the contents of the corresponding register remain unchanged.

If the LTU abnormally wants to end the Data Write mode, it shall send the "Hold State" or "Return to Normal" message, depending upon if the LTU wants to retain any latched state or not. If the NTU/REG receives any other message, three times consecutively and identically, it shall enter the UTC mode.

5.5.3.4 HDSL eoc data write mode requirements

The protocol state for the data write mode is always message/echo-response. The message field can contain a command or data.

1) *message (command)/echo (command)-response protocol state*

- a) The HDSL eoc shall enter the Data Write mode of operation when the LTU sends a "Write Data" message for a specific register.
- b) The response by the NTU/REG to this message shall be the echo response.
- c) This protocol state shall be repeated until the LTU receives three identical and consecutive HDSL eoc frames containing the correct echo response.

- 2) *message (Data)/echo (Data)-response protocol state*
- a) Upon receiving three identical consecutive echo responses that match the register-specific Data Write message, the LTU shall send a data frame with the first byte of data and with bits three and four set to ZERO (indicating that the information field contains data) and bit five set to ONE (indicating "odd byte").
 - b) The NTU/REG shall respond to this transmission with the echo response.
 - c) The data byte shall be written by the NTU/REG unit upon receiving the data byte three times identically and consecutively.
 - d) This protocol state shall be repeated until the LTU receives three identical and consecutive HDSL eoc frames containing the correct echo response.
 - e) If the LTU is writing to a one byte register, the Data Write mode shall be completed upon the LTU receiving three identical and consecutive echoes of the data byte it had transmitted.
 - f) If the LTU is writing to a multi-byte register, the LTU shall continue sending additional bytes of data, while toggling bit five for each byte of data sent successfully.
 - g) When the LTU has no more bytes of data to write, the LTU shall send a "End of Data" message to release the NTU/REG from the Data Write protocol state.

5.5.4 HDSL eoc message list

The HDSL eoc protocol uses various messages listed in table 9 for activating various functions at the NTU/REG. The "Read Data" and "Write Data" commands can support up to 16 Registers each. The commands and the corresponding encoding used in this ETR, are shown in tables 10 and 11. The register that a "Read Data" or "Write Data" message operates on is specified as a subfield of the "Read Data" or "Write Data" opcode. Additional message opcodes have been reserved for future standardization.

Some actions initiated in the NTU/REG by HDSL eoc messages, such as loopbacks, and intentional corrupted CRC are "latching". Latching means that a different message is required to cancel the function. This permits the HDSL eoc to exercise multiple functions simultaneously, in spite of the "one message outstanding" rule. All latched functions may be unlatched with the "Return To Normal" HDSL eoc message. The "Return To Normal" message returns the NTU/REG to a known state. Repetition of this message continues to hold the NTU/REG in this known state. Hence, the "Return To Normal" message is also defined as the "idle code" for the NTU/REG. On the other hand, if all the latched functions were to be maintained in their latched state, the "Hold State" command is sent.

- 1) The LTU shall continuously send the activating message after the receipt of the three valid echoes or, alternatively, it shall switch to sending the "Hold State" message if it wants to maintain latched conditions.
- 2) The "loopback" and "Request/Notify corrupted crc" commands shall be latching, permitting multiple HDSL eoc-initiated actions to be in effect simultaneously.
- 3) To release all latched conditions, a separate message "Return to Normal" shall be transmitted by the LTU. When the NTU/REG correctly receives the "Return to Normal" message from the LTU (3 times identically and consecutively), it shall unlatch all currently latched conditions initiated by prior HDSL eoc messages.

5.5.5 HDSL eoc message set requirements

The HDSL eoc message set is shown in table 9. The actions taken by the NTU/REG and LTU in response to correctly received HDSL eoc messages shall be as follows:

1) *Unable to Comply (UTC)*

The NTU/REG shall send this message when it receives an HDSL eoc message (three times consecutively and identically) that the NTU/REG cannot perform, either because it does not recognize or has not implemented the command, or because the command is unexpected given the current state of the HDSL eoc operations (e.g., the command indicates that the information field contains data, but the command was not preceded by a "Write Data" command).

2) *Return to Normal all active condition*

This message shall release all outstanding latched conditions at the NTU/REG initiated by prior HDSL eoc messages. The function of the "Return to Normal" message may be used as an eoc reset function for the NTU/REG. Therefore, the proper evaluation of this message in a single NTU/REG subsystem results in a reset of all pending functions in this subsystem. This code sent with the NTU-address "00" shall also be sent during idle states.

3) *Loopback of application frame at NTU*

This message shall direct the NTU to loopback the application bit stream toward the LTU until canceled by a "Return to normal" message.

4) *Hold State*

This message shall be sent by the LTU to maintain the NTU/REG HDSL eoc processor and any active HDSL eoc controlled operations in their present state.

5) *Analogue Loopback 1A in REG*

This function directs the REG to loopback the user-data bitstream toward the LTU. This is a transparent loopback. Since this is a function of each individual subsystem REG, the LTU needs to take care, that these messages are acknowledged by each individual subsystem.

6) *Request Corrupted CRC (NOTE 1)*

Sometimes the appearance of error free transmission may result because the CRC circuit is not functioning properly. Hence, when the performance monitoring circuit is suspected of malfunction, corrupted CRCs can be sent to test the crc logic as well as the circuits that collect, process and store performance data.

6a) *Request Corrupted CRC NTU (note 2)*

-No REG present

Corrupted CRCs are requested to be sent from the NTU to test the CRC checking circuit at the LTU until canceled with the "Request End of Corrupted CRC NTU" message.

-REG present

Corrupted CRCs are requested to be sent from the NTU to test the CRC checking circuit at the REG-C until canceled with the "Request End of Corrupted CRC NTU" message. This results in the transmission of an active rcbe-bit by the REG towards the LTU and NTU as soon as corrupted CRCs are detected from the NTU.

6b) *Request Corrupted CRC REG-R* (note 2)

Corrupted CRCs are requested to be sent from the REG towards the LTU to test the CRC checking circuit at the LTU until canceled with the "Request End of Corrupted CRC REG-R" message.

6c) *Request Corrupted CRC REG-C*

Corrupted CRCs are requested to be sent from the REG towards the NTU to test the CRC checking circuit at the NTU until canceled with the "Request End of Corrupted CRC REG-C" message. This results in the transmission of an active febe-bit by the REG towards the NTU towards the LTU as soon as corrupted CRCs are detected from the REG.

7a) *Request End of Corrupted CRC NTU* (note 2)

This message shall request the NTU to stop sending corrupted CRCs towards the REG or LTU as applicable.

7b) *Request End of Corrupted CRC REG-R* (note 2)

This message shall request the REG to stop sending corrupted CRCs towards the LTU.

7c) *Request End of Corrupted CRC REG-C*

This message shall request the REG to stop sending corrupted CRCs towards the NTU.

8a) *Notify of Corrupted CRC NTU* (note 2)

-No REG present

This message shall notify the NTU that intentionally corrupted CRCs will be sent towards the NTU by the LTU. This message shall be used in the NTU to disable any alarm indication circuitry activated by the detection of corrupted CRCs. The febe-bit towards the LTU shall be still active however.

-REG present

This message shall notify the NTU that intentionally corrupted CRCs will be sent towards the NTU by the REG. This message shall be used in the NTU to disable any alarm indication circuitry activated by the detection of corrupted CRCs. The febe-bit towards the LTU shall be still active however.

8b) *Notify Corrupted CRC REG-R* (note 2)

This message shall notify the REG that intentionally corrupted CRCs will be sent towards the REG by the LTU. This message shall be used in the REG to disable the transmission of an active rrbe-bit towards the NTU, as soon as corrupted CRCs are detected from the NTU. The rcbe-bit towards the LTU shall be still active however.

8c) *Notify Corrupted CRC REG-C*

This message shall notify the REG that intentionally corrupted CRCs will be sent towards the REG by the NTU. This message shall be used in the REG to disable the transmission of an active rcbe-bit towards the NTU, as soon as corrupted CRCs are detected from the NTU. The rcbe-bit towards the LTU shall be still active however.

9a) *Notify End of Corrupted CRC NTU* (note 2)

This message shall notify the NTU that the LTU or REG has stopped sending intentionally corrupted CRCs and that the NTU may enable again any alarm circuitry detecting corrupted CRCs.

9b) *Notify End of Corrupted CRC REG-R* (note 2)

This message shall notify the REG that the LTU has stopped sending intentionally corrupted CRCs and that the REG may enable again the transmission of a valid rrbe-bit towards the NTU when detecting corrupted CRCs from the LTU.

9c) *Notify End of Corrupted CRC REG-C*

This message shall notify the REG that the NTU has stopped sending intentionally corrupted CRCs and that the REG may enable again the transmission of a valid rcbe-bit towards the NTU when detecting corrupted CRCs from the NTU.

10) *End of Data*: This message shall be sent by the LTU after it has written all bytes of data to the NTU/REG and by the NTU/REG when the LTU requests more bytes than are available in the NTU/REG register during a data read procedure.

11) *Next Byte*: This message shall be sent by the LTU in the Data Read mode after the NTU/REG has acknowledged the previously sent "Read Data" command. This message shall be continually sent by the LTU when it is in the Data Read mode until all data have been read. This message, coupled with the toggling of bit four, allows multi-byte data to be read.

12) *Write Data (Register #)*: This message shall be sent by the LTU to set the NTU/REG in a mode to receive data in the register specified. The number of the register at the NTU/REG that shall receive data is encoded in the command itself. After receiving this message correctly, the NTU/REG shall enter the Data Write mode, ready to receive the data contained in the data messages to follow, and store the data in the register number encoded in the command.

13) *Read Data (Register #)*: This message shall be sent by the LTU to set the NTU/REG in a mode to read the data in the register specified. The number of the register at the NTU/REG from which the data are to be read is encoded in the command itself. After receiving this message correctly, the NTU/REG shall enter in the Data Read mode and transmit data from the register encoded in the command, one byte at a time, in response to successive "Next Byte" messages (with changes in bit four) from the LTU.

NOTE 1: No specific algorithm for the corruption is to be defined.

NOTE 2: For the messages signed by indices .a and .b the same opcode is used. The equipment concerned is indicated by the address contained in the message.

Table 9: eoc opcode messages

Hex-code	Opcode description
06	Unable to Comply (UTC)
07	Return to Normal all active conditions
08	Loopback of application frame at NTU (note 1)
10	Hold State
19	Analogue Loopback in REG (note 1, note 2)
20	Request Corrupted CRC NTU/REG-R (note 1, note 3)
22	Request Corrupted CRC REG-C (note 1)
28	Request End of Corrupted CRC NTU/REG-R (note 3)
29	Request End of Corrupted CRC REG-C
3F	Notify Corrupted CRC NTU/REG-R (note 1, note 3)
50	Notify Corrupted CRC REG-C (note 1)
5F	Notify End of Corrupted CRC NTU/REG-R (note 3)
60	Notify End of Corrupted CRC REG-C
9F	End of Data
AF	Next Byte
D0-DF	Write Data Register (numbers 0 to F)
E0-EF	Read Data Register (numbers 0 to F)
F0-F3	Vendor defined
NOTE 1:	Latching; this means that a release message is required to cancel the function.
NOTE 2:	Due to the used transmission system, separate loopbacks for each pair have to be setup in the regenerator. The O&M unit in the LTU has to assure that the individual loopback is closed, before acknowledging the proper operation to the application interface.
NOTE 3:	This opcode is used for messages concerning the NTU or the REG-R. A distinction between both is possible by the address contained in the message.
NOTE 4:	No need has been identified for the messages 18, 30, 38, 6F, 7F in Europe. They may be used by network operators outside Europe, e.g. in North America as defined in an ANSI specification.
NOTE 5:	All other messages are reserved for future applications.

5.5.6 Data registers in the NTU and in regenerators

The NTU and the regenerator each contain 16 registers. These registers can be used for read only or for read and write operations. The registers used inside Europe are defined in tables 10 and 11. The registers #1 to 9 may be used by network operators outside Europe, e. g. in North America as defined in an ANSI specification. The register F is not used at present. Only the registers E in the NTU and C, D and E in the REG are individual for each transceiver of a two or three pairs system. All other registers contain equipment relevant data and are available over all pairs in parallel. Individual registers (register D) at the REG are required for equipment identification when separate regenerators are used in each pair.

Table 10: eoc data registers for the NTU

Reg# (HEX)	USE	LENGTH	NAME	DESCRIPTION
A	R	TBD	NTU status	NTU status information bits
B	R/W	TBD	NTU configuration	NTU configuration bits
D	R	TBD	equipment identification	
E	R	1 byte	noise margin	
NOTE:	The number of bytes and the contents of the status and configuration registers, as well as the encoding of the different bits is left to the individual network operator.			

Table 11: eoc data registers for regenerators

Reg# (HEX)	USE	LENGTH	NAME	DESCRIPTION
A	R	TBD	REG-status	REG status information bits
C	R	1 byte	noise margin REG-C	
D	R	TBD	equipment identification	
E	R	1 byte	noise margin REG-R	
NOTE: The number of bytes and the contents of the status register, as well as the encoding of the different bits is left to the individual administration.				

5.5.7 Noise margin

5.5.7.1 General

For the evaluation of the noise margin a Gaussian noise is assumed. The noise value is calculated based on a sample taken each second for each pair separately. The evaluating range is between + 27 dB and - 5 dB, where 0 dB indicates the noise margin for which a BER of 10^{-7} for each pair is expected. The accuracy of the values shall be 1 dB in the range between + 5 dB and - 5 dB.

5.5.7.2 Coding of the noise margin values

The coding shall use a logarithmic law and have an increment of 0,5 dB. It uses one byte from which the first bit (MSB) is fixed to ONE, the second bit indicates the sign and the remaining six bits are used for the value of the noise margin, as shown in table 12.

Table 12: Coding of noise margin values

Noise margin	MSB								LSB	
	1	2	3	4	5	6	7	8		
+ 31,5 dB	1	0	1	1	1	1	1	1		
+ 27,5 dB	1	0	1	1	0	1	1	1		not relevant
+ 27,0 dB	1	0	1	1	0	1	1	0		
										expected BER $<10^{-7}$
+ 0,5 dB	1	0	0	0	0	0	0	1		
0 dB	1	0	0	0	0	0	0	0		expected BER 10^{-7}
- 0,5 dB	1	1	1	1	1	1	1	1		expected BER $>10^{-7}$
- 5,0dB	1	1	1	1	0	1	1	0		
- 5,5 dB	1	1	1	1	0	1	0	1		not relevant
- 31,5 dB	1	1	0	0	0	0	0	1		

5.6 Start-up procedure

5.6.1 General

5.6.1.1 Start-up

The start-up procedure is designed as a local procedure for each pair, it is a process characterized by a sequence of signals produced by the NTU, the LTU and the REG. Start-up results in an establishment of two-way transmission (if possible) between the application interfaces, i.e. synchronization of the receivers, training of the echo-cancelers and training of the equalizers to the point that the requirements for reliable communications are met. Also, tip-ring polarity reversal and pair interchanges are automatically detected and compensated at the NTU. It is the task of the operation and maintenance block to detect when the start up procedure for all pairs is completed and to initiate a transparent transmission of user data.

5.6.1.2 Activation of HDSL transceiver pairs

Activation is the process for the establishment of duplex communication over a single pair. This process is established between the HDSL transceivers at the LTU and the NTU, or between the LTU and the REG-R and the REG-C and the NTU respectively.

5.6.1.3 Transparency

Prior to the completion of activation the transmission is not transparent, the signals that are present at the line interfaces of the HDSL transceivers are special start-up patterns generated by the HDSL transceivers.

Each HDSL transceiver shall provide transparent transmission of data to the core function after completion of the individual activation procedure.

The HDSL core shall provide transparent transmission on each HDSL transceiver only when the pair identification as defined in subclause 5.6.7 has been checked. The operational status is determined by the application.

5.6.1.4 Noise margin

The noise margin is estimated at the receivers on both sides of each pair. This value is used to estimate the Bit Error Ratio (BER) of the received data.

During the start-up procedure the noise margin is compared to a value of - 5 dB.

NOTE: This value does not allow data transmission, it is chosen to be in compliance with existing equipment using the noise margin as a criteria for start-up.

5.6.2 Control and status signals

The following virtual control and status signals are involved in the activation procedure. They are related to the operation of the individual HDSL transceiver.

5.6.2.1 Control signals

5.6.2.1.1 QUIET

QUIET = ONE will cause a transition of the HDSL transceiver from any state (except the Inactive State) to the Deactivated State, where no energy is transmitted to the line. The QUIET = ONE command will not cause any change if the HDSL transceiver is in the Inactive State.

5.6.2.1.2 ACTREQ

Activation Request (ACTREQ) defaults to ONE at power up. The HDSL transceiver at the LTU will begin the activation process only if ACTREQ is equal to ONE.

5.6.2.2 Status signals

All of the following status signals are defined per pair.

5.6.2.2.1 LOSW

The absence of the *Loss of Synch Word* signal (LOSW = ZERO) indicates that HDSL frame synchronization is completed. When LOSW = ONE the receiver has not yet acquired frame synchronization, or it has lost it (see figure 13).

5.6.2.2.2 LOSWT

LOSWT = ONE indicates that the frame synchronization has been lost for more than 2 seconds.

5.6.2.2.3 LOS

The *Loss of Signal* signal (LOS = ONE) in the NTU indicates that no signal is detected on the line from the LTU. LOS = ZERO indicates that a signal from the LTU has been detected.

5.6.2.2.4 LOST

The LOST = ONE in the LTU indicates that no signal is detected on the line from the NTU for more than 1 second.

5.6.2.2.5 INDC

When an HDSL transceiver at the LTU is ready to receive data the indicator INDC is set (INDC = ONE). The condition for INDC = ONE is:

((LOSW = ZERO) & (noise margin > - 5 dB) & (PID detected)) or ((LOSW = ZERO) & (T-Act expired)).

5.6.2.2.6 INDR

When an HDSL transceiver at the NTU is ready to receive data the indicator INDR is set (INDR = ONE). The condition for INDR = ONE is:

((LOSW = ZERO) & (noise margin > - 5 dB) & (PID detected)) or ((LOSW = ZERO) & (T-Act expired)).

NOTE: The indicators INDC and INDR are different from the *indc*- and *indr*-bits as described in tables 3 and 4.

5.6.2.2.7 PID

The path identification process which is independent for each HDSL transceiver takes place in each HDSL transceiver after the HDSL frame synchronization is established (LOSW = 0). If during six consecutive HDSL frames specific pair identifications are valid, represented by Z-bits in the HDSL payload, then the Path Identification Detect (PID) is acknowledged. This procedure is described in detail in subclause 5.6.7.

5.6.2.2.7.1 PID for the three pairs system

Each HDSL transceiver at the NTU looks at bits Z_1 , Z_2 and Z_3 in the HDSL frame it receives and if one of the valid patterns as defined in table 14 is detected in six consecutive HDSL frames it's PID is set to ONE.

5.6.2.2.7.2 PID for the two pairs system

Each HDSL transceiver at the NTU looks at bits Z_1 and Z_2 in the HDSL frame it receives and if one of the valid patterns as defined in table 15 is detected in six consecutive HDSL frames it's PID is set to ONE.

5.6.3 Transmitted signals

The following is the description of the transmitted signals during activation.

5.6.3.1 Silent

No signal is transmitted to the line.

5.6.3.2 S0 signal

The S0 signal is a framed two level scrambled-ones signal and the stuff symbols shall be used every other frame period. The scrambler is operating at the line bit rate and only the sign bit is used to select the level of the signal. The stuffing bits shall be used every other frame. The scrambler is disabled during the transmission of the HDSL frame synch word and stuffing bits. The transmitted levels of all symbols in the S0 signal are + 3 and - 3.

5.6.3.3 S1 signal

The S1 signal is a framed four level scrambled signal. The frame consists of the HDSL frame synch word, the stuffing bits, the valid overhead bits and an all-ones signal as the payload. The scrambler is operating at full rate and is disabled during the transmission of the HDSL frame synch word and the stuffing bits. The transmitted levels are + 3,+ 1,- 1 and - 3.

5.6.3.4 2B1Q data

This signal is application dependent until the start-up procedure is finished for all transceiver pairs.

5.6.4 Timers

The following timers are involved in the activation procedure of the HDSL transceivers. The timeline of the activation sequence is given in figures 10 and 14 and the timer values are given in table 13. The precise role of the timers in the start-up procedure is described in subclause 5.6.5.

5.6.4.1 T1

T1 is the duration which the HDSL transceiver at the LTU continues to transmit a S0 signal after it has detected a S0 signal from the NTU.

5.6.4.2 T2

T2 is the duration between the time that the HDSL transceiver at the NTU detects signal from the HDSL transceiver at the LTU and the time that it starts to transmit the S0 signal.

5.6.4.3 T3

T3 is the duration between the time that the HDSL transceiver at the NTU detects the S1 signal from the HDSL transceiver at the LTU and the time that it starts to transmit the S1 signal.

5.6.4.4 T4

T4 is the duration between the HDSL transceiver at the NTU starts to transmit the S0 signal and guaranteed stable timing.

5.6.4.5 T5

T5 is the time to transmit six HDSL frames necessary to gain valid PID.

5.6.4.6 T6

T6 is the time of six HDSL frames sent between the valid PID and starting transparent signal transmission.

5.6.4.7 T-Act

The activation time for the HDSL transceivers (T-Act) is the time in which the activation procedure in the HDSL transceivers at the LTU or at the NTU should have successfully been completed, starting from the point in time where the HDSL transceiver at the NTU starts to transmit the S0 signal.

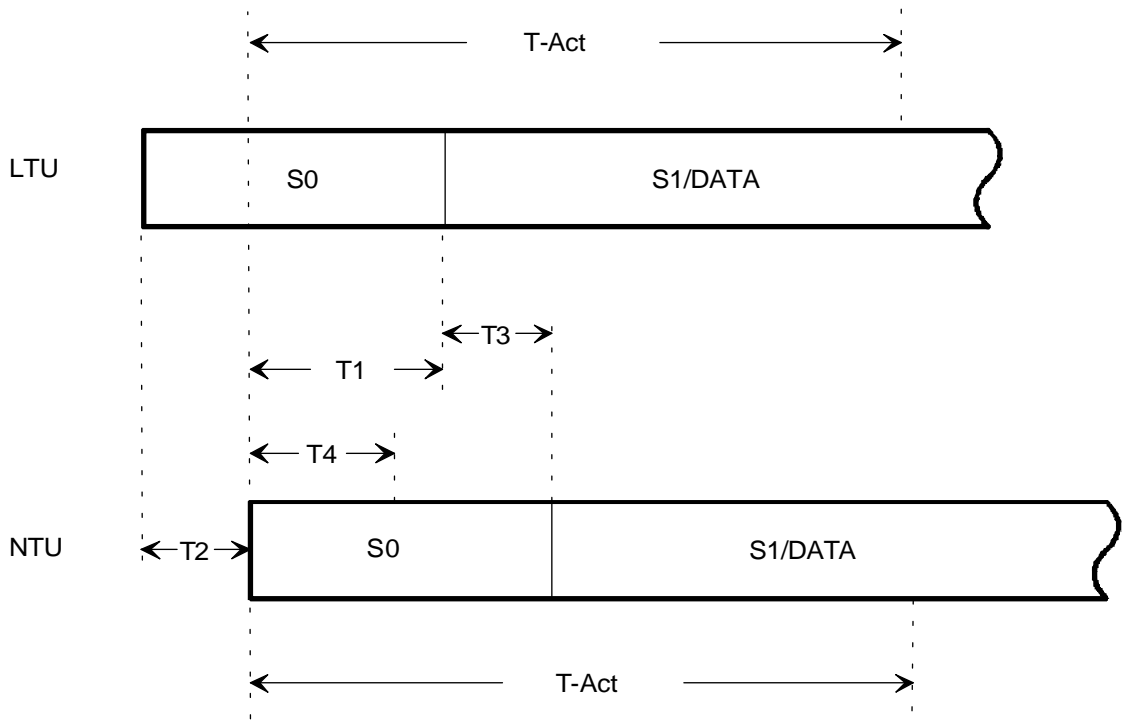


Figure 10: Activation timeline

5.6.4.8 Timer values

The timer values are listed in table 13.

Table 13: Timer values for start-up

Lower Bound		Timer		Upper Bound
5 s	<	T1	<	10 s
1,9 s	<	T2	<	2,1 s
		T3	<	4 s
		T4	<	4 s
36 ms	<	T5		
35 ms	<	T6	<	37 ms
		T-Act	<	28 s

5.6.5 Activation state diagrams

The following describe the state diagrams for the HDSL transceivers at the NTU and LTU, see figures 11 and 12 respectively.

5.6.5.1 HDSL transceiver states at the NTU

When the system is powered on, it enters the Inactive State after completing self-tests.

Certain transitions depend on the detection of the INDC = ONE status. The HDSL transceiver at the NTU will confirm INDC = ONE only if it detects this condition in six consecutive HDSL frames.

5.6.5.1.1 Inactive State

During the Inactive State the HDSL transceiver at the NTU is silent, LOSW = ONE and LOS = ONE. Upon the detection of a signal from the HDSL transceiver at the LTU (LOS = ZERO) it changes to the Activating State.

5.6.5.1.2 Activating State

On detection of a signal from the LTU the NTU changes from the Inactive State to the Activating State, waits the time T2 while transmitting no signal then starts to transmit S0 and the activation timer (T-Act). When the NTU detects valid four level data from the LTU (LOSW = ZERO) it starts T3. On expiry of T3 the NTU transmits S1. Recognition of INDR = ONE causes the NTU to change to the Active Rx State similarly if data received from the LTU indicates that the LTU has INDC = ONE, the NTU changes to Active Tx State. If T-Act expires the NTU enters the Deactivated State.

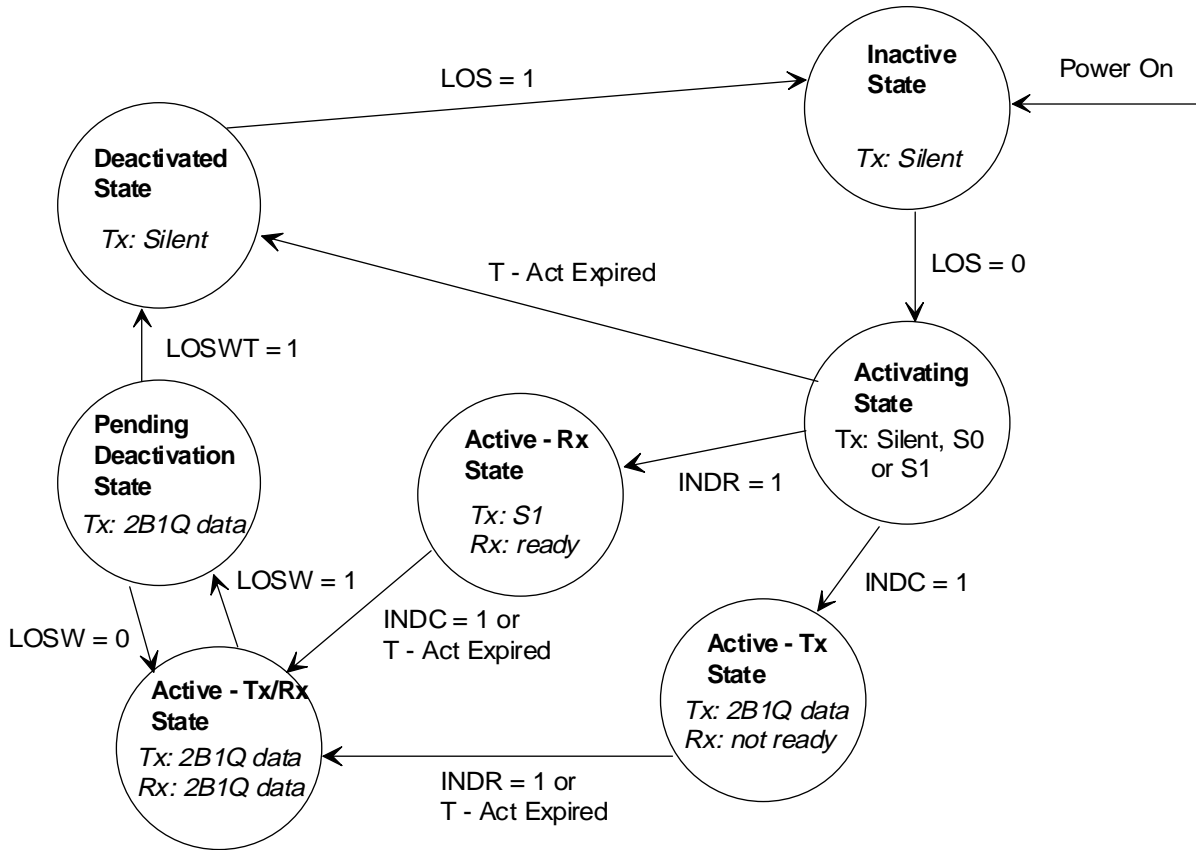


Figure 11: NTU activation state diagram

5.6.5.1.3 Active-Rx State

During the Active-Rx State INDC = ZERO, INDR = ONE and the HDSL transceiver at the NTU is transmitting the S1 signal and at the same time is ready to receive 2B1Q Data from the HDSL transceiver at the LTU. If the HDSL transceiver at the NTU senses from the data arriving from the HDSL transceiver at the LTU that INDC = ONE, or if the T-Act timer expires, it changes to the Active-Tx/Rx State. The HDSL transceiver at the NTU continues to monitor the HDSL frame synch word according to figure 13.

5.6.5.1.4 Active-Tx State

During the Active-Tx State INDC = ONE, INDR = ZERO and the HDSL transceiver at the NTU is transmitting 2B1Q data and at the same time is receiving the S1 signal from the HDSL transceiver at the LTU. When INDR = ONE, or when the T-Act timer expires, the HDSL transceiver at the NTU changes to the Active-Tx/Rx State and continues to monitor the HDSL frame synch word according to figure 13.

5.6.5.1.5 Active-Tx/Rx State

Upon entering the Active-Tx/Rx State the T-Act timer is deactivated. The transmitted signal is 2B1Q data.

If the HDSL frame synchronization is lost (LOSW = ONE) the HDSL transceiver at the NTU changes to the Pending Deactivation state.

5.6.5.1.6 Pending Deactivation State

During the Pending Deactivation State $LOS\ W = ONE$, and the transmitted signal is 2B1Q Data. When the HDSL transceiver at the NTU enters this state a 2 second timer is started. If the HDSL frame synchronization is regained then $LOS\ W = ZERO$ and the HDSL transceiver at the NTU returns to the Active-Tx/Rx State. If the 2 second timer expires, then $LOS\ W\ T = ONE$ and the HDSL transceiver at the NTU changes to the Deactivated State.

5.6.5.1.7 Deactivated State

During the Deactivated State, no signal is transmitted to the line and $LOS\ W = ONE$. When the HDSL transceiver at the NTU enters this state it looks for signal power from the HDSL transceiver at the LTU and when no power is detected ($LOS = ONE$) it changes to the Inactive State.

5.6.5.2 HDSL transceiver states at the LTU

The command QUIET at any state (except the Inactive State) will cause a transition to the Deactivated State. The command QUIET at the Inactive State will not cause any transition. When the system is powered on, it enters the Inactive State after completing the self-tests.

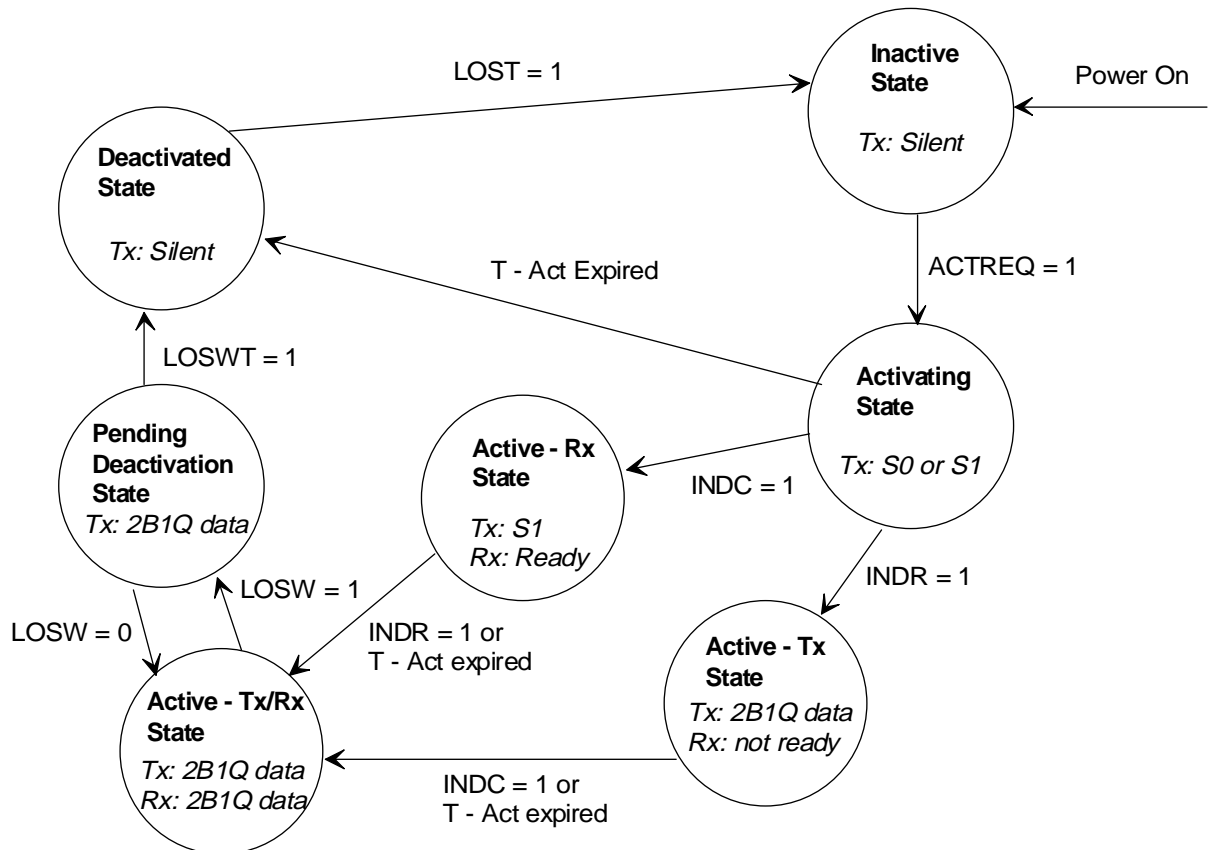


Figure 12: LTU activation state diagram

Certain transitions in the state diagrams depend on the detection of $INDR = ONE$ being recognized in the incoming data. The HDSL transceiver at the LTU will confirm that $INDR = ONE$ only if it detects this condition in six consecutive HDSL frames.

5.6.5.2.1 Inactive State

During the Inactive State the HDSL transceiver at the LTU is silent and $LOS\ W = ONE$, it waits for the $ACTREQ = ONE$ command, and then moves to the Activating State.

5.6.5.2.2 Activating State

During the Activating State the transmitted signal can be either S0 or S1. When the HDSL transceiver at the LTU enters this state from the Inactive State, it starts to transmit the S0 signal. During the transmission of the S0 signal, when it senses for the first time a signal from the HDSL transceiver at the NTU it starts the T1 timer and the T-Act timer. When the T1 timer expires the HDSL transceiver at the LTU starts to transmit the S1 signal. During the transmission of the S1 signal, if the HDSL frame synchronization is detected then LOSW = ZERO. If the HDSL transceiver at the LTU senses from the data arriving from the HDSL transceiver at the NTU that INDR = ONE it changes to the Active-Tx State. If INDC = ONE the HDSL transceiver at the LTU changes to the Active-Rx State. If the T-Act timer expires the HDSL transceiver at the LTU changes to the De-activated State.

5.6.5.2.3 Active-Rx State

During the Active-Rx State INDC = ONE, INDR = ZERO and the HDSL transceiver at the LTU is transmitting the S1 signal and at the same time is ready to receive 2B1Q Data from the HDSL transceiver at the NTU. When the HDSL transceiver at the LTU senses from the data arriving from the HDSL transceiver at the NTU that INDR = ONE, or when the T-Act timer expires, it changes to the Active-Tx/Rx State. The HDSL transceiver at the LTU continues to monitor the HDSL frame synch word according to figure 13.

5.6.5.2.4 Active-Tx State

During the Active-Tx State INDC = ZERO, INDR = ONE and the HDSL transceiver at the LTU is transmitting 2B1Q data and at the same time it is receiving the S1 signal from the HDSL transceiver at the NTU. When INDC = ONE or when the T-Act timer expires, the HDSL transceiver at the LTU changes to the Active-Tx/Rx State. The HDSL transceiver at the LTU continues to monitor the HDSL frame synch word according to figure 13.

5.6.5.2.5 Active Tx/Rx State

Upon entering the Active-Tx/Rx State the T-Act timer is deactivated. The transmitted signal is 2B1Q data.

If the HDSL frame synchronization is lost (LOSW = ONE) the HDSL transceiver at the LTU changes to the Pending Deactivated State.

5.6.5.2.6 Pending Deactivation State

During the Pending Deactivation State LOSW = ONE and the transmitted signal is 2B1Q Data. When the HDSL transceiver at the LTU enters this state a 2 second timer is started. If the HDSL frame synchronization is regained then LOSW = ZERO and the HDSL transceiver at the LTU returns to the Active-Tx/Rx State. If the 2 second timer expires, then LOSWT = ONE and the HDSL transceiver at the LTU changes to the De-activated State.

5.6.5.2.7 Deactivated State

During the Deactivated State, no signal is transmitted to the line and LOSW = ONE. When the HDSL transceiver at the LTU enters this state it looks for signal power from the HDSL transceiver at the NTU. When no power is detected (LOS = ONE) a 1 second timer is started. When this timer expires (LOST = ONE) the HDSL transceiver at the LTU changes to the Inactive State.

5.6.5.3 The HDSL synchronization state machine

The HDSL synchronization state machine is described in figure 13 and contains the states described below.

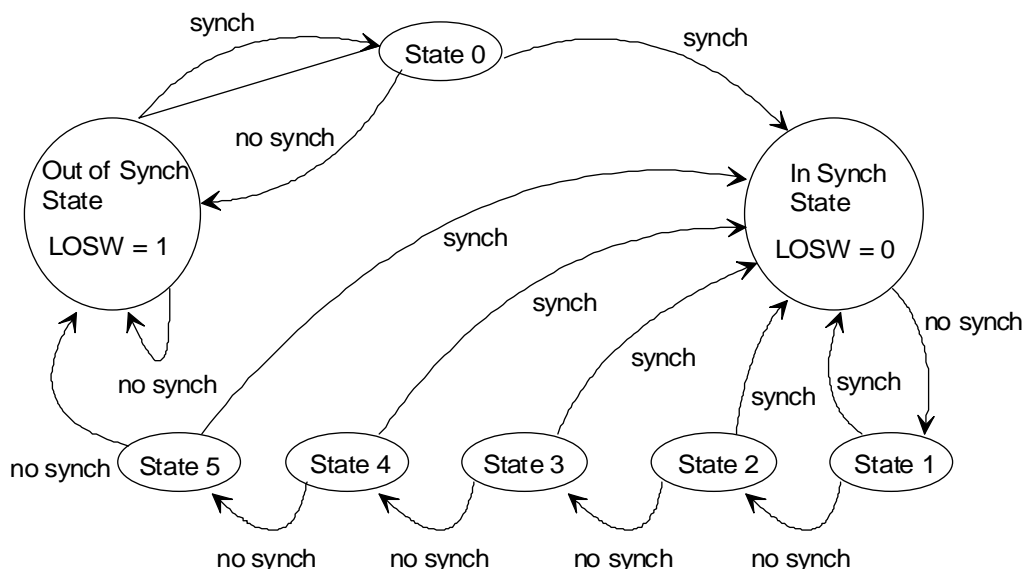


Figure 13: HDSL synchronization state machine

5.6.5.3.1 In Synch State

In this state HDSL synchronization has been achieved, i.e. LOSW = ZERO.

5.6.5.3.2 State 1

When frame synch word is lost for the first time the HDSL transceiver moves to State 1.

5.6.5.3.3 State 2

When in State 1 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again the HDSL transceiver will move to State 2.

5.6.5.3.4 State 3

When in State 2 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again the HDSL transceiver will move to State 3.

5.6.5.3.5 State 4

When in State 3 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again the HDSL transceiver will move to State 4.

5.6.5.3.6 State 5

When in State 4 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again the HDSL transceiver will move to State 5.

5.6.5.3.7 Out of Synch State

When in State 5 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again the HDSL transceiver will move to the Out of Synch State. When synchronization is regained the HDSL transceiver moves to State 0, otherwise it will remain in the Out of Synch State.

5.6.5.3.8 State 0

When in State 0 and the frame synch word is recovered the HDSL transceiver will return to the In Synch State. When the frame synch word is lost again then the HDSL transceiver will move to the Out of Synch State.

5.6.6 Regenerator related procedures

For the achievement of higher ranges of distances for data transmission within an HDSL-link, the use of one regenerator (REG) is necessary.

A REG has to be provided separate for each pair. The REG unit integrates two parts. The first is the corresponding part for co-operation with the LTU (REG-R) and the second is the corresponding part for co-operation with the NTU (REG-C), containing an HDSL-transceiver for each direction of co-operation. An internal connection of REG-R and REG-C provides the communication between both parts during start-up and normal operation.

The REG-R contains all functions for the communication with the LTU (NTU characteristics) and the REG-C contains all functions for the communication with the NTU (LTU characteristics).

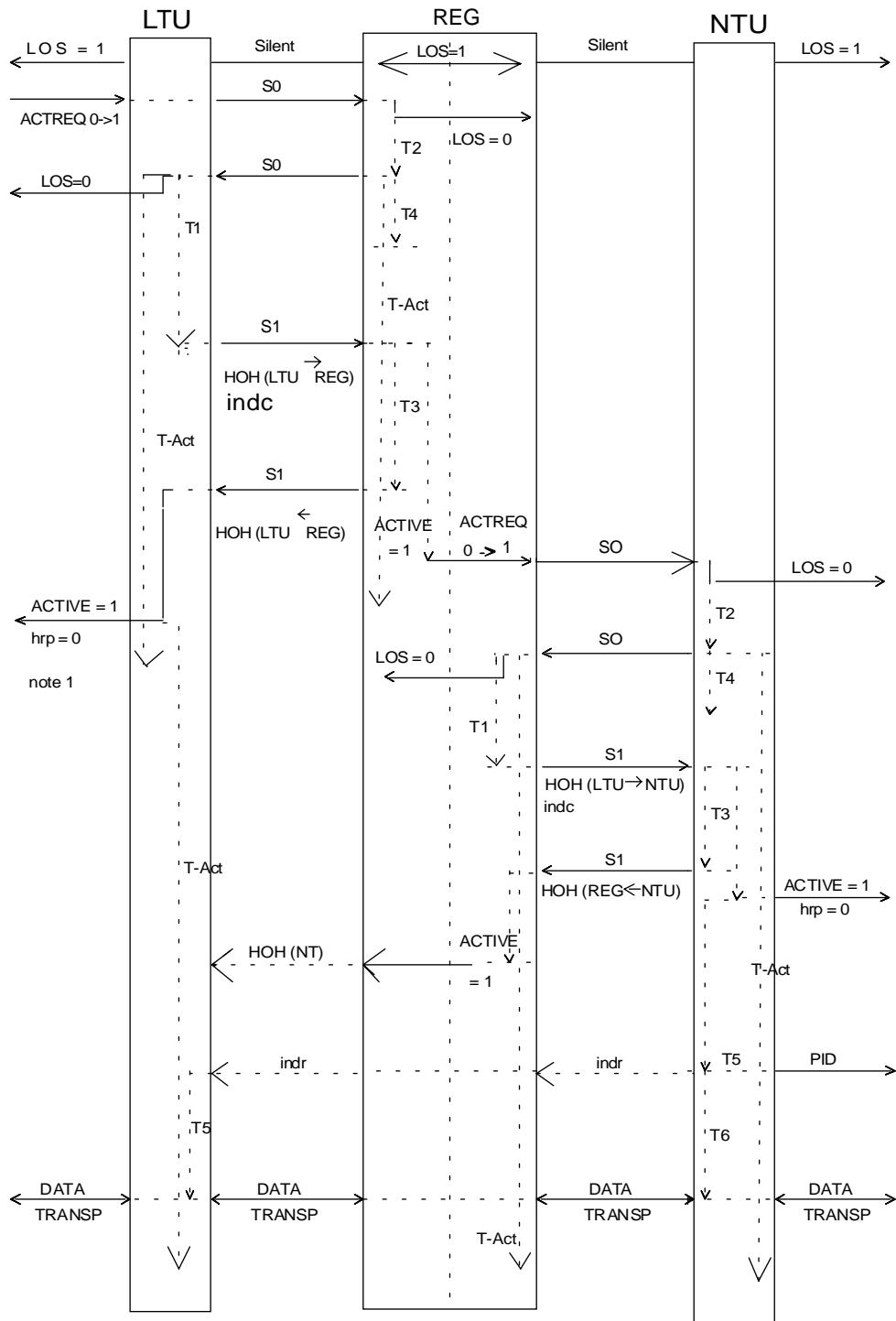
A connection which uses a regenerator has two separated HDSL links, each of them follows the above described start-up procedure.

The link between the LTU and the REG is the first to be activated. After the completion of the start-up procedure of this link the second link between the REG and the NTU will be activated.

The following flow diagram shows the start-up sequences for the link between the LTU and the NTU.

5.6.7 The pair identification mechanism

The pair identification procedure is based on the use of the Z-bits. The following is a definition of a pair identification mechanism that has to be completed for each pair separately, and agrees with the local procedures for activation. The pair identification procedure is operated only between the LTU and the NTU, the optional REG transfers the related information transparently.



NOTE: If hrp = ONE is detected (no REG present) the second T-Act timer will not be started. The path identification procedure, as described in the second half of the diagram, has to be evaluated before the first T-Act timer in the LTU has been expired.

Figure 14: Start-up procedure with regenerator

5.6.7.1 Pair identification initial values

At the beginning of the start-up procedure, each HDSL transceiver in the LTU is assigned with a pair identification number, which may be 1, 2 or 3 for three pairs systems or 1 or 2 for two pairs systems. The HDSL transceivers in the NTU are not assigned.

When the HDSL transceiver at the LTU reaches the phase in the activation procedure where it starts to transmit the S1 signal (in the Activating State), the indicator bits Z_{m1} , Z_{m2} and Z_{m3} for three pairs systems or Z_{m1} and Z_{m2} for two pairs systems are set according to tables 14 and 15, using the pair identification number it was assigned. When the HDSL transceiver at the NTU reaches the phase in the activation procedure where it starts to transmit the S1 signal (in the Activating State), the indicator bits Z_{m1} , Z_{m2} and Z_{m3} for the three pairs system or Z_{m1} and Z_{m2} only for the two pairs system are all set to ONE.

Table 14: Pair identification bit assignment for the three pairs system

Pair Number	Zm1	Zm2	Zm3
1	$Z_{11} = 1$	$Z_{12} = 0$	$Z_{13} = 0$
2	$Z_{21} = 0$	$Z_{22} = 1$	$Z_{23} = 0$
3	$Z_{31} = 0$	$Z_{32} = 0$	$Z_{33} = 1$
HDSL transceiver at the NTU initial State	$Z_{m1} = 1$	$Z_{m2} = 1$	$Z_{m3} = 1$

Table 15: Pair identification bit assignment for the two pairs system

Pair Number	Zm1	Zm2
1	$Z_{11} = 1$	$Z_{12} = 0$
2	$Z_{21} = 0$	$Z_{22} = 1$
HDSL transceiver at the NTU initial State	$Z_{m1} = 1$	$Z_{m2} = 1$

5.6.7.2 Pair identification at the NTU

When the HDSL transceiver at the NTU achieves HDSL frame synchronization (LOSW = ZERO) the common circuitry starts to look at the Z-bits. If it detects a valid pattern according to table 14 or 15 respectively in six consecutive HDSL frames then the evaluation process is completed successfully and the outgoing pair identification Z-bits are set to equal the incoming Z-bits. HDSL transceivers at the NTU report to the HDSL framer their pair identification numbers, so that the correct data assignment can be achieved.

5.6.7.3 Pair identification at the LTU

When the HDSL transceiver at the LTU achieves HDSL frame synchronization (LOSW = ZERO) common circuitry starts to look at the Z-bits. Initially, it should detect that all the pair identification Z-bits are ONE. When the HDSL transceiver at the NTU achieves PID = ONE and reflects the Z-bits of the HDSL transceiver at the LTU, the common circuitry at the LTU will detect the pair identification number. When it finds its own valid pattern in six consecutive HDSL frames, then PID is set to ONE. This means that the NTU has acknowledged the pair identification set by the LTU. If the procedure cannot be finished successfully within the start-up supervision time of 28 s (56 s with regenerator), the HDSL link will be deactivated and a new start-up procedure is initiated.

The identification procedure introduces a delay of at least 12 frames (72 ms) between HDSL frame synchronism and transparent data transfer, because valid patterns are required for six consecutive frames at each side.

5.6.7.4 Redefinition of pair sequence

When unintended changes of the pair indication have occurred a redefinition of the byte sequence in the NTU is necessary. Table 16 for the three pairs system and table 17 for the two pairs system show all possibilities of modified byte sequences depending on the status of the received Z-bits.

Table 16: Z-bits set to ONE and corresponding core frame bytes

Active Z-bits			Byte # of Core frame in Pair 1	Byte # of Core frame in Pair 2	Byte # of Core frame in Pair 3
Z11	Z22	Z33	Byte 1	Byte 2	Byte 3
Z11	Z23	Z32	Byte 1	Byte 3	Byte 2
Z12	Z21	Z33	Byte 2	Byte 1	Byte 3
Z12	Z23	Z31	Byte 2	Byte 3	Byte 1
Z13	Z21	Z32	Byte 3	Byte 1	Byte 2
Z13	Z22	Z31	Byte 3	Byte 2	Byte 1

Table 17: Z-bits set to ONE and corresponding core frame bytes

Active Z-bits		Byte # of Core frame in Pair 1	Byte # of Core frame in Pair 2
Z11	Z22	Byte 1	Byte 2
Z12	Z21	Byte 2	Byte 1

The columns for "active Z-bits" indicate all possible and valid combinations of Z-bits set to ONE, where the first index behind Z relates to the pair allocation preset in the NTU and the second indicating which of the received Z-bits is set to ONE.

The columns for "Byte # of core frame" show how the received bytes have to be reallocated to build up the correct core frame, depending on the received combination of Z-bits. By linking the received data in the sequence byte 1, byte 2, byte 3,... the original core frame will be provided. After completion of the above mentioned procedure the NTU will insert the upstream core frame bytes into the HDSL frames in the same sequence.

5.7 Operation and maintenance

This subclause deals with operation and maintenance for transmission systems using HDSL technique. The O&M aspects for such systems are separated between the O&M functions of the HDSL core and those supported by the applications.

The following subclauses are divided with respect to the applications supported. Commands and responses of the system can either be transmitted through the application interfaces or via external O&M interfaces at maintenance reference points at the NTU and LTU as appropriate. Only the functionality of these O&M reference points will be specified in this ETR.

The support of partial operation in a failure situation and of fractional installation shall be possible as an option.

5.7.1 Functions at the LTU external O&M reference point

These O&M functions requested by an external O&M entity are originated within the O&M functional block (maintenance) at the LTU. The network elements addressed by these commands are identified in table 18.

Control functions at the external O&M interface:

Table 18: Control functions at the external O&M interface

Function	HDSL transceiver pair	Addressed network element (note 2)
Loopback control	all	LTU/REG
Loopback control of application frame	note 5	NTU (note 3)
Start-up control	all	LTU
Reset control	all	LTU/NTU/REG
CRC error reporting on each pair	all	LTU/NTU/REG (note 1)
Set corrupted CRC on each pair	all	LTU/NTU/REG
Response from each pair for corrupted CRC	all	LTU/NTU/REG
Request for noise margin on each pair	all	LTU/NTU/REG
Response for noise margin from each pair.	all	LTU/NTU/REG
Set configuration	note 5	LTU/NTU (interface block)
Read configuration	note 5	LTU/NTU (interface block)
Status report	note 6	LTU/NTU/REG
Function	HDSL transceiver pair	Addressed network element (note 2)
Excessive error ratio on each pair	all	LTU/NTU/REG (interface block) (note 4)
Identification of equipment	note 5	LTU/NTU/REG
Other failure indications	all	LTU/NTU/REG
NOTE 1: The calculation of these parameters is based on the CRC-6 procedure inside each subsystem.		
NOTE 2: The use of a regenerator is optional.		
NOTE 3: The location of the loopback of the application frame shall be as near as possible to the application interface. The loopback shall be complete.		
NOTE 4: The excessive error rate indication may be set if 150 errored frames out of 166 frames (1 second) are detected.		
NOTE 5: This function is transported transparently through the HDSL core. This note is not relevant if a regenerator is addressed.		
NOTE 6: The status report of network elements within the access digital section shall reflect the status of the HDSL core and the application.		

5.7.2 Functions at the NTU external O&M reference point

The NTU external O&M reference point may be implemented as an option and is not completely specified in this ETR.

Only the use of visible indications towards the customer are dealt with. The use of a data interface for reporting to/from the customer is not foreseen. Access to the operators TMN system via this reference point shall not be possible.

Examples of reporting towards the customer at the NTU may be:

- indication of power;
- indication of severe failures;
- indication of testing from the network side.

5.7.3 O&M messages and functions supported by the HDSL core

In this subclause messages are described which are conveyed inside the core frame for O&M purposes. In addition O&M functions related to these messages are defined which have to be located inside the HDSL core. These messages and functions are listed in table 19.

Table 19: O&M messages and functions supported by the HDSL core

Messages/functions	O&MCore	local	Core related function	available on each pair	HOH- bit	eoc message	addressed element		
							L T U	R E G	N T U
Reset control	→	*	y	n			*		
Start up control	→	*	y	n			*		
Active indication	←	*	y	n			*		
Loopback control for LTU line side	→	*	y	n			*		
Loopback control for REG	→		y	n		*		*	
Loopback control for application frame	→		n	n		*			*
CRC error detected at LTU	←	*	y	y			*		
CRC error detected at REG-R	←		y	y	rrbe			*	
CRC error detected at REG-C	←		y	y	rcbe			*	
CRC error detected at NTU	←		y	y	febe				*
Corrupted CRC at LTU	→	*	y	y			*		
Corrupted CRC at REG-R	→		y	y		*		*	
Corrupted CRC at REG-C	→		y	y		*		*	
Corrupted CRC at NTU	→		y	y		*			*
LOS/LFA at LTU line side (note 1)	←	*	y	y			*		
LOS/LFA at REG- R (note 1)	←		y	y				*	
LOS/LFA at REG- C (note 1)	←		y	y				*	
LOS/LFA at line side of NTU (note 1)	←		y	y					*
Pair identification	→		y	y	Z01-Z03		*		
Request noise margin LTU	→	*	y	y			*		
Request noise margin REG-R (REG-C)	→		y	y		*		*	
Request noise margin NTU	→		y	y		*			*
Noise margin LTU	←	*	y	y			*		
Noise margin REG-R (REG-C)	←		y	y		*		*	
Noise margin NTU	←		y	y		*			*
Request status REG	→		y	y		*		*	
Request status NTU	→		y	n		*			*
REG status (note 2)	←		y	y		*		*	
NTU status (note 2)	←		y	n		*			*
Read NTU configuration (note 3)	→		n	n		*			*
Write NTU configuration (note 3)	→		n	n		*			*
NTU configuration	←		n	n		*			*
Request equipment identification REG	→		y	y		*		*	
Request equipment identification NTU	→		n	n		*			*

(continued)

Table 19 (concluded): O&M messages and functions supported by the HDSL core

Messages/functions	O&MCore	local	Core related function	available on each pair	HOH- bit	eoc message	addressed element		
							L T U	R E G	N T U
Equipment identification REG	←		n	y		*		*	
Equipment identification NTU	←		n	n		*			*
internal alarm in NTU (note 4)	←		y	n	rta				*
internal alarm in REG (note 4)	←		y	y	rega		*		
LOS at the application interface of the LTU (note 5)	→		n	n	losd (LTU→NTU)	*			
LOS at the application interface of the NTU (note 5)	←		n	n	losd (NTU→LTU)				*
Bipolar violation at the application interface of the LTU (note 5)	→		n	n	bpv (LTU→NTU)	*			
Bipolar violation at the application interface of the NTU (note 5)	←		n	n	bpv (NTU→LTU)				*
NOTE 1:	LOS or LFA at the line side of the LTU, NTU or REG leads to a deactivation of the respective path after 2 seconds and therefore always results in an LOS message from the HDSL core to the O&M functional block in the LTU. The LTU O&M unit cannot determine, however, the location of the fault.								
NOTE 2:	The status register contains single bits representing the current status of the equipment. This information can be used to get detailed information, e. g. after receiving internal alarm bits rta or rega.								
NOTE 3:	The configuration register of the NTU contains dedicated bits which allow for remote configuration of the equipment by the LTU. Examples are transparent/non transparent mode, masking of alarms, equipment behaviour during fault conditions (e.g. transmitting of AIS).								
NOTE 4:	The internal alarm bits are used for signalling equipment internal failure conditions, which are not covered by separate indicator bits. Possible events are: - loss of internal clock sources; - max delay difference between pairs exceeded; - ROM/RAM test negative.								
NOTE 5:	The general need for this function has not been identified. It is left to the network operators to request this functions for particular applications.								

5.7.4 Power feeding related O&M functions

Table 20: Power feeding related functions

Function	O&M P	local	HOH-bits	eoc-messages	location		
					LTU	REG	NTU
NTU power source 1 failure	←		ps1				
NTU power source 2 failure	←		ps2				

5.7.5 Regenerator behaviour

5.7.5.1 Response to LOS/LFA

A regenerator shall respond to LOS/LFA. When LOS/LFA is recognised the behaviour of the REG shall be as follows:

Both sides of the REG shall be deactivated autonomously by the REG when LOS/LFA is detected on any HDSL line interface. The conditions for detecting LOS/LFA are described in subclause 5.6.

Note: This will finally result in deactivation of the subsystem after detection of LOS/LFA anywhere in the subsystem and both LTU and NTU will identify LOS/LFA for this subsystem. The LOS/LFA detection is a function of the individual HDSL transceivers.

5.7.5.2 Operation of loopback 1A

The activation of loopback 1A in any subsystem of the transceiver is initiated by the LTU by the appropriate eoc message as described in subclause 5.5. The loopback request may be started simultaneously with the beginning of the startup procedure or during an already active HDSL link.

In the first case the loopback request may be transmitted toward the REG as soon as signal S1 according to subclause 5.6 is transmitted in the direction LTU → NTU. After the eoc message has been detected in the REG the loopback is closed accordingly.

In the second case of an already active link the control unit in the REG closes the loop as soon as the eoc-message has been detected. The detailed procedure of reaching the synchronous loopback state is up to the vendor.

(It may be necessary to reset the REG-C transceiver, so that its equaliser and echo canceller coefficients may converge under the loopback conditions).

A successfully closed loopback may be detected in the LTU by evaluating the valid received Z-bits used for path identification.

The loopback is transparent, i.e. the looped back signal is also transmitted toward the NTU.

During an active loopback 1A the operation of the HDSL overhead bits shall be as follows:

- the eoc channel is not looped back but is fully operating between the LTU and the REG as described in subclause 5.5 as long as the messages sent by the LTU contain the REG address "10". When detecting any other address the REG inserts the "Hold State" message with its own address in the direction REG → LTU;
- all indicator bits, except the REG specific bits hrp, rega, rrbe and rcbe which are operating normally, are looped back.

To deactivate loopback 1A the LTU transmits the "Return to Normal" message together with the address "10" in the eoc channel. After detecting this message the REG control unit deactivates autonomously the REG-C transceiver and cancels the loopback operation.

If the HDSL link between the LTU and the REG is still active the REG control unit immediately starts to activate the link between the REG and the NTU as described in subclause 5.6.

The successful completion of the start-up procedure may be detected by the LTU by evaluating the Z-bits used for path identification.

5.8 Electrical characteristics of a single 2B1Q transceiver

5.8.1 General

This subclause describes the electrical characteristics of a single HDSL transceiver.

The electrical characteristics of a HDSL transceiver shall be such as to enable the performance requirements of the applications listed in clause 7 to be met. In addition, the following specific electrical characteristics are required.

Means should be provided in order to enable the testing of the electrical characteristics of a single 2B1Q transceiver.

5.8.2 Transmitter/Receiver impedance and return loss

The nominal driving point impedance at the line side of an HDSL transceiver shall be 135 ohms.

The minimum return loss with respect to 135 ohms, over a frequency band of 1 kHz to 1 MHz shall be as shown in figure 15 for 392 kbaud and in figure 16 for 584 kbaud systems.

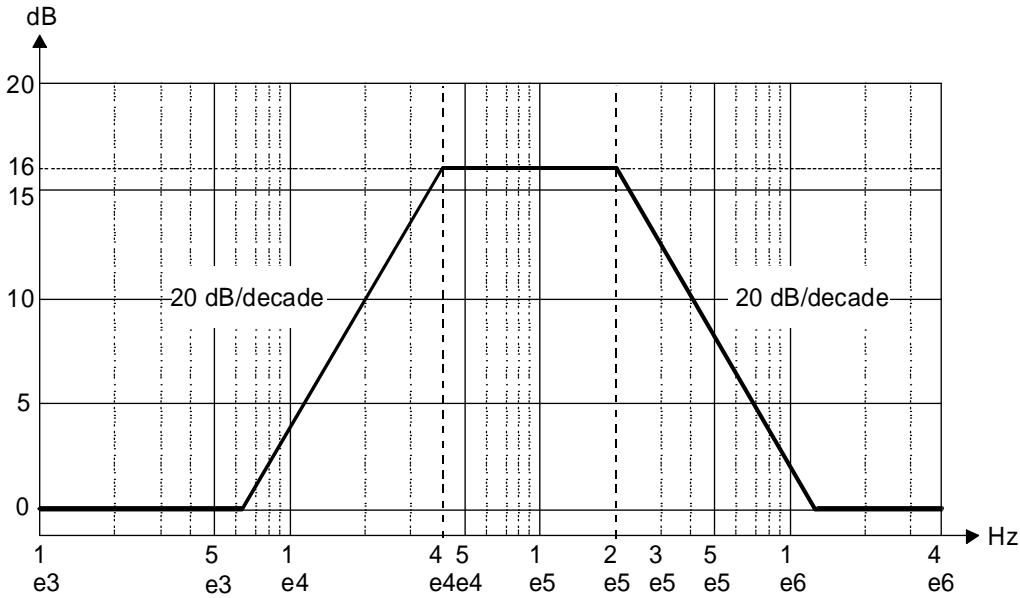


Figure 15: Minimum return loss of a 392 kbaud system

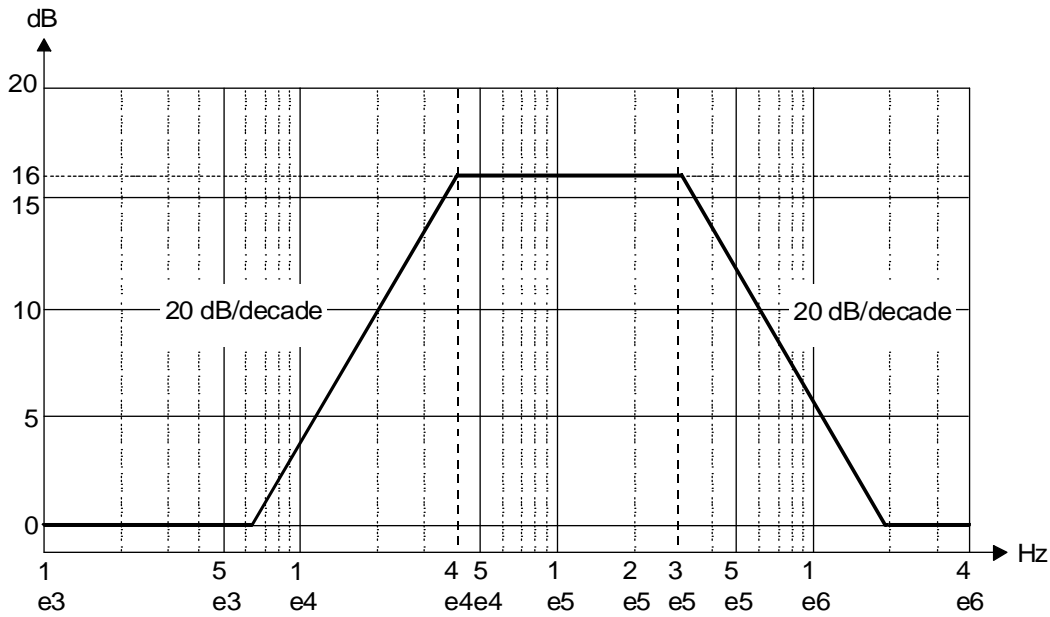


Figure 16: Minimum return loss of a 584 kbaud system

5.8.3 Transceiver reference clock

The reference clock shall be:

- for two pair 1 168 kHz ± 32 ppm;
- for three pair 784 kHz ± 32 ppm.

5.8.4 Transmitter output characteristics

Unless otherwise indicated, the following specification apply with a resistive load impedance corresponding to the nominal.

5.8.4.1 Pulse amplitude

The nominal peak of the largest pulse shall be 2,64 V.

5.8.4.2 Pulse shape

The transmitted pulse shall have the shape specified in figure 17.

The pulse mask for the four quaternary symbols shall be obtained by multiplying the normalised pulse mask shown in figure 17 by 2,64 V, 0,88 V, - 0,88 V or - 2,64 V.

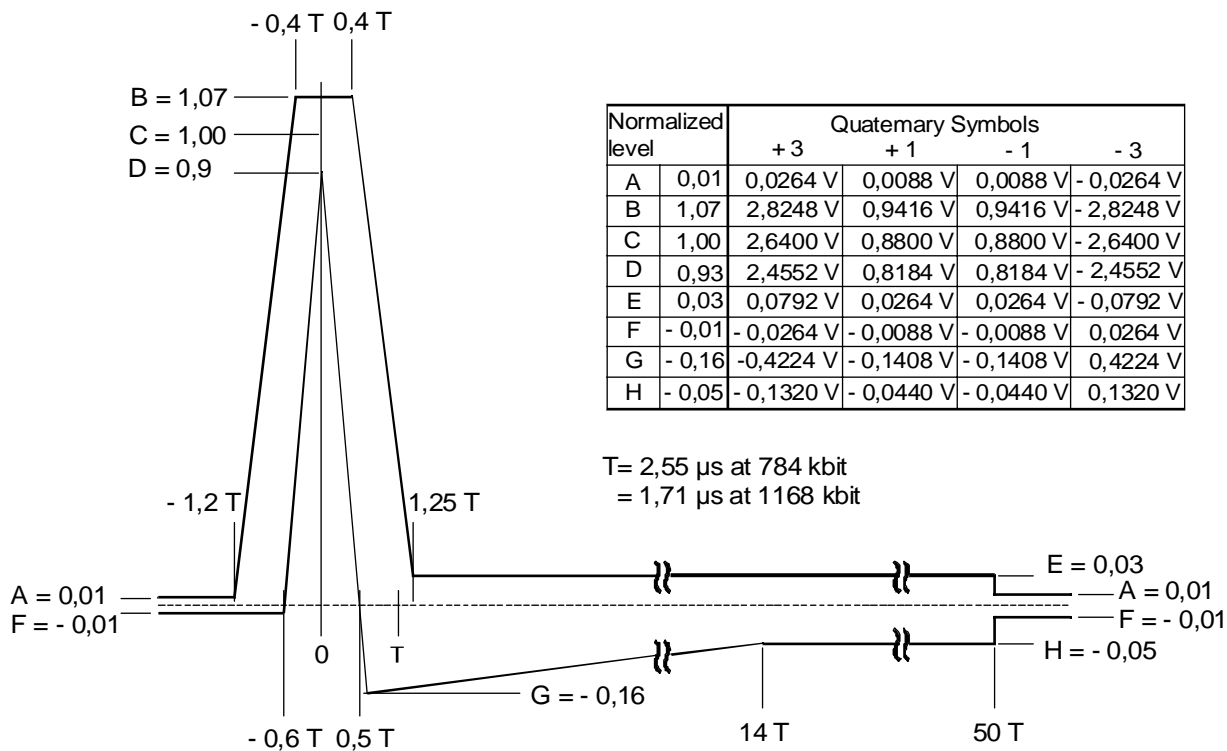


Figure 17: Transmit pulse; normalised pulse mask

5.8.4.3 Power spectral density

5.8.4.3.1 Power spectral density for 392 kbaud systems

The upper bound of the average power spectral density of the signal transmitted by the HDSL transmitter shall be as described in figure 18.

- 38 dBm/Hz from 0 Hz to 196 kHz

- 80 dB/decade fall from - 38 dBm/Hz at 196 kHz to - 118 dBm/Hz at 1,96 MHz - 118 dBm/Hz above 1,96 MHz

5.8.4.3.2 Power spectral density for 584 kbaud systems

The upper bound of the average power spectral density of the signal transmitted by the HDSL transmitter shall be as described in figure 19.

- 40 dBm/Hz from 0 Hz to 292 kHz.
- 80 dB/decade fall from - 40 dBm/Hz at 292 kHz to - 120 dBm/Hz at 2,92 MHz.
- 120 dBm/Hz above 2,92 MHz.

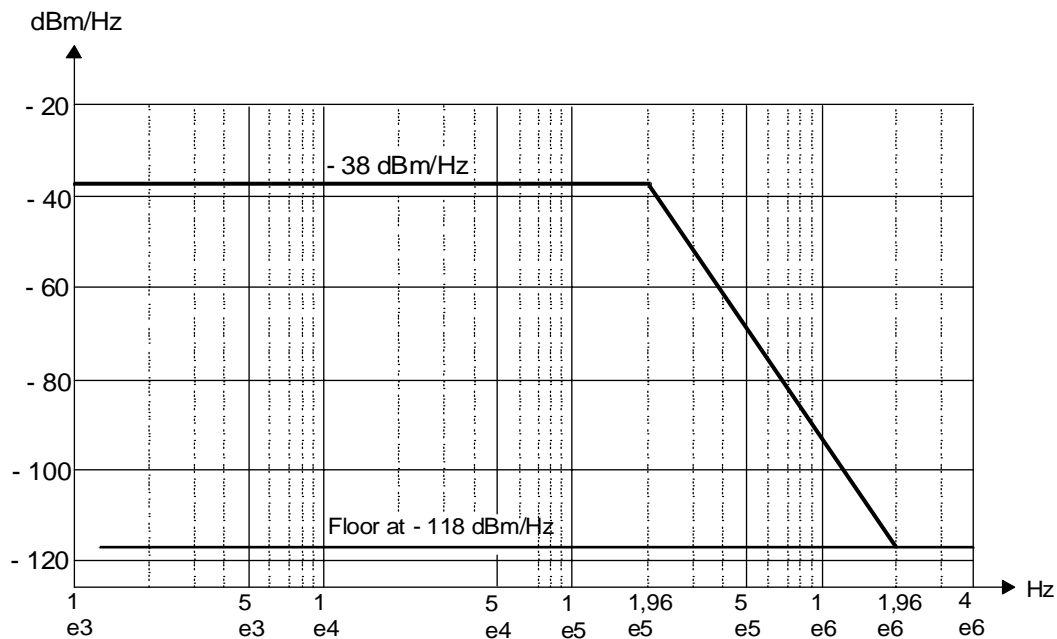


Figure 18: Upper bound of the average power spectral density of a 392 kbaud system

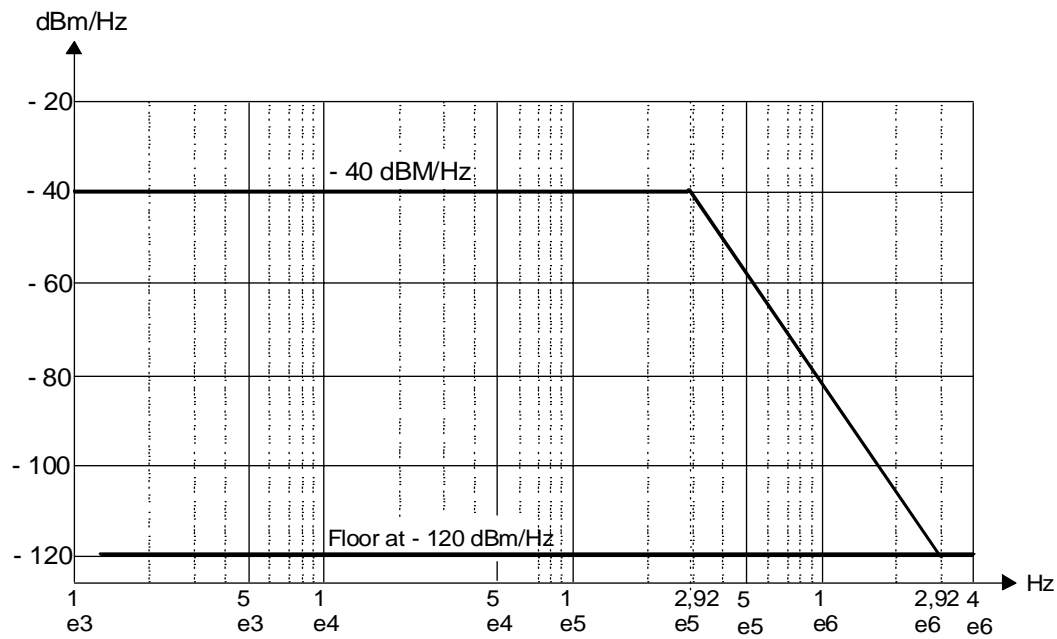


Figure 19: Upper bound of the average power spectral density of a 584 kbaud system

5.8.4.4 Total power

The average power of a signal consisting of a framed sequence of symbols with a frame word and equiprobable symbols in all other positions should be between 13,0 dBm and 14,0 dBm over the frequency band from 0 Hz to 784 kHz for 392 kbaud systems and from 0 Hz to 1 168 kHz for 584 kbaud systems.

5.8.5 Unbalance about earth

5.8.5.1 Longitudinal conversion loss

The longitudinal conversion loss is given by:

$$LCL = 20 \log (e_l/e_m) \text{ [dB]},$$

where e_l is the applied longitudinal voltage referenced to the building ground,

and e_m is the resultant metallic voltage appearing across a 135 ohms termination.

The longitudinal conversion loss of the system shall meet the requirement shown in figure 20 for a 392 kbaud system and in figure 21 for a 584 kbaud system. This requirement ensures that the overall LCL is not significantly worse than that of the DLLs alone.

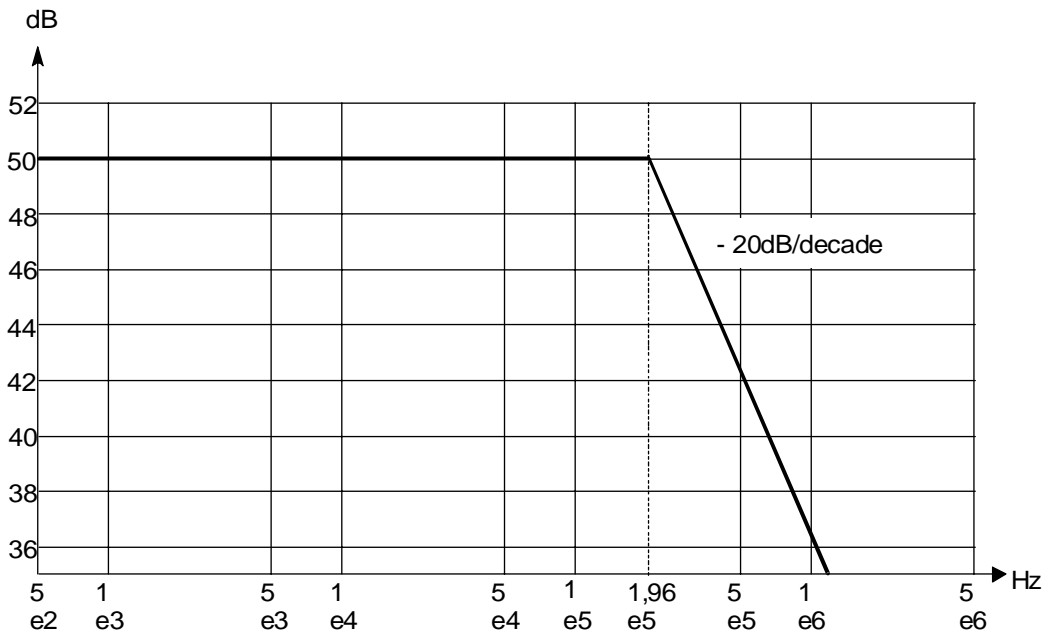


Figure 20: Minimum longitudinal conversion loss for a 392 kbaud system

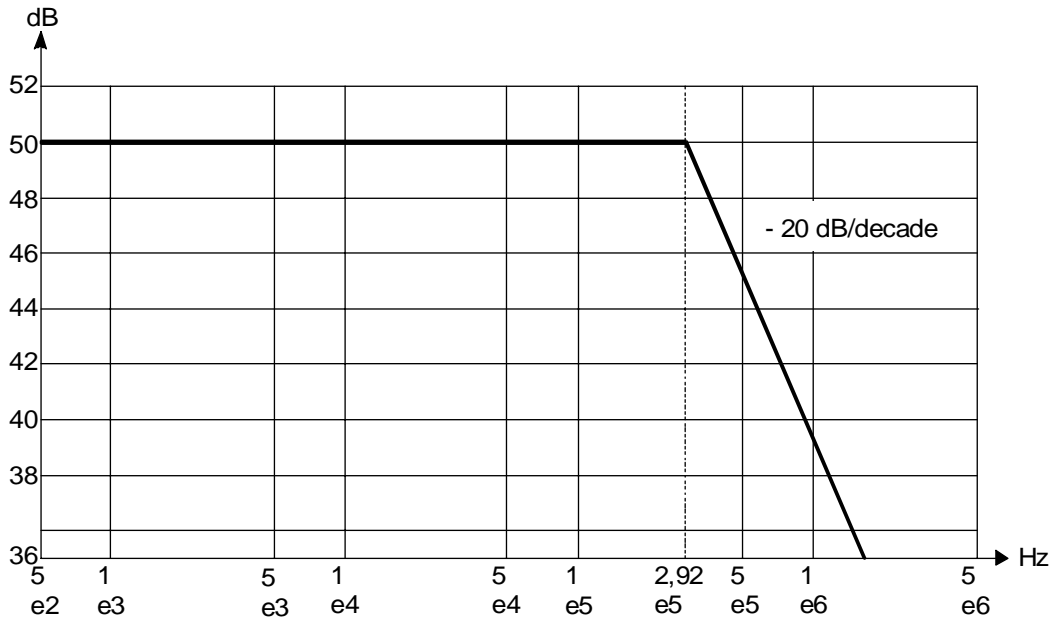


Figure 21: Minimum longitudinal conversion loss for a 584 kbaud system

Figure 22 defines a measurement method for longitudinal conversion loss. For direct use of this configuration, measurement should be performed with the IUT powered up but inactive (no transmitted signal; driving 0 V).

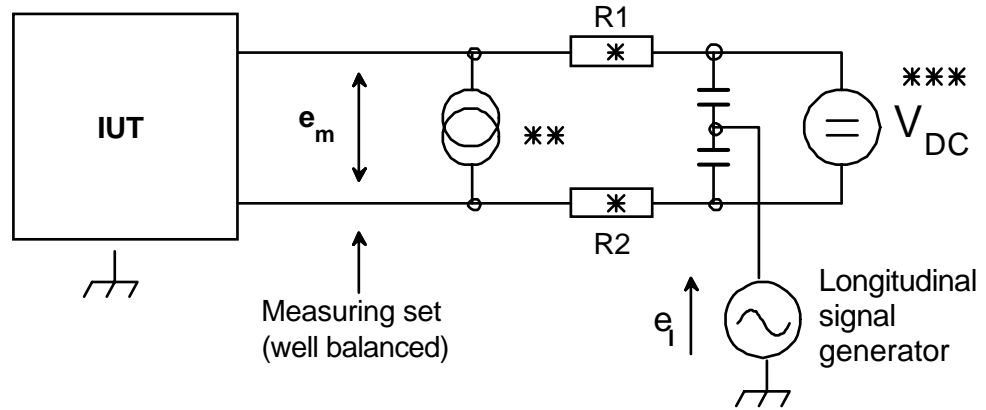
5.8.5.2 Longitudinal output voltage

The longitudinal component of the output signal shall have an rms voltage, in any 4 kHz equivalent bandwidth averaged in any second period, < - 50 dBV over the frequency range 100 Hz to 400 kHz. Compliance with this limitation is required with a longitudinal termination having an impedance of 100 Ohms in series with 0,15 μF nominal.

NOTE: The EMC requirements of subclause 7.4 also need to be met.

Figure 23 defines a measurement method for longitudinal output voltage. For direct use of this test configuration, the IUT should be able to generate a signal in the absence of a signal from the far end.

The ground reference for this measurements shall be the building ground.



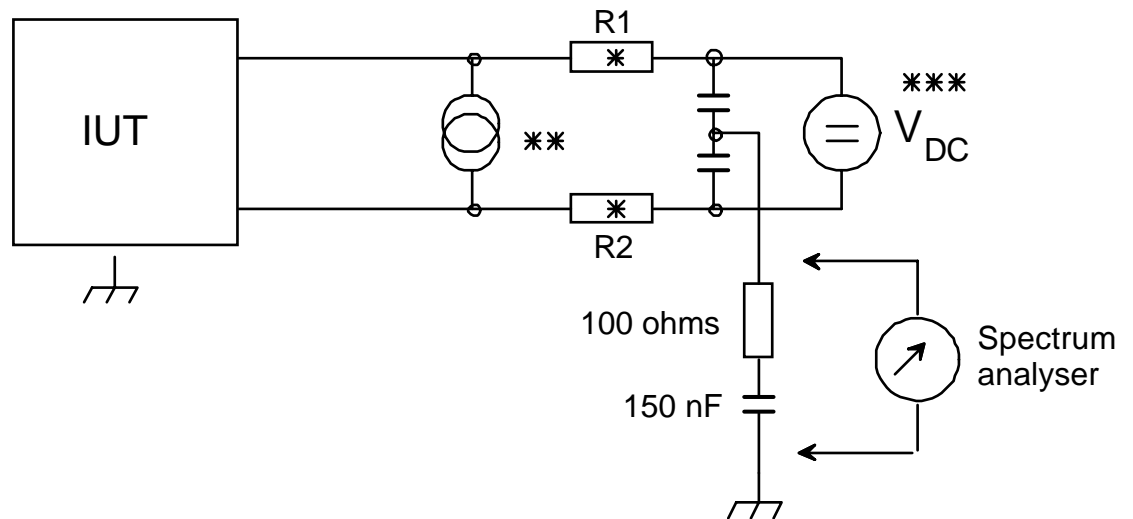
* These resistors have to be matched: $R1 = R2 = 135/2$ ohms and $R1/R2 = 1 \pm 0,1 \%$.

** For LTU test only.

*** For NTU test only.

NOTE: During regenerator test (where required) each wire on the side which is not under test has to be connected to ground by a terminating impedance having the value of $135/2$ ohms in series with a capacitance of $0,33 \mu\text{F}$.

Figure 22: Measurement method for longitudinal conversion loss



* These resistors have to be matched: $R1 = R2 = 135/2$ ohms and $R1/R2 = 1 \pm 0,1 \%$.

** For LTU test only.

*** For NTU test only.

NOTE: During regenerator test (where required) each wire on the side which is not under test has to be connected to ground by a terminating impedance having the value of $135/2$ ohms in series with a capacitance of $0,33 \mu\text{F}$.

Figure 23: Measurement method for longitudinal output voltage

5.9 Performance of individual HDSL Transceivers

5.9.1 Performance requirements

Performance limits for the overall system are defined in clause 7. The performance of the individual HDSL transceivers shall be such that these overall performance limits are met. As the binary signal of the individual transceivers is not available at an external interface for testing, it is not considered feasible to test the performance of the individual HDSL transceivers. For the purpose of conformance, each HDSL system is required to have an individual performance such that the overall application performance requirements defined in clause 7 for the appropriate application is met.

5.9.2 DLL physical models (test loops)

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in clause 7.

5.9.3 Jitter and wander

5.9.3.1 General

The jitter and performance limits specified in clause 7 shall be supported by the jitter limits of the individual HDSL transmission systems. However, due to the bi-directional transmission on the two-wire line and due to severe intersymbol interference no well defined signal transitions are available on the two-wire signal. It will therefore be necessary to provide clock interfaces to enable the following requirements to be tested. The jitter limits given below need to be satisfied regardless of the length of the local line and the inclusion of regenerators, provided that they are covered by the transmission media characteristics of subclause 5.2. The limits shall be met regardless of the transmitted signal. In this subclause, jitter is specified in terms of unit intervals (UI) of the nominal line baud rate which is 392 kbaud (2,551µs) for the three pairs system and 584 kbaud (1,7123 µs) for the two pairs system.

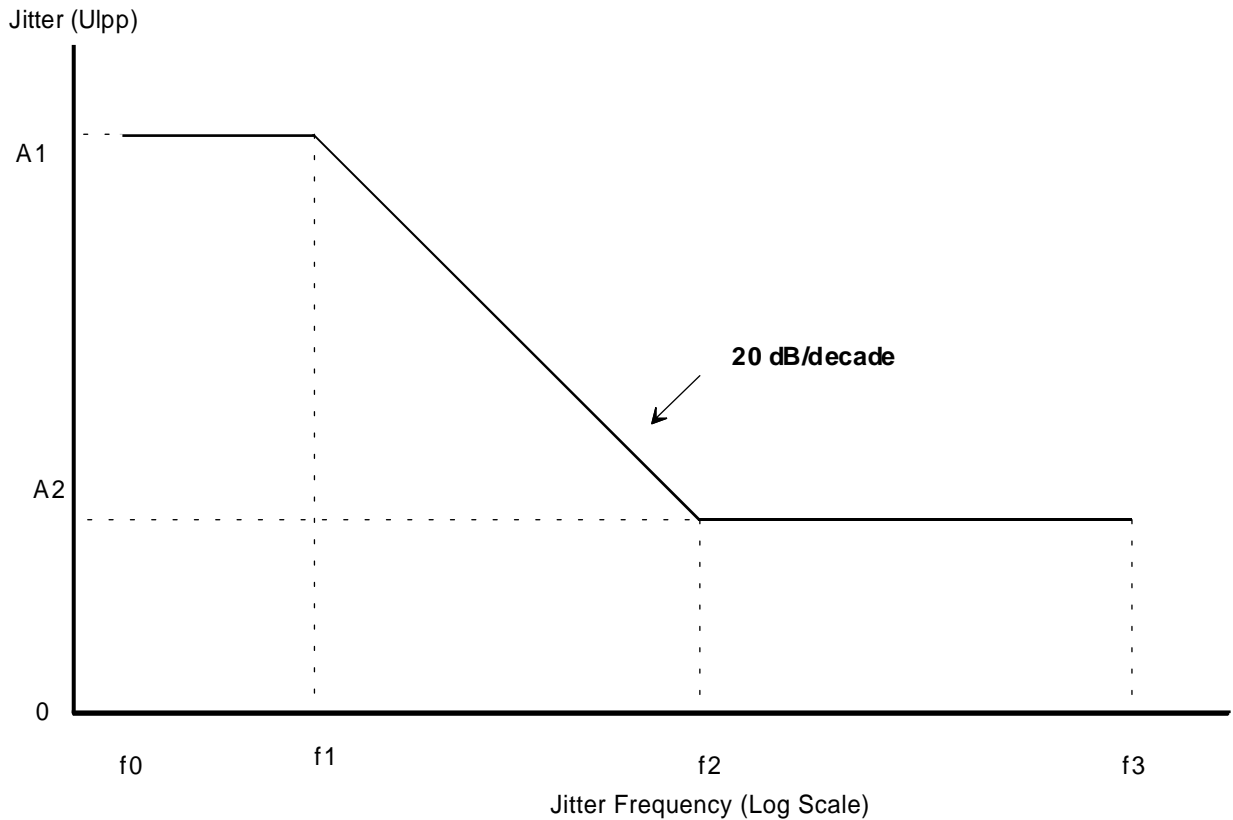
NOTE: Manufacturers are asked to report to the responsible ETSI STC if they find that it is not feasible to meet these requirements.

5.9.3.2 Input jitter tolerance at the HDSL transceiver at the NTU

The NTU shall meet the performance objectives specified in clause 7 with wander/jitter sinusoidal characteristics as indicated in figure 24, and with values as defined in table 21 below for single jitter frequencies in the range of 0,1 Hz to 100 kHz superimposed on the test clock source, and with the received signal baud rate in the range of ± 32 ppm.

Table 21: Values for wander/jitter characteristics

A1	A2	f0	f1	f2	f3
0,15 UIpp	0,015 UIpp	0,1 Hz	0,5 Hz	5 Hz	100 kHz



NOTE: Unit Interval (UI) = 2 551 nsec for 392 kbaud systems.
Unit Interval (UI) = 1 712 nsec for 584 kbaud systems.

Figure 24: Range of permissible sinusoidal input jitter

5.9.3.3 Output jitter limitations at the HDSL transceiver at the NTU

The jitter on the transmitted 2B1Q signal of the NTU towards the LTU in the absence of input jitter shall be less than A2 when measured with a band pass filter having a 20 dB/decade roll off with cut off frequencies at f2 and f3 .

The maximum (peak) departure of the phase of the output signal from its average phase measured over 1/f0 seconds shall not exceed A1.

5.9.3.4 Input jitter tolerance at the HDSL transceiver at the LTU

The LTU shall meet the performance objectives specified in clause 7 with wander/jitter of A2 for single jitter frequencies in the range of f0 to f3 superimposed on the test clock source, and with the signal baud rate in the range ± 32 ppm.

5.9.3.5 Output jitter limitation of the HDSL transceiver at the LTU

The jitter on the transmitted 2B1Q signal of the LTU towards the NTU shall be less than A2 when measured with a band pass filter having a 20 dB/decade roll off with cut off frequencies at f2 and f3.

6 Common circuitry specification

6.1 Delay difference buffer

In order to compensate for any difference in total transmission time of the HDSL frames on different pairs, due to the pair differences described in subclause 5.2.4.2, as well as to delays due to signal processing in the HDSL transceivers in the LTU, NTU and possible REG, a delay difference buffer shall be implemented in the common circuitry. The function of this delay difference buffer is to align the HDSL frames so that the core frames can be correctly reassembled. This buffer should be capable of absorbing a maximum delay difference $D_3 = 60 \mu\text{s}$.

7 Application specific requirements

7.1 Application specific requirements for ISDN PRA

7.1.1 Mapping of 2 048 kbit/s to HDSL

As described in subclause 5.4 (Frame Structure) the 2 048 kbit/s application data has to be mapped into a core frame with 144 bytes and 500 μs length. The data at the application interfaces T and V3 (see figures 1 and 2 and ETS 300 233 [4]) contain only 128 bytes per 500 μs and the unused bytes have to be filled up with 16 stuffing bytes, called Y- and R-bytes and containing all binary ONES, as shown in figures 6.a to 6.b. The use of the stuffing bytes for other purposes e.g. forward error correction is for further study. The bits Z_{m9} to Z_{m48} are unused and set to ONE. To achieve total decoupling of the HDSL from the core frame and a minimum signal delay the location of timeslot 0 within the core frame is arbitrary. This means that, with exception of the location occupied by the Y- and R-stuffing bytes, the first bit of timeslot 0 may occur anywhere in the frame. In addition loss of frame alignment at the application interfaces T and V3 does not lead to a resynchronization of the HDSL transceivers, because the core frame is transmitted totally transparent through the HDSL transceiver systems.

7.1.2 Mapping of HDSL maintenance functions to the interface

The application dependant maintenance functions, the definition of the Function Elements (FE) for the signalling across the application interfaces and the coding of the FE, using the E-, A-, Sa5- and Sa6-bits of timeslot 0 in the application frame, are defined in ETS 300 233 [4], clause 9 for the V3 reference point and in ETS 300 011 [2] table 1 for the T reference point. All these functions have to be performed in the interface blocks according to figure 1 by evaluating frame alignment, signal patterns and CRC-4 error detection.

For the detection of the states "Normal operation of the DS", "LOS/LFA at line side of the NT1" and "LOS at the line side of the LT" the maintenance functions "LOS/LFA at line side of the NTU" and "Active indication (INDR)", which are created by the common core at the NTU, respectively "LOS/LFA at LTU line side" and Active indication (INDC)", which are created by the common core at the LTU, have to be taken into account.

The access digital section shall be considered operational when all the transceiver pairs have indicated completion of the activation procedure and correct pair identification has been achieved in the core frame, as described in subclause 5.6, and no further failure condition is detected. If one of the transceiver pairs is indicating non-operational condition or incorrect pair identification, the access digital section shall be considered non-operational.

The only maintenance function of this application which has to be achieved by the common core is "Loopback 1 command" as described in table 22.

Table 22: Loopback

Function	Localisation	Controlled by	Requested via
Loopback 1	As near as possible to the line	O&M in block M in LTU, note	V3 interface
NOTE:	When loopback 1 is activated a complete and transparent loopback shall be activated in all HDSL transceivers at the line side of the LTU. These loopbacks are controlled by an O&M function inside functional block M in LTU.		

7.1.3 Performance

7.1.3.1 Performance specification (ISDN PRA Application)

The overall performance shall be such that the performance limits given in ITU-T Recommendation G.826 [13] can be met. For the purpose of conformance, an HDSL transmission system is required to meet the specific laboratory performance test that are defined in the following subclauses.

The performance requirements have been specified so that the HDSL transceivers are tolerant to NEXT, impulsive noise and shaped noise, and not optimised for only one operating condition.

The oneway signal transfer delay, which is the mean value of the delay time in both directions of transmission between the T and V3 reference points as defined in ETS 300 233 [4], shall not exceed 1250 μ s, the allocation shall be as follows:

- LTU - $\leq 450 \mu$ s;
- NTU - $\leq 450 \mu$ s;
- REG - $\leq 200 \mu$ s;
- Line - $\leq 150 \mu$ s.

7.1.3.2 Clock specification for external interfaces

7.1.3.2.1 NTU clock tolerance

The tolerance of the free running NTU clock is 2 048 kHz \pm 50 ppm.

7.1.3.2.2 LTU clock tolerance

The tolerance of the clock provided at the LTU is 2 048 kHz \pm 50 ppm.

7.1.3.2.3 Jitter and wander specifications

7.1.3.2.3.1 Tolerance to input jitter and wander

The required tolerance to input jitter and wander are defined in terms of the amplitude and frequency of sinusoidal jitter which, when modulating a $2^{15}-1$ pseudo-random test pattern, should not cause any significant degradation in the operation of the equipment. This test method is used for convenience of testing and is not, in itself, intended to be representative of the type of jitter to be found in practice.

The interfaces should be able to tolerate input jitter and wander having an amplitude-frequency relationship defined in figure 25 and with the limits shown in tables 23 and 24.

Jitter (UI p p)

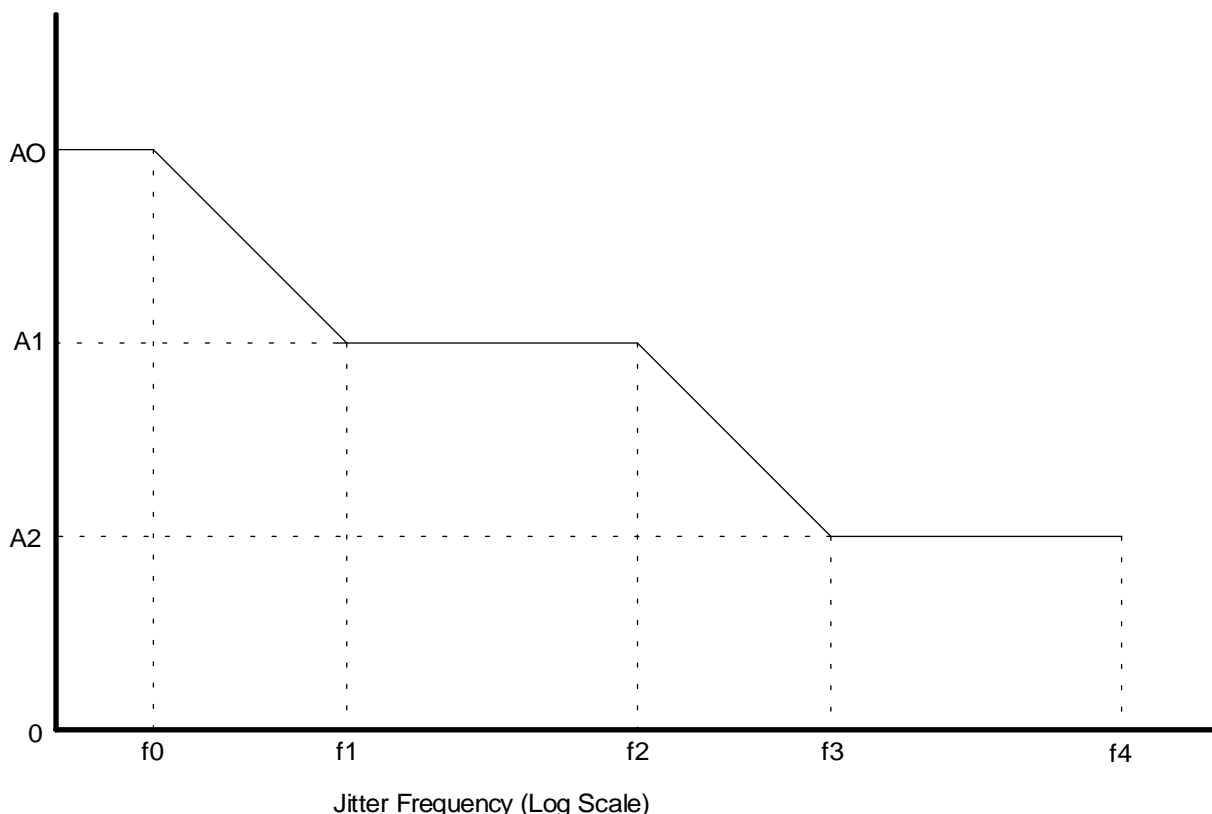


Figure 25: Lower limit of maximum tolerable input jitter and wander

Table 23: Parameter values for input jitter and wander tolerance at the T interface

T Interface	Peak-to-peak amplitude			Frequency				
Parameter:	A0	A1	A2	f0	f1	f2	f3	f4
Value	20,5	1,0	0,2	12	20	3 600	18	100
Units	U _{Ipp}	U _{Ipp}	U _{Ipp}	μHz	Hz	Hz	kHz	kHz
NOTE 1:	U _{Ipp} = Unit Interval peak-peak. 1 U _{Ipp} = 1/2 048 kHz= 488 ns for the ISDN PRA application.							
NOTE 2:	These values are taken from ITU-T Recommendation I.431 [14] in accordance with ETS 300 011 [2] as required by ETS 300 233 [4].							

Table 24: Parameter values for input jitter and wander tolerance at the V3 interface

V3 Interface	Peak-to-peak amplitude			Frequency				
Parameter:	A0	A1	A2	f0	f1	f2	f3	f4
Value	36,9	1,5	0,2	12	20	2400	18	100
Units	U _{Ipp}	U _{Ipp}	U _{Ipp}	μHz	Hz	Hz	kHz	kHz
NOTE 1:	U _{Ipp} = Unit Interval peak-peak. 1 U _{Ipp} = 1/2 048 kHz= 488 ns for ISDN PRA application.							
NOTE 2:	These values are taken from ITU-T Recommendation G.823 [12] as required by ETS 300 233 [4].							
NOTE 3:	No jitter reducer is required at the V3 interface.							

7.1.3.2.3.2 Output jitter

The maximum permitted values of output jitter are specified in table 25.

The maximum output jitter in the absence of input jitter for a $2^{15}-1$ pseudorandom test pattern is measured with the jitter detector. B1 is measured after a bandpass filter with a lower cut-off frequency of f_1 and an upper cutoff of f_4 following the detector. B2 is measured similarly, but with the detector followed by the bandpass filter with a lower cut-off frequency of f_3 and an upper cut-off frequency of f_4 .

Table 25: Maximum permitted values of output jitter

	Maximum permissible jitter		Measurement filter parameters		
	B1= (f1-f4)	B2= (f3-f4)	f1	f3	f4
At T interface	1,1	0,11	20	400	100
At V3 Interface	1,5	0,2	20	18 000	100
	U _{lpp}	U _{lpp}	Hz	Hz	kHz
NOTE:	The values for the T interface are taken from ETS 300 011 [2] as required by in ETS 300 233 [4].				
	The values for the V3 interface are taken from ITU-T Recommendation G.823 [12].				

7.1.3.3 Laboratory performance measurements

7.1.3.3.1 General

The laboratory performance measurement of a particular HDSL transmission system requires the following preparations:

- definition of a number of DLL models to represent physical and electrical characteristics encountered in local line distribution networks;
- simulation of the electrical environment caused by impulsive noise and finite crosstalk coupling loss to other pairs in the same cable;
- specification of laboratory performance tests to verify that the performance limits referred to in subclause 7.1.3.1 will be met.

Some representative models of DLLs (test loops) for evaluating the performance of transceivers for transmission systems are defined in figure 26, the basic test cable characteristics are given in annex A.

7.1.3.3.2 Test configuration

It is assumed that the access digital section shall be required to operate either over two pairs, with each pair being connected to an individual 1 168 kbit/s 2B1Q duplex HDSL transmission system or over three pairs, with each pair being connected to an individual 784 kbit/s 2B1Q duplex HDSL transmission system. Performance requirements should relate to the integrity of the data at the application interface when individual transmission systems are subjected to the application of synthesised impairments. In this way access is not required to the raw data transported by the individual transceivers. Data errors can therefore be measured at the application interface, avoiding the need for test access to the individual data channels.

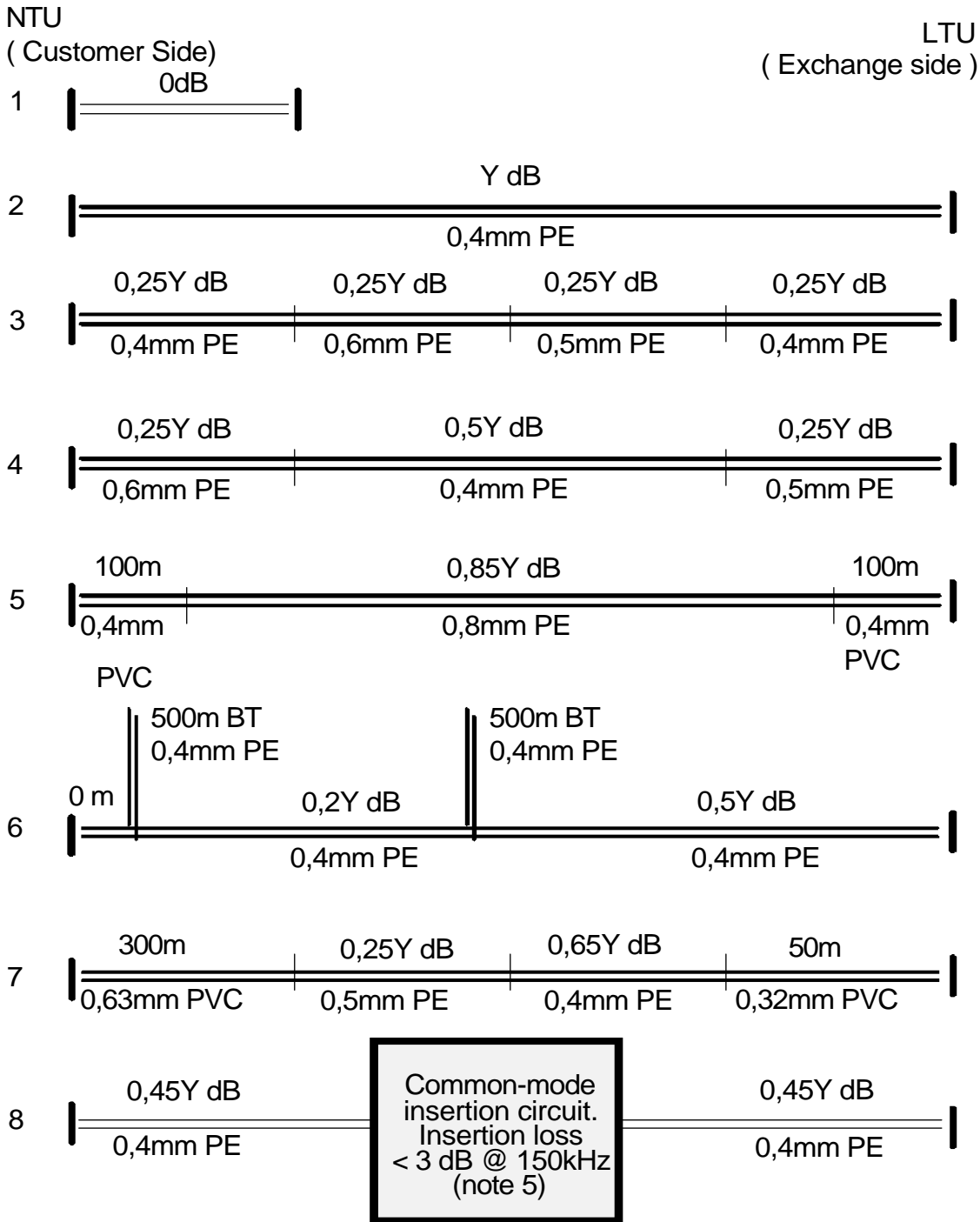
A representative test arrangement is shown in figure 28.

The Bit Error Ratio Test Set (BERTS) applies a 2 048 kbit/s $2^{15}-1$ Pseudo Random Bit Sequence (PRBS) test signal to the transmitter in the direction under test. Impairments (when required by the test) are injected at the input of the appropriate HDSL transceivers at the receiver end of the path, and the reconstructed data is then returned to the BERTS. The transmitter in the opposing direction shall be fed with a similar PRBS signal, although the reconstructed signal in this path need not be monitored.

The test performance of the HDSL transceiver shall be such that the Bit Error Ratio (BER) on the disturbed system is better than $1/2 \times 10^{-7}$ for the HDSL two pairs system and $1/3 \times 10^{-7}$ for the HDSL three pairs system while transmitting a pseudo random data sequence. The BER should be measured after at least 10^9 bits have been transmitted.

The tests are carried out with zero margin, that is, with no additional attenuation added to the test pairs. It is expected that network operators will calculate their own margins for planning purposes based on a knowledge of the relationship between this standard test set and their cable characteristics.

It is considered sufficient to use representative combination of test pairs for performance testing. The test pairs should be adjusted to achieve the sinewave insertion loss of the individual sections when measured at 150 kHz. (It is not considered reliable to measure the overall sinewave attenuation, as impedance discontinuities can result in non-linear effects in the frequency response of some pairs).



NOTE 1: The value for Y (insertion loss) is to be found in tables 26 and 27.

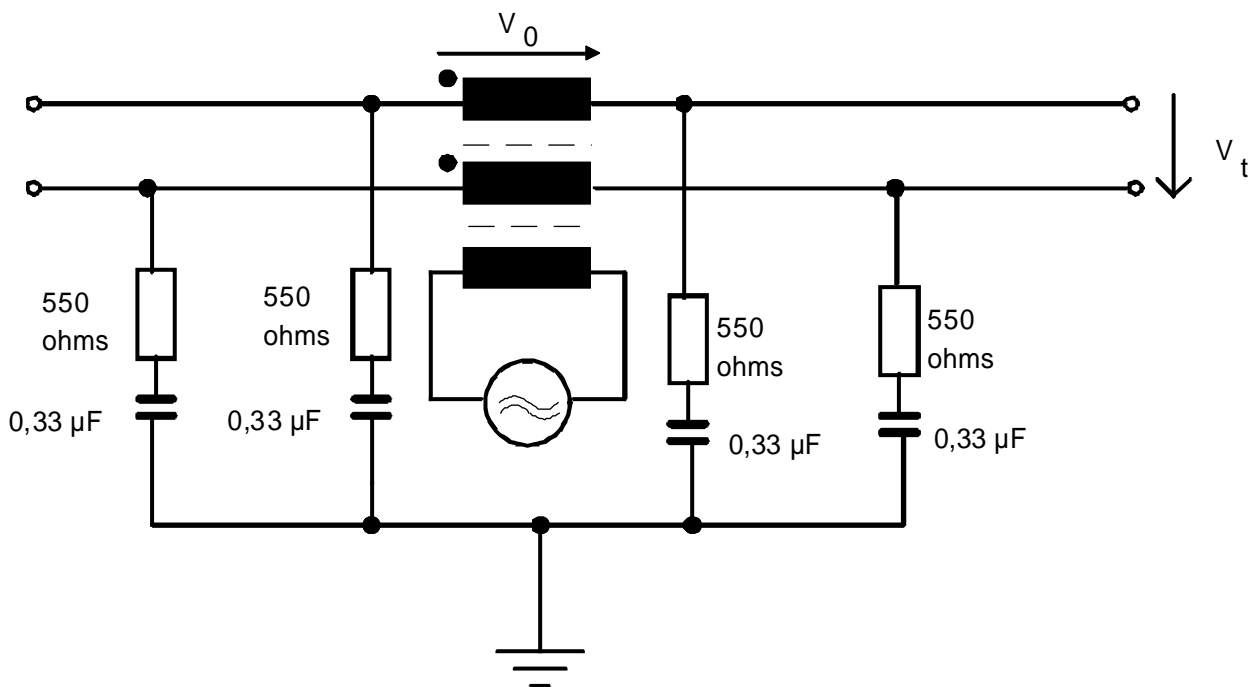
NOTE 2: Due to mismatches and Bridged Taps (BTs) the total DLL attenuation differs from the sum of the attenuation of the parts. Annex A provides theoretical values for the transmission parameters of the loops above.

NOTE 3: Attenuation of separate sections is measured with a 135 ohms termination.

NOTE 4: These test loops and artificial cable parameters include worst case examples as well as those more typical of a local network. They are chosen to provide the wide range of different echoes and distortions which may occur in European networks.

NOTE 5: See figure 27.

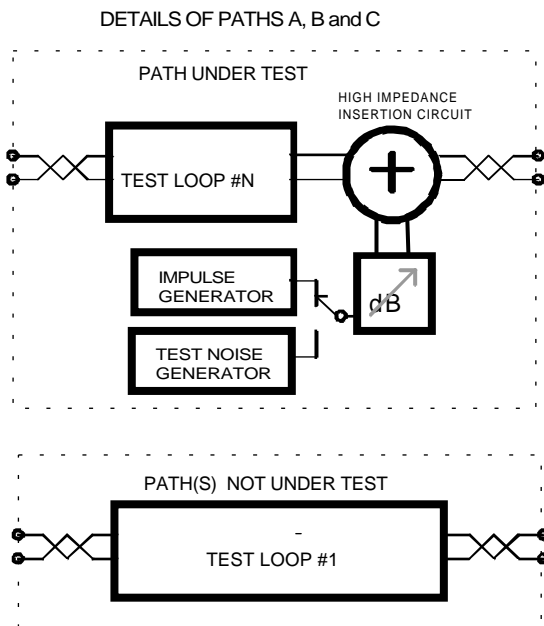
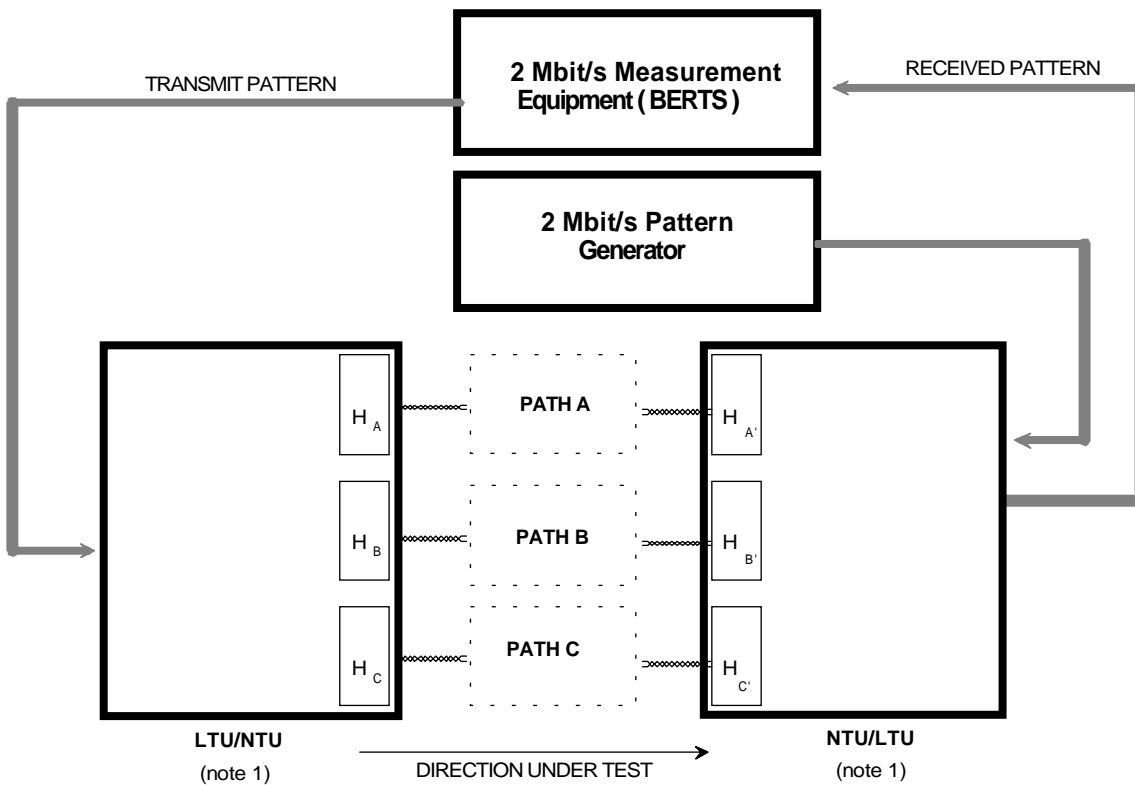
Figure 26: DLL physical models for laboratory testing



NOTE 1: The minimum return loss of the terminated test insertion circuit shall be better than the minimum return loss of the system.

NOTE 2: The minimum longitudinal conversion loss $[20 \log (V_o/V_t)]$ of the test insertion circuit shall be better than 80 dB at 50 Hz, decreasing with 20 dB/decade up to 1 kHz (above 1 kHz transversal voltage is negligible compared with the test noise).

Figure 27: Common mode insertion test circuit



NOTE 1: Some tests are carried out in both the forward and reverse direction.

NOTE 2: A fully equipped access digital section consists of two or three HDSL transceiver systems.

Figure 28: Configuration for performance tests of an access digital section

Two distinct classes of added disturbance are injected: Test noise (specified in subclause 7.1.3.3.3) and Impulses (defined in subclause 7.1.3.3.4). A further test (specified in subclause 7.1.3.3.5) tests the common mode rejection capability of the system under test.

The proposed test sequence for the HDSL two pairs system is shown in table 26 and for the three pairs system in table 27.

Table 26: Test sequence for the two pairs system

N	Path A	Path B	Direction	Comment
1	#1	#1*	FORWARD	Y = 0 dB; N2 = 30 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
2	#2	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
3	#1*	#2	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
4	#3	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
5	#1*	#3	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
6	#3	#1*	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
7	#1*	#3	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
8	#4	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
9	#1*	#4	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
10	#4	#1*	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
11	#1*	#4	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
12	#5	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
13	#1*	#5	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
14	#5	#1*	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
15	#1*	#5	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
16	#6	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
17	#1*	#6	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
18	#6	#1*	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
19	#1*	#6	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
20	#7	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
21	#1*	#7	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
22	#7	#1*	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
23	#1*	#7	REVERSE	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
24	#8	#1*	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
25	#1*	#8	FORWARD	Y = 27 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
26	note 3	note 3	FORWARD/ REVERSE	Y = 17 dB; N2 = 30 $\mu\text{V}/\sqrt{\text{Hz}}$; Worst path from above tests
27	#2	#1*	FORWARD	Y = 27 dB; Impulse test as described in subclause 7.1.3.3.4

(continued)

Table 26 (concluded): Test sequence for the two pairs system

N	Path A	Path B	Direction	Comment
28	#1*	#2	FORWARD	Y = 27 dB; Impulse test as described in subclause 7.1.3.3.4
29	Note 3	Note 3	FORWARD/ REVERSE	Y = 30 dB; no added impairment; Worst path from above tests
30			FORWARD	Micro interruption test as described in subclause 7.1.3.3.6
NOTE 1:	Loop #1, #2, #3,... refer to test loops as defined in figure 26.			
NOTE 2:	The path not being tested shall be connected with a dummy loop (*), normally loop #1 (Zero Loop).			
NOTE 3:	The noise is added to the worst path from the previous tests, with a dummy loop for the remaining path. If there are no errors, then loop #2 on path A is taken as default, with dummy loop on path B.			

Table 27: Test sequence for the three pairs system

N	Path A	Path B	Path C	Direction	Comment
1	#1	#1*	#1*	FORWARD	Y = 0 dB; N2=30 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
2	#2	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
3	#1*	#2	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
4	#1*	#1*	#2	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
5	#3	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
6	#1*	#3	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
7	#1*	#1*	#3	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
8	#3	#1*	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
9	#1*	#3	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
10	#1*	#1*	#3	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
11	#4	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
12	#1*	#4	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
13	#1*	#1*	#4	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
14	#4	#1*	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
15	#1*	#4	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
16	#1*	#1*	#4	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
17	#5	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
18	#1*	#5	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
19	#1*	#1*	#5	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
20	#6	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
21	#1*	#6	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
22	#1*	#1*	#6	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
23	#6	#1*	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
24	#1*	#6	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
25	#1*	#1*	#6	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
26	#7	#1*	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
27	#1*	#7	#1*	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3

(continued)

Table 27 (concluded): Test sequence for the three pairs system

N	Path A	Path B	Path C	Direction	Comment
28	#1*	#1*	#7	FORWARD	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
29	#7	#1*	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
30	#1*	#7	#1*	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
31	#1*	#1*	#7	REVERSE	Y = 31 dB; N2=10 $\mu\text{V}/\sqrt{\text{Hz}}$; Tests as in 7.1.3.3.3
32	#8	#1*	#1*	FORWARD	Y = 31 dB. Tests as 7.1.3.3.5
33	#1*	#8	#1*	FORWARD	Y = 31 dB. Tests as 7.1.3.3.5
34	#1*	#1*	#8	FORWARD	Y = 31 dB. Tests as 7.1.3.3.5
35	NOTE 3	NOTE 3	NOTE 3	FORWARD/ REVERSE	Y = 21 dB. N2 = 30 $\mu\text{V}/\sqrt{\text{Hz}}$; Worst path from above tests
36	#2	#1*	#1*	FORWARD	Y = 31 dB. Impulse test of 7.1.3.3.4
37	#1*	#2	#1*	FORWARD	Y = 31 dB. Impulse test of 7.1.3.3.4
38	#1*	#1*	#2	FORWARD	Y = 31 dB. Impulse test of 7.1.3.3.4
39	NOTE 3	NOTE 3	NOTE 3	FORWARD/ REVERSE	Y = 34 dB. No added impairment. Worst path.
40				FORWARD	Micro interruption test - see 7.1.3.3.6

NOTE 1: Loop #1, #2, #3,... refer to test loops as defined in figure 26.
 NOTE 2: The path not being tested shall be connected with a dummy loop (*), normally loop #1 (Zero Loop).
 NOTE 3: The noise is added to the worst path from the previous tests, with dummy loops for the remaining two paths. If there are no errors, then loop #2 on path A is taken as default, with dummy loops on path B and path C.

7.1.3.3.3 Test procedure with shaped noise source

The noise in local network lines can be best represented by an artificial noise source as described below. This artificial noise offers a worst case test condition for intersystem and intrasystem crosstalk, as well as external impulsive noise effects, for all presently known disturbers.

The shaped noise source is defined as a sawtooth function superimposed with an artificial noise with an extremely low crest factor. The resulting spectral density is shown in figure 29.

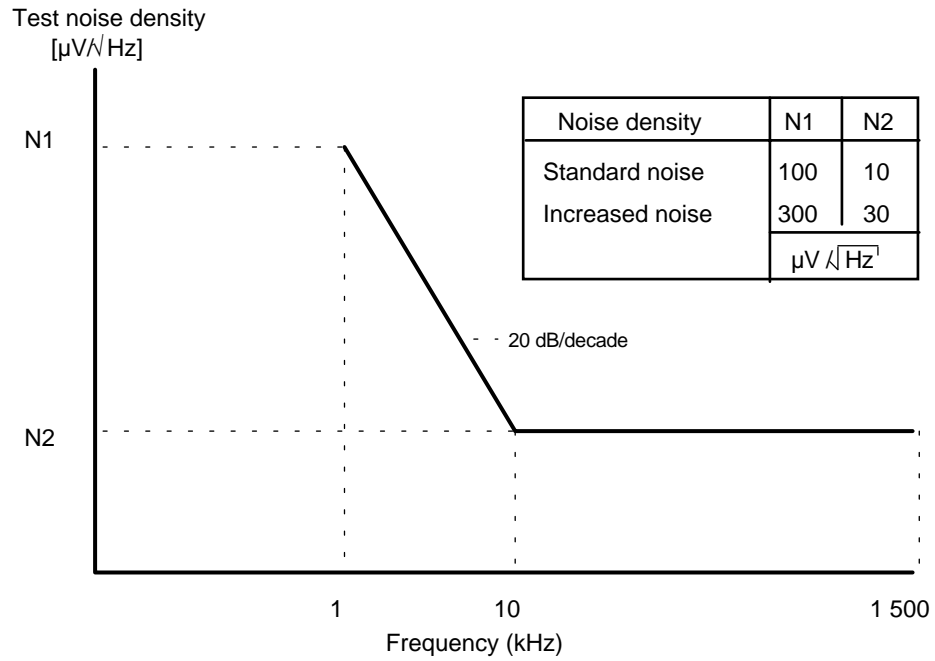


Figure 29: Test noise characteristics

Two levels of noise density (defined in the range 10 kHz to 1 500 kHz) are used for test purposes:

- 10 µV/√Hz for standard tests (corresponding to 53 dB NEXT at 150 kHz);
- 30 µV/√Hz for worst case tests (corresponding to 41 dB NEXT at 150 kHz).

The injection circuit should have a 4 kohms Thevenin output impedance, and the shaped noise voltage density should be measured at the output of the shunt injection circuit, loaded with a 67,5 ohms resistor.

This shaped noise can be created by:

- defined amplitude-values, stored in memory;
- read out with a clock rate greater than 2.336 MHz (more than four times the baud rate of the two pairs system);
- the repetition rate of the sawtooth function shall be in the range between 250 Hz and 500 Hz. A recommended value is 320 Hz;
- The amplitude of the sawtooth function is:

$$V_{pp} = \pi * \sqrt{2} * U_{1kHz} * 1\,000 \text{ Hz} / \sqrt{f_{rep}}$$

where U_{1kHz} is the PSD (V/√Hz) at 1 kHz;

and f_{rep} is the repetition rate of the sawtooth function [Hz].

For further information on the implementation of this noise generation requirements refer to "SHAPIRO RUDIN signal" in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS VOL. CAS-33 No. 10 OCTOBER 1986. "Multitone signals with low crest factor" , Stephen Boyd.

This results in a waveform having a crest factor of approximately 2,6.

7.1.3.3.4 Test procedure for impulse noise

7.1.3.3.4.1 Impulse noise test waveform

The impulse noise waveform $V(t)$ (hereafter called the "test impulse" and also known as the "COOK pulse") is defined as:

$$V(t) = +K|t|^{-3/4} \quad (t > 0);$$

$$V(t) = 0 \quad (t = 0);$$

$$V(t) = -K|t|^{-3/4} \quad (t < 0),$$

where t is time given in units of seconds (s) and K is a constant defined numerically in tables 29 and 30.

A sampled version of the test impulse should be used with samples at $t = (2n-1)T/2$. The sampling rate ($1/T$) should be at least twice the baud rate of the system under test. A minimum number of 8 k (i.e. ± 4 k) samples is required with an amplitude accuracy of at least 12 bits. It is important to note that there is no sample at $t = 0$. A window on the sampled test impulse is shown in figure 30.

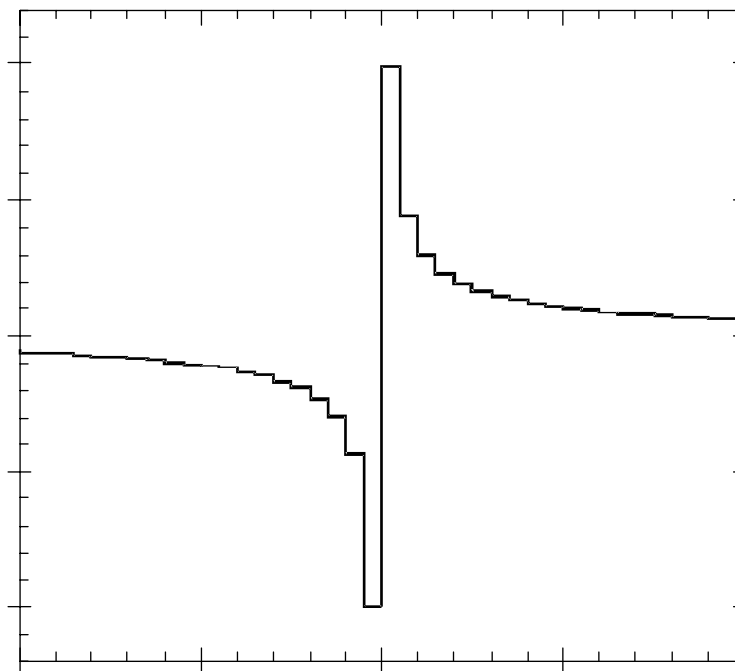


Figure 30: Time domain representation of the test impuls sampled at 2 MSamples/s with 12 bit accuracy

7.1.3.3.4.2 Impulse noise test measurement

The test impulse shall be applied to the system under test at a rate of 10 Hz. The test period shall be at least 10 s (i.e. >100 impulses should be applied).

The test configuration shall be as described in subclause 7.1.3.3.2, with the Bit Error Ratio Test Set (BERTS) configured to display bit error ratio.

The test impulse waveform shall be transformer coupled to the line via a well balanced shunt injection circuit. The injection circuit should have 4 kohms Thevenin impedance to present minimal loading to the transmission line.

The minimum value of Y (pair attenuation in dB at 150 kHz) to be used for the impulse noise measurement at the two pair system is given in table 28 and for the HDSL three pair system in table 29.

7.1.3.3.4.3 Impulse noise test performance requirements

The maximum bit error ratio for the three levels of impulse noise is given in table 28 for a two pairs system and in table 29 for a three pairs system. The peak-to-peak amplitude of the test impulse noise is given in mV (and in dB relative to a reference level of 318 mV) measured at the output of the shunt injection circuit, loaded with a 67,5 ohms resistor.

Table 28: Performance requirements for a two pairs system

The minimum attenuation of the test pair (Y) should be 27 dB		
Peak-to-peak amplitude (Vpp) of the test impulse when sampled at 2 Msamples/s (<i>Note</i>)	K	Bit error ratio upper limit when measured at the application interface
318 mV (0 dB level)	1.775×10^{-6}	4.500×10^{-4}
159 mV (- 6 dB level)	8.875×10^{-7}	5.625×10^{-5}
79 mV (- 12 dB level)	4.4375×10^{-7}	7.030×10^{-6}
NOTE: The peak-to-peak amplitude will vary with sampling rate and may be easily calculated from the following expression for sampling rates other than 2 Msamples/s. If the sampling rate is 1/T samples/s then $V_{pp} = 2K T/2 ^{-3/4}$.		

Table 29: Performance requirements for a three pairs system

The minimum attenuation of the test pair (Y) should be 31 dB		
Peak-to-peak amplitude (Vpp) of the test impulse when sampled at 2 Msamples/s (<i>note</i>)	K	Bit error ratio upper limit when measured at the application interface
318 mV (0 dB level)	$1,775 \times 10^{-6}$	3.00×10^{-4}
159 mV (- 6 dB level)	$8,875 \times 10^{-7}$	3.75×10^{-5}
79 mV (- 12 dB level)	$4,4375 \times 10^{-7}$	4.68×10^{-6}
NOTE: The peak-to-peak amplitude will vary with sampling rate and may be easily calculated from the following expression for sampling rates other than 2 Msamples/s. If the sampling rate is 1/T samples/s then $V_{pp} = 2K T/2 ^{-3/4}$.		

7.1.3.3.5 Common mode rejection test

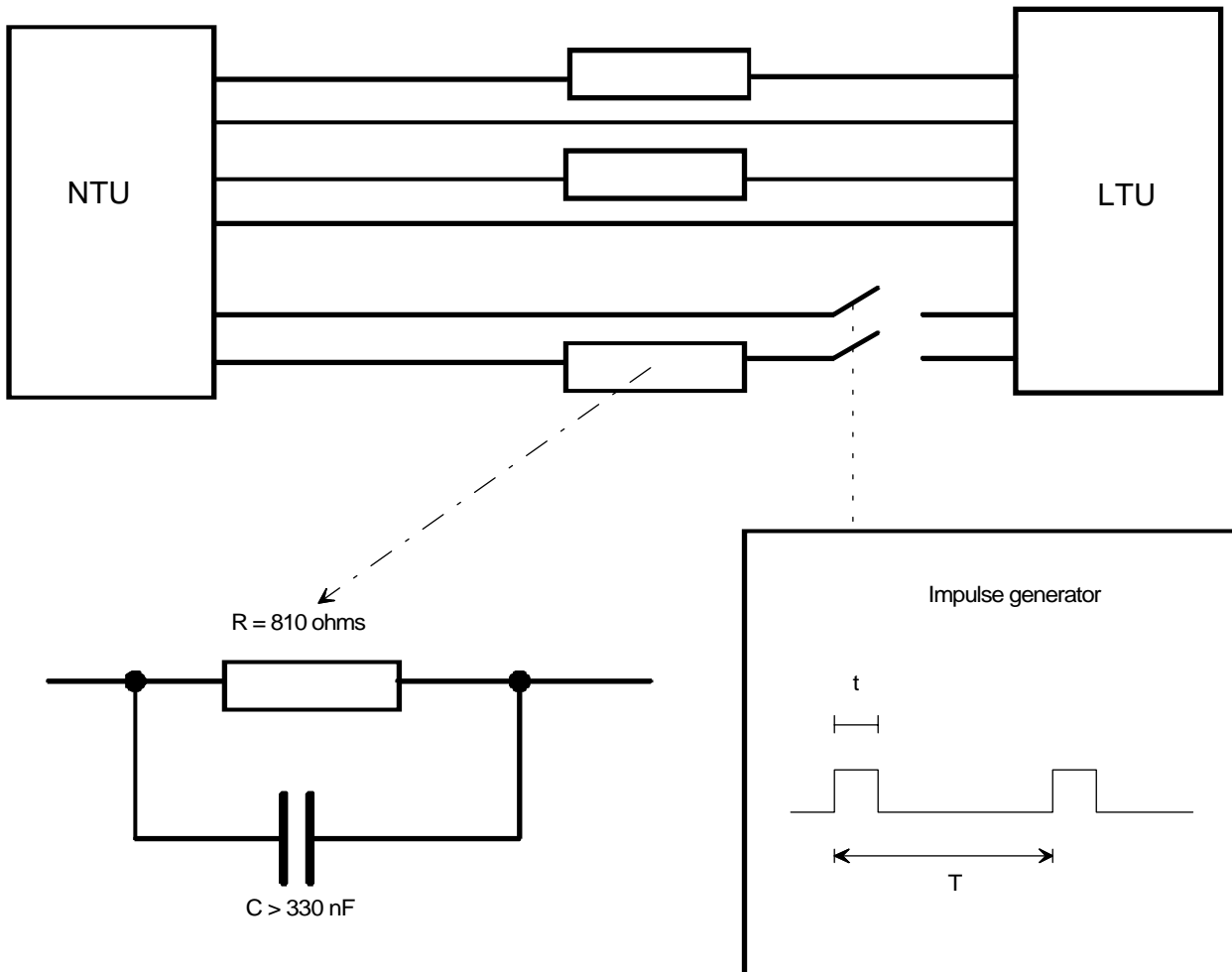
This procedure is intended to test the common mode rejection capability of an implementation. Test Loop 8 shall be used with a common mode triangle signal of 50 Hz with a voltage of 15 V rms for the first harmonic (25,5 Vp). The 21st harmonic (1 050 Hz) shall be 53 to 56 dB below the level of the first harmonic. The measured BER shall be less than $1/2 \cdot 10^{-7}$ for a two pairs system and $1/3 \cdot 10^{-7}$ for a three pairs system.

The circuit for common mode insertion is shown in figure 27.

7.1.3.3.6 Micro interruption test

The configuration for micro interruption susceptibility test is shown in figure 31.

In this arrangement a periodic trigger signal S stimulates a micro-relay device inducing periodic micro-interruptions on one of the pairs forming the transmission link. It is expected that, on the basis of the proposed test arrangement, each HDSL transceiver should tolerate a micro interruption of (at least) $t = 10$ ms when stimulated with a signal of period $T = 5$ s.



NOTE: The test shall be carried out for each transceiver pair constituting the transmission link.

Figure 31: Micro interruption test circuit

8 Power feeding

8.1 General

This subclause deals with remote power feeding of regenerator or customer sited equipment and wetting current requirements.

Line powering of customer sited equipment is only required in some applications. Line powering of optional regenerators is a requirement. However a detailed specification of a regenerator is outside the scope of this ETR.

The case where regenerator and customer sited equipment are both remotely powered is excluded since it is considered not feasible within the limited power budget available.

Due to the:

- different national safety requirements;
- different DLL planning rules;
- the optional use of regenerators;
- and the application dependant requirement to power customer sited equipment,

no detailed power feeding requirement is provided. Instead general guidelines are provided for the situations where remote powering is required.

8.2 Wetting current

Wetting current may be used to prevent corrosion of contacts. In the case of remote power feeding the feeding current is enough to fulfil the wetting current requirements.

Figure 32 gives the basic concept for the provision of wetting current.

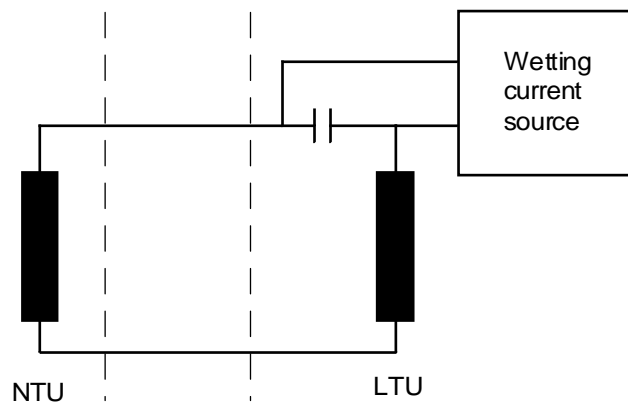


Figure 32: Basic method for provision of wetting current

The wetting current shall be less than 20 mA.

8.3 Remote power feeding aspects

Parallel power feeding is recommended as basic method of power feeding for all HDSL applications and configurations (e.g. 1, 2 or 3 pairs, partial operation).

Figure 33 shows the basic circuit for parallel power feeding.

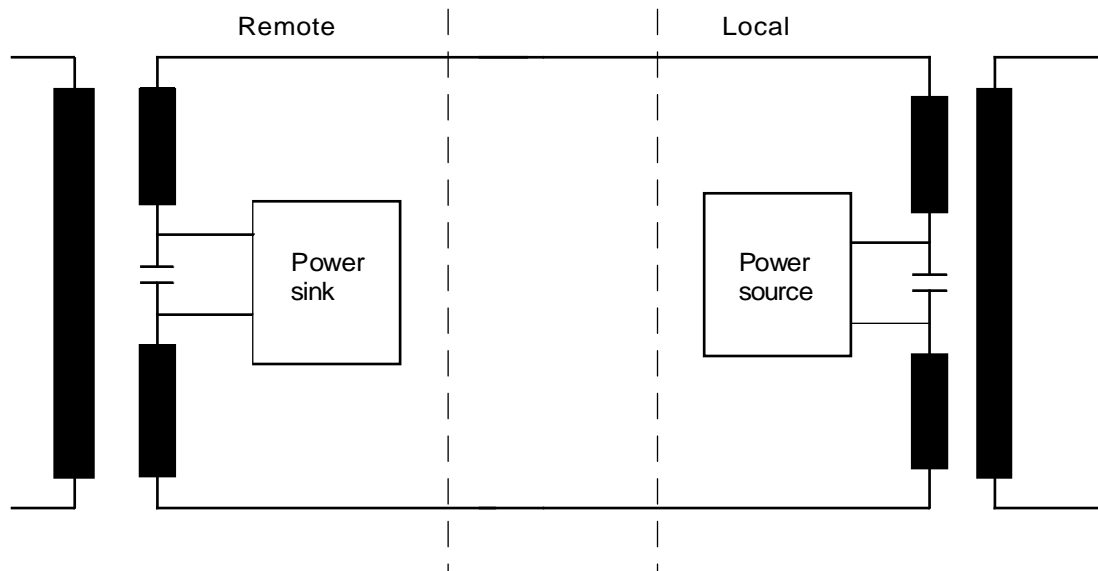


Figure 33: Parallel power feeding

The remote unit should be able to deal with polarity reversal.

8.3.1 Remote power feeding aspects at the NTU

Power will be delivered to the NTU via each HDSL pair. The total power (derived from all available pairs) can be used to operate the NTU. HDSL transceivers which are not active may be placed in a low power consumption mode or switched off.

8.3.2 Remote power feeding aspects at the regenerator

Remote power feeding of a regenerator should be done on a per pair basis. In case of a fault in the regenerator the regenerator and the two cable sections can be exchanged to restore the HDSL system.

The regenerator should, if required, also provide wetting current towards the NTU. The amount of wetting current which can be provided may be dependant on the available power budget.

Figure 34 shows the basic circuit for remote powering a regenerator and provision of wetting current.

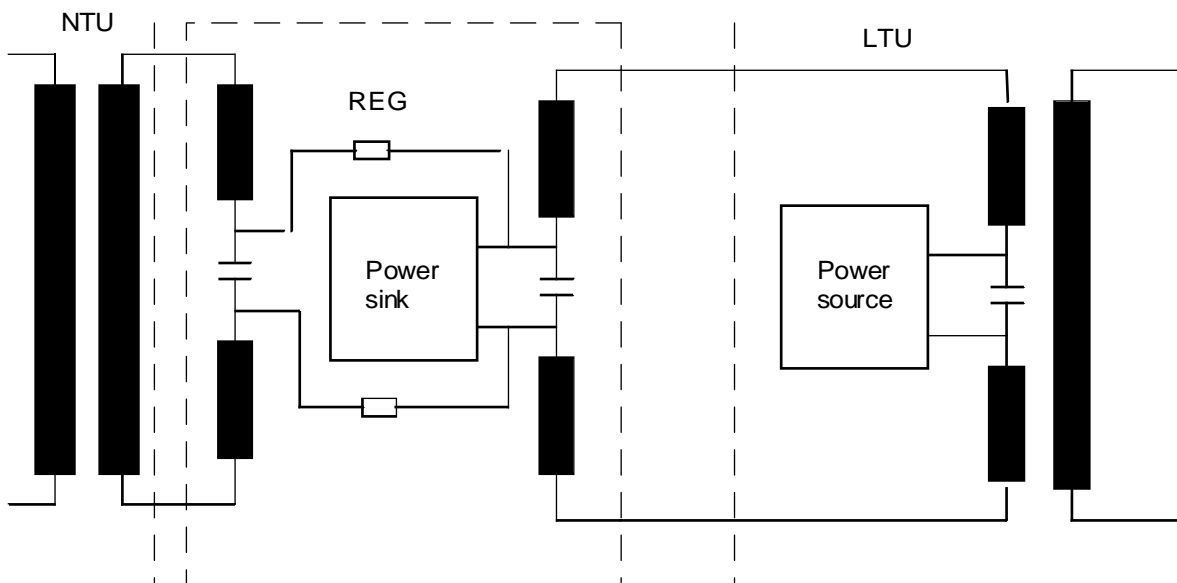


Figure 34: Basic concept to power a regenerator and to provide wetting current

8.3.3 Remote power feeding aspects at the LTU

If the LTU provides remote power this power is shared over all the available pairs. This should prevent that the majority of the power is transported over the pair with the lowest resistance.

The provision of power feeding in partial operation is for further study.

9 Environmental requirements

9.1 Climatic conditions

Climatograms applicable to the operation of HDSL equipment can be found in ETS 300 019 [3]. The choice of classes is under national responsibility.

9.2 Safety

Only general references are given. Dependent on the application as well as on the national regulations, other requirements may also be applicable.

For the NTU: in conformance with EN 41003 [10] and EN 60950 [11].

For the LTU: in conformance with EN 41003 [10] and EN 60950 [11].

For the REG: in conformance with EN 41003 [10] and EN 60950 [11].

9.3 Overvoltage protection

Only general requirements are given. Dependent on the application as well as on the national regulations, other requirements may also be applicable.

For the NTU: in conformance with ITU-T Recommendation K.21 [19].

For the LTU: in conformance with ITU-T Recommendation K.20 [17] and K.21 [19].

For the REG: in conformance with ITU-T Recommendation K.17 [16].

9.4 Electromagnetic compatibility (EMC)

The EMC requirements shall be defined nationally according to the equipment type and as described in ETS 300 386 [7].

A.2 Theoretical characteristics of test loops

Table A.8: Loop 2

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		15,2	19,0	23,4	28,6	31,0	33,3	42,5	46,8
Phase (deg)		- 97	- 165	- 280	- 611	- 889	- 1 168	- 2 277	- 2 823
Group Delay (µs)		21,7	17,0	15,4	15,4	15,5	15,6	15,3	15,1
Impedance () at NTU	Re.	228	179	146	126	122	120	117	117
	Im.	- 209	- 129	- 82	- 39	- 28	- 23	- 14	- 13
Impedance () at LTU	Re.	228	179	146	126	122	120	117	117
	Im.	- 209	- 129	- 82	- 39	- 28	- 23	- 14	- 13

Table A.9: Loop 3

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		16,4	20,0	23,2	28,3	31,3	34,5	45,9	50,3
Phase (deg)		- 114	- 191	- 336	- 770	- 1 129	- 1 489	- 2 896	- 3 588
Group Delay (µs)		23,8	20,2	20,1	20,0	20,0	19,9	19,4	19,1
Impedance () at NTU	Re.	219	199	166	120	123	120	117	116
	Im.	- 152	- 98	- 91	- 41	- 27	- 26	- 13	- 13
Impedance () at LTU	Re.	257	190	134	128	121	116	118	120
	Im.	- 201	- 151	- 84	- 33	- 34	- 19	- 17	- 12

Table A.10: Loop 4

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		15,3	19,3	23,3	28,2	31,2	34,3	45,6	50,0
Phase (deg)		- 113	- 195	- 339	- 768	- 1 126	- 1 484	- 2 887	- 3 578
Group Delay (µs)		25,5	20,9	19,6	19,9	20,0	19,9	19,3	19,1
Impedance () at NTU	Re.	128	110	114	105	109	108	103	103
	Im.	- 143	- 68	- 26	- 18	- 18	- 11	- 9	- 7
Impedance () at LTU	Re.	263	210	192	159	165	159	157	157
	Im.	- 205	- 122	- 75	- 30	- 34	- 16	- 13	- 12

Table A.11: Loop 5

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		14,7	17,6	19,7	25,7	30,5	34,8	48,6	53,8
Phase (deg)		- 169	- 307	- 577	- 1 376	- 2 025	- 2 661	- 5 126	- 6 317
Group Delay (µs)		38,5	37,6	37,5	36,5	35,6	35,5	33,2	32,5
Impedance () at NTU	Re.	165	144	126	87	67	57	60	80
	Im.	- 95	- 70	- 60	- 55	- 44	- 31	+ 8	+ 11
Impedance () at LTU	Re.	165	144	126	87	67	57	60	80
	Im.	- 95	- 70	- 60	- 55	- 44	- 31	+ 8	+ 11

Table A.12: Loop 6

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		12,	16,1	21,9	31,2	27,0	28,1	35,7	41,4
Phase (deg)		- 1	- 138	- 232	- 413	- 612	- 833	- 1 613	- 1 977
Group Delay (µs)		18,	14,1	12,1	8,3	12,1	12,3	11,6	10,1
Impedance () at NTU	Re.	124	88	65	49	68	75	68	52
	Im.	- 67	- 97	- 64	- 9	0	- 19	- 18	3
Impedance () at LTU	Re.	253	188	144	125	124	120	117	117
	Im.	- 200	- 133	- 88	- 43	- 29	- 21	- 14	- 13

Table A.13: Loop 7

Frequency (kHz)		10	20	40	100	150	200	400	500
Attenuation (dB)		15,6	19,7	24,6	30,9	33,7	36,5	49,7	55,0
Phase (deg)		- 111	- 191	- 328	- 720	- 1 047	- 1 380	- 2 666	- 3 300
Group Delay (µs)		25,0	20,2	18,4	18,2	18,3	18,5	17,6	17,3
Impedance () at NTU	Re.	125	87	56	48	73	96	73	60
	Im.	- 180	- 111	- 64	- 6	+ 17	- 11	+ 2	- 17
Impedance () at LTU	Re.	214	163	132	103	91	81	57	53
	Im.	- 211	- 134	- 91	- 59	- 53	- 49	- 31	- 21

History

Document history	
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