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ETSI

European Telecommunications Standards Institute

ETSI Secretariat

Postal address: F-06921 Sophia Antipolis CEDEX - FRANCE
Office address: 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
X.400: c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

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Foreword

This ETSI Technical Report (ETR) has been produced by the Transmission and Multiplexing (TM) Technical Committee of the European Telecommunications Standards Institute (ETSI).

ETRs are informative documents resulting from ETSI studies which are not appropriate for European Telecommunication Standard (ETS) or Interim European Telecommunication Standard (I-ETS) status. An ETR may be used to publish material which is either of an informative nature, relating to the use or the application of ETSs or I-ETSs, or which is immature and not yet suitable for formal adoption as an ETS or an I-ETS.

This ETR gives guidance to network operators and equipment manufacturers regarding the functional architecture of Synchronous Digital Hierarchy (SDH)-based transport networks.

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1 Scope

This ETR covers the functional architecture and network issues of transport networks as applied to Synchronous Digital Hierarchy (SDH)-based networks. It is firmly based upon ITU-T Recommendation G.803 [1] and the generic functional architecture of transport networks covered under ETR 085 [2]. It also covers interconnection of Plesiochronous Digital Hierarchy (PDH)-based and SDH-based networks and evolution to SDH-based transport networks.

This ETR does not consider:

- timing and synchronisation issues (being addressed under Work Item DE/TM-03017 [3]);

- path management processes (being addressed under Work Item DTR/TM-03009 [4]);

- issues associated with the circuit layer (as defined in ETR 085 [2]) other than the definition of the inter-layer adaptation at the boundary between the circuit layer network and the path layer network;

- the service related issues of exploiting path layer networks to users (for example, for the provision of leased lines).

2 References

This ETR incorporates by dated or undated reference, provisions from other publications. These references are cited in the appropriate places in the text and the publications are listed below. For dated references, subsequent amendments to any of these publications apply to this ETR only when incorporated in it by amendment or revision. For undated references, the latest edition of the publication referred to applies.

[1] ITU-T Recommendation G.803 (1993): "Architecture of transport networks based on the synchronous digital hierarchy".

[2] ETR 085: "Transmission and Multiplexing (TM); Generic functional architecture of transport network".

[3] DE/TM-03017: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH) Timing and synchronisation".

[4] DTR/TM-03009: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH) Trail management process".

[5] ITU-T Recommendation G.708 (1993): "Network node interface for the synchronous digital hierarchy".

[6] prETS 300 147 2nd Edition (1993): "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH) Multiplexing structure".

[7] prETS 300 337: "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells) at the CCITT Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[8] ETS 300 167 (1993): "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".

[9] CCITT Recommendation G.702 (1988): "Digital hierarchy bit rates".

[10] CCITT Recommendation G.783 (1990): "Characteristics of synchronous digital hierarchy (SDH) multiplexing equipment functional blocks".

3 Abbreviations

ADM	Add/Drop Multiplex
AIS	Alarm Indication Signal
APS	Automatic Protection Switch
ATM	Asynchronous Transfer Mode
AUG	Administrative Unit Group
AU-n	Administrative Unit (level) n
BIP-n	Bit Interleaved Parity (of order) n
B-ISDN	Broadband aspects of Integrated Services Digital Network
DXC	Digital Cross-Connect
LTE	Line Termination Equipment
MST	Multiplex Section Termination
NNI	Network Node Interface
PDH	Plesiochronous Digital Hierarchy
PRC	Primary Reference Clock
PSTN	Public Switched Telephony Network
SDH	Synchronous Digital Hierarchy
STM-N	Synchronous Transport Module (level) N
TCP	Termination Connection Point
TMN	Telecommunication Management Network
TU-n	Tributary Unit (level) n
VC-n	Virtual Container (level) n

4 Structure of this ETR

Clause 5 contains a vocabulary of SDH-specific terms for defining SDH network architecture (other terms can be found in ETR 085 [2]). Clause 6 contains the detailed description of the architecture in functional terms. Clause 7 uses the functional description and applies it to actual network topologies, structures and network elements which are likely to be required. Clause 8 contains a description of protection and restoration from a functional architecture viewpoint. Clause 9 identifies the applications envisaged for the various types of primary rate mappings into the VC-11 and VC-12. Clause 10 describes the introduction of SDH networks in terms of the choices which need to be made by an operator and the implications on network aspects and on interworking between PDH and SDH.

5 Vocabulary for SDH network architecture

The vocabulary for network architecture given in ETR 085 [2] applies to SDH-based transport networks. Further clarifications of terms, as they relate to SDH-based transport networks are given below.

SDH lower-order path layer network: a path layer network (as defined in ETR 085 [2]) which is concerned with the transfer of information between SDH lower-order path layer access points in support of certain types of circuit layer network. Within regions conforming to ETSI standards, the SDH lower-order path layer networks are the VC-12, VC-2, VC-2-nc and VC-3 layers.

SDH higher-order path layer network: a path layer network (as defined in ETR 085 [2]) which is concerned with the transfer of information between SDH higher-order path layer access points in support of SDH lower-order path layer networks and certain types of circuit layer network. Within regions conforming to ETSI standards, the SDH higher-order path layer network is the VC-4 (and VC-4-nc) layer.

Section layer network: a layer network which is concerned with the transfer of information between section layer access points. In the case of SDH, the section layer network is further divided into the multiplex section layer network and the regenerator section layer network.

Physical media layer network: a layer network which is concerned with the actual optical fibre, metallic pair or radio frequency which supports the section layer network.

Multiplex section layer network: a layer network which may be media dependent and which is concerned with the transfer of information between multiplex section layer access points.

Regenerator section layer network: a layer network which is media dependent and which is concerned with the transfer of information between regenerator section layer access points.

NOTE: The relationship between the various sub-divisions of the transmission media layer is shown in figure 1.

Circuit: a trail in the circuit layer network.

Path: a trail in the path layer network.

Section: a trail in the section layer network.

Path termination: a trail termination in the path layer network.

Section termination: a trail termination in the section layer network.

6 Transport functional architecture of SDH-based networks

6.1 General

The generic functional architecture of transport networks given in ETR 085 [2], applies to SDH-based networks. Further clarification as it relates to SDH-based transport networks is given below.

6.2 SDH transport network layers

6.2.1 SDH administrative path layers

As described in ETR 085 [2], the path layer can be decomposed into administrative path layers. In the case of SDH, the decomposition of the path layer results in lower-order path layers and higher-order path layers as described in table 1.

Table 1: SDH administrative path layers

	Regions complying with ETSI standards	**Other regions**
Lower-order paths	VC-11 VC-12 VC-2 VC-2-n VC-3	VC-11 VC-12 VC-2 VC-2-nc
Higher-order paths	 VC-4 VC-4-nc	VC-3 VC-4 VC-4-nc

ITU-T Recommendation G.708 [5], gives the rules for interconnections between the regions.

The potential for remote control of the connectivity in path layer networks is a key feature of SDH networks.

6.2.2 SDH administrative transmission media layers

As described in ETR 085 [2], the transmission media layer can be decomposed into administrative transmission media layers. In the case of SDH, the decomposition of the transmission media layer results in the section layer and the physical media layer. Section layer networks are concerned with all the functions which provide for the transfer of information between two nodes in path layer networks. Whereas physical media layer networks are concerned with the actual fibre, metallic pair or radio frequency channel which supports a section layer network. In the case of SDH, the section layer can be further decomposed into two administrative layers: a multiplex section layer and a regenerator section layer. The multiplex section layer is concerned with the end-to-end transfer of information between locations which route or terminate paths. Whereas the regenerator section layer is concerned with the transfer of information between individual regenerators and between regenerators and locations which route or terminate paths.

In the future it may be desirable to identify further layers to describe optical wavelength division multiplexing and wavelength routing.

6.2.3 SDH client/server associations

The layered relationship for SDH-based transport networks is illustrated in figure 1. Table 2 provides examples of the client/server associations currently defined in ETSs in which SDH layers participate.

Table 2: Adaptation function references

Client layer	Server layer	Adaptation reference	Client network characteristic information
1 544 kbit/s asynch	VC-11 path	ETS 300 147 [6]	1 544 kbit/s ± 50ppm
1 544 kbit/s byte synch	VC-11 path	ETS 300 147 [6]	1 544 kbits nominal, octet structured ETS 300 167 [8]
2 048 kbit/s asynch	VC-12 path	ETS 300 147 [6]	2 048 kbit/s ± 50 ppm
2 048 kbit/s byte synch	VC-12 path	ETS 300 147 [6]	2 048 kbit/s nominal octet structured ETS 300 167 [8]
34 368 kbit/s asynch	VC-3 path	ETS 300 147 [6]	34 368 kbit/s ± 20 ppm
44 736 kbit/s asynch	VC-3 path	ETS 300 147 [6]	44 736 kbit/s ± 20 ppm
139 264 kbit/s asynch	VC-4 path	ETS 300 147 [6]	139 264 kbit/s ± 15 ppm
ATM virtual path	VC-4 path or VC-4-nc (NOTE)	ETS 300 147 [6]	53-octet cells
VC-11 path	VC-12 LO path	ETS 300 147 [6]	VC-11 + frame offset
VC-12 path	VC-4 HO path	ETS 300 147 [6]	VC-12 + frame offset
VC-12 path	34 368 kbit/s path	ETS 300 337 [7]	VC-12 + frame offset
VC-12 path	139 264 kbit/s path	ETS 300 337 [7]	VC-12 + frame offset
VC-2 path	VC-4 HO path	ETS 300 147 [6]	VC-2 + frame offset
VC-2 path	139 264 kbit/s path	ETS 300 337 [7]	Vc-2 + frame offfset
VC-3 LO path	VC-4 path	ETS 300 147 [6]	VC-3 + frame offset
VC-3 LO path	139 264 kbit/s path	ETS 300 337 [7]	VC-3 + frame offset
VC-4 path	STM-N section	ETS 300 147 [6]	VC-4 + frame offset

LO = Lower-order HO = Higher-order

NOTE: Mappings into other SDH virtual containers will be included in future revisions of ETS 300 147 [6].

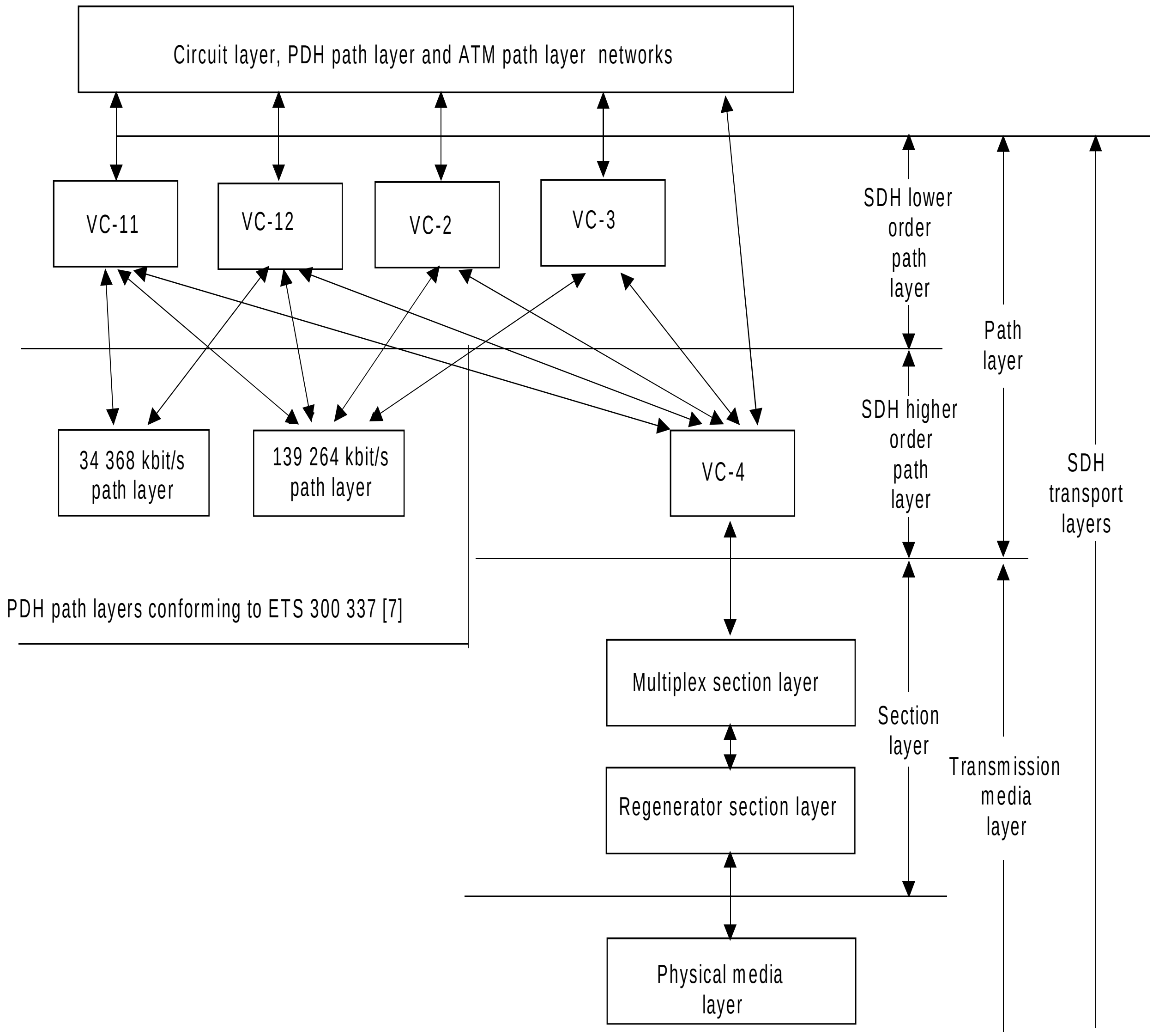


Figure 1: SDH-based transport network layered model

7 Application of concepts to network topologies and structures

Some examples of the application of the concepts of functional architecture are given in ETR 085 [2].

8 Transport network availability enhancement techniques

Some general considerations on protection and restoration, and in particular on trail protection and sub-network connection protection, are given in ETR 085 [2].

8.1 SDH trail protection examples

Some specific types of multiplex section protection schemes used in SDH are given below. They are characterized by the detection of failure events by the Multiplex Section Termination (MST) function, and the resultant reconfiguration uses the protection switching functions that are in the multiplex section protection sub-layer.

The resultant reconfiguration may involve protection switching in multiple SDH network elements. The co-ordination of such switching in multiple SDH network elements is by means of an Automatic Protection Switching (APS) protocol.

8.1.1 SDH multiplex section 1+1 protection

(Refer to ETR 085 [2], figure 16).

SDH multiplex section 1+1 protection is characterised by two parallel multiplex sections, each of which has a capacity capable of supporting the maximum capacity of the higher-order paths.

The APS protocol for multiplex section 1+1 protection is given in CCITT Recommendation G.783 [10].

8.1.2 SDH multiplex section 1:N protection

SDH multiplex section 1:N protection is characterised by there being one more multiplex section than actually required to support the higher-order path capacity to be protected. When not required to support protected higher-order paths, this additional multiplex section capacity can be used to support "extra traffic". This extra traffic is not itself protected.

The APS protocol for multiplex section 1 : N protection is given in CCITT Recommendation G.783 [10].

8.1.3 SDH multiplex section shared protection rings

(Refer to figure 2).

Multiplex section shared protection rings are characterised by dividing the total payload per multiplex section equally into working and protection capacity, e.g. for a two fibre STM-N ring there are N/2 administrative unit groups (AUGs) available for working and N/2 AUGs for protection whilst in a four fibre STM-N ring there are N AUGs available for working and N AUGs available for protection. The notation of sharing refers to the fact that the ring protection capacity can be shared by any multiplex section of a multinode ring under a section or node failure condition. Sharing of protection capacity may lead to improved traffic carrying under normal conditions over other ring types.

Multiplex section ring protection is based on detection of failures by the multiplex section function on both sides of the failed portion of the ring and reconfiguration takes place in the protection switching client layer.

Under non-failure conditions, the protection capacity can be used to support lower priority traffic.

The APS protocol for multiplex section shared protection rings will be based on an enhancement of the K-byte protocol for 1 : N APS currently defined in CCITT Recommendation G.783 [10]. The operation of this type of ring is always dual ended.

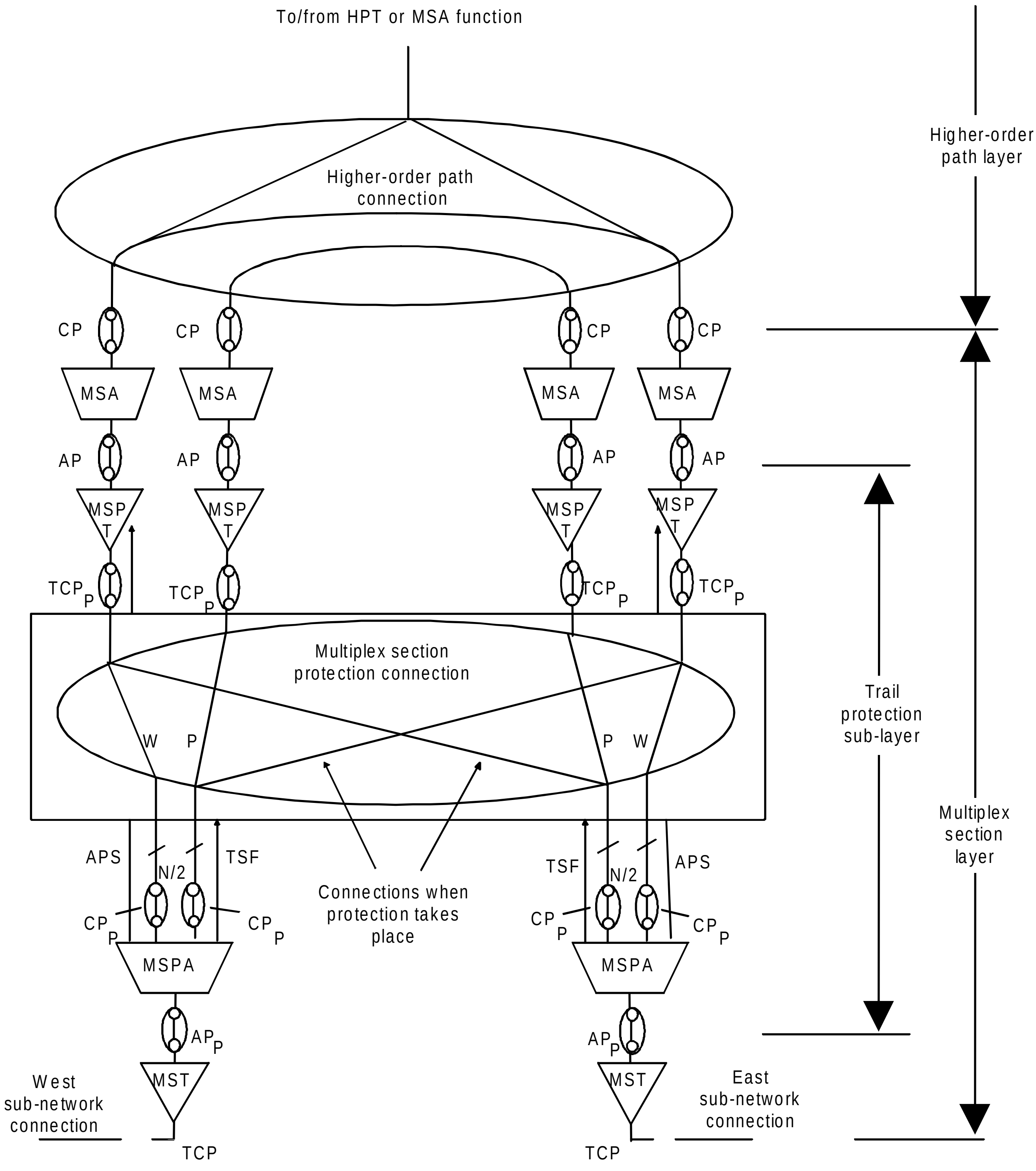
8.1.4 SDH multiplex section dedicated rings

(Refer to figure 3).

The multiplex section dedicated ring protection is characterised by a 1 : 1 protection scheme. The scheme is based on unidirectional operation.

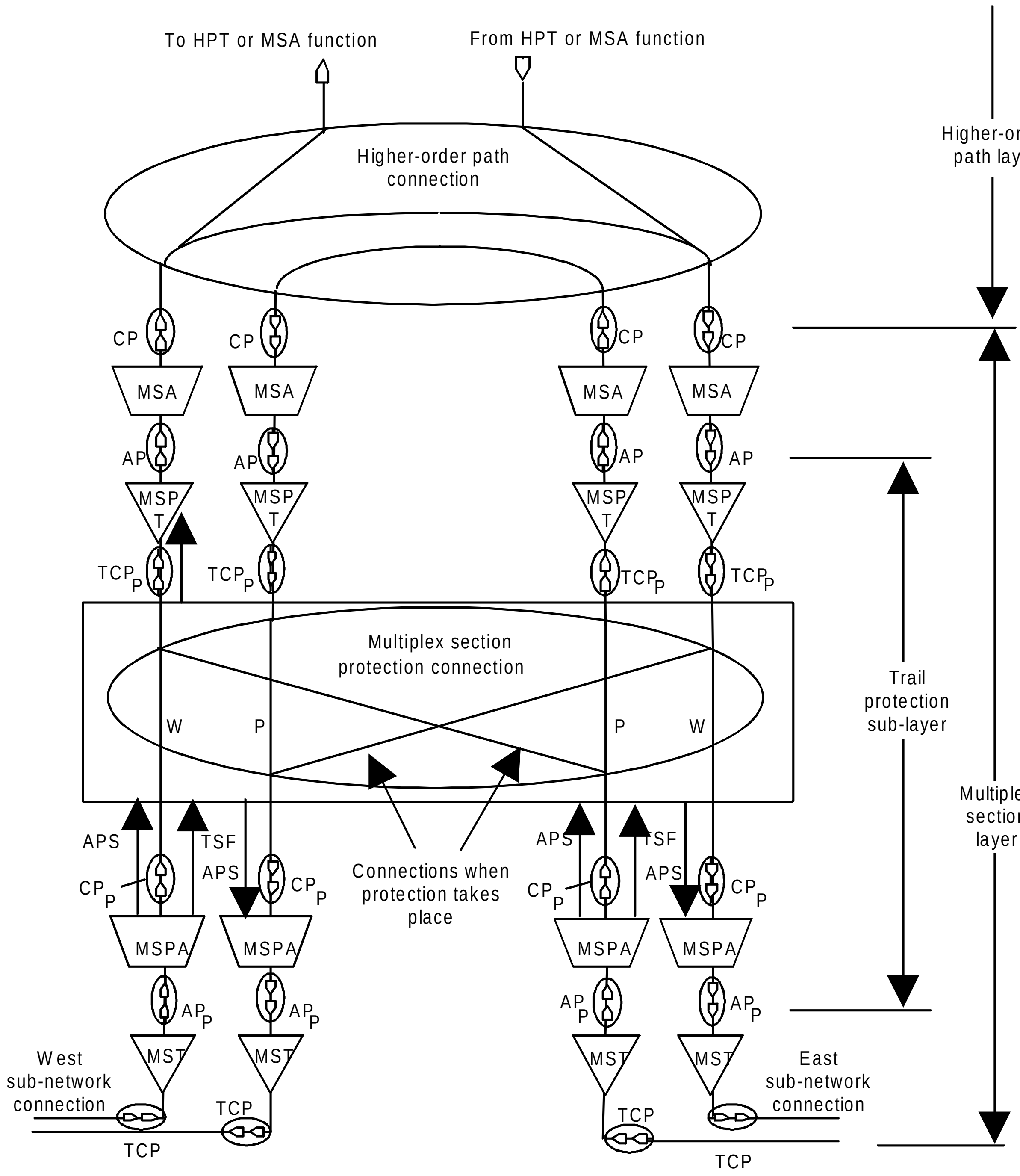
Under failure conditions, the entire AUG is looped to the protection channel. Multiplex section dedicated ring protection is based on the detection of failures by the MST functions in the SDH network elements. The operation of this type of ring class is always dual ended.

The APS protocol of multiplex section dedicated protection rings will be based on an enhancement of the K-byte protocol for 1 : 1 APS currently defined in CCITT Recommendation G.783 [10].



TSF:	Trail Signal Fail
APS:	Automatic Protection Switch channel
HPT:	Higher-order Path Termination
MSPT:	Multiplex Section Protection Termination
MSPA:	Multiplex Section Protection Adaptation
MSA:	Multiplex Section Adaptation
MST:	Multiplex Section Termination
TCP_P:	Protection TCP
AP_P:	Protection Access Point
CP_P:	Protection Connection Point

Figure 2: Multiplex section shared protection ring



TSF: Trail Signal Fail
APS: Automatic Protection Switch channel
HPT: Higher-order Path Termination
MSPT: Multiplex Section Protection Termination
MSPA: Multiplex Section Protection Adaptation
MSA: Multiplex Section Adaptation
MST: Multiplex Section Termination
TCP_P: Protection TCP
AP_P: Protection Access Point
CP_P: Protection Connection Point

Figure 3: Multiplex section dedicated protection ring

8.2 SDH sub-network connection protection examples

Examples of SDH higher-order path layer and lower-order path layer ring applications are given below.

8.2.1 SDH higher-order ring protection

Higher-order ring protection, sometimes known as "higher-order path switched ring protection", is characterised by transmission of the higher-order path characteristic information both ways round the ring (using a higher-order path protection switching function at the network element at which the higher-order path enters the ring). At the network element at which the higher-order path exits the ring, one of the signals is selected. The higher-order paths are switched individually and unidirectionally based on purely local information at the network element at which the higher-order path exits the ring. Therefore, it is possible to implement higher-order ring protection without any APS protocol.

Using inherent monitoring: the detection of the failure events "administrative unit loss of pointers" or "administrative unit AIS" (or local MST detected failures which result in AIS on all administrative units) at the network element at the exit from the ring results in reconfiguration of the higher-order path protection switching functions. This scheme does not detect (or protect against) impairments that impact only the monitored high order paths, but not the multiplex section that terminates at that site (e.g. errors introduced in a preceding multiplex section).

Using non-intrusive monitoring: this is implemented by adding a higher order path protection termination function as indicated in ETR 085 [2], figure 20. This allows the detection of failures or degradations on individual paths.

8.2.2 SDH lower-order ring protection

SDH lower-order ring protection is similar in principle to higher-order ring protection as show generically in ETR 085 [2], figure 18.

Lower-order ring protection is characterised by transmission of the lower-order path characteristic information both ways round the ring (using a lower-order path protection switching function at the network element at which the lower-order path enters the ring). At the network element at which the lower-order path exits the ring, one of the signals is selected. The lower-order paths are switched individually and unidirectionally based on purely local information at the network element at which the lower-order path exits the ring. Therefore, it is possible to implement lower-order ring protection without any APS protocol.

Inherent monitoring: the detection of the failure events "tributary unit loss of pointers" or "tributary unit AIS" (or local MST or higher-order path termination detected failures which result in AIS on all tributary units) at the network element at the exit from the ring results in reconfiguration of the lower-order path protection switching functions. This scheme does not detect (or protect against) impairments that impact only the monitored low order paths, but not the higher order path that terminates at that site (e.g. errors introduced in a preceding higher order path).

Using non-intrusive monitoring: this is implemented by adding the lower order path protection termination function as indicated in ETR 085 [2], figure 20. This allows the detection of failures or degradations on individual paths.

9 Choice of primary rate mapping

9.1 Features of the primary rate mappings

There are three ways of mapping 1 544 and 2 048 kbit/s primary rate signals into the VC-11 and VC-12 respectively as defined ETS 300 147 [6]: asynchronous; bit synchronous and byte synchronous. These mappings have different features and networking considerations. The choice of mapping is application dependent. The features of the three types of mapping are described below.

9.1.1 Asynchronous mapping

This mapping has the following features:

a) it provides bit sequence independent support of the primary rate signal without any assumptions on its structure (the signal can be framed, as defined in ETS 300 167 [8], or unstructured);

b) it does not allow the VC-1x direct visibility of any 64 or N x 64 kbit/s signals contained within the primary rate signal; the primary rate signal needs to be reconstructed in order to access any 64 or N x 64 kbit/s signals;

c) it includes a justification process which can accommodate a primary rate signal with a timing tolerance of ± 50 ppm;

d) it is potentially universally applicable although, in cases where 64 kbit/s switches or DXCs have STM-N interfaces, the lack of direct visibility of the constituent 64 or N x 64 kbit/s signals may be a significant drawback (see also Clause 10).

9.1.2 Bit synchronous

This mapping has the following features:

a) it provides bit sequence independent support of the primary rate signal without any assumptions on its structure (the signal can be framed, as defined in ETS 300 167 [8], or unstructured);

b) it does not allow the VC-1x direct visibility of any 64 or N x 64 kbit/s signals contained within the primary rate signal; the primary rate signal needs to be reconstructed in order to access any 64 or N x 64 kbit/s signals;

c) it does not include any justification processes so the primary rate signal needs to be synchronous with the VC-1x.

9.1.3 Byte synchronous

This mapping has the following features:

a) it requires the primary rate signal to be framed according to ETS 300 167 [8];

b) it allows the VC-1x direct visibility of the 64 or N x 64 kbit/s signals when the payload of the primary rate signal is octet structured. In this case, the primary rate signal need not be reconstructed in order to access the 64 kbit/s or the N x 64 kbit/s signals since the octets of the primary rate signal (including the primary rate signal framing information) are mapped into defined positions in the VC-1x;

c) it does not include any justification processes so the primary rate signal needs to be synchronous with the VC-1x;

d) it has two versions:

   1) **floating mode:** in this mode, the VC-1xs can "float" in frequency and phase with respect to each other within the higher-order VC-4. Their location in the higher-order VC-4 is identified using the pointer mechanism which also allows the VC-1xs to be independently switched in a VC-1x DXC or ADM with minimum delay;

   2) **locked mode:** in this mode, the VC-1xs are locked in frequency and phase with respect to each other and to the higher-order VC-4. The VC-1xs do not have a pointer which means that they cannot be independently switched in a VC-1x DXC or ADM without a significant delay penalty. Locked mode is essentially a direct mapping of 64 kbit/s or Nx64 kbit/s signals into the higher-order VC-4;

e) when the frame is octet structured, the mapping can be used on 64 kbit/s switches and 64 kbit/s DXCs with STM-N interfaces.

9.2 Selection of mapping options

Given the features of the mappings the following is recommended for SDH networking:

a) asynchronous mapping should be used only for asynchronous/ plesiochronous type signals. This includes PDH path mappings into SDH paths (i.e. 64 kbit/s signals in PDH format may be carried via the asynchronous mapping);

b) bit synchronous mapping should not be used;

c) byte synchronous floating mode mapping should be used for primary rate signals as defined in ETS 300 167 [8]; the signal needs to be framed and the payload can be either octet structured (64 kbit/s and N x 64 kbit/s) or not; the signal needs to be normally synchronous with the VC-1x;

d) byte synchronous locked mode mapping can be used as an alternative for c) above for primary rate signals with octet structured payload (64 kbit/s and N x 64 kbit/s signals) but only in cases where VC-1 x DXCs or ADMs are not used nor envisaged to be used.

Clause 10 provides more information on interworking of 64 and N x 64 kbit/s signals between PDH-based transport networks and SDH-based transport networks.

10 Introduction of SDH-based transport networks

10.1 General

There are many choices which need to be made when introducing SDH-based transport networks. These choices, such as the time order in which different types of SDH-based equipment are introduced and the types of mapping used, will affect subsequent stages of evolution to SDH-based transport networks and may pose networking or PDH/SDH interworking constraints. These choices and the level of deployment of SDH-based transport networks compared with PDH or other transport networks are a matter for the network operator concerned.

This subclause firstly identifies the types of circuit layer signals which can be supported on SDH paths and the types of circuit layer signals which can be supported on PDH paths. It then describes the three basic introductory scenarios for SDH-based equipment. For each type of circuit layer signal and introductory scenario, the consequences on networking, PDH/SDH interworking and subsequent transport network evolution are described.

Figure 4 shows the introductory paths that are available and illustrates the basic choices and provides a reference during the following discussion.

10.2 Types of circuit layer signals

10.2.1 SDH case

In the case of SDH, path layers support the following two types of circuit layer signals in accordance with the mappings defined in ETS 300 147 [6]:

a) circuit layer signals which directly support telecommunications services.

These circuit layer signals include:

1) 64 kbit/s-based signals (adapted into the SDH path layers using byte synchronous mappings);

2) leased line signals at CCITT Recommendation G.702 [9] bit rates at or above the primary rate;

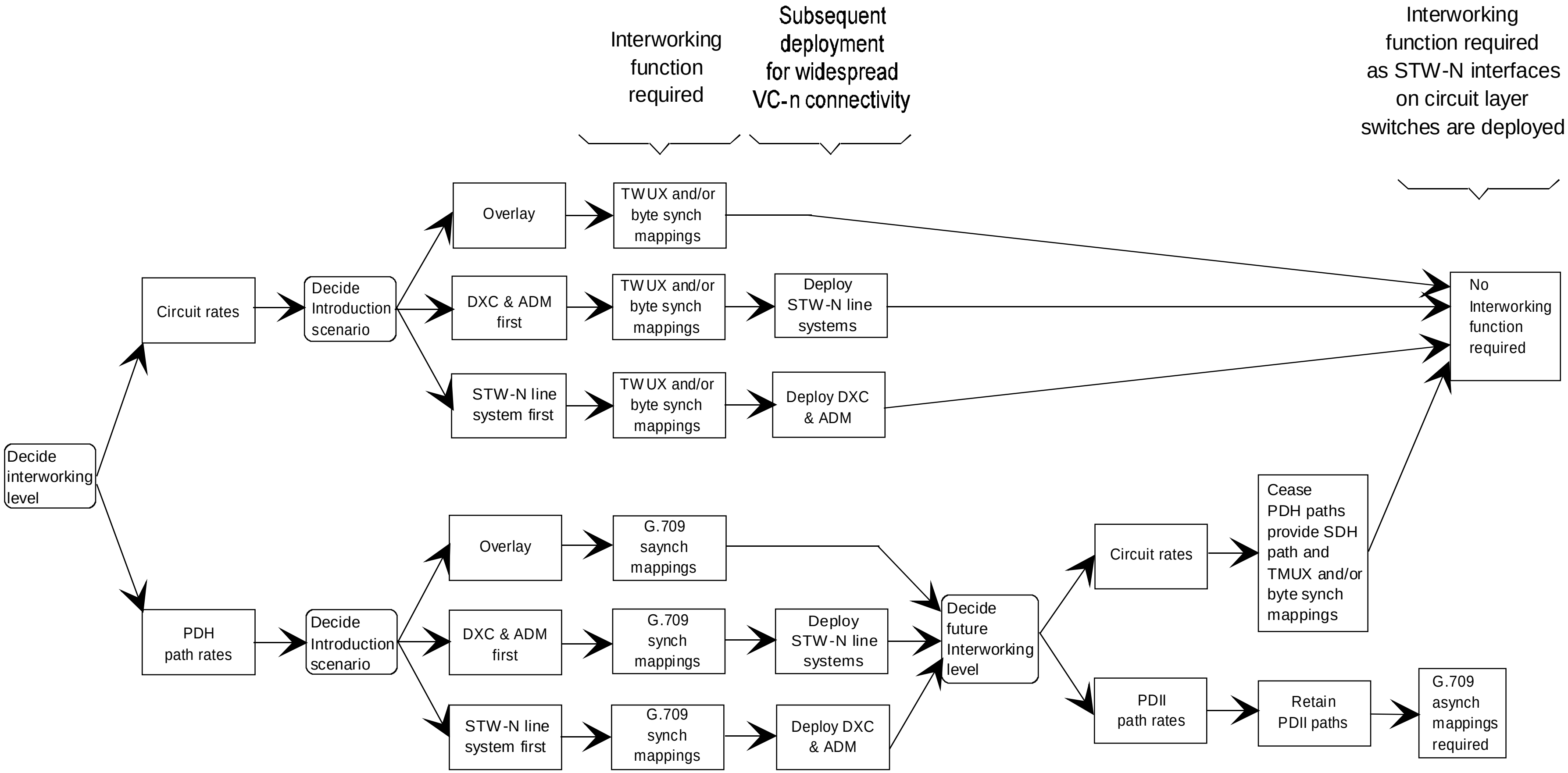
3) other signals (e.g. ATM cells) the bit rate of which might be optimised to the payload of the SDH path layers.

b) PDH path layer signals (at bit rates given in CCITT Recommendation G.702 [9] at or above the primary rate) which, in turn, support either:

1) circuit layer signals as in a) above;

2) lower-order PDH path layer signals.

SDH-based transport network equipment is concerned with control of connectivity of SDH paths and not with control of connectivity of the circuit layer. Therefore, in case b) above, the SDH-based equipment cannot be used to individually network the signals identified in b) 1) and 2); primary rate and/or higher-order PDH multiplexing functionality is required to facilitate this connectivity. This constraint could be significant in cases where SDH-based transport networks become widespread. Where this is likely to be the case, it is recommended that the support of such signal is minimised from the outset or, that during subsequent stages of transport network evolution, steps are taken to minimise the redundant PDH path layer signals.



DXC Digital cross-connect
ADM Add/drop multiplex
PDH Plesiochronous digital hierarchy
TWUX Transmultiplex

Figure 4: Introductory paths for SDH-based transport networks

10.2.2 PDH case

In the case of PDH, path layer signals support the following two types of circuit layer signals:

a) circuit layer signals which directly support telecommunications services. These circuit layer signals include:

   1) 64 kbit/s based signals (adapted into the PDH path layers in accordance with ETS 300 167 [8]);

   2) leased line signals at the bit rates given in CCITT Recommendation G.702 [9] at or above the primary rate;

   3) other signals (e.g. ATM cells) the bit rate of which might be optimised to the payload of the PDH layers.

b) SDH path layer signals which, in turn, support circuit layer signals identified in subclause 10.2.1 above. Mappings of SDH path layer signals into PDH path layer signals are defined in ETS 300 337 [7]. Such mapping functionality may be needed as a transitional stage of transport network evolution. The functionality is referred to below as "modem" functionality (since it is analogous to the transition from the "old" analogue network to the "new" digital network where modems allowed signals from the "new" network to be supported over the "old" network). In cases where the modem functionality provides multiplexing of several SDH path layer signals into the PDH path layer, control of the connectivity of the individual SDH path layer signals is not possible in the PDH path layer network.

10.3 Initial introduction of SDH-based equipment

There are three basic ways of initially introducing SDH-based equipment:

a) deployment of an overlay network comprising the simultaneous deployment of SDH line systems and VC-n cross-connect functionality to provide widespread path layer connectivity (NOTE). In addition, to increase geographical coverage in such overlay network, the link connections in the SDH path layer could be adapted into PDH paths using the modem functionality as mentioned in subclause 10.2.2, point b). Initially this overlay network is likely to be "thin" and might be targeted at supporting particular circuit layer types (e.g. circuit layers which support leased line services) but later "thickened" to include other services;

   NOTE: VC-n cross-connect functionality is realised in SDH Digital Cross-Connect (DXC) equipment and/or Add/Drop Multiplex (ADM) equipment. Such functionality is referred to below as DXC/ADM.

b) deployment of SDH DXC/ADMs only with interfaces at the bit rates given in CCITT Recommendation G.702 [9]. This is likely to take the form of DXCs in central locations where control of the connectivity of PDH paths at the site is the desired initial benefit. In terms of the functional network architecture. VC-n paths in the DXC/ADMs support sub-network connections in the PDH path layer. SDH line systems could be deployed at a later stage to provide more widespread VC connectivity. Similarly, PDH paths with the modem functionality could be used as mentioned in a) above to provide more widespread VC-n connectivity;

c) Deployment of SDH line systems only with intra-office interfaces at the bit rates given in CCITT Recommendation G.702 [9]. Such systems are functionally similar to PDH line systems in that they support link connections in the PDH path layer. In terms of the functional network architecture, VC-n paths in the SDH line systems support link connections in the PDH path layer. SDH DXC/ADMs could be deployed at a later date to provide more widespread VC-n connectivity.

Each option is valid and the choice of one or more options is determined by the initial requirements of the network operator. The choice of one option by one network operator need not affect the choice of another network operator. The three options can co-exist.

10.4 Interworking between PDH- and SDH-based transport networks

10.4.1 Interworking levels

Interworking between PDH-based transport networks and SDH-based transport networks can occur at one of the following three levels:

a) at the circuit level for signals identified in subclause, point 10.2.1 a) and subclause 10.2.2, point a). Such interworking generally requires the termination of the respective PDH and SDH paths and the adaptation functions between the respective path layers and the circuit layer. This combination of functions is referred to below as Transmultiplexing (TMUX). This approach does not necessarily imply additional physical interfaces. In the particular case of 64 kbit/s circuit layer signals, the byte synchronous mappings allow circuit level interworking without necessarily terminating the PDH path. In the particular case of leased line signals at the bit rates given in CCITT Recommendation G.702 [9] at or above the primary rate, the asynchronous mappings allow circuit level interworking. In cases where the PDH and SDH circuit layer signals have the same bit rate, interworking at the circuit level does not necessarily require processing of the circuit layer signal;

b) at the PDH path level for signals identified in subclause 10.2.1, point b). Such interworking requires the adaptation of the PDH path layer signals into appropriate SDH path layers using the asynchronous mappings;

c) at the SDH path level where the SDH path layer signals, described in subclause 10.2.2, point b), are adapted into PDH paths using the modem functionality. This case is for further study.

The choice of interworking level and SDH equipment introduction scenario will have an impact on subsequent transport network evolution stages as discussed below.

10.4.2 SDH overlay

The two interworking levels are considered as follows:

a) the requirements for interworking at the circuit level are given in subclause 10.4.1, point a).

   in cases where PDH paths are used to provide VC-n connectivity, "modem" functionality will be required for adaptation to the PDH path layer;

   in cases where subsequently STM-N interfaces are provided on network elements which process the circuit layer signals (e.g. circuit layer switches), there are no interworking requirements between such network elements and the SDH transport network;

b) the requirements for interworking at the PDH path level are given in subclause 10.4.1, point b). Primary rate and/or higher-order PDH multiplexing functionality will continue to be required in the PDH-based transport network:

   in cases where PDH paths are used to provide VC-n connectivity, "modem" functionality will be required for adaptation to the PDH path layer;

   in cases where subsequently STM-N interfaces are provided on network elements which process circuit layer signals, primary rate and/or higher order PDH multiplexing functionality and asynchronous mappings will continue to be required to provide interworking functionality between such network elements and the SDH transport network;

in cases where it is subsequently desired to interwork at the circuit level, it will be necessary to cease the SDH paths supporting PDH path layers and provide new SDH paths which directly support the circuit layer. Primary rate and/or higher-order PDH multiplexing functionality will not be required.

10.4.3 SDH DXC/ADMs

The two interworking levels are considered as follows:

a) the requirements for interworking at the circuit level are given in subclause 10.4.1, point a).

   In cases where subsequently more widespread SDH path layer networking is required. SDH line systems could be deployed; interworking functionality is not required between DXC/ADM and the SDH line systems. The considerations in subclause 10.4.2, point a) also apply;

b) the requirements for interworking at the PDH path level are given in subclause 10.4.1, point b).

   In cases where subsequently more widespread SDH path layer networking is required, SDH line systems could be deployed; interworking functionality is not required between the DXC/ADM and the SDH line systems. The considerations in subclause 10.4.2, point b) also apply.

10.4.4 SDH line systems

The two interworking levels are considered as follows:

a) the requirements for interworking at the circuit level are given in subclause 10.4.1, point a).

   In cases where subsequently more widespread SDH path layer networking is required, SDH DXC/ADMs could be deployed; interworking functionality is not required between DXC/ADM and the SDH line systems. The considerations in subclause 10.4.2, point a) also apply;

b) the requirements for interworking at the PDH path level are given in subclause 10.4.1, point b).

   In cases where subsequently more widespread SDH path layer networking is required, SDH DXC/ADMs could be deployed; interworking functionality is not required between the DXC/ADM and the SDH line systems. The considerations in subclause 10.4.2, point b) also apply.

10.5 Introduction STM-N interfaces on 64 kbit/s switches (and DXCs)

In the case of PDH-based transport networks, 64 kbit/s switches are interconnected by primary rate synchronous paths structured according to ETS 300 167 [8]. In terms of the functional architecture, the link connections between sub-networks in the 64 kbit/s circuit layer are supported by paths in the PDH path layer network. The introduction of STM-N interfaces on one of two interconnected 64 kbit/s switches requires PDH/SDH interworking.

Interworking can take place at either the 64 kbit/s circuit level or the PDH path level. Considering these two cases:

a) interworking at the 64 kbit/s circuit level requires the use of byte synchronous mappings to adapt the 64 kbit/s circuit layer signals into the SDH path layer;

b) interworking at the PDH path level requires the use of asynchronous mappings to adapt the PDH paths into the SDH path layer.

In the case where subsequently STM-N interfaces are introduced on the other 64 kbit/s switch and there is the potential for SDH path layer connectivity between the two switches, interworking functionality will be required if one switch uses byte synchronous mapping and the other switch uses asynchronous mapping. In cases where the two switches are in different operators networks, responsibility for providing the interworking functionality (if required) rests with the operator of the switch which uses asynchronous mapping unless otherwise agreed bilaterally.

History

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