# ETSI TECHNICAL REPORT

**ETR 017**

**December 1992**

Source: ETSI TC-TE

Reference: T/TE 04-11

ICS: 33.080

**Key words:** Terminal Equipment, DTE, DCE

# Terminal Equipment (TE); Requirements for the attachment of Data Terminal Equipment comprising CCITT V.series type interfaces to data circuit-terminating equipment for low and medium data signalling rates

**ETSI**

European Telecommunications Standards Institute

**ETSI Secretariat**

**Postal address:** F-06921 Sophia Antipolis CEDEX - FRANCE
**Office address:** 650 Route des Lucioles - Sophia Antipolis - Valbonne - FRANCE
**X.400:** c=fr, a=atlas, p=etsi, s=secretariat - **Internet:** secretariat@etsi.fr

Tel.: +33 92 94 42 00 - Fax: +33 93 65 47 16

# Contents

Blank page

## Foreword

This ETSI Technical Report (ETR) has been produced by the Terminal Equipment (TE) Technical Committee of the European Telecommunications Standards Institute (ETSI).

ETRs are informative documents resulting from ETSI studies which are not appropriate for European Telecommunication Standard (ETS) or Interim European Telecommunication Standard (I-ETS) status. An ETR may be used to publish material which is either of an informative nature, relating to the use or application of ETSs or I-ETSs, or which is immature and not yet suitable for formal adoption as an ETS or an I-ETS.

NOTE: Some Administrations may pose requirements in excess of those summarised in the main body of this ETR. Where such requirements apply, reference is made to Annex A of the ETR by putting an indication in the form (*nnn) at an appropriate place within the main body of the ETR, where "nnn" stands for the 3 digit code for the representation of the name of the respective country, in compliance with ISO 3166. "nnn" indicates which Administration poses an additional requirement. Annex A to this ETR gives a more detailed explanation.

Blank page

# 1 Scope

This ETR contains technical advice for designers of Data Terminal Equipment (DTE) comprising V. series type interfaces, and intended for connection to Data Circuit-terminating Equipment (DCE) for low and medium signalling rates (*DMK, GBR).

Administrations may, or may not, require the verification of compliance of a given DTE with technical requirements contained herein as a prerequisite for attachment to their network(s). For cases where such verification is intended by an Administration, a supplier or other party, indications are given as to the requirements for which compliance should be verified.

This ETR does not place any obligation on an Administration to automatically provide any particular type of DCE.

The ETR may be applicable for connections to the Public Switched Telephone Network (PSTN), fixed connections on analogue facilities and connections to Packet Switched Public Data Networks (PSPDN) in compliance with CCITT Recommendation X.28 [14], if functionally harmonised DCE is utilised in those networks.

This ETR may also be applicable for connections to the Circuit Switched Public Data Network (CSPDN) and fixed connections across digital facilities.

The interface between DTE and DCE may be of a conventional type, i.e. according to CCITT Recommendations V.24 [5] and V.28 [8] (alternatively CCITT Recommendation V.10 [3]) and ISO 2110 [10], or may be either type specified in CEPT Recommendations T/CD 01-12 [13] and CEPT T/CD 01-14 [9] for plug-in DCEs to be accommodated inside DTEs.

Auto-dialling methods, according to CCITT Recommendations V.25 [6] and V.25 bis [7] have been taken into account in this ETR.

# 2 References

For the purposes of this ETR the following references apply.

[1] IS0 3166 (1988): "Codes for the representation of names of countries".

[2] CEPT Recommendation T/CD 04-03 (1985): "Safety requirements for the DTE-DCE interface".

[3] CCITT Recommendation V.10 (1988): "Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications".

[4] CCITT Recommendation V.14 (1988): "Transmission of start-stop characters over synchronous bearer channels".

[5] CCITT Recommendation V.24 (1988): "List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE)".

[6] CCITT Recommendation V.25 (1988): "Automatic answering equipment and/or parallel automatic calling equipment on the general switched telephone network including procedures for disabling of echo control devices for both manually and automatically established calls".

[7] CCITT Recommendation V.25 bis (1988): "Automatic calling and/or answering equipment on the General Switched Telephone Network (GSTN) using the 100-series interchange circuits".

[8] CCITT Recommendation V.28 (1988): "Electrical characteristics for unbalanced double-current interchange circuits".

[9] CEPT Recommendation T/CD 01-14 (1986): "Specification of equipment practice for data transmission equipment".

[10] ISO 2110 (1980): "Data communication - 25 pin DTE/DCE interface connector and pin assignments".

[11] ISO 7480 (1991): "Information technology - Telecommunications and information exchange between systems - Start-stop".

[12] CCITT Recommendation V.42 (1988): "Error correcting procedures for DCEs using asynchronous-to-synchronous conversion".

[13] CEPT Recommendation T/CD 01-12 (1983): "Specification of engineering requirements for three types of plug-in DCEs operating with a user data signalling rate of 2 400 bit/s".

[14] CCITT Recommendation X.28 (1988): "DTE/DCE interface for a start-stop mode data terminal equipment accessing the packet assembly/disassembly facility (PAD) in a public data network situated in the same country".

[15] ETS 300 001 (1992): "Attachments to Public Switched Telephone Network (PSTN); General technical requirements for equipment connected to an analogue subscriber in the PSTN (Candidate NET 4)".

[16] ISO 9067 (1987): "Information processing systems - Data communication - Automatic fault isolation procedures using text loops".

[17] ISO 9543 (1989): "Information processing systems - Information exchange between systems - Synchronous transmission signal quality at DTE/DCE interfaces".

## 3 Abbreviations

For the purposes of this ETR the following abbreviations apply.

| | |
|---|---|
| CSPDN | Circuit Switched Public Data Network |
| CRI | Call request with number provided with the identification number |
| CRN | Call request with number provided |
| CRS | Call request with memory address provided |
| DTE | Data Terminal Equipment |
| DCE | Data Circuit Terminating Equipment |
| EMC | Electromagnetic Compatibility |
| ETR | ETSI Technical Report |
| ETS | European Telecommunication Standard |
| IC | Integrated Circuit |
| I-ETS | Interim European Telecommunication Standard |

| | |
|---|---|
| PSPDN | Packet Switched Public Data Network |
| PSTN | Public Switched Telephone Network |
| GSTN | General Switched Telephone Network |

# 4 General requirements

The requirements specified hereafter may apply irrespective of the application of the DTE concerned in one of the possible public networks.

## 4.1 Safety requirements

The DTE shall meet the requirements of CEPT Recommendation T/CD 04-03 [2].

NOTE: For an interim period, national safety requirements may still apply.

## 4.2 Electromagnetic compatibility

The requirements concerning Electromagnetic Compatibility (EMC) are currently under discussion by other international bodies.

NOTE: For an interim period, national EMC requirements may still apply.

# 5 Technical requirements for DTEs intended for connection to DCEs attached to the Public Switched Telephone Network (PSTN)

## 5.1 Data Circuit-Terminating Equipment (DCE) that may be provided by Administrations for connection to the PSTN

The provision of certain DCEs and of certain types of networks is entirely a subject of national regulations. Users are referred to existing national or CEPT documentation on the subject.

## 5.2 The interface

The DTE interchange circuits shall meet electrical, functional and operational requirements which are specified in the relevant Recommendations of the CCITT V. series (e.g. CCITT Recommendations V.10 [3], V.14 [4], V.24 [5], V.25 [6], V.25 bis [7] and V.28 [8]), of CEPT (e.g. T/CD 01-14 [9]) or ISO (e.g. ISO 2110 [10], ISO 7480 [11]). For the definitions of interchange circuits see CCITT Recommendation V.24 [5]. The following subclauses attempt to summarise requirements which may otherwise only be found dispersed in the referenced international documentation.

### 5.2.1 Interchange circuits at the data interface

In DCEs, interchange circuits may be provided on a mandatory or an optional basis in accordance with existing Recommendations published by the CCITT or CEPT.

Interchange circuits that are mandatory in certain types of DCEs need not necessarily likewise be provided mandatorily in attached DTEs. Only those circuits necessary to assure satisfactory operation of the application the DTE are intended to support the need to be controlled or monitored by the DTE. If, however, an interchange circuit is provided on an optional basis in a given DTE, it shall meet the functional and operational requirements as specified herein.

Certain interchange circuits are required to be monitored by the DTE. "Monitoring" in the context of this ETR implies that the relevant circuit shall not only be terminated by a receiver, but that all signals on this circuit shall be recognized by the DTE, and subsequent actions shall be taken, as specified herein.

The receivers of control circuits directed from the DCE to the DTE shall not solely be edge-triggered but shall, in addition, recognise changed states on the respective interchange circuit.

Receiver circuits may be provided in the DCE or the DTE for which no generator is provided in the complementary equipment. Therefore, where a receiver is not connected to a generator, means should be provided in the equipment (DTE or DCE) where the receiver is located to inhibit or disregard any possible false triggering of the receiver.

### 5.2.2 Functional and operational requirements for interchange circuits

#### 5.2.2.1 Circuit 102 "signal ground or common return"

This circuit is always essential.

If protective ground is provided in the DTE, it should be possible to connect signal ground to protective ground. Whether or not the two may actually be connected with each other may be a subject of national regulations.

Conformance should be checked by inspection.

NOTE 1: Pole 1 of the 25-pole interface connector according to ISO 2110 [10] is assigned for connecting the shields between tandem sections of shielded interface cables. Subject to national regulations, this contact may be connected to protective ground (if provided in the DTE), to signal ground, or may remain unconnected.

NOTE 2: It is good engineering practice to connect the shield of the interface cable only at one side (DTE or DCE) to pole 1 of the respective interface connector, to prevent ground loops.

#### 5.2.2.2 Circuit 103 "transmitted data"

This circuit is essential for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

The OFF condition of circuit 106 "indicates that the DCE is not prepared to accept data signals from the DTE" (see CCITT Recommendation V.24 [5]). Any data that is transmitted to the DCE while 106 is OFF may be lost.

Conformance should be checked by inspection.

NOTE 1: The data signalling rate on this circuit may be different from the data signalling rate on circuit 104 "received data" for certain applications ("asymmetrical duplex mode of operation").

In some applications, DTEs transmitting and receiving start-stop characters are operated with synchronous DCEs incorporating asynchronous-to-synchronous converters according to CCITT Recommendation V.14 [4]. In these cases, only character lengths of 8, 9, 10 and 11 bits can be used, and the intracharacter signalling rate on circuit 103 shall not deviate by more than + 1 % or - 2,5 % (for the "normal rate range") and + 2,3 % or - 2,5 % (for the "extended rate range") from the nominal value (see also subclause 5.2.2.3 for further details).

Conformance should be checked by inspection.

NOTE 2: DCEs equipped with an asynchronous (start-stop) to synchronous converter according to CCITT Recommendation V.14 [4] will transmit a "start" polarity of length M to 2 M + 3 bits (where M is the number of bits per character in the selected format) as 2 M + 3 bits of "start" polarity (referred to as "break signal"). If the converter detects more than 2 M + 3 bits all of "start" polarity, it transmits all these bits as "start" polarity.

The DTE shall transmit on circuit 103 at least 2 M bits of "stop" polarity after the "start" polarity break signal before sending further data characters.

Conformance should be checked by inspection.

This circuit may be used to signal a DTE not-ready condition to the associated DCE, where this DCE has an error correcting capability according to CCITT Recommendation V.42 [12]. In this case, a DTE not-ready condition is recognized by the DCE by the reception of a DC3 character on this circuit, and shall be cleared by the reception of a DC1 character as specified in the international alphabet (IA) No. 5. This method is be susceptible to misfunctioning where DC1 and DC3 characters can appear within the stream of user data, e. g. at the transfer of binary files. An alternate method of flow control using circuit 133 is therefore specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

For requirements concerning the signal quality on this circuit see Clause 8.

#### 5.2.2.3 Circuit 104 "received data"

This circuit is essential for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

NOTE 1: The data signalling rate on this circuit may be different from the data signalling rate on circuit 103 "transmitted data" for certain applications ("asymmetrical duplex mode of operation").

In some applications, DTEs transmitting and receiving start-stop characters are operated with synchronous DCEs incorporating asynchronous to synchronous converters according to CCITT Recommendation V.14 [4]. In these cases, only character lengths of 8, 9, 10 and 11 bits can be used. Furthermore, it should be noted that the length of the stop elements of received characters may be reduced by 12,5 % (in the "normal signalling rate range") or 25 % (in the "extended signalling rate range") of the nominal length, depending on the signalling rate range chosen (these values are theoretical and may be slightly exceeded in practical implementations due to technical constraints). DTEs intended for these applications shall be capable of coping with this condition. The definitions of the signalling rate ranges are contained in CCITT Recommendation V.14 [4].

NOTE 2: Where the DCE associated with the DTE concerned has an error correcting capability according to CCITT Recommendation V.42 [12], this circuit may be used to signal a DCE not-ready condition. In this case, the DTE should recognize a DC3 character received on this circuit as a DCE not-ready condition, and the reception of a DC1 character as clearance of this condition. The coding of these characters is in accordance with international alphabet (IA) No. 5. It should be noted that this method can be susceptible to misfunctioning, where DC1 and DC3 characters can appear within the stream of user data, e. g. where binary files are transferred. An alternate method of flow control is therefore specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

For requirements concerning the signal quality on this circuit see Clause 8.

#### 5.2.2.4 Circuit 105 "request to send"

This circuit is essential where the DTE is intended to be connected to half-duplex DCEs.

If this circuit is provided, it shall not be turned OFF in the transmitting mode of the DTE prior to the trailing edge of the last transmitted data bit being presented to the DCE on circuit 103 "transmitted data".

Conformance should be checked by inspection.

If this circuit is provided for the half-duplex mode of operation and is turned ON and OFF to turn around the transmitting direction of the data channel, it shall not be turned ON prior to circuit 106 "ready for sending" having gone OFF as a response to circuit 105 previously having been turned OFF.

Conformance should be checked by inspection.

#### 5.2.2.5 Circuit 106 "ready for sending"

This circuit is essential and should be monitored by the DTE.

No data shall be presented to the DCE on circuit 103 "transmitted data" prior to circuit 106 being ON.

Conformance should be checked by inspection.

NOTE 1: The implementation of an error correcting capability inside the DCE requires that a flow control of transmitted data be feasible between the DTE and the associated DCE, with the DCE turning circuit 106 ON and OFF. Therefore, an interworking with a DCE where this feature is present and activated may not be possible if circuit 106 is not implemented in the DTE. However, the rules for the flow control have not yet been established in international standardisation. It should be noted that DTEs may not monitor the status of circuit 106 prior to each byte to be sent, but only after blocks of data of variable length. Therefore, a buffer of suitable size should be implemented in the DCE. The size of this buffer is not specified in any international documentation. However, it is assumed that the minimum size should be 8 KBytes which would suffice to buffer the contents of a CRT screen, including control characters, etc...

NOTE 2: Where a circuit 107 ON to circuit 106 ON time-out function is performed by the DTE, it should be noted that the respective delay may be several seconds with certain types of DCEs.

NOTE 3: Where the DCE associated with the DTE concerned has an error correcting capability according to CCITT Recommendation V.42 [12], this circuit may be used to signal a DCE not-ready condition. In this case, the OFF condition of this circuit indicates a DCE not-ready condition which will be cleared by again turning this circuit ON. An alternate method of flow control using DC1/DC3 characters of international alphabet (IA) No.5 on circuit 104 is specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

#### 5.2.2.6 Circuit 107 "data set ready"

This circuit is essential where the DTE is equipped with an automatic answering or calling facility (*DEU).

Implementers are advised to pay particular attention to paragraph 4.4 of CCITT Recommendation V.24 [5].

#### 5.2.2.7 Circuits 108/1 "connect data set to line" and 108/2 "data terminal ready"

One of these circuits shall be provided.

If circuit 108/1 is provided for answering controlled by the DTE, and the DTE is not capable of recognizing indication INC ("incoming call"), then also circuit 125 shall be provided.

NOTE 1: Once circuit 108/x has been turned to the ON condition and data communication has been established, the communication ceases as soon as the respective circuit is turned OFF.

If an automatic answering or calling facility is provided, either circuit 108/1 (direct call case) or circuit 108/2 (addressed call case) shall be provided. It shall be ensured that no erroneous lock-up can occur at the connection. If, with circuit 107 being ON, no data transfer is initiated until the expiration of a certain time-out, circuit 108/x shall be turned OFF by the DTE.

NOTE 2: This may be accomplished by the provision of a time-out function in the DTE ("non-activity timer") with a duration of e. g. less than two minutes, which is started after an incoming call has been detected by the DCE, and the DCE has turned ON circuit 125 "incoming call".

Conformance should be checked by inspection.

#### 5.2.2.8 Circuit 109 "data channel received line signal detector"

This circuit is essential and should be monitored for applications where at the transmitting side of a connection circuit 105 "request to send" is turned ON and OFF to control flow of information and/or to turn around the transmitting direction of half-duplex DCEs.

Alternatively to this mode of operation, the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 109 is optional.

NOTE: In this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the transmitting direction of the connection has actually been turned around.

#### 5.2.2.9 Circuit 111 "data signalling rate selector (DTE source)"

The circuit may be used in conjunction with modems which allow the selection of two or more data signalling rates. If this circuit is provided, it may be controlled by internal logic, a manually activated switch in the DTE or any other suitable means.

#### 5.2.2.10 Circuit 112 "data signalling rate selector (DCE source)"

This circuit is essential where:

- the DTE is intended to be connected to DCEs which may (i.e. are conditioned to) perform automatic selection between two or more data signalling rates; and

- any of the following conditions apply:

  - circuit 113 "Transmitter signal element timing (DTE source)" is used; or

  - the DTE is not capable of discerning the changed data signalling rate from the lower (or higher) clock frequency of circuit 115 "Receiver signal element timing (DCE source)"; or

  - the DTE is working in the asynchronous (start-stop) mode (only possible with certain types of DCEs) and the DTE is not capable of discerning the changed data signalling rate from the received data.

#### 5.2.2.11 Circuit 113 "transmitter signal element timing (DTE source)"

This circuit may be provided optionally.

If this circuit is provided, the tolerance of the frequency of the timing signal presented on it shall be ± 0,01 % or better. The condition on this circuit shall be ON and OFF for nominally equal periods of time, and the transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 103 "Transmitted data" (further details may be found in the documentation referenced in Clause 8).

The circuit shall be turned to the OFF condition when it is implemented in the DTE but not used (because circuit 114 "transmitter signal element timing (DCE source)" is used, or in case of start-stop operation).

Conformance should be checked by inspection.

#### 5.2.2.12 Circuit 114 "transmitter signal element timing (DCE source)"

This circuit is essential where the DTE is intended to transmit data in a synchronous mode of operation, and circuit 113 "transmitter signal element timing (DTE source)" is not used. If this circuit is implemented in the DCE but not used (e.g. in case of start-stop operation), it shall be clamped to the OFF condition by the DCE.

NOTE 1: The condition on this circuit is ON and OFF for nominally equal periods of time (further details may be found in the documentation referenced in Clause 8).

The DTE shall present a data signal on circuit 103 "transmitted data" in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of circuit 114.

Conformance should be checked by inspection.

NOTE 2: In some applications, circuit 114 may be connected to circuit 115 "receiver signal element timing (DCE source)" inside the DCE. It should be noted that in some DCEs this condition may be restricted to the frequency of the timing signal output on the two circuits, while the correlation of signal phase angles may be at random. The DTE should be capable of coping with this condition.

#### 5.2.2.13 Circuit 115 "receiver signal element timing (DCE source)"

This circuit is essential where the DTE is intended to receive data in a synchronous mode of operation.

NOTE: The condition of this circuit is ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition nominally indicates the centre of each signal element on circuit 104 "received data". Further details may be found in the documentation referenced in Clause 8.

#### 5.2.2.14 Circuit 118 "transmitted backward channel data"

This circuit is essential where the DTE is intended to transmit data in the backward channel and to transmit separate data in the main channel.

No data shall be presented to the DCE on this circuit prior to circuit 121 "Backward channel ready" being ON.

Conformance should be checked by inspection.

#### 5.2.2.15 Circuit 119 "received backward channel data"

This circuit is essential where the DTE is intended to receive data in the backward channel and to receive separate data in the main channel.

#### 5.2.2.16 Circuit 120 "transmit backward channel line signal"

This circuit is also essential where circuit 118 "Transmitted backward channel data" is provided and a half-duplex mode of operation is intended in the backward channel.

If this circuit is provided, it shall not be turned OFF in the transmitting mode of the DTE prior to the trailing edge of the last transmitted backward channel data bit being presented to the DCE on circuit 118 "transmitted backward channel data".

Conformance should be checked by inspection.

If this circuit is provided and is turned ON and OFF, e.g. to control flow of information and/or to turn around the transmitting direction of the backward channel, it shall not be turned ON prior to circuit 122 "backward channel received line signal detector" being OFF.

Conformance should be checked by inspection.

#### 5.2.2.17 Circuit 121 "backward channel ready"

This circuit is also essential where circuit 120 "transmit backward channel line signal" is provided.

Where this circuit is provided, no data shall be presented on circuit 118 "transmitted backward channel data" to the DCE prior to circuit 121 being ON.

Conformance should be checked by inspection.

#### 5.2.2.18 Circuit 122 "backward channel received line signal detector"

This circuit is essential and should be monitored for applications where also circuit 119 "Received backward channel data" is provided and where, at the transmitting side of a connection circuit, 120 "transmit backward channel line signal" is turned ON and OFF to control flow of information and/or to turn around the transmitting direction of half-duplex DCEs.

Alternatively to this mode of operation, the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 122 is optional.

NOTE: In this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the transmitting direction of the connection has actually been turned around.

#### 5.2.2.19 Circuit 125 "calling indicator"

This circuit is essential and should be monitored if it is intended to use circuit 108/1 "connect data set to line" for an automatic answering facility in the DTE and if the DTE is not capable of recognizing indication INC "incoming call". Furthermore, it is essential and should be monitored if circuit 108/2 "data terminal ready" is generally held in the OFF condition and is used to respond to an incoming call.

NOTE 1: The ON condition on this circuit may be pulsed in sympathy with the incoming ringing signals. Details about the specifications of the incoming ringing signals in various national networks may be found in ETS 300 001 [15].

NOTE 2: If the serial automatic calling function according to CCITT Recommendation V.25 bis [7] is implemented in the DTE, then, to prevent call collision, either circuit 125 is essential and should be monitored, or the DTE should be capable of recognising indication INC "incoming call".

NOTE 3: If circuit 108/2 "data terminal ready" is used as described above, it is recommended that the DTE turn circuit 108/2 to the ON condition within 500 ms after circuit 125 is turned ON by the DCE.

#### 5.2.2.20 Circuit 133 "ready for receiving"

This circuit may be provided to control the transfer of data on circuit 104, e.g. where the DCE has an error correcting capability according to CCITT Recommendation V.42 [12]. Further details may be found in paragraph 7.3.1 of CCITT Recommendation V.42 [12], where an alternate method of flow control indication is also specified.

#### 5.2.2.21 Circuit 140 "loopback / maintenance test"

This circuit may be provided optionally.

NOTE: If this circuit is provided, its use should be as outlined in ISO 9067 [16].

#### 5.2.2.22 Circuit 141 "local loopback"

This circuit may be provided optionally.

NOTE: If this circuit is provided, its use should be as outlined in ISO 9067 [16].

#### 5.2.2.23 Circuit 142 "test indicator"

This circuit is essential and should be monitored if either circuit 140 or circuit 141, or both, are provided in the DTE.

Where provided, circuit 142 going ON shall cause the DTE to cease data communication and either:

- remain in stand-by mode until circuit 142 goes OFF, after which data communication may be resumed; or

- enter a test condition.

Conformance should be checked by inspection.

NOTE: The definition of the "stand-by mode" for any given DTE is implementation dependent.

### 5.2.3 Interface connectors and electrical characteristics of the interchange circuits

Three types of interface connectors may be used:

- The 25-pole interface connector with pole allocation according to ISO 2110 [10]. The male part of the connection is at the DTE side.

  If this interface connector is chosen, its dimensions and pole allocation shall be in compliance with the above mentioned standard. The provision of certain latching facilities at the interface connector may be a subject of national regulations.

  The electrical characteristics of the interchange circuits shall be in compliance with either CCITT Recommendations V.28 [8] or V.10 [3]. Zero voltage at an interchange circuit provided in the DTE is an illegal condition as long as the DTE is powered up.

- The 32-pole interface connector with pole allocation according to CEPT Recommendation T/CD 01-12 [13]. The female part of this connector is at the DTE side.

  If this connector is used, the electrical characteristics of the interchange circuits shall be in compliance with CEPT Recommendation T/CD 01-14 [9], Section 3.

- The 64/96-pole interface connector with pole allocation according to CEPT Recommendation T/CD 01-14 [9]. The male part of the connection is at the DTE side.

  The use of the b-row of this type of connector is a national option. Only in accordance with national regulations may non-standardised interchange circuits be allocated to contacts in the b-row of the connector. If it is not intended to utilise nationally standardised interchange circuits, the b-row of the connector part at the DTE side should not be populated with pole.

  If this connector is used, the electrical characteristics of the interchange circuits shall be in compliance with CEPT Recommendation T/CD 01-14 [9], Clause 3.

In table 1, the interchange circuit numbers, names and pole allocations for the three possible types of connectors are summarised.

**Table 1: List of interchange circuits and pole allocations for the data interface**

| Cct | Interchange circuit name | ISO 2110 [10] | T/CD 01-12 [13] | T/CDN° 01-14 [9] |
|---|---|---|---|---|
| 102 | Signal ground or common return | 7 | a3, a4, b4 | a,b,c1 a,b,c31 a,b,c32 |
| 103 | Transmitted data | 2 | b6 | c11 |
| 104 | Received data | 3 | a5 | c12 |
| 105 | Request to send | 4 | b7 | c13 |
| 106 | Ready for sending | 5 | a15 | c14 |
| 107 | Data set ready | 6 | a14 | c15 |
| 108/1 | Connect data set to line | 20 | a9 | c16 |
| 108/2 | Data terminal ready | 20 | a9 | a16 |
| 109 | Data channel received line signal detector | 8 | a6 | c18 |
| 111 | Data signal rate selector (DTE) | 23 | b15 | a20 |
| 112 | Data signal rate selector (DCE) | 12 | b15 | c22 |
| 113 | Transm. signal element timing (DTE) | 24 | a10 | a21 |
| 114 | Transm. signal element timing (DCE) | 15 | a10 | a11 |
| 115 | Recvr. signal element timing (DCE) | 17 | b5 | a13 |
| 118 | Transmitted backward channel data | 14 | - | a10 |
| 119 | Received backward channel data | 16 | - | a12 |
| 120 | Transm. backward channel line signal | 19 | - | a15 |
| 121 | Backward channel ready | 13 | - | c23 |
| 122 | Backward channel received line signal detector | 12 | - | c22 |
| 125 | Calling indicator | 22 | b16 | a19 |
| 133 | Ready for receiving | 4 | b7 | c13 |
| 140 | Loopback / Maintenance test | 21 | a8 | a18 |
| 141 | Local loopback | 18 | a7 | a14 |
| 142 | Test indicator | 25 | a12 | a22 |
| - | Power supply + 5 V | - | a2,b2,b3 | a,b,c29 |
| - | Power supply - 5 V | - | - | a,b,c26 |
| - | Power supply + 12 V | - | b1 | a,b,c28 |
| - | Power supply -12 V | - | a1 | a,b,c27 |

NOTE 1: For the usage of pole 1 of the ISO 2110 [10] interface connector see NOTE 1 of subclause 5.2.2.1.

NOTE 2: The use of power supply voltages - 5 V, + 12 V and - 12 V for plug-in DCEs is subject to national regulations.

NOTE 3: The indicated voltages of the power supply are nominal values.

## 5.3 Requirements for DTEs intended to be connected to automatic answering and/or automatic calling equipment

Requirements as contained in this subclause apply when a DTE is intended to be connected to automatic answering and/or parallel automatic calling equipment according to CCITT Recommendation V.25 [6] or to DCEs where the automatic calling and/or answering function according to CCITT Recommendation V.25 bis [7] is implemented.

### 5.3.1 General requirements

The requirements of CCITT Recommendations V.25 [6] and V.25 bis [7], respectively, apply where applicable.

Certain requirements apply concerning pause intervals between and total number of repeated calls to the same destination in the case of an unsuccessful call. These requirements are specified in ETS 300 001 [5]. For an interim period, national regulations may apply.

### 5.3.2 Interchange circuits at the interface to automatic answering and/or parallel automatic calling equipment according to CCITT Recommendation V.25, using the 200-series of interchange circuits

Table 2 contains the list of interchange circuits which are essential in a DTE for the automatic answering and/or parallel automatic calling procedure according to CCITT Recommendation V.25 [6].

**Table 2: List of interchange circuits to be provided for the parallel automatic dialling interface (CCITT Recommendation V.25 [6])**

| Interchange circuit N° | Interchange circuit name | Pole N° |
|---|---|---|
| 201 | Signal ground or common return | 7 |
| 202 | Call request | 4 |
| 203 | Data line occupied | 22 |
| 204 | Distant station connected | 13 |
| 205 (NOTE) | Abandon call | 3 |
| 206 | Digit signal (20) | 14 |
| 207 | Digit signal (21) | 15 |
| 208 | Digit signal (22) | 16 |
| 209 | Digit signal (23) | 17 |
| 210 (NOTE) | Present next digit | 5 |
| 211 | Digit present | 2 |
| 213 (NOTE) | Power indication | 6 |
| NOTE: This interchange circuit shall be continuously monitored by the DTE during the process of automatic calling. | | |

The connector and the pole assignment for this interface shall be in accordance with International Standard ISO 2110 [10], table 2, column L. The electrical characteristics of the interchange circuits shall be in accordance with CCITT Recommendation V.28 [8].

Conformance should be checked by inspection.

### 5.3.3 Interchange circuits to be used for the serial automatic calling and/or answering procedure according to CCITT Recommendation V.25 bis, using the 100-series of interchange circuits

In table 3, interchange circuits out of the 100-series of interchange circuits according to CCITT Recommendation V.24 [5] are summarised which are essential in the DTE for this type of call set-up and/or answering.

Conformance should be checked by inspection.

**Table 3: Interchange circuits for automatic calling and/or answering according to CCITT Recommendation V.25 bis [7]**

| Interchange Circuit N° | Interchange Circuit name |
|---|---|
| 102 | Signal ground or common return |
| 103 | Transmitted data |
| 104 | Received Data |
| 106 | Ready for sending |
| 107 | Data set ready |
| 108/1 | Connect Data set to line (NOTE 1) |
| 108/2 | Data terminal ready (NOTE 2) |
| 125 | Calling indicator (NOTE 3) |

NOTE 1: To be used for the direct call and/or answer controlled by the DTE.

NOTE 2: To be used for the addressed call and/or answer authorised by the DTE.

NOTE 3: Circuit 125 "calling indicator" is essential where the DTE is not capable of recognising indication INC "incoming call".

NOTE 4: All types of interface connectors as specified in subclause 3.2.3 may apply. For the appropriate pole allocations see table 1.

NOTE 5: The DTE may hold circuit 105 (where provided) ON during the automatic calling procedure, but the DCE need not recognise this condition.

### 5.3.4 Commands to be generated and indications to be recognised by a DTE for the automatic calling and/or answering procedure according to CCITT Recommendation V.25 bis

As a minimum requirement, the DTE shall be capable of generating a call request command ("call request with number provided (CRN)", "call request with number provided with the identification number (CRI)" or "call request with memory address provided (CRS)") and of detecting the INV indication. The use of these call request commands for certain applications may be a subject of national regulations.

Conformance should be checked by inspection.

If interchange circuit 125 "calling indicator" is not implemented in the DTE, the DTE shall recognise indication INC ("incoming call") at any time, even during the issue of commands.

Conformance should be checked by inspection.

# 6 Technical requirements for DTEs intended to be connected to DCEs attached to fixed connections over analogue facilities

## 6.1 General

The requirements specified below shall primarily apply when a DTE is intended to be connected to DCEs that are operated at analogue facilities (i.e. carrier sections). These requirements may also apply for connections over digital facilities. However, additional requirements may become necessary.

## 6.2 The interface

The DTE interchange circuits shall meet electrical, functional and operational requirements which are specified in relevant CCITT Recommendations of the V.series (e.g. V.10 [3], V.14 [4], V.24 [5], V.28 [8]), CEPT Recommendations (e.g. T/CD 01-14 [9]) or ISO (e.g. IS0 2110 [10], IS0 7480 [11]). For the definitions of interchange circuits see CCITT Recommendation V.24 [5]. The following subclauses attempt to summarise requirements which may otherwise only be found dispersed in the referenced international documentation.

### 6.2.1 Interchange circuits at the data interface

In DCEs, interchange circuits may be provided on a mandatory or optional basis, in accordance with existing CCITT or CEPT Recommendations.

Interchange circuits that are mandatory in certain types of DCEs need not necessarily be provided in attached DTEs (e.g. circuit 113, "transmitter signal element timing (DTE source)"). If an interchange circuit is provided in DCEs on an optional basis, its provision in DTEs may or may not be optional, as specified below.

Certain interchange circuits are required to be monitored by the DTE. "Monitoring" in the context of this ETR implies that the relevant circuit shall not only be terminated by a receiver, but that any signals on this circuit shall be recognised by the DTE and subsequent actions shall be taken, as specified herein or elsewhere in other relevant documentation.

The receivers of control circuits directed from the DCE to the DTE shall not solely be edge triggered but shall in addition recognise changed states on the respective interchange circuit.

Receiver circuits may be provided in the DCE or the DTE for which no generator is provided in the complementary equipment. Therefore, where a receiver is not connected to a generator, it is recommended that means be provided in the equipment (DTE or DCE) where the receiver is located to inhibit or disregard any possible false triggering of the receiver.

### 6.2.2 Functional and operational requirements for interchange circuits

#### 6.2.2.1 Circuit 102 "signal ground or common return"

This circuit shall always be provided.

If protective ground is provided in the DTE, it shall be possible to connect signal ground to protective ground. Whether or not the two circuits may actually be connected with each other may be a subject of national regulations.

Conformance should be checked by inspection.

NOTE 1: Pole 1 of the 25-pole interface connector according to ISO 2110 [10] is assigned for connecting the shields between tandem sections of shielded interface cables. Subject to national regulations, this contact may be connected to protective ground (if provided in the DTE), to signal ground, or may remain unconnected.

NOTE 2: It is good engineering practice to connect the shield of the interface cable only at one side (DTE or DCE) to pole 1 of the respective interface connector, to prevent ground loops.

#### 6.2.2.2 Circuit 103 "transmitted data"

This circuit is essential for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

The OFF condition of circuit 106 "indicates that the DCE is not prepared to accept data signals from the DTE" (see CCITT Recommendation V.24 [5]). Any data that is transmitted to the DCE while 106 is OFF may be lost.

Conformance should be checked by inspection.

NOTE 1: The data signalling rate on this circuit may be different from the data signalling rate on circuit 104 "received data" for certain applications ("asymmetrical duplex mode of operation").

In some applications, DTEs transmitting and receiving start-stop characters are operated with synchronous DCEs incorporating asynchronous to synchronous converters in accordance with CCITT Recommendation V.14 [4]. In these cases, only character lengths of 8, 9, 10 and 11 bits can be used, and the intracharacter signalling rate on circuit 103 shall not deviate by more than + 1 % or - 2,5 % (for the "normal rate range") and + 2,3 % or - 2,5 % (for the "extended rate range") from the nominal value. See also subclause 6.2.2.3 for further details.

Conformance should be checked by inspection.

NOTE 2: DCEs equipped with an asynchronous (start-stop) to synchronous converter according to CCITT Recommendation V.14 [4] will transmit a "start" polarity of length M to 2 M + 3 bits (where M is the number of bits per character in the selected format) as 2 M + 3 bits of "start" polarity (referred to as "break signal"). If the converter detects more than 2 M + 3 bits all of "start" polarity, it transmits all these bits as "start" polarity.

The DTE shall transmit on circuit 103 at least 2 M bits of "stop" polarity after the "start" polarity break signal before sending further data characters.

Conformance should be checked by inspection.

This circuit may be used to signal a DTE not-ready condition to the associated DCE, where this DCE has an error correcting capability according to CCITT Recommendation V.42 [12]. In this case, a DTE not-ready condition will be recognised by the DCE by the reception of a DC3 character on this circuit, and will be cleared by the reception of a DC1 character as specified in the international alphabet (IA) No.5. This method may be susceptible to misfunctioning where DC1 and DC3 characters can appear within the stream of user data, e.g. at the transfer of binary files. An alternate method of flow control using circuit 133 is therefore specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

For requirements concerning the signal quality on this circuit see Clause 8.

#### 6.2.2.3 Circuit 104 "received data"

This circuit is essential for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

NOTE 1: The data signalling rate on this circuit may be different from the data signalling rate on circuit 103 "transmitted data" for certain applications ("asymmetrical duplex mode of operation").

In some applications, DTEs transmitting and receiving start-stop characters are operated with synchronous DCEs incorporating asynchronous to synchronous converters according to CCITT Recommendation V.14

[4]. In these cases, only character lengths of 8, 9, 10 and 11 bits can be used. Furthermore, it should be noted that the length of the stop elements of received characters may be reduced by 12,5 % (in the "normal signalling rate range") or 25 % (in the "extended signalling rate range") of the nominal length, depending on the signalling rate range chosen (these values are theoretical and may be slightly exceeded in practical implementations due to technical constraints). DTEs intended for these applications shall be capable of coping with this condition. The definitions of the signalling rate ranges are contained in CCITT Recommendation V.14 [4].

NOTE 2: Where the DCE associated with the DTE concerned has an error correcting capability according to CCITT Recommendation V.42 [12], this circuit may be used to signal a DCE not-ready condition. In this case, the DTE should recognise a DC3 character received on this circuit as a DCE not-ready condition, and the reception of a DC1 character as clearance of this condition. The coding of these characters is in accordance with international alphabet (IA) No. 5. It should be noted that this method may be susceptible to misfunctioning, where DC1 and DC3 characters can appear within the stream of user data, e.g. where binary files are transferred. An alternate method of flow control is therefore specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

For requirements concerning the signal quality on this circuit see Clause 8.

#### 6.2.2.4 Circuit 105 "request to send"

This circuit is essential where the DTE is intended to be connected to half-duplex DCEs.

If this circuit is provided, it shall not be turned OFF in the transmitting mode of the DTE prior to the trailing edge of the last transmitted data bit being presented to the DCE on circuit 103 "transmitted data".

Conformance should be checked by inspection.

If this circuit is provided for the half-duplex mode of operation and is turned ON and OFF to turn around the transmitting direction of the data channel, it shall not be turned ON prior to circuit 106 "ready for sending" having gone OFF as a response to circuit 105 previously having been turned OFF.

Conformance should be checked by inspection.

#### 6.2.2.5 Circuit 106 "ready for sending"

This circuit is essential and should be monitored by the DTE.

No data shall be presented to the DCE on circuit 103 "Transmitted data" prior to circuit 106 being ON.

Conformance should be checked by inspection.

NOTE 1: The implementation of an error correcting capability inside the DCE requires that a flow control of transmitted data be feasible between the DTE and the associated DCE, with the DTE turning circuit 106 ON and OFF. Therefore, an interworking with a DCE where this feature is present and activated is not possible if circuit 106 is not implemented in the DTE. However, the rules for the flow control have not yet been established in international standardisation. DTEs may not monitor the status of circuit 106 prior to each byte to be sent, but only after blocks of data of variable length. Therefore, a buffer of suitable size needs to be implemented in the DCE. The size of this buffer is not specified in any international documentation. However, it is assumed that the minimum size should be 8 KBytes which would suffice to buffer the contents of a CRT screen, including control characters, etc...

NOTE 2: Where a circuit 107 ON to circuit 106 ON time-out function is performed by the DTE. The respective delay may be several seconds with certain types of DCEs.

NOTE 3: Where the DCE associated with the DTE concerned has an error correcting capability according to CCITT Recommendation V.42 [12], this circuit may be used to signal a DCE not-ready condition. In this case, the OFF condition of this circuit indicates a DCE not-ready condition which is cleared by again turning this circuit ON. An alternate method of flow control using DC1/DC3 characters of international alphabet (IA) No. 5 on circuit 104 is specified in CCITT Recommendation V.42 [12], paragraph 7.3.1.

#### 6.2.2.6 Circuit 107 "data set ready"

This circuit is essential and should be monitored by the DTE if also circuit 108/1 "Connect data set to line" is provided and utilised to control the DCE.

Where this circuit is implemented, it shall be used to detect either a power-off condition in the attached DCE or the disconnection of the interconnecting cable. The receiver for this circuit shall interpret these conditions as OFF conditions.

Conformance should be checked by inspection.

#### 6.2.2.7 Circuits 108/1 "connect data set to line" and 108/2 "data terminal ready"

Either of these circuits may be provided optionally (*BEL).

#### 6.2.2.8 Circuit 109 "data channel received line signal detector"

This circuit is essential and should be monitored for applications where, at the transmitting side of a connection circuit 105, "request to send" is turned ON and OFF to control flow of information and/or to turn around the transmitting direction of half-duplex DCEs.

Alternatively to this mode of operation, the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 109 is optional.

NOTE: In this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the transmitting direction of the connection has actually been turned around.

#### 6.2.2.9 Circuit 111 "data signalling rate selector (DTE source)"

The provision of this circuit in the DTE is optional (*GBR).

The circuit may be used in conjunction with DCEs which allow the selection of two or more data signalling rates. If this circuit is provided, it should be controlled by internal logic or by a manually activated switch in the DTE.

#### 6.2.2.10 Circuit 112 "data signalling rate selector (DCE source)"

This circuit is essential where:

- the DTE is intended to be connected to DCEs which may (i.e. are conditioned to) perform automatic selection between two or more data signalling rates; and

- any of the following conditions apply:

  - circuit 113 "transmitter signal element timing (DTE source)" is used; or

  - the DTE is not capable of discerning the changed data signalling rate from the lower (or higher) clock frequency of circuit 115 "Receiver signal element timing (DCE source)"; or

- the DTE is working in the asynchronous (start-stop) mode of operation (only applicable with certain types of DCEs) and it is not capable of discerning the changed data signalling rate from the received data.

(*GBR)

#### 6.2.2.11 Circuit 113 "transmitter signal element timing (DTE source)"

This circuit may be provided optionally (*GBR).

If this circuit is provided, the tolerance of the frequency of the timing signal presented on it shall be ± 0,01 % or better. The condition on this circuit shall be ON and OFF for nominally equal periods of time, and the transition from ON to OFF condition shall nominally indicate the centre of each signal element on circuit 103 "transmitted data". Further details may be found in the documentation referenced in Clause 8.

The circuit shall be turned to the OFF condition when it is implemented in the DTE but not used (because circuit 114 "transmitter signal element timing (DCE source)" is used or in case of start-stop operation).

Conformance should be checked by inspection.

NOTE: The usage of this interchange circuit may not be permissible in some networks, or it may be restricted to distinct applications only.

#### 6.2.2.12 Circuit 114 "transmitter signal element timing (DCE source)"

This circuit is essential where the DTE is intended to transmit data in a synchronous mode of operation, and circuit 113 "transmitter signal element timing (DTE source)" is not used. If this circuit is implemented in the DCE but not used (e.g. in case of start-stop operation), it shall be clamped to the OFF condition by the DCE.

NOTE 1: The condition on this circuit is ON and OFF for nominally equal periods of time (further details may be found in the documentation referenced in Clause 8).

The DTE shall present a data signal on circuit 103 "transmitted data" in which the transitions between signal elements nominally occur at the time of the transitions from OFF to ON condition of circuit 114.

Conformance should be checked by inspection.

NOTE 2: In some applications, circuit 114 may be connected to circuit 115 "receiver signal element timing (DCE source)" inside the DCE. In some DCEs this condition may be restricted to the frequency of the timing signals output on the two circuits, while the correlation of signal phase angles may be at random. The DTE should be capable of coping with this condition.

#### 6.2.2.13 Circuit 115 "receiver signal element timing (DCE source)"

This circuit is essential where the DTE is intended to receive data in a synchronous mode of operation.

NOTE: The condition of this circuit is ON and OFF for nominally equal periods of time, and a transition from ON to OFF condition nominally indicates the centre of each signal element on circuit 104 "received data". Further details may be found in the documentation referenced in Clause 8.

#### 6.2.2.14 Circuit 118 "transmitted backward channel data"

This circuit is essential where the DTE is intended to transmit data in the backward channel and to transmit separate data in the main channel (*GBR).

No data shall be presented to the DCE on this circuit prior to circuit 121 "backward channel ready" being ON.

Conformance should be checked by inspection.

#### 6.2.2.15 Circuit 119 "received backward channel data"

This circuit is essential where the DTE is intended to receive data in the backward channel and to receive separate data in the main channel (*GBR).

#### 6.2.2.16 Circuit 120 "transmit backward channel line signal"

This circuit is also essential where circuit 118 "transmitted backward channel data" is provided and a half-duplex mode of operation is intended in the backward channel (*GBR).

If this circuit is provided, it shall not be turned OFF in the transmitting mode of the DTE prior to the trailing edge of the last transmitted backward channel data bit being presented to the DCE on circuit 118 "transmitted backward channel data".

Conformance should be checked by inspection.

If this circuit is provided and is turned ON and OFF, e.g. to control flow of information and/or to turn around the transmitting direction of the backward channel, it shall not be turned ON prior to circuit 122 "backward channel received line signal detector" being OFF.

Conformance should be checked by inspection.

#### 6.2.2.17 Circuit 121 "backward channel ready"

This circuit is also essential where circuit 120 "transmit backward channel line signal" is provided (*GBR).

Where this circuit is provided, no data shall be presented on circuit 118 "transmitted backward channel data" to the DCE prior to circuit 121 being ON.

Conformance should be checked by inspection.

#### 6.2.2.18 Circuit 122 "backward channel received line signal detector"

This circuit is also essential where circuit 119 "received backward channel data" is provided and where at the transmitting side of a connection circuit 120 "transmit backward channel line signal" is turned ON and OFF to control flow of information and/or to turn around the transmitting direction of half-duplex DCEs (*GBR).

Alternatively to this mode of operation, the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 122 is optional.

NOTE: In this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the transmitting direction of the connection has actually been turned around.

#### 6.2.2.19 Circuit 133 "ready for receiving"

This circuit may be provided to control the transfer of data on circuit 104, e.g. where the DCE has an error correcting capability according to CCITT Recommendation V.42 [12]. Further details may be found in paragraph 7.3.1 of CCITT Recommendation V.42 [12], where an alternate method of flow control indication is also specified.

#### 6.2.2.20 Circuit 140 "loopback / maintenance test"

This circuit may be provided optionally.

NOTE: If this circuit is provided, its use should be as outlined in ISO 9067 [16].

#### 6.2.2.21 Circuit 141 "local loopback"

This circuit may be provided optionally.

NOTE: If this circuit is provided, its use should be as outlined in ISO 9067 [16].

#### 6.2.2.22 Circuit 142 "test indicator"

This circuit is essential and should be monitored if either circuit 140 or circuit 141, or both are provided in the DTE.

Where provided, circuit 142 going ON shall cause the DTE to cease data communication and either:

- remain in stand-by mode until circuit 142 goes OFF, after which data communication may be resumed; or

- enter a test condition.

Conformance should be checked by inspection.

NOTE: The definition of the "stand-by mode" for any given DTE is implementation dependent.

### 6.2.3 Interface connectors and electrical characteristics of the interchange circuits

The same three types of interface connectors as specified in subclause 5.2.3 of this ETR may be used.

## 7 Requirements for DTEs intended to accommodate plug-in DCEs

### 7.1 General

Table-top DCEs, DCEs to be accommodated inside racks and DCEs to be accommodated inside DTEs (referred to below as "plug-in DCEs") may be used. The following requirements refer to the accommodation of DCEs specified in CEPT Recommendation T/CD 01-12 [13] or specified and referred to as "Type I" in CEPT Recommendation T/CD 01-14 [9]. Requirements that may be posed for the accommodation of "Types II and III" in accordance with CEPT Recommendation T/CD 01-14 [9] are for further study (*GBR).

The general requirements such as dimensions, mechanical and electrical characteristics of the interface, power consumption, power supply requirements, etc..., may be found in CEPT Recommendations T/CD 01-12 [13] and T/CD 01-14 [9].

### 7.2 Technical requirements

The electrical characteristics for the interface of each type of plug-in DCE are specified in CEPT Recommendation T/CD 01-14 [9], paragraph 3.1. The DTE shall comply with those requirements at the interface it presents to the DCE. The power supply requirements are contained in CEPT Recommendations T/CD 01-12 [13], section A, paragraph 5, and T/CD 01-14 [9], paragraph 3.3.1. Three

(four, respectively) supply voltages are specified, i.e. + 5 V or - 5 V, + 12 V or - 12 V. Supply of + 5 V only may be sufficient. It is the supplier's responsibility to specify which supply voltages are provided in the DTE at the interface connector to the plug-in DCE.

The DTE or parts of it (except fuses) shall withstand a short-circuit of unlimited duration (one hour in the test) of the power supply line(s) to common return.

Conformance should be checked by inspection.

(*DEU)

## 8 Signal quality

Implementors are referred to ISO 7480 [11] and ISO 9543 [17].

These international standards specify requirements including synchronous start-stop distortion, gross start-stop distortion, minimum signal element duration, character intervals, synchronous margin, jitter, signal element duty cycle and accuracy and timing displacements.

# Annex A (informative): List of national network-dependent requirements

In some countries specific requirements apply as to the provision and/or the usage of interchange circuits of DTEs for applications in certain networks, or the design of the DTEs. For the convenience of implementors, these additions, modifications and deletions are referenced by (*nnn) in the main part of this ETR and specified below. This list of national network-dependent requirements should not be regarded as exhaustive. The requirements may, however, be subject to changes.

## A.1 Clause 1 (scope)

**Denmark (DMK):**

This ETR is to be used only for information and guidance purposes within Denmark.

For services conveyed via analogue network facilities the point of connections of privately owned equipment to the public telecommunications network is at the line side of the DCE. Approval requirements based on the CCITT Recommendation V.series interfaces are therefore not applicable in this instance.

Technical information and the Danish approval requirements for connection to digital services for the classes of apparatus (DTE) covered by this ETR may be obtained by reference to the CEPT Year Book.

**United Kingdom (GBR):**

This ETR is to be used only for information and guidance purposes within the UK.

For services conveyed via analogue network facilities the point of connections of privately owned equipment to the public telecommunications network is at the line side of the DCE. Approval requirements based on the CCITT Recommendation V.series interfaces are therefore not applicable in this instance.

Approval requirements for connection to packet switched services are contained in NET 2.

Technical information and the UK approval requirements for connection to digital services for the classes of apparatus (DTE) covered by this ETR may be obtained by reference to the CEPT Year Book.

## A.2 Clause 5

See subclause 5.2.2.6 (Circuit 107 "data set ready").

**Germany (DEU):**

Circuit 107 is essential and should be monitored for applications in the Public Switched Telephone Network (PSTN). Whenever during a data transfer phase the DCE presents an OFF condition to the DTE on circuit 107, the DTE shall immediately regard the call aborted and shall, within 2 s, confirm disconnection by switching circuit 108/1 (or 108/2) to the OFF condition for a minimum of 100 ms (both time delay values are tentative).

Conformance should be checked by inspection.

## A.3 Clause 6

See subclauses 6.2.2.4 (Circuit 105 "request to send") and 6.2.2.7 (Circuits 108/1 "connect data set to line" and 108/2 "data terminal ready").

**Belgium (BEL):**

One or both circuits 105 and 108/1 shall mandatorily be provided for X.28 leased line connections to the Packet Switched Public Data Network (PSPDN).

See subclauses 6.2.2.9 to 6.2.2.11 and 6.2.2.14 to 6.2.2.18 of the main text.

**United Kingdom (GBR):**

Interchange circuits 111, 112, 113, 118, 119, 120, 121 and 122 are not implemented on digital private circuit DCEs within the UK.

## A.4 Clause 7

See subclause 7.1 (general).

**United Kingdom (GBR):**

Clause 7 is not applicable for the United Kingdom.

See subclause 7.2 (Technical requirements).

**Germany (DEU):**

Additional technical requirements for the accommodation of a plug-in DCE inside a DTE:

- the DTE shall present the respective guiding bars and/or latching facilities (subject to the type of plug-in DCE) and the requested counterpart of the interface connector. The telecommunications line cord is a part of the DCE. However, the DTE shall provide suitable means for fixing and guiding this cord;

- the DCE shall be easily accessible;

- if it is required that the DCE may be plugged into or pulled out of the DTE while this is connected to the mains supply, the DCE shall be accessible without a necessity to open any parts of the DTE;

- if it is permissible to disconnect the DTE from mains power for accessing the DCE, a cover or equivalent part of the DTE over the DCE is allowed;

- persons who are mounting or demounting the DCE, shall not be exposed to hazardous voltages present in the DTE;

- it shall be made sure that the DTE cannot be damaged by the mounting or demounting of the DCE as long as normal care is exercised;

- no more than one person shall be needed to mount or demount a plug-in DCE;

- if screws are to be loosened at the DTE for accessing the DCE, they shall be captive and marked as access to the DCE.

# Annex B (informative): Test methods

NOTE: Throughout this Annex, the convention for the representation of signed numerals is adhered to so that numerals increase monotonously from negative infinite to positive infinite.

## B.1 Test equipment requirements

Voltages shall be measured with a voltmeter having a minimum internal resistance of 50 kΩ/V for measurements at an interface with electrical characteristics in accordance with CCITT Recommendation V.10 [3] or V.28 [8], and of 1 MΩ for measurements at an interface with electrical characteristics in accordance with CEPT Recommendation T/CD 01-14 [9].

Currents shall be measured with an ammeter having a maximum internal resistance of 5 Ω.

Waveforms and interrelationships between interchange circuits shall be measured with a dual channel storage oscilloscope having a slewing rate greater than 50 V/µs and a minimum internal resistance of 1 MΩ / 10 pF. Alternatively, a logic analyser with comparable characteristics may be used. Where conditions allow, also other test equipment with comparable characteristics and with a minimum internal resistance of 100 kΩ / 100 pF may be used. Wherever hereunder "oscilloscope" is referenced, this may apply.

Frequencies (e.g. signal element timing signals) shall be measured with a frequency counter having a tolerance of $10^{-6}$ or better.

Where resistances and capacitances are used (e.g. to terminate interchange generators) these shall have a tolerance of 2 % or better.

## B.2 Interchange equivalent circuit

Each interchange circuit may be represented as an equivalent circuit consisting of a generator and a load with defined parameters as indicated in figure B.1. This equivalent circuit is independent of whether the generator is located in the DCE and the load in the DTE or vice versa.

The impedance associated with the generator (load) includes any cable impedance on the generator (load) side of the interchange point. The equipment at both sides of the interface may implement generators as well as receivers in any connection.

The interface cabling is provided by the DTE. This introduces the line of demarcation (A - B in figure B.1) between the DTE plus interface cable and the DCE. This line is also called the interchange point and is physically implemented in the form of a connector.

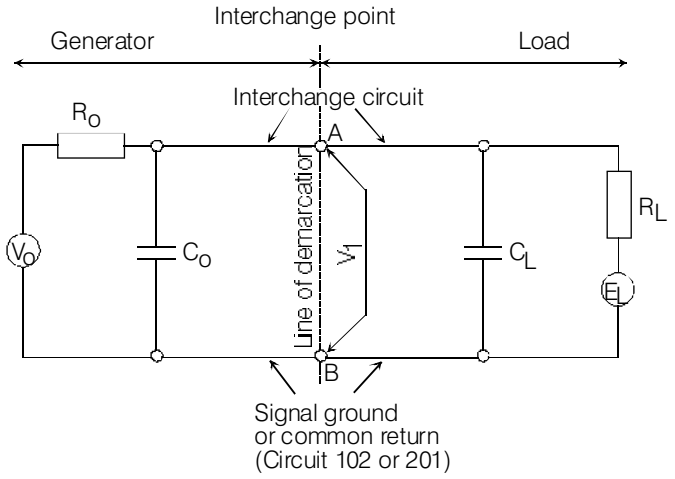



**Figure B.1: Interchange equivalent circuit**

## B.3 Electrical characteristics

Three sets of electrical characteristics may apply, as specified in the main part of this ETR, viz:

- the characteristics according to CCITT Recommendation V.10 [3];

- the characteristics according to CCITT Recommendation V.28 [8];

- the LS-TTL/CMOS compatible characteristics according to CEPT Recommendation T/CD 01-14 [9].

### B.3.1 Electrical characteristics according to CCITT Recommendation V.10

The detailed electrical characteristics and the methods to verify these may be found in the referenced CCITT Recommendation.

### B.3.2 Electrical characteristics according to CCITT Recommendation V.28

Integrated Circuits (ICs) for generators and loads according to CCITT Recommendation V.28 [8] are being offered from a number of manufacturers. Where such ICs are used in a given DTE, compliance measurements against the requirements of CCITT Recommendation V.28 [8], as specified below, may not become necessary, provided that data sheets for the ICs used are available from the respective IC manufacturer, and that any additional circuitry between the ICs and the interchange points will have no material affect upon the electrical characteristics of the respective interchange circuit (e.g. it does not include inductive components, nor only minimal resistances or capacitances).

A number of the electrical characteristics specified hereunder reference a "test capacitance of 2 500 pF". This capacitance is understood as to include the capacitance of the interchange cable. If the interchange cable is an integral part of the DTE, from which it can not be disconnected, the capacitance of the interchange cable (if known) shall be subtracted from the value of 2 500 pF. Otherwise the interchange cable shall be removed from the DTE and a fixed capacitance of 2 500 pF directly applied at the interchange point.

#### B.3.2.1 Generator characteristics

Many existing interchange circuit generators do not provide for meeting the maximum rise time requirements of CCITT Recommendation V.28 [8] when driving a capacitance of greater than 2 500 pF, the maximum permitted load capacitance (CL) which includes the capacitance of the DTE supplied interface cable.

##### B.3.2.1.1 Protection against short-circuit conditions

The generator shall not be damaged by the application of the following tests after which the generator shall comply with the requirements of subclauses 5.2.1.3, 5.2.1.4 and 5.2.1.5.

a) Generator in the binary ZERO (ON) state. The following three tests shall be applied sequentially for a period of 10 minutes each:

   1) the generator output at the interchange point shall be connected to common return;

   2) the generator output at the interchange point shall be connected to a load of 3 000 Ω, where the open-circuit voltage (EL) of the load is + 2 V;

   3) the generator output at the interchange point shall be connected to a load of 3 000 Ω, where the open-circuit voltage (EL) of the load is - 2 V.

b) Generator in the binary ONE (OFF) state. The following three tests shall be applied sequentially for a period of 10 minutes each:

   1) the generator output at the interchange point shall be connected to common return;

2) the generator output at the interchange point shall be connected to a load of 3 000 Ω, where the open-circuit voltage (EL) of the load is + 2 V;

3) the generator output at the interchange point shall be connected to a load of 3 000 Ω, where the open-circuit voltage (EL) of the load is - 2 V.

NOTE 1: An ammeter may be connected at the interchange point to measure the steady state maximum current for each test.

NOTE 2: a)1/2 and b)1/2 do not represent the worst case where multiple short circuits occur.

#### B.3.2.1.2 Generator output current limit

The output current of the generator with a short circuit applied between the generator output at the interchange point and any other interchange circuit shall not exceed 0,5 A in any state of the DTE.

Conformance should be checked by connecting a generator whose output is held in the binary ONE (OFF) state to a generator whose output is held in the binary ZERO (ON) state and measuring the current.

#### B.3.2.1.3 Generator output voltage limit

The open circuit generator voltage shall not exceed + 25 V.

Conformance should be checked by measurement.

#### B.3.2.1.4 Generator output voltage limit under maximum load conditions

The output voltage with reference to common return, as measured at the interchange point, shall not be less than + 5 V when the generator output is terminated in a resistance of 3 000 Ω.

Conformance should be checked by measurement.

#### B.3.2.1.5 Generator output voltage limit under minimum load conditions

The output voltage with reference to common return, as measured at the interchange point, shall not exceed + 15 V when the generator output is terminated in a resistance of 7 000 Ω.

Conformance should be checked by measurement.

### B.3.2.2 Load characteristics

#### B.3.2.2.1 Load resistance

The load resistance (RL) shall have a minimum value of 3 000 Ω and a maximum value of 7 000 Ω.

Conformance should be checked by applying a voltage (VL) of:

a) 3 V, and measuring 1,7 mA > IL > 0,143 mA;

b) 15 V, and measuring 5,7 mA > IL > 1,86 mA;

c) - 3 V, and measuring - 1,7 mA < IL < - 0,143 mA;

d) - 15 V, and measuring - 5,7 mA < IL < - 1,86 mA.

The test conditions for measuring the load impedance are shown in figure B.2.

#### B.3.2.2.2 Maximum load open-circuit voltage

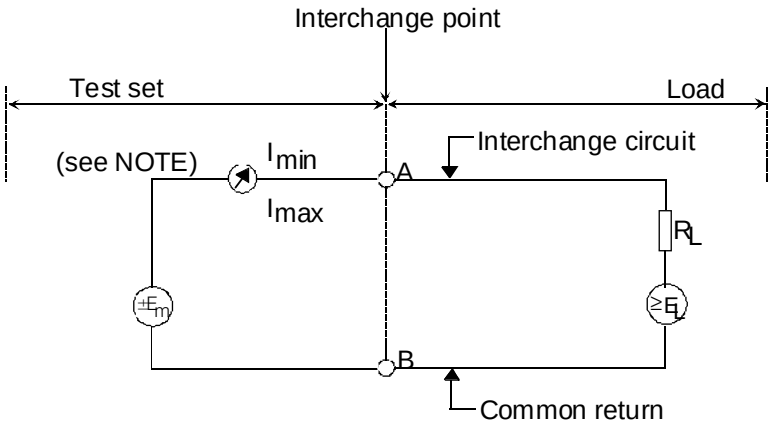
The open-circuit voltage (EL) shall not exceed + 2 V when disconnected from the generator.

It is recommended to check conformance by disconnecting the generator and measuring the voltage at the interchange point.

#### B.3.2.2.3 Maximum load shunt capacitance

The total load shunt capacitance (CL) as seen from the interchange point shall not exceed 2 500 pF.

Conformance may be checked by evaluating the circuitry diagram. Alternatively, a special capacitance measurement may be applied (for further study).




NOTE: The internal resistance of the ammeter shall be much less than the load resistance ($R_L$).

**Figure B.2: Load resistance measuring set-up**

#### B.3.2.2.4 Load impedance

The reactive component of the load impedance as measured at the interchange point with an open-circuit condition shall be capacitive in the frequency range from 0 to 20 kHz.

Conformance may be checked by evaluating the circuitry diagram. Alternatively, a special capacitance measurement may be applied (for further study).

### B.3.2.3 Transitions between significant signal states

The region between + 3 V and - 3 V is referred to as the transition region.

#### B.3.2.3.1 Waveform

Interchange signals entering the transition region shall proceed through this region to the opposite signal state in a monotonous progression; i.e. a transition from - 3 V to + 3 V shall have no negative going component in the waveform; a transition from + 3 V to - 3 V shall have no positive going component in the wave-form.

Conformance should be checked by means of a storage oscilloscope connected across points A and B (see figure B.1) in both of the following cases:

a) with a purely resistive load of 7 000 Ω;

b) with a resistive load of 3 000 Ω in parallel with the test capacitance of 2 500 pF.

#### B.3.2.3.2 Maximum transition time on control interchange circuits

The time required for the signal to traverse the transition region during a change state shall not exceed 1 ms.

It is recommended to check conformance by means of an oscilloscope connected across points A and B (see figure B.1) with the generator terminated in a load of 3 000 Ω in parallel with a capacitance of 2 500 pF.

#### B.3.2.3.3 Maximum transition time on data and timing circuits

The time required for the signal to traverse the transition region during a change in signal state shall not exceed 1 ms or 3 % of the nominal element period on the interchange circuit, whichever is the lesser.

It is recommended to check conformance by means of an oscilloscope connected across points A and B (see figure B.1) with the generator terminated in a load of 3 000 Ω in parallel with a capacitance of 2 500 pF.

#### B.3.2.3.4 Maximum instantaneous rate of voltage change

It shall not be possible for an interchange circuit to produce an instantaneous rate of voltage change of more than 30 V/µs.

Conformance should be checked by means of an oscilloscope connected across points A and B (see figure B.1) with the generator terminated in a load of 7 000 Ω.

### B.3.3 Electrical characteristics according to CEPT Recommendation T/CD 01-14

According to conventions in the specifications of (LS-) TTL integrated circuits, a load current is associated with a positive sign when it is directed towards the generator, and is associated with a negative sign when it is directed towards the receiver (load).

#### B.3.3.1 Generator characteristics

#### B.3.3.1.1 Protection against short-circuit condition

A generator shall not be damaged when it is connected to common return, and a binary ONE (OFF) state and a binary ZERO (ON) state are sequentially applied for a period of 10 minutes each.

After this test, the generator shall comply with subclauses 5.3.1.2, 5.3.1.3 and 5.3.1.4.

Conformance should be checked by measurement.

#### B.3.3.1.2 Generator output voltage limit under maximum load condition

The output voltage with reference to common return, as measured at the generator output at the interchange point when a binary ONE (OFF) condition is applied, shall not be less than 4 V when the generator is terminated in a resistance of 100 kΩ, connected to common return.

Conformance should be checked by measurement.

#### B.3.3.1.3 Generator output voltage limit under minimum load condition

The output voltage with reference to common return, as measured at the generator output at the interchange point when a binary ZERO (ON) condition is applied, shall not be greater than 0,4 V when a load current of 0,4 mA flows into the generator.

Conformance should be checked by measurement with a measuring set-up in accordance with figure B.3.

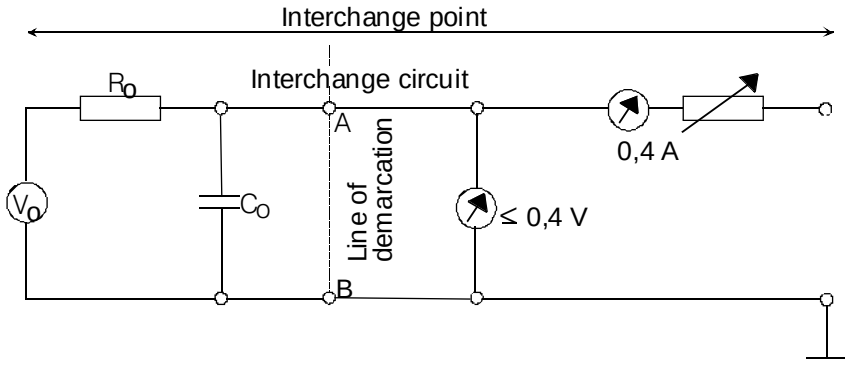



**Figure B.3: Minimum load measuring set-up**

#### B.3.3.1.4 Generator output voltage limit

The open circuit generator voltage shall not be greater than 5,5 V for the binary ONE (OFF) state and not be less than - 0,5 V for the binary ZERO (ON) state.

Conformance should be checked by measurement.

### B.3.3.2 Load characteristics

#### B.3.3.2.1 Load resistance

The load resistance of this interface depends on the voltage applied to the load.

Conformance is tested by applying a voltage of:

a) 4 V and measuring a current > - 400 µA;

b) 0,4 V and measuring a current < 0,4 mA.

The test conditions are the same as for the CCITT Recommendation V.28 [8] type interface.

#### B.3.3.2.2 Load thresholds

The load shall consider the interchange circuit to be in the binary ONE (OFF) condition when the voltage on the interchange circuit measured at the interchange point is between 3,6 V and 5,5 V. The load shall consider the interchange circuit to be in the binary ZERO (ON) condition when the voltage on the interchange circuit measured at the interchange point is between 0,7 V and - 0,5 V.

Conformance should be checked by measurement.

#### B.3.3.2.3 Maximum load shunt capacitance

The total effective load shunt capacitance (CL) as measured at the interchange point shall not exceed 50 pF.

Conformance may be checked by evaluating the circuit diagram. Alternatively, a special capacitance measurement may be applied (under study).

#### B.3.3.3 Transition between significant signal states

The region between 0,7 V and 3,6 V is referred to as the transition region.

##### B.3.3.3.1 Waveform

Interchange signals entering the transition region shall proceed through this region to the opposite signal state in a monotonous progression, i.e. a transition from 0,7 V to 3,6 V shall have no negative going component in the waveform; a transition from 3,6 V to 0,7 V shall have no positive going component in the waveform.

Conformance should be checked by means of a storage oscilloscope connected across points A and B when the generator is terminated in a load of the same equipment in parallel with a capacitance of 50 pF minus the capacitance of the oscilloscope probe (the specification of a normalized load is for further study).

##### B.3.3.3.2 Maximum transition times

The time required for the signal to traverse the transition region during a change in signal state shall not exceed 500 ns.

Conformance should be checked by means of an oscilloscope connected across points A and B when the generator is terminated in a load of the same equipment in parallel with a capacitance of 50 pF minus the capacitance of the oscilloscope probe (the specification of a normalised load is for further study).

## B.4 Provision of interchange circuits

In Clauses 5 and 6 of this ETR, indications are given as to under which conditions individual interchange circuits are essential.

Conformance should be checked by comparing these indications with the intended application(s).

## B.5 Logical interrelationships between interchange circuits

In Clauses 5 and 6 of this ETR, logical interrelationships are stated for various interchange circuits.

Conformance should be checked by means of a dual channel oscilloscope or of a logic analyser.

## History

| Document history | |
|---|---|
| December 1992 | First Edition |
| March 1996 | Converted into Adobe Acrobat Portable Document Format (PDF) |
| | |
| | |
| | |