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FOREWORD

ETSI Technical Reports (ETRs) are informative documents resulting from ETSI studies which are not appropriate for European Telecommunication Standard (ETS) or Interim - European Telecommunication Standard (I-ETS) status. An ETR may be used to publish material which is either of an informative nature, relating to the use or application of ETSs or I-ETSs, or which is immature and not yet suitable for formal adoption as an ETS or I-ETS.

This ETR has been produced by Terminal Equipment (TE) Technical Committee of the European Telecommunications Standards Institute (ETSI) under the auspices of Question TA6 regarding the harmonization of the technical requirements for data terminal equipment to be attached to high speed digital fixed-connection services considering that several Network Operators currently offer such services, often with different technical requirements.

1 SCOPE

This document contains technical advice for designers of data terminal equipment intended to be connected to high speed digital fixed-connection services, i.e. permanent or semi-permanent high speed leased circuits presenting a digital interface to the user. This document is to be used for information and guidance purposes only.

Data terminal equipment to be connected to these circuits will have to be equipped with a corresponding digital interface. The characteristics of the digital interface, insofar as they are relevant for the proper interworking of the circuits concerned, are the subject of this document. At the same time the technical requirements are intended to ensure that the service available to users of public telecommunications systems is not interfered with, nor that any public system will be adversely affected. Safety requirements are included for the protection of personel operating the public telecommunication systems.

Digital services may be based on a variety of data rates and user interfaces and may or may not require the terminal to adhere to a certain protocol in order to interwork properly with the service concerned. The present technical requirements are applicable for terminals requiring a transparent, i.e. protocol independent, circuit with a data rate of 48 kbit/s or higher, employing a CCITT G-series interface, V-series interface or a CEPT T/CD 01-14 interface. In particular the following combinations are considered:

- data terminal equipments with a data rate of 64 kbit/s, n × 64 kbit/s, (n_{max} = 31), 2 048 kbit/s, 8 448 kbit/s, 34 368 kbit/s, and 139 264 kbit/s employing a G.703 (G.704) interface;

- data terminal equipments with a data rate of 48 kbit/s, 56 kbit/s, 64 kbit/s and n × 64 kbit/s (n_{max} = 31) employing a V-series interface (V.35, V.36);

- data terminal equipments with a data rate of 48 kbit/s, 56 kbit/s, 64 kbit/s, n × 64 kbit/s (n_{max} = 31), 2 048 kbit/s or 8 448 kbit/s, employing a CEPT T/CD 01-14 interface.

These technical requirements are not applicable for terminals with data rates lower than 48 kbit/s and terminals employing an X.21 interface or an ISDN interface according to the I-series Recommendations.

This document is applicable only if the relevant type of service is being provided in the Member Country concerned. By no means does the document impose any obligation to provide any particular type of service.

NOTE 1: Def. or semi-permanent, see CCITT Blue Book Volume III, Fascicle III.5.

NOTE 2: The provision of synchronous interfaces at 8 448 kbit/s and 34 368 kbit/s are foreseen.

2 CONTENTS

3 GENERAL REQUIREMENTS

The requirements hereunder will apply irrespective of the application of the data terminal equipment concerned in one of the possible services.

3.1 Safety requirements

Data terminal equipment to be connected to digital circuits shall comply with CEPT Recommendation T/CD 04-03, European Standard EN 60950 and prEN 41003.

NOTE: For an interim period, some specific national safety requirements may still apply. Existing national safety requirements may be indicated in Annex A to this document.

4 NETWORK INTERFACE REQUIREMENTS

4.1 Requirements for connection to a 64 kbit/s G.703 interface

4.1.1 Data rate and timing

The terminal shall operate with a data rate of 64 kbit/s ± 100 ppm. Timing arrangements shall be according to the co-directional version of the G.703 interface, i.e. the timing for the transmitted signal shall be derived from the received signal.

4.1.2 Interface coding

The coding of the signals transmitted via the terminal interface shall be in accordance with CCITT Recommendation G.703 § 1.2.1.1.5.

It is not mandatory for the terminal to either utilize the 8 kHz timing signal specified in CCITT Recommendation G.703 § 1.2.1 or include such timing in its transmitted signal. The terminal shall however function correctly when an 8 kHz timing signal is included in its input signal.

4.1.3 Interface signal characteristics

The interface signal shall have the following characteristics, measured with a test load impedance of 120 ohms:

-	nominal peak voltage of a mark (pulse)	1.0 V
-	peak voltage of a space (no pulse)	0 ± 0.10 V
-	nominal pulse width	3.9 µs (single pulse) / 7.8 µs (double pulse)
-	ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
-	ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

The interface signal pulse shapes shall be as indicated in figs. 1 and 2 for single and double pulses respectively. The masks shown apply to positive as well as to negative polarity pulses.

The terminal shall continue to operate correctly with the received signal connected via a cable with up to 3 dB attenuation, measured at a frequency of 128 kHz.

The cable should be specified as having an attenuation characteristic which is proportional to $\sqrt{f}$.

To provide nominal immunity against interference, the terminal input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s co-directional signal, and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal.

The interfering signal should have a bit rate within the limits specified in this document but should not be synchronous with the wanted signal.

The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal to interference ratio of 20 dB.

The binary content of the interfering signal should comply with CCITT Rec. 0.152 (2E11-1 bit period).

No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the terminal input port.

4.1.4 Connection requirements

The terminal shall be connected to the digital circuit by one symmetrical cable pair per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. If screened symmetrical pairs are used, provision shall be made for connecting the screen to the terminal signal earth. The characteristic impedance of the circuit at the termination point is 120 ohms.

4.1.5 Return loss

The return loss as measured at the terminal digital input port shall be better than the boundary values indicated below, when referred to 120 ohms.

Frequency range (kHz)	Minimum return loss (dB)
4 - 13	12
13 - 256	18
256 - 384	14

4.1.6 Balance to functional earth

The balance to functional earth of the terminal input and output port shall be better than the boundary values indicated in fig. 3 for all operating and non-operating conditions of the terminal, with the power supply either switched on or off. The measurement set-up used to test this parameter is given in fig. 4. The value of resistor R in figure 4 shall be 60 ohms ± 0,1 %.

4.1.7 Jitter characteristics

4.1.7.1 Jitter production

When supplied with a jitter-free input signal, the jitter present in the output signal from the terminal shall not exceed 0.78 µs peak-to-peak (0.05 unit intervals), when measured via a band-pass filter with cut-off frequencies of 20 Hz and 20 kHz and a roll-off of 20 dB/decade.

4.1.7.2 Jitter transfer

The jitter transfer characteristics of the terminal, expressed as 20 times the logarithm of the ratio of the jitter amplitudes of the transmitted and the received signal, shall be better than the boundary values indicated in fig. 5. A test signal containing the sequence of binary 1 000 shall be used.

4.1.7.3 Jitter tolerance

The terminal shall be able to tolerate an input signal containing jitter with the characteristics depicted in fig. 6. This will be measured using a pseudorandom signal with a lenght of 2E11 - 1 bits (CCITT Rec. 0.152), sine-wave modulated in time in accordance with the frequency characteristics shown in fig. 6.

4.1.8 Overvoltage protection requirement

The input and output ports shall withstand without damage 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of UVdc (5 negative and 5 positive impulses). For the definition of this impulse see CCITT Rec. K.17 Ref. 1 (IEC 60-2/1973).

At the interface for symmetrical pairs:

- Differential mode: with a pulse of generator of Fig. 20, the value of U is under study (a value of 20 V has been mentioned).

- Common mode: with a pulse generator of Fig. 21, U = 100 Vdc.

Possible pulse generators are described in Fig. 20 and Fig. 21.
(Ref. CCITT Rec. G.703 Annex B, Blue Book).

4.2 Requirements for connection to a nx64 kbit/s and 2 048 kbit/s G.703 interface

4.2.1 Data rate and timing

The terminal shall operate with a data rate of 2 048 kbit/s ± 50 ppm. Subject to national regulations, the timing for transmitted signal may be derived from the received signal or from an internal oscillator in the terminal or from an external source.

4.2.2 Interface coding

The signals transmitted via the terminal interface shall comply with the HDB3 coding rules as described in CCITT Recommendation G.703 Annex A.

4.2.3 Interface signal characteristics

The interface signal shall have the characteristics of one of the following options when measured with a test load impedance of either 75 ohms or 120 ohms as appropriate:

		75 ohms	120 ohms
-	nominal peak voltage of a mark (pulse)	2.37 V	3 V
-	peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
-	nominal pulse width	244 ns	
-	ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
-	ratio of widths of positive and negative pulses measured at the nominal half amplitude	0.95 to 1.05	

The interface signal pulse shape shall be as indicated in fig. 7.

The mask shown applies to positive as well as to negative polarity pulses.

The terminal shall continue to operate correctly with the received signal connected via a cable up to 6 dB attenuation, measured at a frequency of 1 024 kHz.

The cable should be specified as having an attenuation characteristic which is directly proportional to $\sqrt{f}$.

To ensure adequate immunity against interference, the terminal input ports are required to meet the following requirements:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal.

The interfering signal should have a bit rate within the limits specified in this document but should not be synchronous with the wanted signal.

The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 ohms (in the case of symmetrical-pair interface), to give a signal to interference ratio of 18 dB.

The binary content of the interfering signal should comply with CCITT Rec. 0.151 (2E15-1 bit period).

No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the terminal input port.

In table 2 gives information relating to characteristic impedance as implemented in different countries.

4.2.4 Connection requirements

4.2.4.1 Connection by coaxial cables

The terminal shall be connected to the digital circuit by one coaxial cable per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. Provisions shall be made for connecting and disconnecting the outer conductor of each coaxial cable to the data terminal equipment signal earth.

The characteristic impedance of the circuit at the termination point is 75 ohms.

4.2.4.2 Connection by symmetrical cables

The terminal shall be connected to the digital circuit by one symmetrical cable pair per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. If screened symmetrical pair are used, provisions shall be made for connecting the screen to the terminal signal earth.

The characteristic impedance of the circuit at the termination point is 120 ohms.

4.2.5 Return loss

The return loss as measured at the terminal digital input port shall be better than the boundary values indicated below, when referred to 75 ohms or 120 ohms as appropriate.

Frequency range (kHz)	Minimum return loss (dB)
51 - 102	12
102 - 2 048	18
2 048 - 3 072	14

4.2.6 Jitter characteristics

4.2.6.1 Jitter production

When supplied with a jitter-free input signal or when operating with an internal oscillator, the jitter present in the output signal from the terminal shall not exceed 24.4 ns peak-to-peak (0.05 unit intervals), when measured via a band-pass filter with cut-off frequencies of 20 Hz and 100 kHz and a roll-off of 20 dB/decade.

4.2.6.2 Jitter transfer

The jitter transfer characteristic of the terminal, expressed as 20 times the logarithm of the ratio of the jitter amplitudes of the transmitted and the received signal, shall be better than the boundary values indicated in fig. 8. A test signal containing the sequence of binary 1 000 shall be used.

4.2.6.3 Jitter tolerance

The terminal shall be able to tolerate an input signal containing jitter with the characteristics depicted in fig. 9. This will be measured using a pseudorandom signal with a lenght of 2E15 - 1 bits (CCITT Rec. 0.151), sine-wave modulated in time in accordance with the frequency characteristics shown in fig. 9.

NOTE: The value for 36.9 UI represents a relative deviation between the incoming signal and the internal timing local signal derived from the reference clock.

4.2.7 Frame structure

2 048 kbit/s digital circuits will in most cases form part of a transmission network with higher order digital systems. Depending on the way in which the network has been implemented, requirements may exist concerning a frame structure for the digital signal transmitted by the equipment. Three categories may be distinguished:

a) No requirements exist for this category of network concerning a frame structure for the transmitted signal.

b) This category of network requires from the terminal a frame structure according to CCITT Recommendation G.704. Time slot 0 is not available for the user of the circuit, see table 1. The remaining 1 984 kbit/s can however be used without restrictions.

c) This category of network requires that both time slots 0 and 16 are used in a particular way and are thus not available for the user of the circuit. The remaining 1 920 kbit/s can be used without further restrictions.

In table 2 gives information relating to frame structure as implemented in different countries.

4.2.8 Interface at 2 048 kbit/s carrying nx64 kbit/s

The electrical characteristics shall follow § 4.2 in this document.

For the accomodation of nx64 kbit/s time slots in the 2 048 kbit/s frame two situations are envisaged, see CCITT Rec. G.704, § 5.2.1 and § 5.2.2, Blue Book.

4.2.9 Overvoltage protection requirement

The input and output ports shall withstand without damage 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of UVdc (5 negative and 5 positive impulses). For the definition of this impulse see CCITT Rec. K 17 Ref. 1 (IEC 60-2/1973).

- At the interface for coaxial pairs:
  - Differential mode: with a pulse generator of Fig. 20, the value of U is under study.
  - Common mode: under study.
- At the interface for symmetrical pairs:
  - Differential mode: with a pulse generator of Fig. 20, the value of U is under study (a value of 20 V has been mentioned).
  - Common mode: with a pulser generator of Fig. 21, U = 100 Vdc.

Possible pulse generators are described in Fig. 20 and Fig. 21.
(Reference CCITT Rec. G.703 Annex B, Blue Book).

4.3 Requirements for connection to a 8 448 kbit/s G.703 interface

4.3.1 Data rate and timing

The terminal shall operate with a data rate of 8 448 kbit/s ± 30 ppm. Subject to national regulations, the timing for the transmitted signal may be derived from the received signal or from an internal oscillator in the terminal or from an external source.

4.3.2 Interface coding

The signals transmitted via the terminal interface shall comply with the HDB3 coding rules as described in CCITT Recommendation G.703 Annex A.

4.3.3 Interface signal characteristics

The interface signal have the following characteristics, measured with a test load impedance of 75 ohms:

-	nominal peak voltage of a mark (pulse)	2.37 V
-	peak voltage of a space (no pulse)	0 ± 0.237 V
-	nominal pulse width	59 ns
-	ratio of the amplitudes positive and negative pulses at the centre of pulse interval	0.95 to 1.05
-	ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

The interface signal pulse shape shall be as indicated in fig. 10.

The mask shown applies to positive as well as to negative polarity pulses.

The terminal shall continue to operate correctly with the received signal connected via a cable, with up to 6 dB attenuation, measured at a frequency of 4 224 kHz.

The cable should be specified as having an attenuation characteristic which is directly proportional to $\sqrt{f}$

To ensure adequate immunity against interference, the terminal input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in as the wanted signal.

The interfering signal should have a bit rate within the limits specified in this document but should not be synchronous with the wanted signal.

The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal to interference ratio of 20 dB.

The binary content of the interfering signal should comply with CCITT Rec. 0.151 (2E15-1 bit period).

No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the terminal input port.

4.3.4 Connection requirements

The terminal shall be connected to the digital circuit by one coaxial cable per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. Provisions shall be made for connecting the outer conductor of the coaxial cable to the data terminal equipment signal ground. The characteristic impedance of the circuit at the termination point is 75 ohms.

4.3.5 Return loss

The return loss as measured at the terminal digital input port shall be better than the boundary values indicated below, when referred to 75 ohms.

Frequency range (kHz)	Minimum return loss (dB)
211 - 422	12
422 - 8 448	18
8 448 - 12 672	14

4.3.6 Jitter characteristics

4.3.6.1 Jitter production

When supplied with a jitter-free input signal or when operating with an internal oscillator, the jitter present in the output signal from the terminal shall not exceed 5.9 ns peak-to-peak (0.05 unit intervals), when measured via a band-pass filter with cut-off frequencies of 20 Hz and 400 kHz and a roll-off of 20 dB/decade.

4.3.6.2 Jitter transfer

The jitter transfer characteristic of the terminal, expressed as 20 times the logarithm of the ratio of the jitter amplitudes of the transmitted and the received signal, shall be better than the boundary values indicated in fig. 11. A test signal containing the sequence of binary 1 000 shall be used.

4.3.6.3 Jitter tolerance

The terminal shall be able to tolerate an input signal containing jitter with the characteristics depicted in fig. 12. This will be measured using a pseudorandom signal with a lenght of 2E15 - 1 (CCITT Rec. 0.151), sine-wave modulated in time in accordance with the frequency characteristics shown in fig. 12.

NOTE: The value for 152 UI represents a relative deviation between the incoming signal and the internal timing local signal derived from the reference clock.

4.3.7 Frame structure

8 448 kbit/s digital circuits will in most cases form part of a transmission network with higher order digital systems. Depending on the way in which the network has been implemented, requirements may exist concerning a frame structure for the digital signal transmitted by the equipment. Two categories may be distinguished:

a) No requirements exist for this category concerning a frame structure for the transmitted signal.

b) This category of network requires from the terminal a frame structure according to CCITT Rec. G.704.

4.3.8 Overvoltage protection requirement

The input and output ports shall withstand without damage 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of UVdc (5 negative and 5 positive impulses). For the definition of this impulse see Rec. K 17 Ref. 1 (IEC 60-2/1973).

At the interface for coaxial pairs:

- Differential mode: with a pulse generator of Fig. 20, the value of U is under study.
- Common mode: under study.

Possible pulse generator is described in Fig. 20.
(Reference CCITT Rec. G.703 Annex B, Blue Book).

4.4 Requirements for connection to a 34 368 kbit/s G.703 interface

4.4.1 Data rate and timing

The terminal shall operate with a data rate of 34 368 kbit/s $\pm$ 20 ppm. Subject to national regulations, the timing for the transmitted signal may be derived from the received signal or from an internal oscillator in the terminal or from an external source.

4.4.2 Interface coding

The signals transmitted via the terminal interface shall comply with the HDB3 coding rules as described in CCITT Recommendation G.703 Annex A.

4.4.3 Interface signal characteristics

The interface signal have the following characteristics, measured with a test load impedance of 75 ohms:

- nominal peak voltage of a mark (pulse)	1.0 V
- peak voltage of a space (no pulse)	0 $\pm$ 0.1 V
- nominal pulse width	14.55 ns
- ratio of the amplitudes of positive and negative pulses at the centre of pulse interval	0.95 to 1.05
- ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05

The interface signal pulse shape shall be as indicated in fig. 13.

The mask shown applies to positive as well as to negative polarity pulses.

The terminal shall continue to operate correctly with the received signal connected via a cable with up to 12 dB attenuation, measured at a frequency of 17 184 kHz.

The cable should be specified as having an attenuation characteristic which is proportional to $\sqrt{f}$.

To ensure adequate immunity against interference, the terminal input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in as the wanted signal.

The interfering signal should have a bit rate within the limits specified in this document but should not be synchronous with the wanted signal.

The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal to interference ratio of 20 dB.

The binary content of the interfering signal should comply with CCITT Rec. 0.151 (2E23-1 bit period).

No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the terminal input port.

4.4.4 Connection requirements

The terminal shall be connected to the digital circuit by one coaxial cable per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. Provisions shall be made for connecting the outer conductor of the coaxial cable to the data terminal equipment signal ground. The characteristic impedance of the circuit at the termination point is 75 ohms.

4.4.5 Return loss

The return loss as measured at the terminal digital input port shall be better than the boundary values indicated below, when referred to 75 ohms.

Frequency range (kHz)	Minimum return loss (dB)
859 - 1 718	12
1 718 - 34 368	18
34 368 - 51 552	14

4.4.6 Jitter characteristics

4.4.6.1 Jitter production

When supplied with a jitter-free input signal or when operating with an internal oscillator, the jitter present in the output signal from the terminal shall not exceed 1.455 ns peak-to-peak (0.05 unit intervals), when measured via a band-pass filter with cut-off frequencies of 100 Hz and 800 kHz and a roll-off of 20 dB/decade.

4.4.6.2 Jitter transfer

The jitter transfer characteristic of the terminal, expressed as 20 times the logarithm of the ratio of the jitter amplitudes of the transmitted and the received signal, shall be better than the boundary values indicated in fig. 14. A test signal containing the sequence of binary 1 000 shall be used.

4.4.6.3 Jitter tolerance

The terminal shall be able to tolerate an input signal containing jitter with the characteristics depicted in fig. 15. This will be measured using a pseudorandom signal with a lenght of 2E23 - 1 (CCITT Rec. 0.151), sine-wave modulated in time in accordance with the frequency characteristics shown in fig. 15.

4.4.7 Frame structure

34 368 kbit/s digital circuits will in most cases form part of a transmission network with higher order digital systems. Depending on the way in which the network has been implemented, requirements may exist concerning a frame structure for the digital signal transmitted by the equipment. Two categories may be distinguished:

a) No requirements exist for this category concerning a frame structure for the transmitted signal.

b) This category of network requires from the terminal a frame structure according to CCITT Rec. G.xxx (for further study).

4.4.8 Overvoltage protection requirement

The input and output ports shall withstand without damage 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of UVdc (5 negative and 5 positive impulses). For the definition of this impulse see Rec. K 17 Ref. 1 (IEC 60-2/1973).

At the interface for coaxial pairs:

- Differential mode: with a pulse generator of Fig. 20, the value of U is under study.
- Common mode: under study.

Possible pulse generator is described in Fig. 20.
(Ref. CCITT Rec. G.703 Annex B, Blue Book).

4.5 Requirements for connection to a 139 264 kbit/s G.703 interface

4.5.1 Data rate and timing

The terminal shall operate with a data rate of 139 264 kbit/s ± 15 ppm. Subject to national regulations, the timing for the transmitted signal may be derived from the received signal or from an internal oscillator in the terminal or from an external source.

4.5.2 Interface coding

The signals transmitted via the terminal interface shall comply with the CMI coding rules as described in CCITT Recommendation G.703 § 9.1.

4.5.3 Interface signal characteristics

The interface signal have the following characteristics, measured with a test load impedance of 75 ohms:

- peak-to-peak voltage	1 ± 0.1 V
- rise time between 10 % and 90 % amplitudes of the measured "steady state" amplitude	≤ 2 ns
- transition timing tolerance (referred to the mean value of the 50 % amplitude points of negative transitions)	Negative transitions: ± 0.1 ns Positive transitions at unit interval boundaries: ± 0.5 ns Positive transitions at mid-unit interval: ± 0.35 ns

The interface signal pulse shape shall be as indicated in fig. 16 and 17.

The terminal shall continue to operate correctly with the received signal connected via a cable with up to 12 dB attenuation, measured at a frequency of 70 MHz.

The cable should be specified as having an attenuation characteristic which is directly proportional to $\sqrt{f}$.

4.5.4 Connection requirements

The terminal shall be connected to the digital circuit by one coaxial cable per direction. The transmit and receive directions with respect to the circuit termination point shall be properly indicated. Provisions shall be made for connecting the outer conductor of the coaxial cable to the data terminal equipment signal ground. The characteristic impedance of the circuit at the termination point is 75 ohms.

4.5.5 Return loss

The return loss as measured at the terminal digital output port shall be better than 15 dB over frequency range 7 MHz to 210 MHz, when referred to 75 ohms.

The return loss characteristics at the input port shall be the same as that specified for the output port.

4.5.6 Jitter characteristics

4.5.6.1 Jitter production

When supplied with a jitter-free input signal or when operating with an internal oscillator, the jitter present in the output signal from the terminal shall not exceed 0.359 ns peak-to-peak (0.05 unit intervals), when measured via a band-pass filter with cut-off frequencies of 200 Hz and 3 500 kHz and a roll-off of 20 dB/decade.

4.5.6.2 Jitter transfer

The jitter transfer characteristic of the terminal, expressed as 20 times the logarithm of the ratio of the jitter amplitudes of the transmitted and the received signal, shall be better than the boundary values indicated in fig. 18. A test signal containing the sequence of binary 1 000 shall be used.

4.5.6.3 Jitter tolerance

The terminal shall be able to tolerate an input signal containing jitter with the characteristics depicted in fig. 18. This will be measured using a pseudorandom signal with a lenght of 2E23 - 1 (CCITT Rec. 0.151), sine-wave modulated in time in accordance with the frequency characteristics shown in fig. 19.

4.5.7 Frame structure

139 264 kbit/s digital circuits will in most cases form part of a transmission network with higher order digital systems. Depending on the way in which the network has been implemented, requirements may exist concerning a frame structure for the digital signal transmitted by the equipment. Two categories may be distinguished:

a) No requirements exist for this category concerning a frame structure for the transmitted signal.

b) This category of network requires from the terminal a frame structure according to CCITT Rec. G.xxx (for further study).

4.5.8 Overvoltage protection requirement

The input and output ports shall withstand without damage 10 standard lightning impulses (1.2/50 µs) with a maximum amplitude of UVdc (5 negative and 5 positive impulses). For the definition of this impulse see CCITT Rec. K 17 Ref. 1 (IEC 60-2/1973).

At the interface for coaxial pairs:

- Differential mode: with a pulse generator of Fig. 20, the value of U is under study.
- Common mode: under study.

Possible pulse generator is described in Fig. 20.
(Re. CCITT Rec. G.703 Annex B, Blue Book).

4.6 Requirements for connection to a V.35 interface

4.6.1 Data rate and timing

The DTE (Data Terminal Equipment) shall operate with one of the following data rates: 48 kbit/s, 56 kbit/s, 64 kbit/s or n x 64 kbit/s, with n an integer between 2 and 31 inclusive.

The DTE shall be capable of operating in one or both of the following timing arrangements:

a. Master timing
The DTE itself acts as a master clock source.
Transmitted data shall be clocked to the timing signal supplied by an internal oscillator, the accuracy of which shall be better than 50 ppm. This timing signal shall be supplied by the DTE on interchange circuit 113. Received data will be clocked to the timing signal supplied to the DTE on interchange circuit 115.

b. Slave timing
The master clock source is included in the circuit beyond the DTE. Received data will be clocked to the timing signal supplied to the DTE on interchange circuit 115.
Transmitted data shall be clocked to the timing signal used for the received data. This timing signal is supplied to the DTE on interchange circuit 114.

The actual timing arrangement to be used depends on the configuration of the digital circuit. In most cases however, timing arrangement b) will be applicable.

4.6.2 Connection requirements

The circuit termination point will be provided with a 34 pole ISO 2593 compatible female connector.

The DTE shall be equipped with a male counterpart ISO 2593 connector, with 1.6 mm diameter poles.

The DTE interchange circuits shall be connected to the connector poles assigned in paragraph 4.6.4 and shall posses the electrical characteristics as indicated for the generator or load types.

Poles not assigned should be left unconnected.

To avoid both interference from other interchange circuits and mis-operation of interchange circuits, any wire not utilized in the DTE connection cable should be left unconnected.

4.6.3 Electrical characteristics of interchange circuits

The electrical characteristics of the unbalanced interchange circuits shall be in accordance with CCITT recommendation V.28.

The electrical characteristics of the balanced interchange circuits shall be in accordance with CCITT recommendation V.35, Appendix II, Red Book.

NOTE: The following note appears with CCITT Recommendation V.35 in the Blue Book:
"Note - It is CCITT's opinion that the information in this Recommendation is out of date and therefore it is not recommended to use the techniques described in the Recommendation for new designs. Alternative techniques are described in Recommendation V.36 and V.37".

It should be noted that other Recommendations make reference to the electrical characteristics described in Appendix II to this Recommendation. As these characteristics are expected to allow interworking with V.11 characteristics, use of V.11 circuits is recommended in those cases.

4.6.4 Interchange circuits required

Interchange circuits to be implemented mandatorily or optionally are:

Pole no	Circuit no	Level	Type *)	Circuit name
B	102	-	-	Signal ground or common return
P, S	103	V.35	G	Transmitted data (A, B)
R, T	104	V.35	L	Received data (A, B)
C	105	V.28	G	Request to send
D	106	V.28	L	Ready for sending
E	107	V.28	L	Data set ready
F	109	V.28	L	Received line signal detector
U, W	113	V.35	G	Transmit clock from DTE (A, B)
Y, AA	114	V.35	L	Transmit clock from DCE (A, B)
V, X	115	V.35	L	Receive clock (A, B)
N	140	V.28	G	Loopback/Maintenance test
L	141	V.28	G	Local loopback
NN	142	V.28	L	Test indicator
*)	G = generator, L = load			

Functional requirements for the interchange circuits mentioned are given in the following paragraphs. Where interchange circuits are required to be "monitored" by the DTE, it is implied that such a circuit shall not only be terminated by a receiver, but that any signals on this circuit will have to be recognized by the DTE and subsequent actions be taken as specified in the relevant paragraph.

4.6.4.1 Circuit 102: signal ground or common return

This circuit shall be provided.

If protective ground is provided in the DTE, it shall be possible to connect signal ground to protective ground. Whether or not the two circuits may actually be connected with each other is subject to national regulations.

Pole A of the 34-way interface connector according to International Standard ISO 259 is assigned for connecting the shields between tandem sections of shielded interface cables. Subject to national regulations, this pole may be connected to protective ground (if provided in the DTE), to signal ground, or may remain unconnected.

4.6.4.2 Circuit 103: transmitted data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 104 "Received data" for certain applications ("asymmetrical duplex mode of operation").

4.6.4.3 Circuit 104: received data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 103 "Transmitted data" for certain applications ("asymmetrical duplex mode of operation").

4.6.4.4 Circuit 105: request to send

The provision of this circuit is not essential for continuous carrier operation.

The circuit shall be provided for the half-duplex mode of operation of the DTE.

If this circuit is provided, the DTE signals its intent to transmit data by turning ON this circuit. Once the DTE is in a transmitting mode, circuit 105 must not be switched OFF prior to the trailing edge of the last transmitted data bit being presented to the DCE on circuit 103 "Transmitted data". The circuit shall not be turned ON prior to circuit 106 "ready for sending", having gone OFF as a response to circuit 105 previously having been turned OFF.

4.6.4.5 Circuit 106: ready for sending

This circuit shall be provided and monitored by the DTE. The OFF condition of circuit 106 "indicates that the DCE is not prepared to accept data signals from the DTE" (CCITT V.24). Any data that is transmitted on circuit 103 to the DCE while 106 is OFF may be lost.

4.6.4.6 Circuit 107: data set ready

This circuit may be provided optionally.

Where this circuit is implemented, it shall be used to detect either a power off condition in the attached DCE or the disconnection of interconnecting cable. The receiver for this circuit shall interpret these conditions as OFF conditions.

4.6.4.7 Circuit 109: data channel received line signal detector

This circuit shall be provided and monitored for applications where at the transmitting side of a connection circuit 105 "Request to send" is turned ON and OFF to control flow of information. Alternatively to this mode of operation the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 109 is optional.

NOTE: It should be noted that in this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the DCE is receiving valid data.

4.6.4.8 Circuit 113: transmitter signal element timing (DTE source)

This circuit may be provided optionally.

If this circuit is provided, the accuracy of the timing signal presented on it shall be 50 ppm or better. The circuit shall be switched to the OFF condition when it is not used.

4.6.4.9 Circuit 114: transmitter signal element timing (DCE source)

This circuit shall be provided if circuit 113 is not used.

In some applications, circuit 114 may be slaved to circuit 115 "Receiver signal element timing (DCE source)".

NOTE: It should be noted that in some DCEs this slaving condition may be restricted to the frequency of the timing signals output onto the two circuits, while the correlation of signal phase conditions may be at random. The DTE shall be capable of coping with this conditions. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

4.6.4.10 Circuit 115: receiver signal element timing (DCE source)

This circuit shall be provided.

For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

4.6.4.11 Circuit 140: loopback/maintenance test

This circuit may be provided optionally.

4.6.4.12 Circuit 141: local loopback

This circuit may be provided optionally.

4.6.4.13 Circuit 142: test indicator

This circuit shall be provided optionally and monitored. It shall be provided, if either interchange circuit 140 "Loopback/Maintenance test" or 141 "Local loopback", or both are implemented in the DTE.

Immediatly after circuit 142 going ON, the DTE shall cease data communication and either:

- remain stand-by until circuit 142 goes OFF, after which data communication may be resumed;
- or enter a test condition.

4.7 Requirements for connection to a V.36 interface

4.7.1 Data rate and timing

The DTE (data terminal equipment) shall operate with one of the following data rates: 48 kbit/s, 56 kbit/s, 63 kbit/s or n x 64 kbit/s, with n an integer between 2 and 31 inclusive.

The DTE shall be capable of operating in one or both of the following timing arrangements:

a. Master timing
The DTE itself acts as a master clock source.
Transmitted data shall be clocked to the timing signal supplied by an internal oscillator, the accuracy of which shall be better than 50 ppm. This timing signal shall be supplied by the DTE on interchange circuit 113. Received data will be clocked to the timing signal supplied to the terminal on interchange circuit 115.

b. Slave timing
The master clock source is included in the circuit beyond the DTE.
Received data will be clocked to the timing signal supplied to the DTE on interchange circuit 115.
Transmitted data shall be clocked to the timing signal used for the received data. This timing signal is supplied to the DTE on interchange circuit 114.

The actual timing arrangement to be used depends on the configuration of the digital circuit. In most cases however, timing arrangement b) will be applicable.

4.7.2 Connection requirements

The circuit termination point will be provided with a 37 pole ISO 4902 compatible female connector with latching facilities.

Thus the DTE shall be equipped with a male counterpart ISO 4902 connector, with latching facilities to match the circuit termination connector.

The DTE interchange circuit shall be connected to the connector poles assigned in paragraph 4.7.4 and shall possess the electrical characteristics as indicated for the generator or load types.

Poles not assigned should be left unconnected.

To avoid both interference from other interchange circuits and mis-operation of interchange circuits, any wire not utilized in the DTE connection cable should be left unconnected.

4.7.3 Electrical characteristics of interchange circuits

The electrical characteristics of the unbalanced interchange circuit shall be in accordance with CCITT recommendation V.10.

The electrical characteristics of the balanced interchange circuits shall be in accordance with CCITT recommendation V.11.

4.7.4 Interchange circuits required

Interchange circuits to be implemented mandatorily or optionally are:

Pole no.	Circuit no.	Level	Type *)	Circuit name
19	102	-	-	Signal ground
37	102a	-	-	DTE common return
20	102b	-	-	DTE common return
4, 22	103	V.11	G	Transmitted data (A, B)
6, 24	104	V.11	L	Received data (A, B)
7, (25)	105	V.10(V.11)	G	Request to send
9, (27)	106	V.10(V.11)	L	Ready for sending
11, (29)	107	V.10(V.11)	L	Data set ready
13, (31)	109	V.10(V.11)	L	Received line signal detector
17, 35	113	V.11	G	Transmit clock to DCE (A, B)
5, 23	114	V.11	L	Transmit clock from DCE (A, B)
8, 26	115	V.11	L	Receive clock (A, B)
14	140	V.10	G	Loopback/Maintenance test
10	141	V.10	G	Local loopback
18	142	V.10	L	Test indicator
*)	G = generator, L = load			

Functional requirements for the interchange circuits mentioned are given in the following paragraphs. Where interchange circuits are required to be "monitored" by the DTE, it is implied that such a circuit shall not only be terminated by a receiver, but that any signal on this circuit will have to be recognized by the DTE and subsequent actions be taken as specified in the relevant paragraphs.

4.7.4.1 Circuits 102/102a/102b: signal ground/DTE/DCE common return

This circuit shall be provided.

If protective ground is provided in the DTE, it shall be possible to connect signal ground to protective ground. Whether or not the two circuits may actually be connected with each other is subject to national regulations.

Pole 1 of the 37-way interface connector according to International Standard ISO 4902 is assigned for connecting the shields between tandem sections of shielded interface cables. Subject to national regulations, this pole may be connected to protective ground (if provided in the DTE), to signal ground, or may remain unconnected.

4.7.4.2 Circuit 103: transmitted data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 104 "Received data" for certain applications ("asymmetrical duplex mode of operation").

4.7.4.3 Circuit 104: received data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 103 "Transmitted data" for certain applications ("asymmetrical duplex mode of operation").

4.7.4.4 Circuit 105: request to send

The provision of this circuit is not essential for continuous carrier operation.

The circuit shall be provided for the half-duplex mode of operation of the DTE.

If this circuit is provided, the DTE signals its intent to transmit data by turning ON this circuit. Once the DTE is in a transmitting mode, circuit 105 must not be switched OFF prior to the trailing edge of the last transmitted data bit being presented to the DCE on circuit 103 "Transmitted data". The circuit shall not be turned ON prior to circuit 106 "ready for sending", having gone OFF as a response to circuit 105 previously having been turned OFF.

4.7.4.5 Circuit 106: ready for sending

This circuit shall be provided and monitored by the DTE. The OFF condition of circuit 106 "indicates that the DCE is not prepared to accept data signals from the DTE" (CCITT V.24). Any data that is transmitted on circuit 103 to the DCE while 106 is OFF may be lost.

4.7.4.6 Circuit 107: data set ready

This circuit may be provided optionally.

Where this circuit is implemented, it shall be used to detect either a power off condition in the attached DCE or the disconnection of interconnecting cable. The receiver for this circuit shall interpret these conditions as OFF conditions.

4.7.4.7 Circuit 109: data channel received line signal detecor

This circuit shall be provided and monitored for applications where at the transmitting side of a connection circuit 105 "Request to send" is turned ON and OFF to control flow of information. Alternatively to this mode of operation the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 109 is optional.

NOTE: It should be noted that in this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the DCE is receiving valid data.

4.7.4.8 Circuit 113: transmitter signal element timing (DTE source)

This circuit may be provided optionally.

If this circuit is provided, the accuracy of the timing signal presented on it shall be 50 ppm or better. The circuit shall be switched to the OFF condition when it is not used.

4.7.4.9 Circuit 114: transmitter signal element timing (DCE source)

This circuit shall be provided if circuit 113 is not used.

In some applications, circuit 114 may be slaved to circuit 115 "Receiver signal element timing (DCE source)".

NOTE: It should be noted that in some DCEs this slaving condition may be restricted to the frequency of the timing signals output on the two circuits, while the correlation of signal phase conditions may be at random. The DTE shall be capable of coping with this conditions. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

4.7.4.10 Circuit 115: receiver signal element timing (DCE source)

This circuit shall be provided.

For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

4.7.4.11 Circuit 140: loopback/maintenance test

This circuit may be provided optionally.

4.7.4.12 Circuit 141: local loopback

This circuit may be provided optionally.

4.7.4.13 Circuit 142: test indicator

This circuit shall be provided optionally and monitored. It shall be provided, if either interchange circuit 140 "Loopback/Maintenance test" or 141 "Local loopback", or both are implemented in the DTE.

Immediatly after circuit 142 going ON, the DTE shall cease data communication and either:

- remain stand-by until circuit 142 goes OFF, after which data communication may be resumed;
- or enter a test condition.

4.8 Requirements for connection to a CEPT T/CD 01-14 interface

4.8.1 Data rate and timing

The DTE (data terminal equipment) shall operate with one of the following data rates: 48 kbit/s, 56 kbit/s, 64 kbit/s, n x 64 kbit/s (with n an integer between 2 and 31 inclusive), 2 048 kbit/s or 8 448 kbit/s.

The DTE shall be capable of operating in one or both of the following timing arrangements:

a) Master timing
The DTE itself acts as a master clock source.
Transmitted data shall be clocked to the timing signal supplied by an internal oscillator, the accuracy of which shall be better than 50 ppm. This timing signal shall be supplied by the DTE on interchange circuit 113. Received data will be clocked to the timing signal supplied to the DTE on interchange circuit 115.

b) Slave timing
The master clock source is included in the circuit beyond the DTE.
Received data will be clocked to the timing signal supplied to the DTE on interchange circuit 115.
Transmitted data shall be clocked to the timing signal used for the received data. This timing signal is supplied to the DTE on interchange circuit 114.

The actual timing arrangement to be used depends on the configuration of the digital circuit. In most cases however, timing arrangement b) will be applicable.

4.8.2 Connection requirements

The circuit termination point will be provided with a 64/96-way interface connector with poles allocation according to CEPT T/CD 01-14. The male part of the connection is at the DTE side.

4.8.3 Electrical characteristics of interchange circuits

The electrical characteristics of interchange circuits shall be in compliance with CEPT T/CD 01-14, section 3 (LS-TTL-CMOS compatible interface).

4.8.4 Interchange circuits required

Interchange circuits to be implemented mandatorily or optionally are:

Pole no.	Circuit no.	Circuit name
a, b, c1	102	Signal ground or common return
a, b, c31	102	Signal ground or common return
a, b, c32	102	Signal ground or common return
c11	103	Transmitted data
c12	104	Received data
c13	105	Request to send
c14	106	Ready for sending
c15	107	Data set ready
c18	109	Received line signal detector
a21	113	Transmit clock to DCE
a11	114	Transmit clock from DCE
a13	115	Receive clock
a18	140	Loopback/Maintenance test
a14	141	Local loopback
a22	142	Test indicator

Functional requirements for the interchange circuits mentioned are given in the following paragraphs. Where interchange circuits are required to be "monitored" by the DTE, it is implied that such a circuit shall not only be terminated by a receiver, but that any signals on this circuit will have to be recognized by the DTE and subsequent actions be taken as specified in the relevant paragraph.

4.8.4.1 Circuit 102: signal ground or common return

This circuit shall be provided.

If protective ground is provided in the DTE, it shall be possible to connect signal ground to protective ground. Whether or not the two circuits may actually be connected with each other is subject to national regulations.

4.8.4.2 Circuit 103: transmitted data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 104 "Received data" for certain applications ("asymmetrical duplex mode of operation").

4.8.4.3 Circuit 104: received data

This circuit shall be provided for the duplex and half-duplex modes of operation. For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

NOTE: The data signalling rate on this circuit may differ from the data signalling rate on circuit 103 "Transmitted data" for certain applications ("asymmetrical duplex mode of operation").

4.8.4.4 Circuit 105: request to send

The provision of this circuit is not essential for continuous carrier operation. This circuit shall be provided for the half-duplex mode of operation of the DTE. If this circuit is provided, the DTE signals its intent to transmit data by turning ON this circuit. Once the DTE is in a transmitting mode, circuit 105 must not be switched OFF prior to the trailing edge of the last transmitted data bit being presented to the DCE on circuit 103 "Transmitted data". The circuit shall not be turned ON prior to circuit 106 "ready for sending", having gone OFF as a response to circuit 105 previously having been turned OFF.

4.8.4.5 Circuit 106: ready for sending

This circuit shall be provided and monitored by the DTE. The OFF condition of circuit 106 "indicates that the DCE is not prepared to accept data signals from the DTE" (CCITT V.24). Any data that is transmitted on circuit 103 to the DCE while 106 is OFF may be lost.

4.8.4.6 Circuit 107: data set ready

This circuit may be provided optionally.

Where this circuit is implemented, it shall be used to detect either a power off condition in the attached DCE or the disconnection of interconnecting cable. The receiver for this circuit shall interpret these conditions as OFF conditions.

4.8.4.7 Circuit 109: data channel received line signal detector

This circuit shall be provided and monitored for applications where at the transmitting side of a connection circuit 105 "Request to send" is turned ON and OFF to control flow of information. Alternatively to this mode of operation the DTE may control the half-duplex mode of operation by a protocol that considers the transmission and reception of blocks of data. In this case the provision of circuit 109 is optional.

NOTE: It should be noted that in this mode of operation the DCE has no means to convey to the DTE an indication as to whether or not the DCE is receiving valid data.

4.8.4.8 Circuit 113: transmitter signal element timing (DTE source)

This circuit may be provided optionally.

If this circuit is provided, the accuracy of the timing signal presented on it shall be 50 ppm or better. The circuit shall be switched to the OFF condition when it is not used.

4.8.4.9 Circuit 114: transmitter signal element timing (DCE source)

This circuit shall be provided if circuit 113 is not used.

In some applications, circuit 114 may be slaved to circuit 115 "Receiver signal element timing (DCE source)".

NOTE: It should be noted that in some DCEs this slaving condition may be restricted to the frequency of the timing signals output on the two circuits, while the correlation of signal phase conditions may be at random. The DTE shall be capable of coping with this conditions. For simplex operation, this circuit may be omitted if only a receiving mode of operation is intended with the DTE concerned.

4.8.4.10 Circuit 115: receiver signal element timing (DCE source)

This circuit shall be provided.

For simplex operation, this circuit may be omitted if only a transmitting mode of operation is intended with the DTE concerned.

4.8.4.11 Circuit 140: loopback/maintenance test

This circuit may be provided optionally.

4.8.4.12 Circuit 141: local loopback

This circuit may be provided optionally.

4.8.4.13 Circuit 142: test indicator

This circuit shall be provided optionally and monitored. It shall be provided, if either interchange circuit 140 "Loopback/Maintenance test" or 141 "Local loopback", or both are implemented in the DTE.

Immediatly after circuit 142 going ON, the DTE shall cease data communication and either:

- remain stand-by until circuit 142 goes OFF, after which data communication may be resumed;
- or enter a test condition.

Annex A: Overview of national network dependant requirements

This annex gives a summary of those national requirements which deviate from the requirements given in the body of this document. The information is given on a per-country basis with a paragraph numbering referring to the relevant paragraph in the main of the text of the document.

BEL

4.1.2 The provision of an 8 kHz timing signal by the terminal is mandatory.

FRA

4.1.2 The provision of an 8 kHz timing signal by the terminal is mandatory.

4.6.3 A different species of the ISO 2593 connector, with a pole diameter of 1 mm, shall be used in some networks.

ITA

4.1.2 The provision of an 8 kHz timing signal by the terminal is mandatory.

4.1.6 Balance to earth: > 40 dB (4 - 256 kHz).

4.1.7.1 Jitter production < 3.9 μs peak-to-peak (0.25 unit intervals) in the stated frequency range: With band-pass filter cut-off frequencies of 3 kHz and 20 kHz, jitter production < 0.78 μs. peak-to-peak (0.05 unit intervals).

NLD

3.1 The following test will be carried out if the applicant for type approval cannot prove that the equipment complies with CEPT Recommendation T/CD 04–03:

A sinusoidal test voltage with a frequency of 50 Hz and an effective value of 1 250 V will be applied for one minute between the through-connected mains leads and an interchange circuit to be designated by the applicant for type approval.

Both leads of a balanced interchange circuit will also be through-connected. No breakdown or flash-over shall occur during the one minute period. The test voltage will be increased and decreased in a gradual way before and after the test.

ESP

4.2.6.1 Jitter production < 97.6 ns peak-to-peak (0.2 unit intervals).

4.3.6.1 Jitter production < 88.5 ns peak-to-peak (0.75 unit intervals) in the frequency range of 20 Hz to 400 kHz.

CHE/LIE

3.1 The following test will be carried out:
A sinusoidal test voltage with a frequency of 50 Hz and a effective value of 2 000 V will be applied for one minute between the through-connected mains leads and an interchange circuit to be designated by the applicant for type-approval. Both leads of a balanced interchange circuit will also be through-connected. No breakdown or flash-over shall occur during the one minute period.

4.2 Impedance unbalance to earth ≥ 40 dB up to 1 024 kHz.

Additional requirements for terminals with a 2 048 and a 8 448 kbit/s G.703 interface:

Immunity to overvoltages.

Interface circuity shall be protected against overvoltages by means of adequate devices which limit overvoltages to ± 8 V for 2 048 kbit/s and ± 6 V for 8 448 kbit/s at terminal input and output leads.

- 5 positive and 5 negative pulses of 1.2/50 µs shape and 100 V amplitude applied at input and output interfaces;

- binary "1" HDB3 signal of ± 8 V for 2 048 kbit/s and ± 6 V for 8 448 kbit/s applied at input interface for at least one minute.

GBR

1. This recommendation is to be used only for information and guidance purposes within the United Kingdom. Technical information and the United Kingdom approval requirements for connection to digital services for the classes of apparatus (DTE) covered by this recommendation may be obtained by reference to the CEPT Year Book.
It should be noted that the information given in this annex is only applicable to services provided by BT. This information may not be applicable to services offered by other network operators within UK.

4.2.5 Minimum return loss: 50-100 kHz = 15 dB, 100-3 000 kHz = 20 dB.

4.2.6.1 Jitter production < 195.2 ns peak-to-peak (0.4 unit intervals) in the frequency range of 20 Hz to 100 kHz and < 97.6 ns peak-to-peak (0.2 unit intervals) in the frequency range of 18 Hz to 100 kHz.
When supplied with a signal conforming to CCITT Rec. G.823.

Additional requirements for terminals with a 2 048 and 8 448 kbit/s G.703 interface:

- The output current with a resistance of not more than 1 ohm applied to the output part shall not exceed 50 mA RMS in any operation state.

- The peak output voltage shall not exceed 2.844 V in any operating state.

4.3.3 Interfering signal: The ratio between the signal and the interference shall be 18 dB.

4.3.5 Minimum return loss: 200-800 kHz = 15 dB, 800-8 000 kHz = 20 dB, 8 000-12 000 kHz = 15 dB.

4.3.6.1 Jitter production < 85 ns peak-to-peak (0.72 unit intervals) in the frequency range of 20 Hz to 400 kHz and < 23.6 ns peak-to-peak (0.2 unit intervals) in the frequency range of 3 kHz to 400 kHz when supplied with a signal conforming to CCITT Rec. G.823.

4.4 and 4.5 Details will be provided when the information becomes available.

4.6.3 The connector is retained by two 6-32 UNC internally threaded bushes.

- End of Annex A -

Annex B: Conformance test methods

For further study.

- End of annex B -

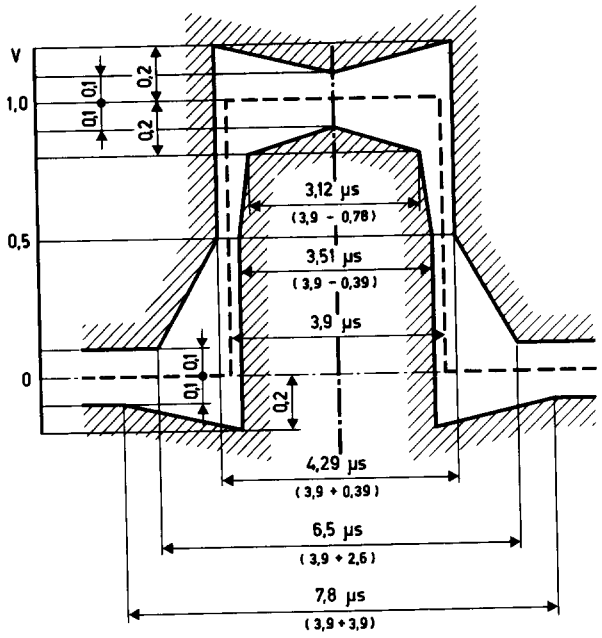


Figure 1: Mask for single pulses at the 64 kbit/s interface

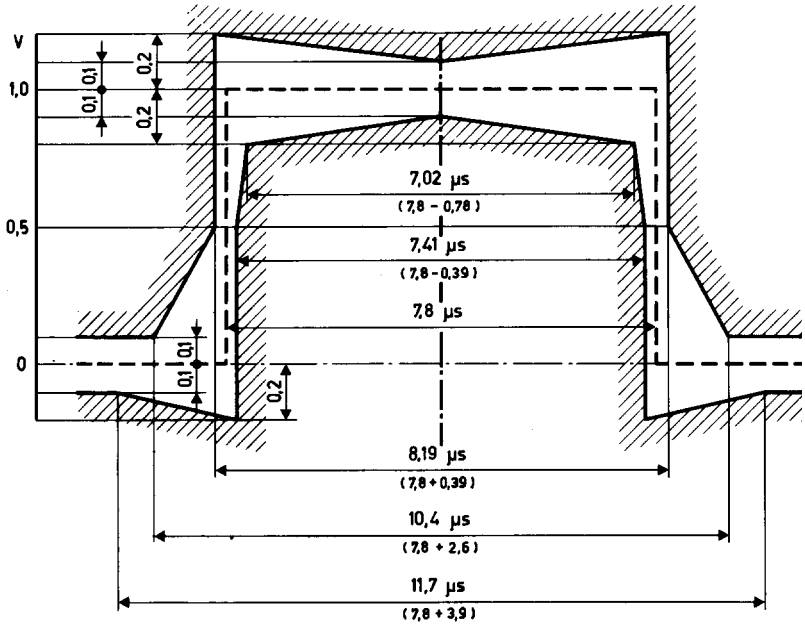


Figure 2: Mask for double pulses at the 64 kbit/s interface

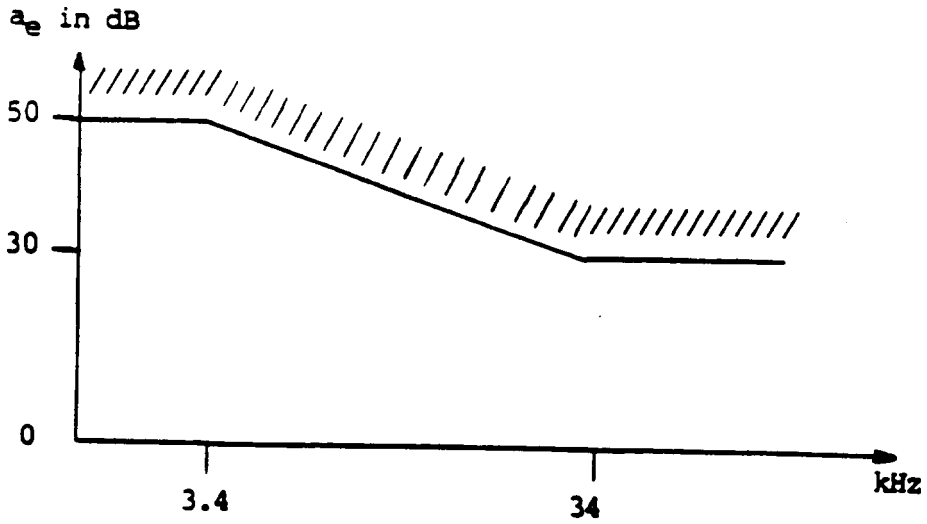
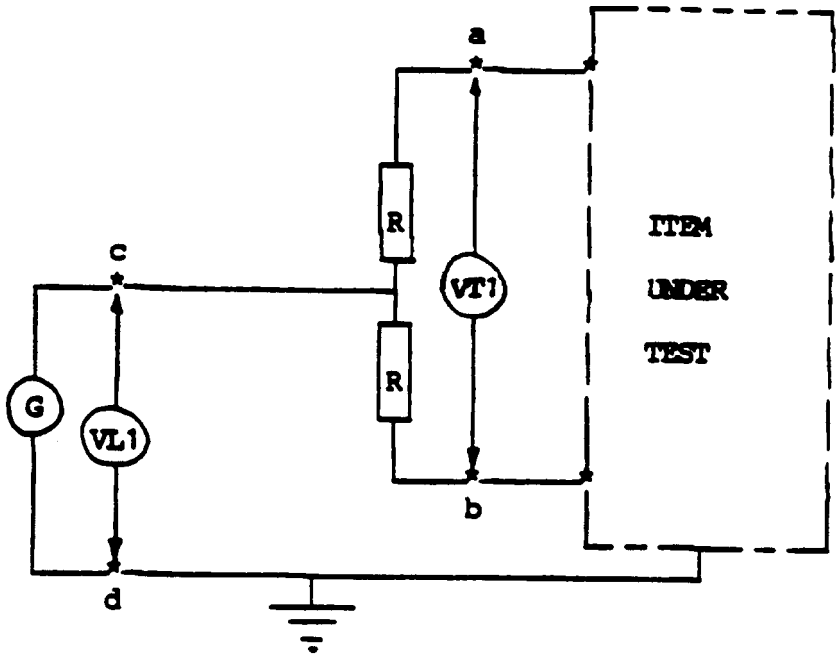


Figure 3: Balance to functional earth at 64 kbit/s



G = Signal Generator

VL1 = Longitudinal Signal Voltage

VT1 = Tranverse Signal Voltage

Longitudinal Conversion Loss (LCL) = $20 \log_{10} \left| \frac{VL1}{VT1} \right|$ dB

(see CCITT Rec. 0.9 Blue Book)

Figure 4: Balance to functional earth measurement set-up

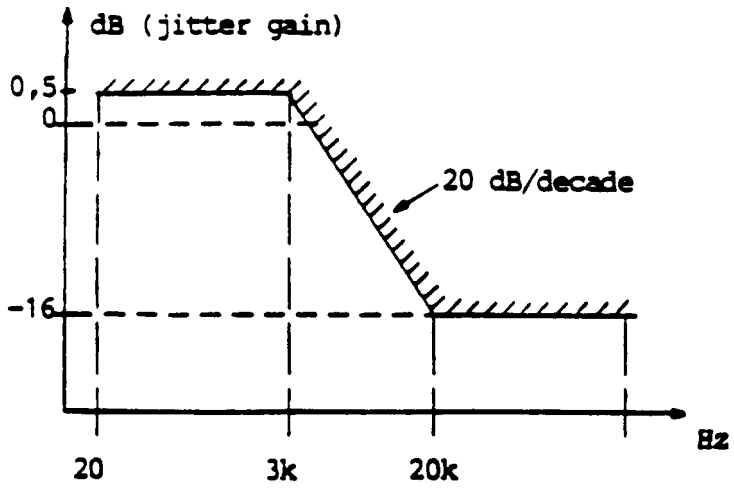


Figure 5: Jitter transfer at 64 kbit/s

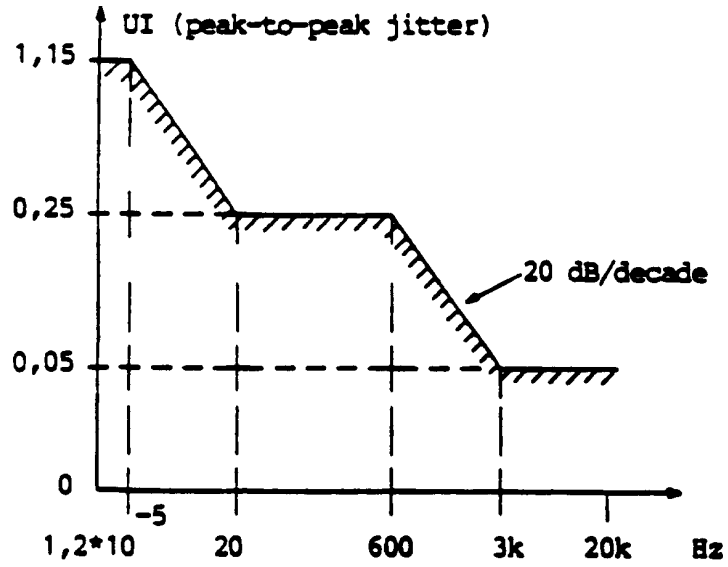


Figure 6: Jitter tolerance at 64 kbit/s

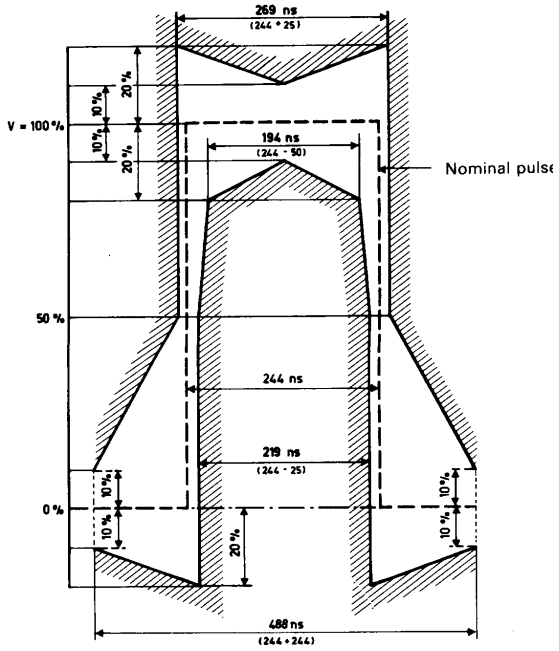


Figure 7: Pulse mask at the 2 048 kbit/s interface

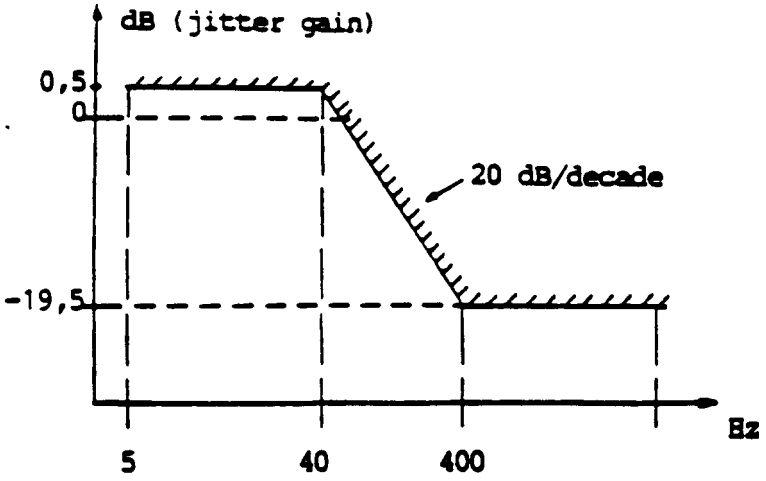


Figure 8: Jitter transfer at 2 048 kbit/s

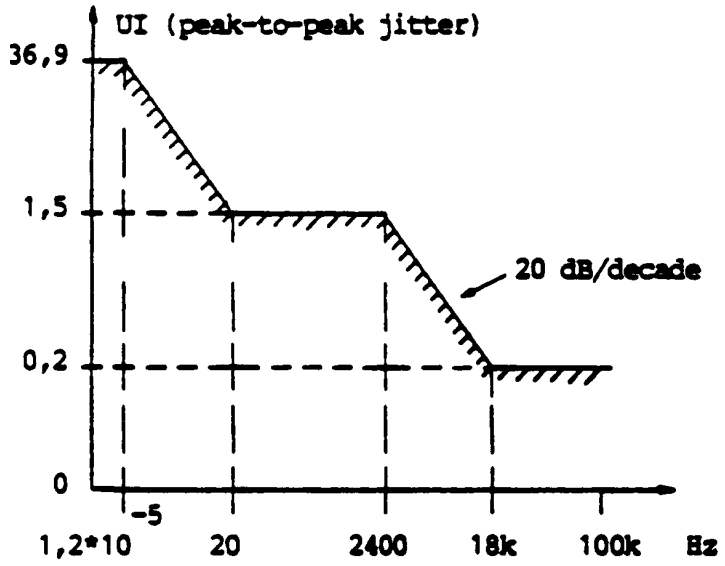


Figure 9: Jitter tolerance at 2 048 kbit/s

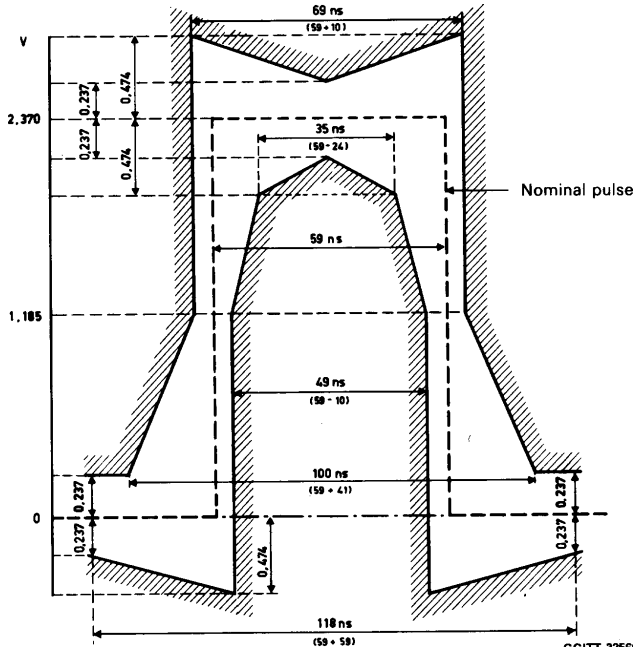


Figure 10: Pulse mask at the 8 448 kbit/s interface

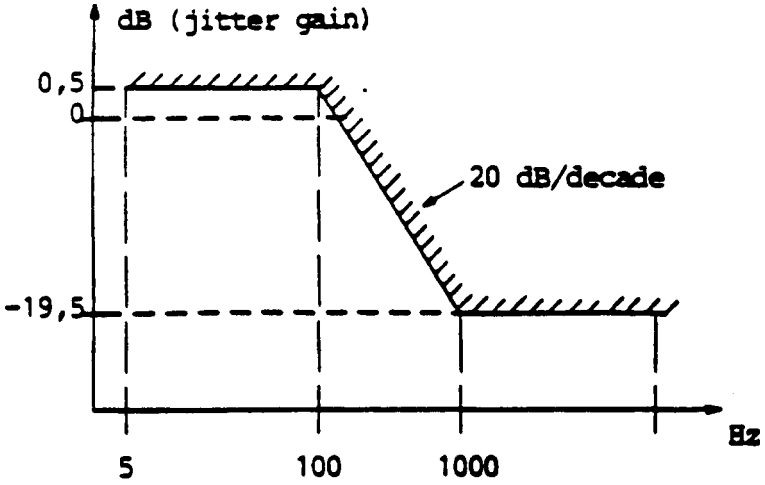


Figure 11: Jitter transfer at 8 448 kbit/s

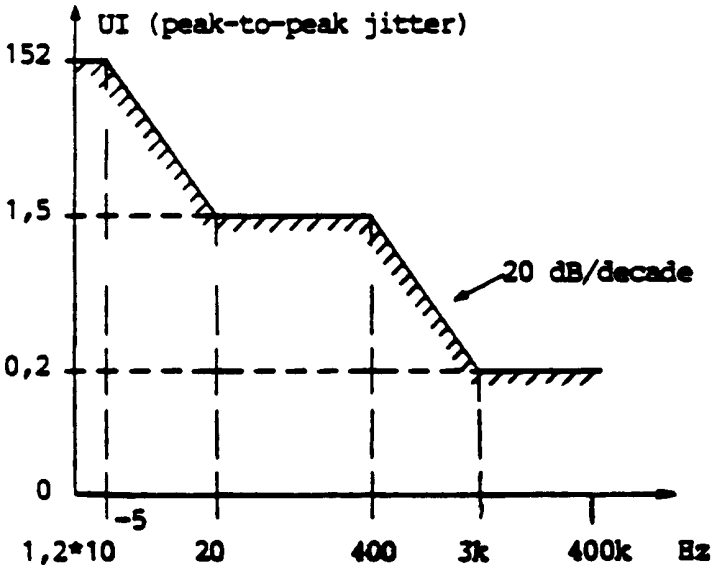


Figure 12: Jitter tolerance at 8 448 kbit/s

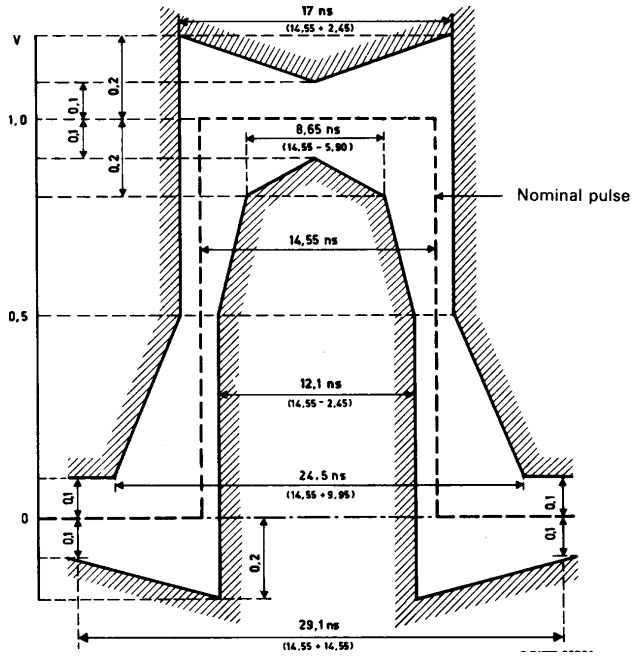


Figure 13: Pulse mask at the 34 368 kbit/s interface

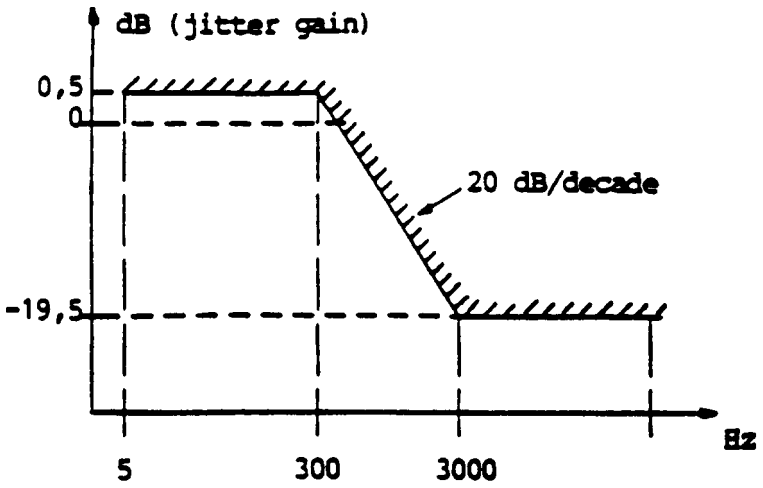


Figure 14: Jitter transfer at 34 368 kbit/s

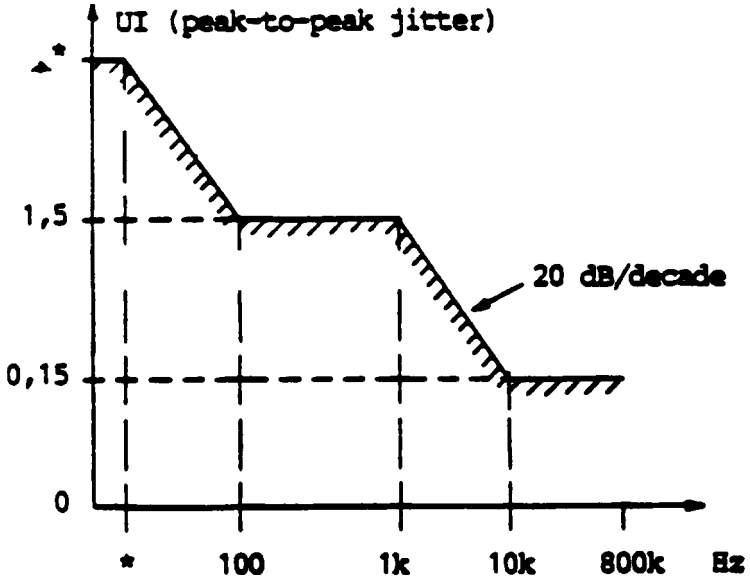


Figure 15: Jitter tolerance at 34 368 kbit/s

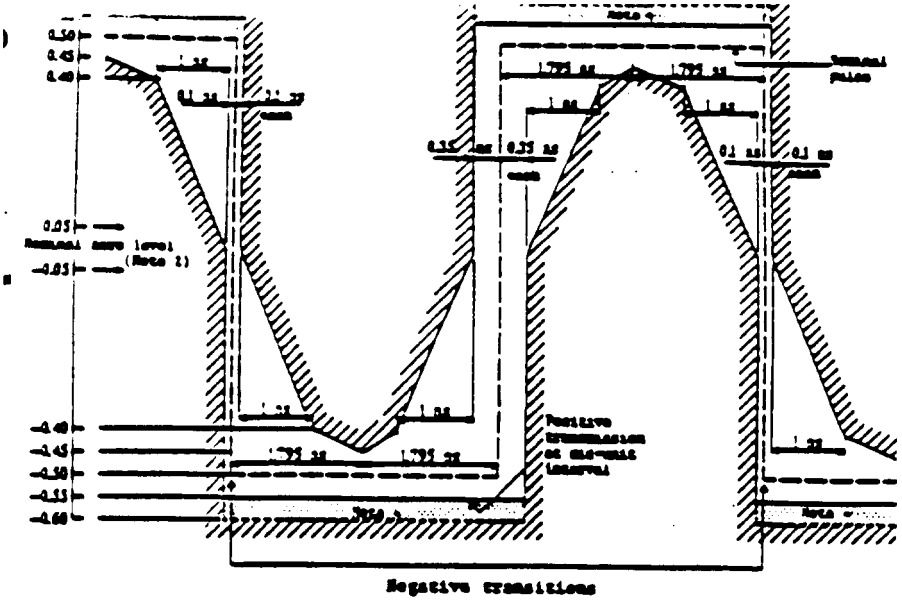


Figure 16: Pulse mask corresponding to binary 0 at the 139 264 kbit/s interface

NOTE 1: V = 1.0 volt.

NOTE 2: For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

NOTE 3: Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139 264 kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-zero and all-ones signals, respectively. (In practice, the signal may contain frame alignment bits per G.751).

NOTE 4: The maximum "steady state" ampitude should not exceed the 0.55 V limit. Overshoots and other transients are premitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 5: For the purpose of these masks, the rise time and decay time should be measured between -0.4 V and 0.4 V, and should not exceed 2 ns.

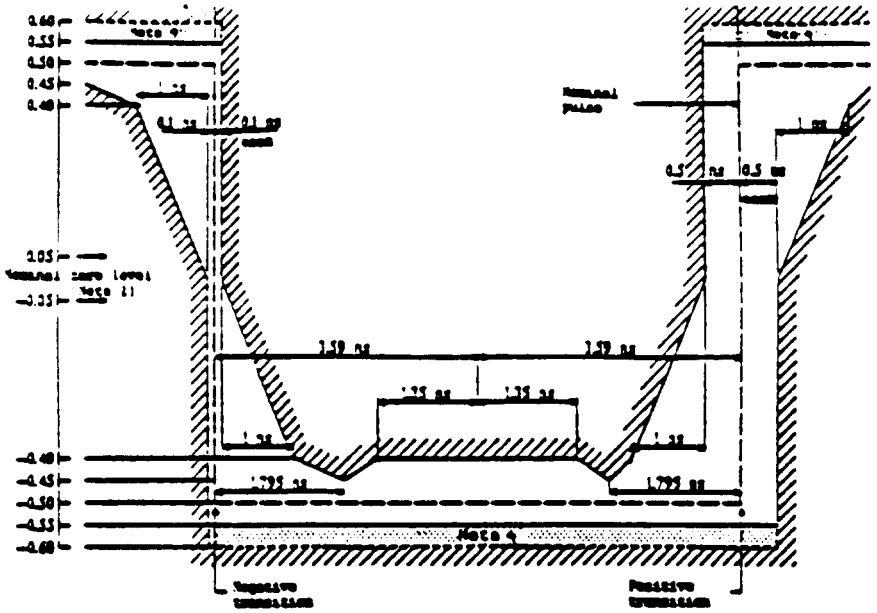


Figure 17: Pulse mask corresponding to binary 1 at the 139 264 kbit/s interface

NOTE 1: V = 1.0 volt.

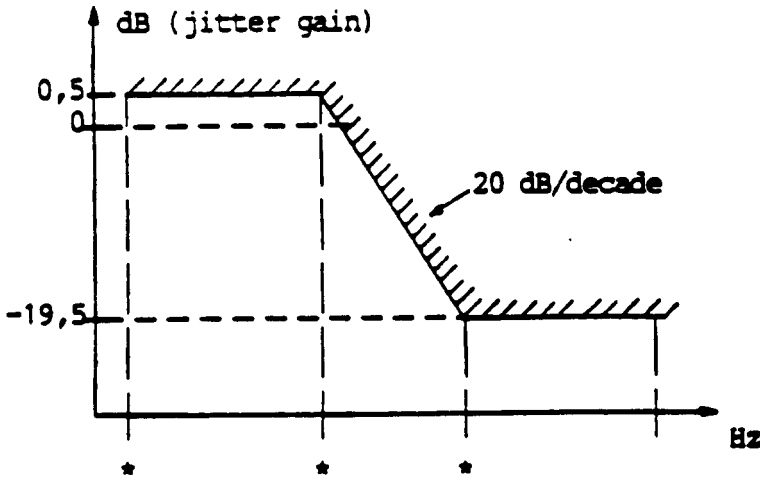
NOTE 2: For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

NOTE 3: Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding and succeeding pulses. For actual verification, if a 139 264 kHz timing signal associated with the source of the interface signal is available, its use as a timing reference for an oscilloscope is preferred. Otherwise, compliance with the relevant mask may be tested by means of all-zero and all-ones signals, respectively. (In practice, the signal may contain frame alignment bits per G.751.)

NOTE 4: The maximum "steady state" ampitude should not exceed the 0.55 V limit. Overshoots and other transients are premitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

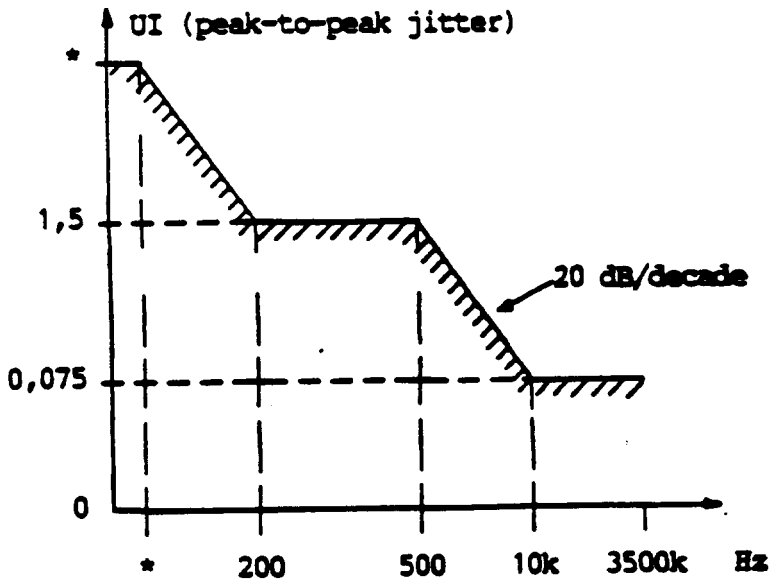
NOTE 5: For the purpose of these masks, the rise time and decay time should be measured between -0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 6: The inverse pulse will have the same characteristics, noting that the timing tolerance at the zero level of the negative and positive transitions are ± 0.1 ns and ± 0.5 ns respectively.



*) Value under study.

Figure 18: Jitter transfer at 139 264 kbit/s



*) Value under study.

Figure 19: Jitter tolerance at 139 264 kbit/s

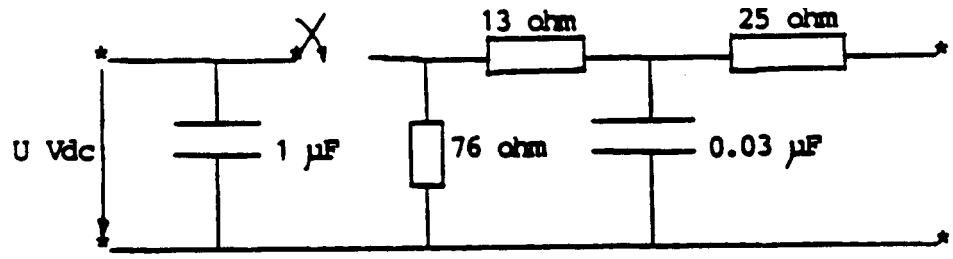


Figure 20: Pulse generator 1.2/50 µs for differential mode voltages

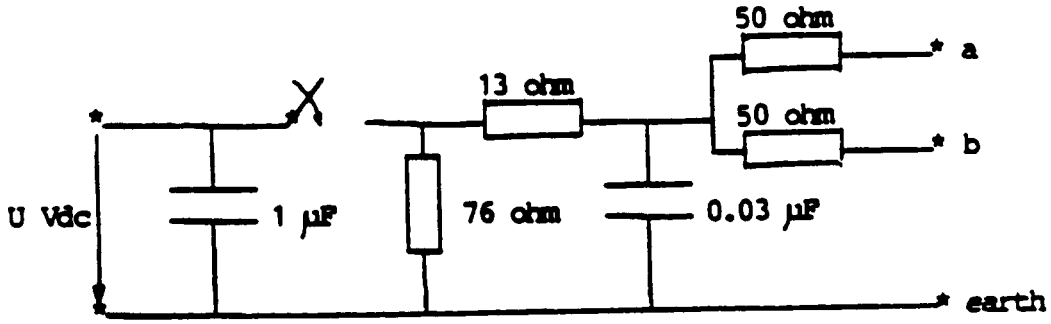


Figure 21: Pulse generator 1.2/50 µs for common mode voltage at symmetrical interfaces

TABLE 1

Frame structure

Frame lenght: 256 bits numbered 1 - 256. The frame repetition rate is 8 000 Hz.

Allocation of bits numbers 1 to 8 of the frame is shown in table below:

Bits number:	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal:	2)	0	0	1	1	0	1	1
Frame not containing the frame alignment signal:	2)	1	3)	4)	4)	4)	4)	4)

2) Bits reserved for international use. One specific use is described in CCITT Rec. G.704, section 2.3.3. If no use is realized, these bits shall be fixed at 1.

3) Remote alarm indication. In undisturbed operation, 0;
in an alarm condition, 1.

4) Spare bits for national use. If no use is realized, these bits shall be fixed at 1. These bits may be recommended by CCITT for use in specific point-to-point applications (e.g. transcoder equipments conforming to CCITT Rec. G.761).

FRA: bit 4 and 5, alarm indication.
bit 6, reserved for future applications.

ESP: bit 4, alarm indication.

- End of Table 1 -

TABLE 2

Table below gives information relating to impedance (§ 4.2.3) and frame structure (§ 4.2.7) as implemented at time of issue of this document in diffferent countries.

COUNTRY	**IMPEDANCE ALTERNATIVE**		**FRAME STRUCTURE ALTERNATIVE**		
	75 Ohms	120 Ohms	a)	b)	c)
AUSTRIA (AUT)		*		*	
BELGIUM (BEL)	*		*		
DENMARK (DNK)	*			*	
FINLAND (FIN)		*	*		
FRANCE (FRA)		*		*	**(*)**
FEDERAL REPUBLIC OF GERMANY (DEU)		*		*	
GREECE (GRC)	*				*
ITALY (ITA)	*		*	**(*)**	
LICHTENSTEIN (LIE)		*		*	
THE NETHERLANDS (NLD)	*			*	
NORWAY (NOR)	*			*	
PORTUGAL (PRT)	-	-	-	-	-
SPAIN (ESP)	*			*	
SWEDEN (SWE)	*			*	
SWITZERLAND (CHE)		*		*	
UNITED KINGDOM (GBR)	*		*		

***)** required in some networks

- End of Table 2 -

History

Document history	
August 1990	First Edition
January 1997	Converted into Adobe Acrobat Portable Document Format (PDF)