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**Network Aspects (NA);
Guidelines for the provision of X.75 links at data rates
higher than 64 kbit/s**

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1 Foreword

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This ETR has been produced by the Network Aspects (NA) Technical Committee of the European Telecommunications Standards Institute (ETSI).

2 References

- [1] CCITT Recommendation X.75 (1988): Packet-switched signalling system between public networks providing data transmission services
- [2] CCITT Recommendation G.703 (1988): Physical/electrical characteristics of hierarchical digital interfaces
- [3] CCITT Recommendation G.704 (1988): Synchronous frame structures used at primary and secondary hierarchical levels
- [4] CCITT Recommendation G.732 (1984): Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s

3 General

Several operators of packet switched networks have expressed their interest in a bit rate of 2 Mbit/s for a single HDLC channel carrying the X.75 [1] protocol. As a result of this manufacturers are developing such interfaces using recently made available powerful processors.

Prototypes have proven the feasibility of running the X.75 [1] protocol at such high bit rates without changing the basics of the protocol.

Certain conditions on propagation delay and bit error rate however have to be respected. These requirements are easily met on European terrestrial links.

This document contains some proposals to standardize the physical layer and to choose the most appropriate options on the link layer. The packet layer is not mentioned hereafter since it is not yet clear if there is any specific requirement due to the high bit rate.

4 Layer 1

It is assumed that the electrical/physical interface is according to CCITT Recommendation G.703 [2].

The functional characteristics are based on 2 Mbit/s frame structure conforming to CCITT Recommendation G.704 [3]. Time slot 0 (TS0) will be used for the detection of faults (cf. CCITT Recommendation G.732 [4]), the indication of alarms, and for maintenance facilities (loopbacks).

The faults that could be detected are:

- loss of frame alignment
- receipt of Alarm Indication Signal (AIS)
- excessive error ratio in frame alignment
- alarm indication in bit 3 of Time Slot 0 (TS0) of frames not containing the frame alignment signal
- Cyclic Redundancy Check (CRC) - failure (cf. CCITT Recommendation G.704 [3], clause 2.3.3)
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The action to be taken after fault detection and the impact on layer 2 is to be agreed.

The method for activating loops by use of the appropriate bits in Time Slot 0 (TS0) is to be agreed.

It is proposed not to use time slot 16 in order to have the same structure as an H12 channel. The remaining 30 time slots should be used as one single bit stream of 1920 kbit/s.

Note 1: Other bit rates (eg 384 kbit/s, Ho channel) by concatenating a number of 64 kbit/s channels are for further study and can be agreed between Administrations on a bilateral basis.

Note 2: For links with non-European networks the requirements of a bit rate of 1544 kbit/s or lower, based on a PCM 24 system, should be studied.

5 Layer 2

Calculations show that, at a bit rate of 1920 kbit/s, the following options should be chosen for terrestrial links:

- modulo 128
- k between 60 and 127 not to reduce the throughput

Satellite links cannot be used without serious loss of throughput due to the long propagation delay if k cannot be larger than 127.

The bit error rate should be better than $10 \exp -5$ not to reduce throughput by sending Reject (REJ) frames and retransmission of Information (I) frames.

Sending of Receiver Not Ready (RNR) frames to stop the transmission of Information (I) frames is not appropriate.

The Multilink Procedure (MLP) is recommended for quality of service reasons. The MLP should run over at least two different PCM systems.

History

Document history	
August 1990	First Edition
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