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ETSI Standard

Dynamic synchronous Transfer Mode (DTM);
Part 6: Mapping of Synchronous
Digital Hierarchy (SDH) over DTM

Reference

RES/TISPAN-02017-DTM

Keywords

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ETSI

650 Route des Lucioles
F-06921 Sophia Antipolis Cedex - FRANCE

Tel.: +33 4 92 94 42 00 Fax: +33 4 93 65 47 16

Siret N° 348 623 562 00017 - NAF 742 C
Association à but non lucratif enregistrée à la
Sous-Préfecture de Grasse (06) N° 7803/88

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Contents

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Foreword

This ETSI Standard (ES) has been produced by ETSI Technical Committee Telecommunications and Internet converged Services and Protocols for Advanced Networking (TISPAN).

The present document is part 6 of a multi-part deliverable covering the Dynamic synchronous Transfer Mode (DTM), as identified below:

ES 201 803-1: "System description";

ES 201 803-2: "System characteristics";

ES 201 803-3: "Physical protocol";

ES 201 803-4: "Mapping of DTM frames into SDH containers";

ES 201 803-5: "Mapping of PDH over DTM";

ES 201 803-6: "Mapping of Synchronous Digital Hierarchy (SDH) over DTM";

ES 201 803-7: "Ethernet over DTM Mapping";

ES 201 803-9: "Mapping of ATM over DTM";

TR 101 803-10: "Routeing and switching of IP traffic over DTM";

ES 201 803-11: "Mapping of video streams over DTM";

ES 201 803-12: "Mapping of MPLS over DTM";

ES 201 803-13: "System description of sub-rate DTM".

Introduction

Dynamic synchronous Transfer Mode (DTM) is a time division multiplex and a circuit-switched network technique that combines switching and transport.

Part 1 describes the general properties of DTM and the DTM service over a unidirectional data channel. The overall system architecture is described and fundamental functions are identified.

Part 2 includes system aspects that are mandatory or optional for nodes from different vendors to interoperate. The interworking granularity should be at node level, such that nodes from different vendors can interoperate with regard to well-defined functions.

Part 3 specifies the physical layer for physical links based on 8B10B encoding.

Part 4 describes how DTM frames are mapped onto SDH containers.

The transport of various tributary signals is specified for PDH (part 5), SDH (part 6), Ethernet (part 7), ATM (part 9), IP (part 10), video streaming (part 11) and MPLS (part 12).

Subrate DTM is described in part 13.

1 Scope

The present document achieves the following:

- specifies a method for mapping SDH VC-11, VC-12, VC-2, VC-3, VC-4 and VC-4-Xc containers over DTM channels;
- specifies a method for grouped mapping of SDH VC-11, VC-12, VC-2, VC-3 and VC-4 containers over DTM channels;
- specifies the characteristics of critical parameters for mapping of SDH VC-11, VC-12, VC-2, VC-3, VC-4 and VC-4-Xc containers over DTM channels;
- specifies the characteristics of critical parameters for grouped mapping of SDH VC-11, VC-12, VC-2, VC-3 and VC-4 containers over DTM channels;
- gives terms and definitions for mapping encoding.

2 References

The following documents contain provisions, which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication and/or edition number or version number) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

Referenced documents, which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

[1] ETSI EN 300 417-1-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 1-1: Generic processes and performance".

[2] ETSI EN 300 417-3-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 3-1: Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".

[3] ETSI EN 300 417-4-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 4-1: Synchronous Digital Hierarchy (SDH) path layer functions".

[4] ETSI EN 301 164: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); SDH leased lines; Connection characteristics".

[5] ETSI EN 301 165: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); SDH leased lines; Network and terminal interface presentation".

[6] ETSI ES 201 803-2-3: "Dynamic synchronous Transfer Mode (DTM); Part 2: System characteristics; Sub-part 3: Transport network and channel adaptation aspects".

[7] ITU-T Recommendation G.707: "Network node interface for the Synchronous Digital Hierarchy (SDH)".

[8] ITU-T Recommendation G.805: "Generic functional architecture of transport networks".

[9] ITU-T Recommendation G.806: "Characteristics of transport equipment - Description methodology and generic functionality".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

Access Point (AP): "reference point" that consists of the pair of co-located "unidirectional access" points, and therefore represents the binding between the trail termination and adaptation functions

NOTE: Adopted from ITU-T Recommendation G.805 [8].

Adapted Information (AI): information passing across an AP

NOTE: See also ITU-T Recommendation G.805 [8]. Adopted from ITU-T Recommendation G.806 [9].

Alarm Indication Signal (AIS): special marker sent in a data slot to mark the lack of transported data as a result of a defect in the transmission path

channel: set of slots allocated from one source access node to one or more destination access nodes in a network

Characteristic Information (CI): signal with a specific format, which is transferred on "network connections"

NOTE: The specific formats will be defined in the technology specific Recommendations. The information passing across a CP or TCP. (Adopted from ITU-T Recommendation G.805 [8] and ITU-T Recommendation G.806 [9]).

Connection Point (CP): reference point where the output of a trail termination source or a connection is bound to the input of another connection, or where the output of a connection is bound to the input of a trail termination sink or another connection

NOTE: Adopted from ITU-T Recommendation G.806 [9].

defect: density of anomalies has reached a level where the ability to perform a required function has been interrupted

NOTE: Defects are used as input for performance monitoring, the control of consequent actions, and the determination of fault cause. (Adopted from ITU-T Recommendation G.806 [9]).

frame: set of slots forming an entity that is transmitted on a physical medium repeatedly every 125 µs (nominally), i.e. 8 000 frames/second

grouped mapping: the mapping of a group of some number of elements being specified in a basic mapping.

NOTE: In grouped mapping, a mapping scheme from the channel to the basic mapping needs to be defined.

idle: special marker sent in a data slot to mark the lack of transported data in the slot

Management Information (MI): signal passing across an access point

NOTE: Adopted from ITU-T Recommendation G.806 [9].

Management Point (MP): reference point where the output of an atomic function is bound to the input of the element management function, or where the output of the element management function is bound to the input of an atomic function

NOTE: The MP is not the TMN Q3 interface. Adopted from ITU-T Recommendation G.806 [9].

Performance Supervision (PS): special marker sent with the data containing per channel Performance Supervision information

physical link: unidirectional connection between the transmitter of one port and the receiver of another port

Server Signal Fail (SSF): signal fail indication output at the CP of an adaptation function

NOTE: Adopted from ITU-T Recommendation G.806 [9].

Signal Fail (SF): signal indicating the associated data has failed in the sense that a near-end defect condition (not being the degraded defect) is active

NOTE: Adopted from ITU-T Recommendation G.806 [9].

slot: time slot within the frame being able to transport 64 bit of data or a number of special codes

Trail Signal Fail (TSF): signal fail indication output at the AP of a termination function

NOTE: Adopted from ITU-T Recommendation G.806 [9].

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

A	Adapted function
aAIS	Alarm Indication Signal action
AI	Adapted Information
AIS	Alarm Indication Signal
AP	Access Point
AP0	APplication layer channel adaptation type 0
AP0e	APplication layer channel adaptation type 0 with empty trail termination
aSSF	Server Signal Fail action
BPn	ByPass layer type n
BPnp	ByPass layer type n Protection
C	Connection function
cAIS	Alarm Indication Signal cause
CH	CHannel layer
CHn	CHannel layer type-n
CHP	CHannel layer Protection
CI	Characteristic Information
CK	ClocK
cLOJ	Loss Of Justification cause
CP	Connection Point
D	Data
dAIS	Alarm Indication Signal defect
DCAP	DTM Channel Adaptation Protocol
DTM	Dynamic synchronous Transfer Mode
fAIS	Alarm Indication Signal fault
FJ-	negative Frequency Justification
FJ+	positive Frequency Justification
fLOJ	Loss Of Justification fault
FS	Frame Start signal
IF	In Frame
II	Idle Insertion
MI	Management Information
Mn	Media layer type-n
MP	Management Point
nAIS	Alarm Indication Signal anomaly
nFJ-	negative Frequency Justification anomaly
nFJ+	positive Frequency Justification anomaly
nLOJ	Loss Of Justification anomaly
OOF	Out Of Frame
pFJ-	negative Frequency Justification performance counter
pFJ+	positive Frequency Justification performance counter
POH	Path OverHead
PS	Performance Supervision
SDH	Synchronous Digital Hierarchy
sFS	Frame Start signal
sII	Idle Insertion signal
Sk	Sink
Sn	SDH higher order VC-n layer (n = 11, 12, 2, 3, 4, 4-Xc)

So	Source
SSF	Server Signal Fail
TI	Timing Information
TP	Timing Point
TSF	Trail Signal Fail
TT	Trail Termination
VC	Virtual Container
VC-n	Virtual Container, level n
VC-n-Xl	Virtual Container, level n, linear concatenation
VC-n-Xv	Virtual Container, level n, virtual concatenation
VC-11	Virtual Container, level 11
VC-12	Virtual Container, level 12
VC-2	Virtual Container, level 2
VC-3	Virtual Container, level 3
VC-4	Virtual Container, level 4
VC-4-Xc	Virtual Container, level 4, contiguous concatenation

4 Overview

The SDH VC-11, VC-12, VC-2, VC-3, VC-4 and VC-4-Xc mapping over DTM (see figure 1) describes the mapping and framing of the virtual containers level 11 (VC-11), level 12 (VC-12), level 2 (VC-2), level 3 (VC-3) and level 4 (VC-4) into DTM channels. The functionality is part of the DTM Application layer and provides a transport service to the SDH higher and lower order path layer similar to the service provided by the SDH Multiplexing Section layer (EN 300 417-3-1 [2] and EN 300 417-4-1 [3]). The transport functionality provides a SDH VC DTM Timeslot connection over a DTM network as if this where a physical link between the SDH nodes. The service can be viewed as a leased VC-11, VC-12, VC-2, VC-3, VC-4 or VC-4-Xc over the DTM network, thus similar to EN 301 164 [4] and EN 301 165 [5].

The grouped mapping of SDH VC-11, VC-12, VC-2, VC-3 and VC-4 containers over DTM provides for an integer number of the same container to be grouped inside the same DTM channel. This allows for ease of management when multiple containers are required for the same service. Such a service includes Virtual conCATenation (VCAT) of NG-SDH.

The grouped mapping allows for separate or common phase of the grouped virtual containers. Separate phase grouping allows for separate connections or other unorganized phase aligned signals to be grouped. Common phase grouping allows for well ordered phase alignment to be maintained over the DTM network, thus reducing or eliminating the need for phase adjustment in the receiving end.

NOTE 1: A number of ungrouped VC-n channels are thus equivalent to being grouped with separate phase, except for the separate channels with associated per channel management. Grouping can reduce the management overhead as well as providing a convenient association between the individual virtual containers.

NOTE 2: A number of ungrouped VC-n channels are not equivalent to the grouped mapping of VC-n with common phase. This is due to the fact that even if the input signals is in phase, the frequency justification is individual and also, the lack of end-to-end association in the setup phase of channels does not guarantee the same path and delay as a single channel will provide.

The SDH Lower order Virtual Containers contain 26 (VC-11), 35 (VC-12) and 107 (VC-2) octets per row, 4 rows per 500 us super-frame. The SDH Higher order Virtual Containers contain 85 (VC-3), 261 (VC-4) and $261 \times X$ (VC-4-Xc) octets per row, 9 rows per frame. The VC frame rate may deviate from the SDH transmission rate by up to ±4,6 ppm (EN 300 417-3-1 [2] and EN 300 417-4-1 [3]) such that frequency justification is required. DTM idle special marker insertion or exclusion upon justification opportunity replaces the SDH frequency justification mechanism of pointer justifications.

NOTE 3: Limited support for frequency deviations up to ±20 ppm can exist but is not guaranteed.

The SDH supervision functionality is mapped over to the DTM functionality and SDH AIS is being encoded into DTM AIS.

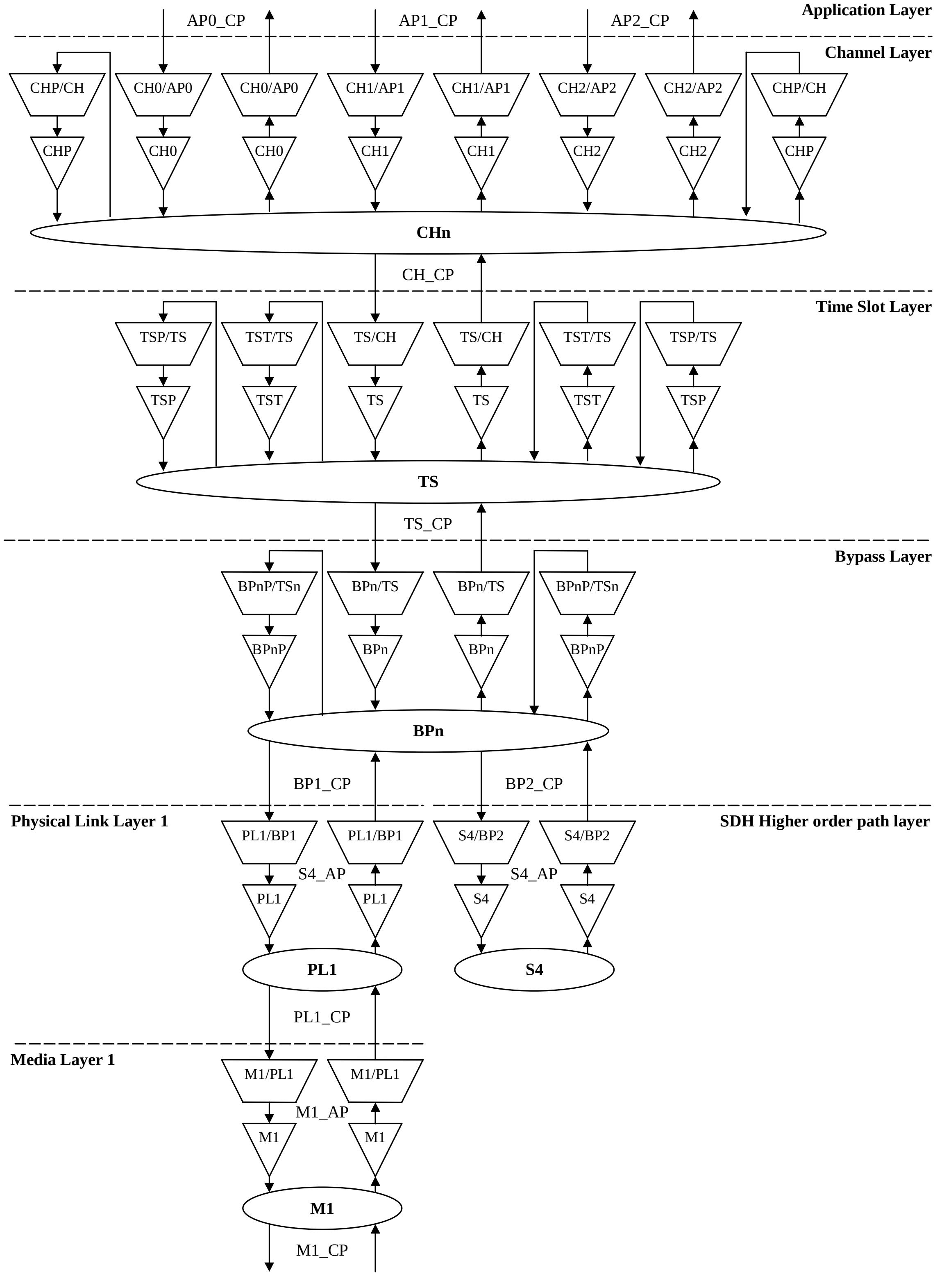

Figure 1: Transport Network Reference Model for DTM

5 DTM SDH Transport Application Layer

The SDH VC-11/VC-12/VC-2/VC-3/VC-4/VC-4-Xc over DTM transport is specified as the adaptation functions on top of the DCAP-0 (ES 201 803-2-3 [6]) trail terminator functions, providing the S11/S12/S2 Lower order trail and the S3/S4 Higher order trail over DTM.

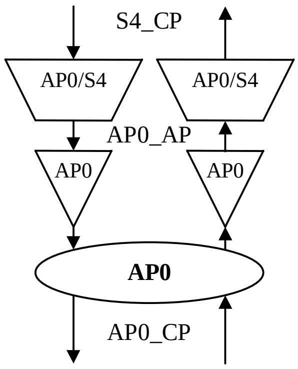

Figure 2: DTM Application layer 0 for SDH VC-4 mapping atomic functions

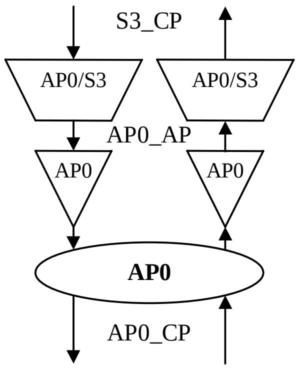

Figure 3: DTM Application layer 0 for SDH VC-3 mapping atomic functions

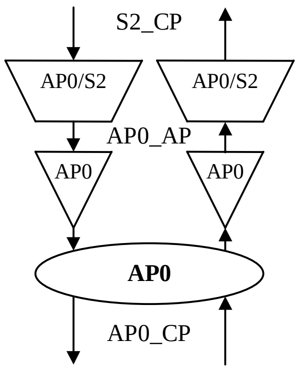

Figure 4: DTM Application layer 0 for SDH VC-2 mapping atomic functions

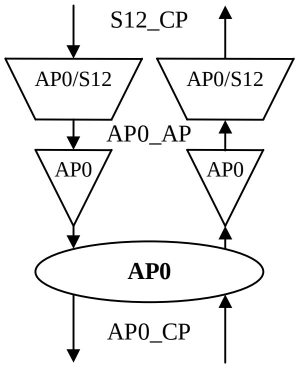

Figure 5: DTM Application layer 0 for SDH VC-12 mapping atomic functions

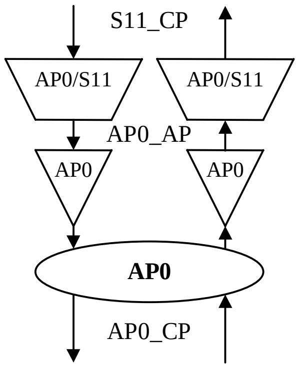

Figure 6: DTM Application layer 0 for SDH VC-11 mapping atomic functions

5.1 Access point information

5.1.1 Characteristic Information

The Characteristic Information (CI) of the Connection Point (CP) is described in EN 300 417-4-1 [3].

5.1.2 Adapted Information

The Adapted Information (AI) of the Adaptation Point (AP) is described in ES 201 803-2-3 [6] as the Application 0 Characteristic Information.

5.1.3 Management Information

The Management Information (MI) of the Management Point (MP) is (for VC-4, VC-3, VC-2, VC-12 and VC-11 respectively):

- the 1 second timer signal AP0/S4_A_So_MI_1second, AP0/S3_A_So_MI_1second, AP0/S2_A_So_MI_1second, AP0/S12_A_So_MI_1second and AP0/S11_A_So_MI_1second;
- the positive frequency justification 1 second performance counter AP0/S4_A_So_MI_pFJ+, AP0/S3_A_So_MI_pFJ+, AP0/S2_A_So_MI_pFJ+, AP0/S12_A_So_MI_pFJ+ and AP0/S11_A_So_MI_pFJ+;
- the negative frequency justification 1 second performance counter AP0/S4_A_So_MI_pFJ-, AP0/S3_A_So_MI_pFJ-, AP0/S2_A_So_MI_pFJ-, AP0/S12_A_So_MI_pFJ- and AP0/S11_A_So_MI_pFJ-;
- the loss of justification cause signal AP0/S4_A_Sk_MI_cLOJ, AP0/S3_A_Sk_MI_cLOJ, AP0/S2_A_Sk_MI_cLOJ, AP0/S12_A_Sk_MI_cLOJ and AP0/S11_A_Sk_MI_cLOJ;

- and the alarm indication signal cause signal AP0/S4_A_Sk_MI_cAIS, AP0/S3_A_Sk_MI_cAIS, AP0/S2_A_Sk_MI_cAIS, AP0/S12_A_Sk_MI_cAIS and AP0/S11_A_Sk_MI_cAIS.

5.1.4 Timing Information

The Timing Information (TI) of the Timing Point (TP) is:

- the Application 0 data clock timing indication AP0_TI_CK;
- and the Application 0 frame start timing indication AP0_TI_FS.

5.2 Connection function (AP0_C)

Not applicable. There are no connection functions defined for this layer.

5.3 Trail Termination functions (AP0e_TT)

The trail termination functions are empty mappings between AI and CI.

5.3.1 Application 0 empty Trail Termination (AP0e_TT)

5.3.1.1 Application 0 empty Termination Source function (AP0e_TT_So)

Symbol:

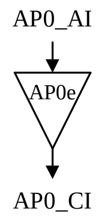

Figure 7: Application 0 empty Trail Termination Source (AP0e_TT_So)

Interfaces:

Table 1: AP0e_TT_So Input and output signals

Input(s)	Output(s)
AP0_AI_D	AP0_CI_D
AP0_AI_CK	AP0_CI_CK
AP0_AI_II	AP0_CI_II
AP0_AI_PSI	AP0_CI_PSI
AP0_AI_TSF	AP0_CI_SSF

Processes and anomalies:

None.

Defects:

None.

Consequent actions:

None.

Defect correlation:

None.

Performance monitoring:

None.

Output mapping:

AP0_CI_D ← AP0_AI_D.

AP0_CI_CK ← AP0_AI_CK.

AP0_CI_II ← AP0_AI_II.

AP0_CI_PSI ← AP0_AI_PSI.

AP0_CI_SSF ← AP0_AI_TSF.

Fault management:

None.

Long term performance monitoring:

None.

5.3.1.2 Application 0 empty Trail Termination Sink function (AP0e_TT_Sk)

Symbol:

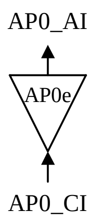

Figure 8: Application 0 empty Trail Termination Sink (AP0e_TT_Sk)

Interfaces:

Table 2: AP0e_TT_Sk Input and output signals

Input(s)	Output(s)
AP0_CI_D	AP0_AI_D
AP0_CI_CK	AP0_AI_CK
AP0_CI_II	AP0_AI_II
AP0_CI_PSI	AP0_AI_PSI
AP0_CI_SSF	AP0_AI_TSF

Processes and anomalies:

None.

Defects:

None.

Consequent actions:

None.

Defect correlation:

None.

Performance monitoring:

None.

Output mapping:

AP0_AI_D ← AP0_CI_D.

AP0_AI_CK ← AP0_CI_CK.

AP0_AI_II ← AP0_CI_II.

AP0_AI_PSI ← AP0_CI_PSI.

AP0_AI_TSF ← AP0_CI_SSF.

Fault management:

None.

Long term performance monitoring:

None.

5.4 Adaptation functions (AP0/Sn_A)

5.4.1 DTM Application 0/SDH Higher order path Adaptation function (AP0/S4_A)

This clause describes the SDH VC-4 adaptation using DCAP-0 trail terminators.

5.4.1.1 Media Adaptation Source function (AP0/S4_A_So)

Symbol:

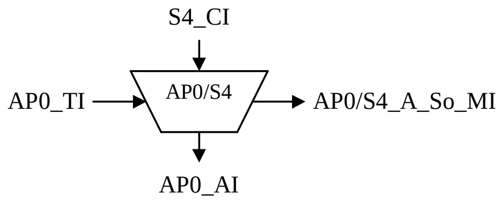

Figure 9: DTM Application 0/SDH Higher order path Adaptation Source (AP0/S4_A_So)

Interfaces:

Table 3: AP0/S4_A_So Input and output signals

Input(s)	Output(s)
S4_CI_D	AP0_AI_D
S4_CI_CK	AP0_AI_CK
S4_CI_FS	AP0_AI_II
S4_CI_SSF	AP0_AI_PSI
AP0_TI_CK	AP0_AI_TSF
AP0_TI_FS	AP0/S4_A_So_MI_pFJ-
AP0/S4_A_So_MI_1second	AP0/S4_A_So_MI_pFJ+

Processes and anomalies:

The generation of frame alignment pattern in order to indicate the initial segment of a multi-segment VC-4 transport stream according to clause 6.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

The division of the VC-4 octet stream into segments as specified in clause 6. See ES 201 803-2-3 [6] clause 6.1.13.5.

The multiplexing of the section alignment signal and the 5 first octets of the segment into an initial slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of 8 contiguous octets in the segment into a data slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of an initial slot and 293 contiguous data slots into a slot stream on AI_D. See ES 201 803-2-3 [6] clause 6.1.13.6.

sII: The indirect multiplexing (performed by the TT_So) of 0, 1 or 2 idle markers prior to the initial segment (see clause 6) by assertion of the Idle Insertion signal (sII). The number of idle markers is given by the frequency justification process, see ES 201 803-2-3 [6] clause 6.1.12.1. See ES 201 803-2-3 [6] clause 6.1.13.6.

sPSI: The Performance Supervision Insertion signal (sPSI) is asserted when the performance supervision special marker of a segment is to be transmitted according to clause 6, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.13.6.

The continuous monitoring of the deviation in phase between the incoming signal and the transmitted signal is performed in order do perform frequency justifications. See ES 201 803-2-3 [6] clause 6.1.8.1.

The performance of positive justification when the incoming signal rate is above the nominal signal rate, by the transmission of a data in replacement of an idle-marker where positive justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 6.1.

The performance of negative justification when the incoming signal rate is below the nominal signal rate, by the transmission of an idle-marker in place of data where negative justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 6.1.

nFJ+: The positive frequency justification anomaly (nFJ+) is asserted when a positive frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

nFJ-: The negative frequency justification anomaly (nFJ-) is asserted when a negative frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

AIS: The Alarm Indication Signal (AIS) insertion into AI_D instead of received signal when the CI_SSF signal is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

None.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Server Signal Fail (SSF) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← CI_SSF.

Defect correlation:

None.

Performance monitoring:

pFJ+ (A_So): The Positive Frequency Justification performance (pFJ+) is the number of positive frequency justifications anomalies (nFJ+) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.1.

pFJ+ ← Σ nFJ+.

pFJ- (A_So): The Negative Frequency Justification performance (pFJ-) is the number of negative frequency justifications anomalies (nFJ-) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.2.

pFJ- ← Σ nFJ-.

Output mapping:

AP0_AI_D ← AI_D.

AP0_AI_CK ← AP0_TI_CK.

AP0_AI_II ← sII.

AP0_AI_PSI ← sPSI.

AP0_AI_TSF ← S4_CI_SSF.

AP0/S4_A_So_MI_pFJ+ ← pFJ+.

AP0/S4_A_So_MI_pFJ- ← pFJ-.

Fault management:

None.

Long term performance monitoring:

FJ+(t-10) (A_Sk): The delayed positive Frequency Justification performance counter (FJ+(t-10)) is the 10 second delayed value of the positive Frequency Justification performance counter (pFJ+). See ES 201 803-2-3 [6] clause 6.8.5.2.

FJ-(t-10) (A_Sk): The delayed negative Frequency Justification performance counter (FJ-(t-10)) is the 10 second delayed value of the negative Frequency Justification performance counter (pFJ-). See ES 201 803-2-3 [6] clause 6.8.5.2.

5.4.1.2 Media Adaptation Sink function (AP0/S4_A_Sk)

Symbol:

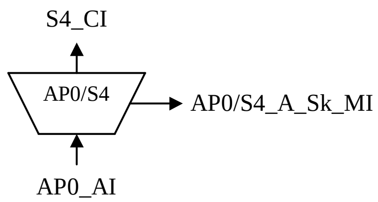

Figure 10: Media Adaptation Sink (AP0/S4_A_Sk)

Interfaces:

Table 4: AP0/S4_A_Sk Input and output signals

Input(s)	Output(s)
AP0_AI_D	S4_CI_D
AP0_AI_CK	S4_CI_CK
AP0_AI_II	S4_CI_FS
AP0_AI_PSI	S4_CI_SSF
AP0_AI_TSF	AP0/S4_A_Sk_MI_cAIS
	AP0/S4_A_Sk_MI_cLOJ

Processes and anomalies:

The monitoring of frame alignment pattern in order to identify the initial segment of a multi-segment VC-4 transport stream according to clause 6.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

sFS: When the initial segment is detected and the first of its data words is transmitted on CI_D shall the Frame Start signal (sFS) be asserted, else it shall be de-asserted. See ES 201 803-2-3 [6] clause 6.1.9.4.

nLOJ: If the initial segment does not occur after the specified justification, then the Loss Of Justification anomaly (nLOJ) is asserted, else nLOJ is not asserted. See clause 6.2.1 and ES 201 803-2-3 [6] clause 6.1.9.4.

The demultiplexing of the initial slot and 293 contiguous data slots from the slot stream on AI_D.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the initial slot to the section alignment signal and the 5 first octets of the segment.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the data slots into 8 contiguous octets in the VC-4 octet stream.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The reconstruction of the VC-4 octet stream from the received segments as specified in clause 6.
See ES 201 803-2-3 [6] clause 6.1.13.5.

The clock smoothing process in order to reduce phase deviations on the transmitted signal. The clock smoothing must comply with the jitter and wander requirements as defined in EN 300 417-1-1 [1]. The resulting clock is delivered as CI_CK. See ES 201 803-2-3 [6] clause 6.1.11.3.

The elastic buffering of the transported signal such that the buffer output is being clocked by the smoothed clock. See ES 201 803-2-3 [6] clause 6.1.11.3.

AIS (A_Sk): The Alarm Indication Signal (AIS) insertion into CI_D instead of received data when the Alarm Indication Signal defect (dAIS) is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

nAIS: The Alarm Indication Signal anomaly (nAIS) is asserted when an AIS-marker is being detected in the AI_D stream. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

The justification persistence state machine monitors the Loss Of Justification anomaly (nLOJ). The default state is Out Of Frame (OOF). When in the OOF state the nLOJ is not asserted on three consecutive justification opportunities, the state of the machine shall change to In Frame (IF). When in the IF state the nLOJ is asserted on five consecutive justification opportunities, the state of the machine shall change to OOF. See ES 201 803-2-3 [6] clause 6.2.4.2.

dLOJ: The Loss Of Justification defect (dLOJ) shall be asserted when the justification persistence state machine is in the OOF state. See ES 201 803-2-3 [6] clause 6.2.4.2.

dAIS (A_Sk): The Alarm Indication Signal defect (dAIS) is asserted when the Alarm Indication Signal anomaly (nAIS) is asserted for more than three consecutive DTM frames, else it is not asserted. See ES 201 803-2-3 [6] clause 6.2.6.1.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Loss Of Justification defect (dLOJ), the Alarm Indication Signal defect (dAIS) is asserted or the Trail Signal Fail (AI_TSF) is. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← dLOJ or dAIS or AI_TSF.

aSSF: The Server Signal Fail action (aSSF) is asserted when the Alarm Indication Signal defect (dAIS) is asserted, the Trail Signal Fail (AI_TSF) is asserted or the Loss Of Justification defect (dLOJ) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.2.

aSSF ← dAIS or AI_TSF or dLOJ.

Defect correlation:

cLOJ: The Loss Of Justification cause (cLOJ) is asserted when the Loss Of Justification defect (dLOJ) is asserted, the Alarm Indication Signal defect (dAIS) not asserted and Trail Signal Fail (AI_TSF) is not asserted.
See ES 201 803-2-3 [6] clause 6.4.4.2.

cLOJ ← dLOJ and (not dAIS) and (not AI_TSF)

cAIS: The Alarm Indication Signal cause (cAIS) is asserted when the Alarm Indication Signal defect (dAIS) is asserted and the Trail Signal Failure (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.6.1.

cAIS ← dAIS and (not AI_TSF)

Performance monitoring:

None.

Output mapping:

S4_CI_D ← CI_D.

S4_CI_CK ← CI_CK.

S4_CI_FS ← sFS.

S4_CI_SSF ← aSSF.

AP0/S4_A_Sk_MI_cLOJ ← cLOJ.

AP0/S4_A_Sk_MI_cAIS ← cAIS.

Fault management:

fAIS (A_Sk): The Alarm Indication Signal fault (fAIS) is asserted when the Alarm Indication Signal cause (cAIS) is asserted consistently for $2,5 \pm 0,5$ seconds and not asserted when the cAIS have been not asserted for $10 \pm 0,5$ seconds.
See ES 201 803-2-3 [6] clause 6.6.1.3.

fLOJ (A_Sk): The Loss Of Justification fault (fLOF) is asserted when the Loss Of Justification cause (cLOJ) is asserted consistently for $2,5 \pm 0,5$ seconds and not asserted when the cLOJ have been not asserted for $10 \pm 0,5$ seconds.
See ES 201 803-2-3 [6] clause 6.6.1.6.

Long term performance monitoring:

None.

5.4.2 DTM Application 0/SDH Higher order path Adaptation function (AP0/S3_A)

This clause describes the SDH VC-3 adaptation using DCAP-0 trail terminators.

5.4.2.1 Media Adaptation Source function (AP0/S3_A_So)

Symbol:

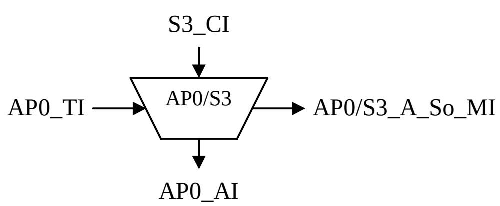

Figure 11: DTM Application 0/SDH Higher order path Adaptation Source (AP0/S3_A_So)

Interfaces:

Table 5: AP0/S3_A_So Input and output signals

Input(s)	Output(s)
S3_CI_D	AP0_AI_D
S3_CI_CK	AP0_AI_CK
S3_CI_FS	AP0_AI_II
S3_CI_SSF	AP0_AI_PSI
AP0_TI_CK	AP0_AI_TSF
AP0_TI_FS	AP0/S3_A_So_MI_pFJ-
AP0/S3_A_So_MI_1second	AP0/S3_A_So_MI_pFJ+

Processes and anomalies:

The generation of frame alignment pattern in order to indicate the initial segment of a multi-segment VC-3 transport stream according to clause 7.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

The division of the VC-3 octet stream into segments as specified in clause 7. See ES 201 803-2-3 [6] clause 6.1.13.5.

The multiplexing of the section alignment signal and the 7 first octets of the segment into an initial slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of 8 contiguous octets in the segment into a data slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of an initial slot and 97 contiguous data slots into a slot stream on AI_D. See ES 201 803-2-3 [6] clause 6.1.13.6.

sII (A_So): The indirect multiplexing (performed by the TT_So) of 0, 1 or 2 idle markers prior to the initial segment (see clause 6) by assertion of the Idle Insertion signal (sII). The number of idle markers is given by the frequency justification process, see ES 201 803-2-3 [6] clauses 6.1.12.1 and 6.1.13.6.

sPSI (A_So): The Performance Supervision Insertion signal (sPSI) is asserted when the performance supervision special marker of a segment is to be transmitted according to clause 6, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.13.6.

The continuous monitoring of the deviation in phase between the incoming signal and the transmitted signal is performed in order do perform frequency justifications. See ES 201 803-2-3 [6] clause 6.1.8.1.

The performance of positive justification when the incoming signal rate is above the nominal signal rate, by the transmission of a data in replacement of an idle-marker where positive justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 7.1.

The performance of negative justification when the incoming signal rate is below the nominal signal rate, by the transmission of an idle-marker in place of data where negative justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 7.1.

nFJ+: The positive frequency justification anomaly (nFJ+) is asserted when a positive frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

nFJ-: The negative frequency justification anomaly (nFJ-) is asserted when a negative frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

AIS: The Alarm Indication Signal (AIS) insertion into AI_D instead of received signal when the CI_SSF signal is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

None.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Server Signal Fail (SSF) is asserted.
See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← CI_SSF.

Defect correlation:

None.

Performance monitoring:

pFJ+ (A_So): The Positive Frequency Justification performance (pFJ+) is the number of positive frequency justifications anomalies (nFJ+) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.1.

pFJ+ ← Σ nFJ+.

pFJ- (A_So): The Negative Frequency Justification performance (pFJ-) is the number of negative frequency justifications anomalies (nFJ-) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.2.

pFJ- ← Σ nFJ-.

Output mapping:

AP0_AI_D ← AI_D.

AP0_AI_CK ← AP0_TI_CK.

AP0_AI_II ← sII.

AP0_AI_PSI ← sPSI.

AP0_AI_TSF ← AP0_CI_SSF.

AP0/S3_A_So_MI_pFJ+ ← pFJ+.

AP0/S3_A_So_MI_pFJ- ← pFJ-.

Fault management:

None.

Long term performance monitoring:

FJ+(t-10) (A_Sk): The delayed positive Frequency Justification performance counter (FJ+(t-10)) is the 10 second delayed value of the positive Frequency Justification performance counter (pFJ+). See ES 201 803-2-3 [6] clause 6.8.5.2.

FJ-(t-10) (A_Sk): The delayed negative Frequency Justification performance counter (FJ-(t-10)) is the 10 second delayed value of the negative Frequency Justification performance counter (pFJ-). See ES 201 803-2-3 [6] clause 6.8.5.2.

5.4.2.2 Media Adaptation Sink function (AP0/S3_A_Sk)

Symbol:

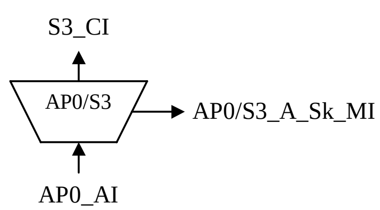

Figure 12: Media Adaptation Sink (AP0/S3_A_Sk)

Interfaces:

Table 6: AP0/S4_A_Sk Input and output signals

Input(s)	Output(s)
AP0_AI_D	S3_CI_D
AP0_AI_CK	S3_CI_CK
AP0_AI_II	S3_CI_FS
AP0_AI_PSI	S3_CI_SSF
AP0_AI_TSF	AP0/S3_A_Sk_MI_cAIS
	AP0/S3_A_Sk_MI_cLOJ

Processes and anomalies:

The monitoring of frame alignment pattern in order to identify the initial segment of a multi-segment VC-3 transport stream according to clause 7.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

sFS: When the initial segment is detected and the first of its data words is transmitted on CI_D shall the Frame Start signal (sFS) be asserted, else it shall be de-asserted. See ES 201 803-2-3 [6] clause 6.1.9.4.

nLOJ: If the initial segment does not occur after the specified justification, then the Loss Of Justification anomaly (nLOJ) is asserted, else nLOJ is not asserted. See clause 6.2.1 and ES 201 803-2-3 [6] clause 6.1.9.4.

The demultiplexing of the initial slot and 97 contiguous data slots from the slot stream on AI_D.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the initial slot to the section alignment signal and the 7 first octets of the segment.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the data slots into 8 contiguous octets in the VC-3 octet stream.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The reconstruction of the VC3 octet stream from the received segments as specified in clause 7.
See ES 201 803-2-3 [6] clause 6.1.13.5.

The clock smoothing process in order to reduce phase deviations on the transmitted signal. The clock smoothing must comply with the jitter and wander requirements as defined in EN 300 417-1-1 [1]. The resulting clock is delivered as CI_CK. See ES 201 803-2-3 [6] clause 6.1.11.3.

The elastic buffering of the transported signal such that the buffer output is being clocked by the smoothed clock. See ES 201 803-2-3 [6] clause 6.1.11.3.

AIS (A_Sk): The Alarm Indication Signal (AIS) insertion into CI_D instead of received data when the Alarm Indication Signal defect (dAIS) is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

nAIS: The Alarm Indication Signal anomaly (nAIS) is asserted when an AIS-marker is being detected in the AI_D stream. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

The justification persistence state machine monitors the Loss Of Justification anomaly (nLOJ). The default state is Out Of Frame (OOF). When in the OOF state the nLOJ is not asserted on three consecutive justification opportunities, the state of the machine shall change to In Frame (IF). When in the IF state the nLOJ is asserted on five consecutive justification opportunities, the state of the machine shall change to OOF. See ES 201 803-2-3 [6] clause 6.2.4.2.

dLOJ: The Loss Of Justification defect (dLOJ) shall be asserted when the justification persistence state machine is in the OOF state. See ES 201 803-2-3 [6] clause 6.2.4.2.

dAIS (A_Sk): The Alarm Indication Signal defect (dAIS) is asserted when the Alarm Indication Signal anomaly (nAIS) is asserted for more than three consecutive DTM frames, else it is not asserted. See ES 201 803-2-3 [6] clause 6.2.6.1.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Loss Of Justification defect (dLOJ), the Alarm Indication Signal defect (dAIS) is asserted or the Trail Signal Fail (AI_TSF) is. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← dLOJ or dAIS or AI_TSF.

aSSF: The Server Signal Fail action (aSSF) is asserted when the Alarm Indication Signal defect (dAIS) is asserted, the Trail Signal Fail (AI_TSF) is asserted or the Loss Of Justification defect (dLOJ) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.2.

aSSF ← dAIS or AI_TSF or dLOJ.

Defect correlation:

cLOJ: The Loss Of Justification cause (cLOJ) is asserted when the Loss Of Justification defect (dLOJ) is asserted, the Alarm Indication Signal defect (dAIS) not asserted and Trail Signal Fail (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.4.2.

cLOJ ← dLOJ and (not dAIS) and (not AI_TSF).

cAIS: The Alarm Indication Signal cause (cAIS) is asserted when the Alarm Indication Signal defect (dAIS) is asserted and the Trail Signal Failure (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.6.1.

cAIS ← dAIS and (not AI_TSF)

Performance monitoring:

None.

Output mapping:

S3_CI_D ← CI_D.

S3_CI_CK ← CI_CK.

S3_CI_FS ← sFS.

S3_CI_SSF ← aSSF.

AP0/S3_A_Sk_MI_cLOJ ← cLOJ.

AP0/S3_A_Sk_MI_cAIS ← cAIS.

Fault management:

fAIS (A_Sk): The Alarm Indication Signal fault (fAIS) is asserted when the Alarm Indication Signal cause (cAIS) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cAIS have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.3.

fLOJ (A_Sk): The Loss Of Justification fault (fLOF) is asserted when the Loss Of Justification cause (cLOJ) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cLOJ have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.6.

Long term performance monitoring:

None.

5.4.3 DTM Application 0/SDH Lower order S2 path Adaptation function (AP0/S2_A)

This clause describes the SDH VC-2 adaptation using DCAP-0 trail terminators.

5.4.3.1 Application 0 to SDH Lower order path S2 Adaptation Source function (AP0/S2_A_So)

Symbol:

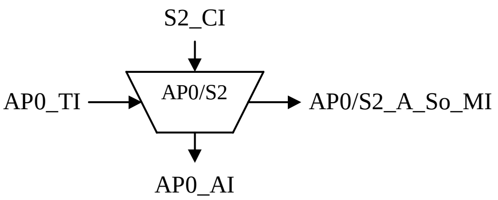

Figure 13: DTM Application 0/SDH Lower order path S2 Adaptation Source (AP0/S2_A_So)

Interfaces:

Table 7: AP0/S2_A_So Input and output signals

Input(s)	Output(s)
S2_CI_D	AP0_AI_D
S2_CI_CK	AP0_AI_CK
S2_CI_FS	AP0_AI_II
S2_CI_SSF	AP0_AI_PSI
AP0_TI_CK	AP0_AI_TSF
AP0_TI_FS	AP0/S2_A_So_MI_pFJ-
AP0/S2_A_So_MI_1second	AP0/S2_A_So_MI_pFJ+

Processes and anomalies:

The generation of frame alignment pattern in order to indicate the initial segment of a multi-segment VC-2 transport stream according to clause 8.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

The division of the VC-2 octet stream into segments as specified in clause 8. See ES 201 803-2-3 [6] clause 6.1.13.5.

The multiplexing of the section alignment signal into an initial slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of 8 contiguous octets in the segment into a data slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of an initial slot and 53 contiguous data slots into a slot stream on AI_D. See ES 201 803-2-3 [6] clause 6.1.13.6.

sII (A_So): The indirect multiplexing (performed by the TT_So) of 0, 1 or 2 idle markers prior to the initial segment (see clause 6) by assertion of the Idle Insertion signal (sII). The number of idle markers is given by the frequency justification process, see ES 201 803-2-3 [6] clauses 6.1.12.1 and 6.1.13.6.

sPSI (A_So): The Performance Supervision Insertion signal (sPSI) is asserted when the performance supervision special marker of a segment is to be transmitted according to clause 6, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.13.6.

The continuous monitoring of the deviation in phase between the incoming signal and the transmitted signal is performed in order do perform frequency justifications. See ES 201 803-2-3 [6] clause 6.1.8.1.

The performance of positive justification when the incoming signal rate is above the nominal signal rate, by the transmission of a data in replacement of an idle-marker where positive justification is allowed.
See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 8.1.

The performance of negative justification when the incoming signal rate is below the nominal signal rate, by the transmission of an idle-marker in place of data where negative justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 8.1.

nFJ+: The positive frequency justification anomaly (nFJ+) is asserted when a positive frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

nFJ-: The negative frequency justification anomaly (nFJ-) is asserted when a negative frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

AIS: The Alarm Indication Signal (AIS) insertion into AI_D instead of received signal when the CI_SSF signal is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

None.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Server Signal Fail (SSF) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← CI_SSF.

Defect correlation:

None.

Performance monitoring:

pFJ+ (A_So): The Positive Frequency Justification performance (pFJ+) is the number of positive frequency justifications anomalies (nFJ+) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.1.

pFJ+ ← Σ nFJ+.

pFJ- (A_So): The Negative Frequency Justification performance (pFJ-) is the number of negative frequency justifications anomalies (nFJ-) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.2.

pFJ- ← Σ nFJ-.

Output mapping:

AP0_AI_D ← AI_D.

AP0_AI_CK ← AP0_TI_CK.

AP0_AI_II ← sII.

AP0_AI_PSI ← sPSI.

AP0_AI_TSF ← AP0_CI_SSF.

AP0/S2_A_So_MI_pFJ+ ← pFJ+.

AP0/S2_A_So_MI_pFJ- ← pFJ-.

Fault management:

None.

Long term performance monitoring:

FJ+(t-10) (A_Sk): The delayed positive Frequency Justification performance counter (FJ+(t-10)) is the 10 second delayed value of the positive Frequency Justification performance counter (pFJ+). See ES 201 803-2-3 [6] clause 6.8.5.2.

FJ-(t-10) (A_Sk): The delayed negative Frequency Justification performance counter (FJ-(t-10)) is the 10 second delayed value of the negative Frequency Justification performance counter (pFJ-). See ES 201 803-2-3 [6] clause 6.8.5.2.

5.4.3.2 Application 0 to SDH Lower order path S2 Adaptation Sink function (AP0/S2_A_Sk)

Symbol:

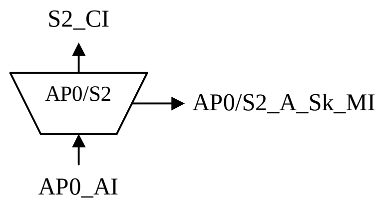

Figure 14: Application 0 to SDH Lower order path Adaptation Sink (AP0/S2_A_Sk)

Interfaces:

Table 8: AP0/S2_A_Sk Input and output signals

Input(s)	Output(s)
AP0_AI_D	S2_CI_D
AP0_AI_CK	S2_CI_CK
AP0_AI_II	S2_CI_FS
AP0_AI_PSI	S2_CI_SSF
AP0_AI_TSF	AP0/S2_A_Sk_MI_cAIS
	AP0/S2_A_Sk_MI_cLOJ

Processes and anomalies:

The monitoring of frame alignment pattern in order to identify the initial segment of a multi-segment VC-2 transport stream according to clause 8.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

sFS: When the initial segment is detected and the first of its data words is transmitted on CI_D shall the Frame Start signal (sFS) be asserted, else it shall be de-asserted. See ES 201 803-2-3 [6] clause 6.1.9.4.

nLOJ: If the initial segment does not occur after the specified justification, then the Loss Of Justification anomaly (nLOJ) is asserted, else nLOJ is not asserted. See clause 8.2.1 and ES 201 803-2-3 [6] clause 6.1.9.4.

The demultiplexing of the initial slot and 53 contiguous data slots from the slot stream on AI_D. See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the initial slot to the section alignment signal. See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the data slots into 8 contiguous octets in the VC-2 octet stream. See ES 201 803-2-3 [6] clause 6.1.13.6.

The reconstruction of the VC-2 octet stream from the received segments as specified in clause 8. See ES 201 803-2-3 [6] clause 6.1.13.5.

The clock smoothing process in order to reduce phase deviations on the transmitted signal. The clock smoothing must comply with the jitter and wander requirements as defined in EN 300 417-1-1 [1]. The resulting clock is delivered as CI_CK. See ES 201 803-2-3 [6] clause 6.1.11.3.

The elastic buffering of the transported signal such that the buffer output is being clocked by the smoothed clock. See ES 201 803-2-3 [6] clause 6.1.11.3.

AIS (A_Sk): The Alarm Indication Signal (AIS) insertion into CI_D instead of received data when the Alarm Indication Signal defect (dAIS) is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

nAIS: The Alarm Indication Signal anomaly (nAIS) is asserted when an AIS-marker is being detected in the AI_D stream. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

The justification persistence state machine monitors the Loss Of Justification anomaly (nLOJ). The default state is Out Of Frame (OOF). When in the OOF state the nLOJ is not asserted on three consecutive justification opportunities, the state of the machine shall change to In Frame (IF). When in the IF state the nLOJ is asserted on five consecutive justification opportunities, the state of the machine shall change to OOF. See ES 201 803-2-3 [6] clause 6.2.4.2.

dLOJ: The Loss Of Justification defect (dLOJ) shall be asserted when the justification persistence state machine is in the OOF state. See ES 201 803-2-3 [6] clause 6.2.4.2.

dAIS (A_Sk): The Alarm Indication Signal defect (dAIS) is asserted when the Alarm Indication Signal anomaly (nAIS) is asserted for more than three consecutive DTM frames, else it is not asserted. See ES 201 803-2-3 [6] clause 6.2.6.1.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Loss Of Justification defect (dLOJ), the Alarm Indication Signal defect (dAIS) is asserted or the Trail Signal Fail (AI_TSF) is. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← dLOJ or dAIS or AI_TSF.

aSSF: The Server Signal Fail action (aSSF) is asserted when the Alarm Indication Signal defect (dAIS) is asserted, the Trail Signal Fail (AI_TSF) is asserted or the Loss Of Justification defect (dLOJ) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.2.

aSSF ← dAIS or AI_TSF or dLOJ.

Defect correlation:

cLOJ: The Loss Of Justification cause (cLOJ) is asserted when the Loss Of Justification defect (dLOJ) is asserted, the Alarm Indication Signal defect (dAIS) not asserted and Trail Signal Fail (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.4.2.

cLOJ ← dLOJ and (not dAIS) and (not AI_TSF).

cAIS: The Alarm Indication Signal cause (cAIS) is asserted when the Alarm Indication Signal defect (dAIS) is asserted and the Trail Signal Failure (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.6.1.

cAIS ← dAIS and (not AI_TSF)

Performance monitoring:

None.

Output mapping:

S2_CI_D ← CI_D.

S2_CI_CK ← CI_CK.

S2_CI_FS ← sFS.

S2_CI_SSF ← aSSF.

AP0/S2_A_Sk_MI_cLOJ ← cLOJ.

AP0/S2_A_Sk_MI_cAIS ← cAIS.

Fault management:

fAIS (A_Sk): The Alarm Indication Signal fault (fAIS) is asserted when the Alarm Indication Signal cause (cAIS) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cAIS have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.3.

fLOJ (A_Sk): The Loss Of Justification fault (fLOF) is asserted when the Loss Of Justification cause (cLOJ) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cLOJ have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.6.

Long term performance monitoring:

None.

5.4.4 DTM Application 0/SDH Lower order S12 path Adaptation function (AP0/S12_A)

This clause describes the SDH VC-12 adaptation using DCAP-0 trail terminators.

5.4.4.1 Application 0 to SDH Lower order path S12 Adaptation Source function (AP0/S12_A_So)

Symbol:

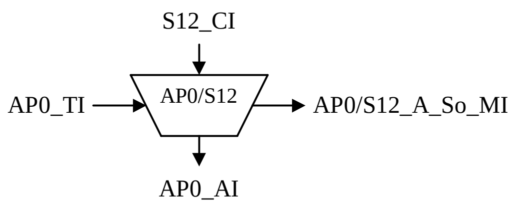

Figure 15: DTM Application 0/SDH Lower order path S12 Adaptation Source (AP0/S12_A_So)

Interfaces:

Table 9: AP0/S12_A_So Input and output signals

Input(s)	Output(s)
S12_CI_D	AP0_AI_D
S12_CI_CK	AP0_AI_CK
S12_CI_FS	AP0_AI_II
S12_CI_SSF	AP0_AI_PSI
AP0_TI_CK	AP0_AI_TSF
AP0_TI_FS	AP0/S12_A_So_MI_pFJ-
AP0/S12_A_So_MI_1second	AP0/S12_A_So_MI_pFJ+

Processes and anomalies:

The generation of frame alignment pattern in order to indicate the initial segment of a multi-segment VC-12 transport stream according to clause 9.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

The division of the VC-12 octet stream into segments as specified in clause 9. See ES 201 803-2-3 [6] clause 6.1.13.5.

The multiplexing of the section alignment signal and the 4 first octets of the segment into an initial slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of 8 contiguous octets in the segment into a data slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of an initial slot and 17 contiguous data slots into a slot stream on AI_D. See ES 201 803-2-3 [6] clause 6.1.13.6.

sII (A_So): The indirect multiplexing (performed by the TT_So) of 0, 1 or 2 idle markers prior to the initial segment (see clause 6) by assertion of the Idle Insertion signal (sII). The number of idle markers is given by the frequency justification process, see ES 201 803-2-3 [6] clauses 6.1.12.1 and 6.1.13.6.

sPSI (A_So): The Performance Supervision Insertion signal (sPSI) is asserted when the performance supervision special marker of a segment is to be transmitted according to clause 6, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.13.6.

The continuous monitoring of the deviation in phase between the incoming signal and the transmitted signal is performed in order do perform frequency justifications. See ES 201 803-2-3 [6] clause 6.1.8.1.

The performance of positive justification when the incoming signal rate is above the nominal signal rate, by the transmission of a data in replacement of an idle-marker where positive justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 9.1.

The performance of negative justification when the incoming signal rate is below the nominal signal rate, by the transmission of an idle-marker in place of data where negative justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 9.1.

nFJ+: The positive frequency justification anomaly (nFJ+) is asserted when a positive frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

nFJ-: The negative frequency justification anomaly (nFJ-) is asserted when a negative frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

AIS: The Alarm Indication Signal (AIS) insertion into AI_D instead of received signal when the CI_SSF signal is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

None.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Server Signal Fail (SSF) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← CI_SSF.

Defect correlation:

None.

Performance monitoring:

pFJ+ (A_So): The Positive Frequency Justification performance (pFJ+) is the number of positive frequency justifications anomalies (nFJ+) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.1.

pFJ+ ← Σ nFJ+.

pFJ- (A_So): The Negative Frequency Justification performance (pFJ-) is the number of negative frequency justifications anomalies (nFJ-) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.2.

pFJ- ← Σ nFJ-.

Output mapping:

AP0_AI_D ← AI_D.

AP0_AI_CK ← AP0_TI_CK.

AP0_AI_II ← sII.

AP0_AI_PSI ← sPSI.

AP0_AI_TSF ← AP0_CI_SSF.

AP0/S12_A_So_MI_pFJ+ ← pFJ+.

AP0/S12_A_So_MI_pFJ- ← pFJ-.

Fault management:

None.

Long term performance monitoring:

FJ+(t-10) (A_Sk): The delayed positive Frequency Justification performance counter (FJ+(t-10)) is the 10 second delayed value of the positive Frequency Justification performance counter (pFJ+). See ES 201 803-2-3 [6] clause 6.8.5.2.

FJ-(t-10) (A_Sk): The delayed negative Frequency Justification performance counter (FJ-(t-10)) is the 10 second delayed value of the negative Frequency Justification performance counter (pFJ-). See ES 201 803-2-3 [6] clause 6.8.5.2.

5.4.4.2 Application 0 to SDH Lower order path S12 Adaptation Sink function (AP0/S12_A_Sk)

Symbol:

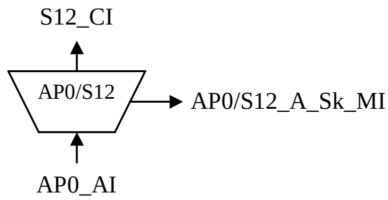

Figure 16: Application 0 to SDH Lower order path S12 Adaptation Sink (AP0/S12_A_Sk)

Interfaces:

Table 10: AP0/S12_A_Sk Input and output signals

Input(s)	Output(s)
AP0_AI_D	S12_CI_D
AP0_AI_CK	S12_CI_CK
AP0_AI_II	S12_CI_FS
AP0_AI_PSI	S12_CI_SSF
AP0_AI_TSF	AP0/S12_A_Sk_MI_cAIS
	AP0/S12_A_Sk_MI_cLOJ

Processes and anomalies:

The monitoring of frame alignment pattern in order to identify the initial segment of a multi-segment VC-12 transport stream according to clause 9.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

sFS: When the initial segment is detected and the first of its data words is transmitted on CI_D shall the Frame Start signal (sFS) be asserted, else it shall be de-asserted. See ES 201 803-2-3 [6] clause 6.1.9.4.

nLOJ: If the initial segment does not occur after the specified justification, then the Loss Of Justification anomaly (nLOJ) is asserted, else nLOJ is not asserted. See clause 9.2.1 and ES 201 803-2-3 [6] clause 6.1.9.4.

The demultiplexing of the initial slot and 17 contiguous data slots from the slot stream on AI_D.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the initial slot to the section alignment signal and the 4 first octets of the segment.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the data slots into 8 contiguous octets in the VC-12 octet stream.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The reconstruction of the VC-12 octet stream from the received segments as specified in clause 9.
See ES 201 803-2-3 [6] clause 6.1.13.5.

The clock smoothing process in order to reduce phase deviations on the transmitted signal. The clock smoothing must comply with the jitter and wander requirements as defined in EN 300 417-1-1 [1]. The resulting clock is delivered as CI_CK. See ES 201 803-2-3 [6] clause 6.1.11.3.

The elastic buffering of the transported signal such that the buffer output is being clocked by the smoothed clock. See ES 201 803-2-3 [6] clause 6.1.11.3.

AIS (A_Sk): The Alarm Indication Signal (AIS) insertion into CI_D instead of received data when the Alarm Indication Signal defect (dAIS) is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

nAIS: The Alarm Indication Signal anomaly (nAIS) is asserted when an AIS-marker is being detected in the AI_D stream. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

The justification persistence state machine monitors the Loss Of Justification anomaly (nLOJ). The default state is Out Of Frame (OOF). When in the OOF state the nLOJ is not asserted on three consecutive justification opportunities, the state of the machine shall change to In Frame (IF). When in the IF state the nLOJ is asserted on five consecutive justification opportunities, the state of the machine shall change to OOF. See ES 201 803-2-3 [6] clause 6.2.4.2.

dLOJ: The Loss Of Justification defect (dLOJ) shall be asserted when the justification persistence state machine is in the OOF state. See ES 201 803-2-3 [6] clause 6.2.4.2.

dAIS (A_Sk): The Alarm Indication Signal defect (dAIS) is asserted when the Alarm Indication Signal anomaly (nAIS) is asserted for more than three consecutive DTM frames, else it is not asserted. See ES 201 803-2-3 [6] clause 6.2.6.1.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Loss Of Justification defect (dLOJ), the Alarm Indication Signal defect (dAIS) is asserted or the Trail Signal Fail (AI_TSF) is. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← dLOJ or dAIS or AI_TSF.

aSSF: The Server Signal Fail action (aSSF) is asserted when the Alarm Indication Signal defect (dAIS) is asserted, the Trail Signal Fail (AI_TSF) is asserted or the Loss Of Justification defect (dLOJ) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.2.

aSSF ← dAIS or AI_TSF or dLOJ.

Defect correlation:

cLOJ: The Loss Of Justification cause (cLOJ) is asserted when the Loss Of Justification defect (dLOJ) is asserted, the Alarm Indication Signal defect (dAIS) not asserted and Trail Signal Fail (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.4.2.

cLOJ ← dLOJ and (not dAIS) and (not AI_TSF).

cAIS: The Alarm Indication Signal cause (cAIS) is asserted when the Alarm Indication Signal defect (dAIS) is asserted and the Trail Signal Failure (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.6.1.

cAIS ← dAIS and (not AI_TSF)

Performance monitoring:

None.

Output mapping:

S12_CI_D ← CI_D.

S12_CI_CK ← CI_CK.

S12_CI_FS ← sFS.

S12_CI_SSF ← aSSF.

AP0/S12_A_Sk_MI_cLOJ ← cLOJ.

AP0/S12_A_Sk_MI_cAIS ← cAIS.

Fault management:

fAIS (A_Sk): The Alarm Indication Signal fault (fAIS) is asserted when the Alarm Indication Signal cause (cAIS) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cAIS have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.3.

fLOJ (A_Sk): The Loss Of Justification fault (fLOF) is asserted when the Loss Of Justification cause (cLOJ) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cLOJ have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.6.

Long term performance monitoring:

None.

5.4.5 DTM Application 0/SDH Lower order S11 path Adaptation function (AP0/S11_A)

This clause describes the SDH VC-11 adaptation using DCAP-0 trail terminators.

5.4.5.1 Application 0 to SDH Lower order path S11 Adaptation Source function (AP0/S11_A_So)

Symbol:

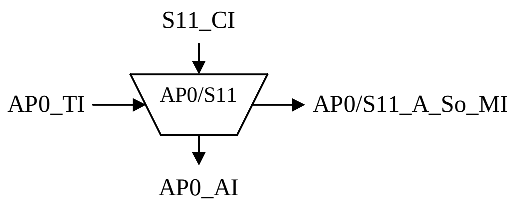

Figure 17: DTM Application 0/SDH Lower order path S11 Adaptation Source (AP0/S11_A_So)

Interfaces:

Table 11: AP0/S11_A_So Input and output signals

Input(s)	Output(s)
S11_CI_D	AP0_AI_D
S11_CI_CK	AP0_AI_CK
S11_CI_FS	AP0_AI_II
S11_CI_SSF	AP0_AI_PSI
AP0_TI_CK	AP0_AI_TSF
AP0_TI_FS	AP0/S11_A_So_MI_pFJ-
AP0/S11_A_So_MI_1second	AP0/S11_A_So_MI_pFJ+

Processes and anomalies:

The generation of frame alignment pattern in order to indicate the initial segment of a multi-segment VC-11 transport stream according to clause 10.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

The division of the VC-11 octet stream into segments as specified in clause 10. See ES 201 803-2-3 [6] clause 6.1.13.5.

The multiplexing of the section alignment signal and the 4 first octets of the segment into an initial slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of 8 contiguous octets in the segment into a data slot. See ES 201 803-2-3 [6] clause 6.1.13.6.

The multiplexing of an initial slot and 13 contiguous data slots into a slot stream on AI_D.
See ES 201 803-2-3 [6] clause 6.1.13.6.

sII (A_So): The indirect multiplexing (performed by the TT_So) of 0, 1 or 2 idle markers prior to the initial segment (see clause 6) by assertion of the Idle Insertion signal (sII). The number of idle markers is given by the frequency justification process, see ES 201 803-2-3 [6] clauses 6.1.12.1 and 6.1.13.6.

sPSI (A_So): The Performance Supervision Insertion signal (sPSI) is asserted when the performance supervision special marker of a segment is to be transmitted according to clause 6, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.13.6.

The continuous monitoring of the deviation in phase between the incoming signal and the transmitted signal is performed in order do perform frequency justifications. See ES 201 803-2-3 [6] clause 6.1.8.1.

The performance of positive justification when the incoming signal rate is above the nominal signal rate, by the transmission of a data in replacement of an idle-marker where positive justification is allowed.
See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 10.1.

The performance of negative justification when the incoming signal rate is below the nominal signal rate, by the transmission of an idle-marker in place of data where negative justification is allowed. See ES 201 803-2-3 [6] clause 6.1.8.1. For justification opportunity, see clause 10.1.

nFJ+: The positive frequency justification anomaly (nFJ+) is asserted when a positive frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

nFJ-: The negative frequency justification anomaly (nFJ-) is asserted when a negative frequency justification has occurred, else it is de-asserted. See ES 201 803-2-3 [6] clause 6.1.8.1.

AIS: The Alarm Indication Signal (AIS) insertion into AI_D instead of received signal when the CI_SSF signal is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

None.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Server Signal Fail (SSF) is asserted.
See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← CI_SSF.

Defect correlation:

None.

Performance monitoring:

pFJ+ (A_So): The Positive Frequency Justification performance (pFJ+) is the number of positive frequency justifications anomalies (nFJ+) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.1.

pFJ+ ← Σ nFJ+.

pFJ- (A_So): The Negative Frequency Justification performance (pFJ-) is the number of negative frequency justifications anomalies (nFJ-) that has occurred during 1 second. See ES 201 803-2-3 [6] clause 6.5.3.2.

pFJ- ← Σ nFJ-.

Output mapping:

AP0_AI_D ← AI_D.

AP0_AI_CK ← AP0_TI_CK.

AP0_AI_II ← sII.

AP0_AI_PSI ← sPSI.

AP0_AI_TSF ← AP0_CI_SSF.

AP0/S11_A_So_MI_pFJ+ ← pFJ+.

AP0/S11_A_So_MI_pFJ- ← pFJ-.

Fault management:

None.

Long term performance monitoring:

FJ+(t-10) (A_Sk): The delayed positive Frequency Justification performance counter (FJ+(t-10)) is the 10 second delayed value of the positive Frequency Justification performance counter (pFJ+). See ES 201 803-2-3 [6] clause 6.8.5.2.

FJ-(t-10) (A_Sk): The delayed negative Frequency Justification performance counter (FJ-(t-10)) is the 10 second delayed value of the negative Frequency Justification performance counter (pFJ-). See ES 201 803-2-3 [6] clause 6.8.5.2.

5.4.5.2 Application 0 to SDH Lower order path S11 Adaptation Sink function (AP0/S11_A_Sk)

Symbol:

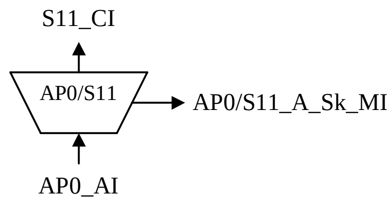

Figure 18: Application 0 to SDH Lower order path S11 Adaptation Sink (AP0/S11_A_Sk)

Interfaces:

Table 12: AP0/S11_A_Sk Input and output signals

Input(s)	Output(s)
AP0_AI_D	S11_CI_D
AP0_AI_CK	S11_CI_CK
AP0_AI_II	S11_CI_FS
AP0_AI_PSI	S11_CI_SSF
AP0_AI_TSF	AP0/S11_A_Sk_MI_cAIS
	AP0/S11_A_Sk_MI_cLOJ

Processes and anomalies:

The monitoring of frame alignment pattern in order to identify the initial segment of a multi-segment VC-11 transport stream according to clause 10.2.1. See ES 201 803-2-3 [6] clause 6.1.9.4.

sFS: When the initial segment is detected and the first of its data words is transmitted on CI_D shall the Frame Start signal (sFS) be asserted, else it shall be de-asserted. See ES 201 803-2-3 [6] clause 6.1.9.4.

nLOJ: If the initial segment does not occur after the specified justification, then the Loss Of Justification anomaly (nLOJ) is asserted, else nLOJ is not asserted. See clause 9.2.1 and ES 201 803-2-3 [6] clause 6.1.9.4.

The demultiplexing of the initial slot and 13 contiguous data slots from the slot stream on AI_D.
See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the initial slot to the section alignment signal and the 4 first octets of the segment. See ES 201 803-2-3 [6] clause 6.1.13.6.

The demultiplexing of the data slots into 8 contiguous octets in the VC-11 octet stream. See ES 201 803-2-3 [6] clause 6.1.13.6.

The reconstruction of the VC-11 octet stream from the received segments as specified in clause 10. See ES 201 803-2-3 [6] clause 6.1.13.5.

The clock smoothing process in order to reduce phase deviations on the transmitted signal. The clock smoothing must comply with the jitter and wander requirements as defined in EN 300 417-1-1 [1]. The resulting clock is delivered as CI_CK. See ES 201 803-2-3 [6] clause 6.1.11.3.

The elastic buffering of the transported signal such that the buffer output is being clocked by the smoothed clock. See ES 201 803-2-3 [6] clause 6.1.11.3.

AIS (A_Sk): The Alarm Indication Signal (AIS) insertion into CI_D instead of received data when the Alarm Indication Signal defect (dAIS) is asserted. See ES 201 803-2-3 [6] clause 6.1.5.1.

nAIS: The Alarm Indication Signal anomaly (nAIS) is asserted when an AIS-marker is being detected in the AI_D stream. See ES 201 803-2-3 [6] clause 6.1.5.1.

Defects:

The justification persistence state machine monitors the Loss Of Justification anomaly (nLOJ). The default state is Out Of Frame (OOF). When in the OOF state the nLOJ is not asserted on three consecutive justification opportunities, the state of the machine shall change to In Frame (IF). When in the IF state the nLOJ is asserted on five consecutive justification opportunities, the state of the machine shall change to OOF. See ES 201 803-2-3 [6] clause 6.2.4.2.

dLOJ: The Loss Of Justification defect (dLOJ) shall be asserted when the justification persistence state machine is in the OOF state. See ES 201 803-2-3 [6] clause 6.2.4.2.

dAIS (A_Sk): The Alarm Indication Signal defect (dAIS) is asserted when the Alarm Indication Signal anomaly (nAIS) is asserted for more than three consecutive DTM frames, else it is not asserted. See ES 201 803-2-3 [6] clause 6.2.6.1.

Consequent actions:

aAIS: The Alarm Indication Signal action (aAIS) is asserted when the Loss Of Justification defect (dLOJ), the Alarm Indication Signal defect (dAIS) is asserted or the Trail Signal Fail (AI_TSF) is. See ES 201 803-2-3 [6] clause 6.3.1.1.

aAIS ← dLOJ or dAIS or AI_TSF.

aSSF: The Server Signal Fail action (aSSF) is asserted when the Alarm Indication Signal defect (dAIS) is asserted, the Trail Signal Fail (AI_TSF) is asserted or the Loss Of Justification defect (dLOJ) is asserted. See ES 201 803-2-3 [6] clause 6.3.1.2.

aSSF ← dAIS or AI_TSF or dLOJ.

Defect correlation:

cLOJ: The Loss Of Justification cause (cLOJ) is asserted when the Loss Of Justification defect (dLOJ) is asserted, the Alarm Indication Signal defect (dAIS) not asserted and Trail Signal Fail (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.4.2.

cLOJ ← dLOJ and (not dAIS) and (not AI_TSF).

cAIS: The Alarm Indication Signal cause (cAIS) is asserted when the Alarm Indication Signal defect (dAIS) is asserted and the Trail Signal Failure (AI_TSF) is not asserted. See ES 201 803-2-3 [6] clause 6.4.6.1.

cAIS ← dAIS and (not AI_TSF)

Performance monitoring:

None.

Output mapping:

S11_CI_D ← CI_D.

S11_CI_CK ← CI_CK.

S11_CI_FS ← sFS.

S11_CI_SSF ← aSSF.

AP0/S11_A_Sk_MI_cLOJ ← cLOJ.

AP0/S11_A_Sk_MI_cAIS ← cAIS.

Fault management:

fAIS (A_Sk): The Alarm Indication Signal fault (fAIS) is asserted when the Alarm Indication Signal cause (cAIS) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cAIS have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.3.

fLOJ (A_Sk): The Loss Of Justification fault (fLOF) is asserted when the Loss Of Justification cause (cLOJ) is asserted consistently for $2{,}5 \pm 0{,}5$ seconds and not asserted when the cLOJ have been not asserted for $10 \pm 0{,}5$ seconds. See ES 201 803-2-3 [6] clause 6.6.1.6.

Long term performance monitoring:

None.

6 Mapping of SDH VC-4 over DTM

The SDH VC-4 (EN 300 417-3-1 [2]) is mapped onto the DTM DCAP-0 ES 201 803-2-3 [6] format, providing means to transport the VC-4 data, VC-4 frame alignment, SSF and providing performance supervision. The VC-4 can be of either VC-4 or VC-4-Xc forms, so mapping must be able to handle X of 1, 4, 16, 64 or 256. Each of the 9 rows of the VC-4 contains $261 \times X$ octets of data, including the POH header. See table 13 for VC-4 and VC-4-Xc mapping characteristics.

Table 13: SDH VC-11, VC-12, VC-2, VC-3, VC-4 and VC-4-Xc basic mapping characteristics

Path layer	VC-11	VC-12	VC-2	VC-3	VC-4	VC-4-4c	VC-4-16c	VC-4-64c	VC-4-256c
Effective octets per line	26	35	107	85	261	1 044	4 176	16 704	66 816
Octets per line	26	35	107	87	261	1 044	4 176	16 704	66 816
Lines	4	4	4	9	9	9	9	9	9
Octets per frame	104	140	428	783	2 349	9 396	37 584	150 336	601 344
Frames per second	2 000	2 000	2 000	8 000	8 000	8 000	8 000	8 000	8 000
Bitrate (Mb/s or Gb/s)	1,664	2,240	6,848	50,112	150,336	601,344	2,405376	9,621504	38,486016
Sections	1	1	1	1	1	4	16	64	256
Octets per section	104	140	428	783	2 349	2 349	2 349	2 349	2 349
Initial slots per section	1	1	1	1	1	1	1	1	1
Octets in initial section	0	4	4	7	5	5	5	5	5
Data Slots per section	13	17	53	97	294	294	294	294	294
PS slots per section	1	1	1	1	1	1	1	1	1
Total slots per section	15	19	55	99	295	295	295	295	295
Total section slots per frame	3,75	4,75	13,75	99	295	1 180	4 720	18 880	75 520
Frequency Justification slots	1	1	1	1	1	1	1	1	1
Total slot count per frame	4	5	14	100	296	1 181	4 721	18 881	75 521

6.1 DCAP-0 slot elements

The DCAP-0 elements of 64 bit data slot, Idle-marker, Performance Supervision-marker (PS-marker), AIS-marker are described in ES 201 803-2-3 [6]. The lines with POH-header and payload are transported in one or more sections holding a complete VC-4 frame.

Each section is prefixed by a PS-marker, holding the channel end-to-end performance supervision, and also acting as a section delimiter. The justification is performed by prefixing 2, 1 or 0 Idle markers before the first section and its PS-marker, thus giving one justification point on each VC-4 frame.

NOTE: The PS-marker of the first section shall include the correct idle marker count of the frequency justification opportunity that just occurred. This is a direct consequence of the DCAP-0 definitions. Similarly, PS-markers for other sections should have zero as their idle marker count values.

6.2 Data slot mapping

The 2 349 octets of each section are divided into one section beginning slot and 293 section data slots. The section data slot holds 8 octets of data while the section beginning slot holds 5 data octets and 3 non-data octets. The non-data octets of the section-beginning slot is used to identify which of the section beginning slots that holds the J1 octet of the transported VC-4. The sections are thus synchronous to the transported VC-4/VC-4-Xc.

6.2.1 Section beginning

The section beginning slots have 3 non-data octets (bit 63 down to 40). One octet is used for identifying the initial segment. The initial segment is encoded as the bit-string 01010101 (bit 63 down to bit 56) and the other segments (if transmitted, i.e. if X > 1) is encoded as the bitstring 00101010 (bit 63 down to bit 56). The lower 7 bits (bit 62 down to bit 56) of the octet is those used to transport an alternating bit pattern such that majority decisions can be performed. Thus, if 4 or more bits indicate initial segment, then the initial segment pattern is detected, else it is not detected. The highest bit (bit 63) of the initial segment identifier octet is reserved. It shall be set to 0 by the transmitter and shall not be interpreted by the receiver.

The 2 unused non-data octets (bit 55 down to 40) are reserved. All bits shall be set to 0 by the transmitting end, and the receiver shall not interpret these octets.

In total 17 bits are reserved and should not be interpreted. The checksum shall however be calculated regardless of the use, i.e. no special measures are required to hide the reserved bits from the checksum calculation.

The 5 data octets (bit 39 down to 0) hold data octets from the VC-4-Xc datastream. If the section beginning is the initial section beginning, the J1 octet of the POH header shall be found in bit 39 down to bit 32 and bit 31 down to bit 0 shall hold the 4 octets immediately after J1 according to normal SDH multiplexing rules (EN 300 417-3-1 [2]).

A frame synchronization state machine continuously monitors the initial segment frame pattern. The state machine has two states, In Frame (IF) and Out Of Frame (OOF). If the state machine is in the OOF state and detects the frame pattern in two sections, being one frame apart (i.e. X sections) then the state machine shall enter the In Frame state. If the state machine is in the IF state and has failed to detect the frame pattern in the expected segment for a total of 5 frames, the state machine shall enter the Out Of Frame state.

6.2.2 Section data

In a section data slot bit 63 down to bit 0 hold shall the next 8 octets of the VC-4 octet stream, beginning with the first octet mapped into bit 63 down to bit 56, and then octet per octet until bit 7 down to 0 have been mapped.

6.3 VC-4 mapping

The VC-4 and VC-4-Xc (including the "fixed stuff" of the POH of column 2 to X) will be converted into X sections, each holding 2 349 octets. The first section for each VC-4 frame will start on the J1 octet (column 1), followed by the octets in normal SDH multiplex order. The section containing the J1 will be marked with a frame marker.

7 Mapping of SDH VC-3 over DTM

The SDH VC-3 (EN 300 417-4-1 [3]) is mapped onto the DTM DCAP-0 ES 201 803-2-3 [6] format, providing means to transport the VC-3 data, VC-3 frame alignment, and SSF and providing performance supervision. Each of the 9 rows of the VC3 contains 85 octets of data, including the POH header. The mapping uses the 87 octets x 9 rows format of the AU-3 (ITU-T Recommendation G.707 [7]) but without the H1, H2 and H3 octets and with fixed phase such that first octet is the J1 octet of the POH header. Column 30 and 59 thus contains fixed stuff (see further in ITU-T Recommendation G.707 [7] clause 7.1.3). See table 13 for VC-3 mapping characteristics.

7.1 DCAP-0 slot elements

The DCAP-0 elements of 64 bit data slot, Idle-marker, Performance Supervision-marker, AIS-marker are described in ES 201 803-2-3 [6]. The lines with POH-header and payload are transported in one section holding a complete VC-3 frame.

Each section is prefixed by a PS-marker, holding the channel end-to-end performance supervision, and also acting as a section delimiter. The justification is performed by prefixing 2, 1 or 0 Idle markers before the section and its PS-marker, thus giving one justification point on each VC-3 frame.

NOTE: The PS-marker of the first section shall include the correct idle marker count of the frequency justification opportunity that just occurred. This is a direct consequence of the DCAP-0 definitions. Similarly, PS-markers for other sections should have zero as their idle marker count values.

7.2 Data slot mapping

The 783 octets of each section are divided into one section beginning slot and 97 section data slots. The section data slot holds 8 octets of data while the section beginning slot holds 7 data octets and 1 non-data octet. The non-data octet of the section-beginning slot is used to identify which of the section beginning slots that holds the J1 octet of the transported VC-3. The section is thus synchronous to the transported VC-3.

7.2.1 Section beginning

The section beginning slots have 1 non-data octet (bit 63 down to 56). One octet is used for identifying the initial segment. The initial segment is encoded as the bit-string 01010101 (bit 63 down to bit 56). The lower 7 bits (bit 62 down to bit 56) of the octet is those used to transport an alternating bit pattern such that majority decisions can be performed. Thus, if 4 or more bits indicate initial segment, then the initial segment pattern is detected, else it is not detected. The highest bit (bit 63) of the initial segment identifier octet is reserved. It shall be set to 0 by the transmitter and shall not be interpreted by the receiver.

In total 1 bit is reserved and should not be interpreted. The checksum shall however be calculated regardless of the use, i.e. no special measures are required to hide the reserved bits from the checksum calculation.

The 7 data octets (bit 55 down to 0) hold data octets from the VC-3 datastream. If the section beginning is the initial section beginning, the J1 octet of the POH header shall be found in bit 55 down to bit 48 and bit 47 down to bit 0 shall hold the 6 octets immediately after J1 according to normal SDH multiplexing rules (EN 300 417-4-1 [3]).

A frame synchronization state machine continuously monitors the initial segment frame pattern. The state machine has two states, In Frame (IF) and Out Of Frame (OOF). If the state machine is in the OOF state and detects the frame pattern in two sections, being one frame apart (i.e. X sections) then the state machine shall enter the In Frame state. If the state machine is in the IF state and has failed to detect the frame pattern in the expected segment for a total of 5 frames, the state machine shall enter the Out Of Frame state.

7.2.2 Section data

In a section data slot bit 63 down to bit 0 shall hold the next 8 octets of the VC-3 octet stream, beginning with the first octet mapped into bit 63 down to bit 56, and then octet per octet until bit 7 down to 0 have been mapped.

7.3 VC-3 mapping

The VC-3 will be converted into 1 section, each holding 783 octets. The first section for each VC-3 frame will start on the J1 octet (column 1), followed by the octets in normal SDH multiplex order. The section containing the J1 will be marked with a frame marker.

8 Mapping of SDH VC-2 over DTM

The SDH VC-2 (EN 300 417-4-1 [3]) is mapped onto the DTM DCAP-0 ES 201 803-2-3 [6] format, providing means to transport the VC-2 data, VC-2 super-frame alignment, SSF and providing performance supervision. Each VC2 super-frame (500 us) contains 428 octets with 107 octets of data per frame, including the POH header. See table 13 for VC-2 mapping characteristics.

8.1 DCAP-0 slot elements

The DCAP-0 elements of 64 bit data slot, Idle-marker, Performance Supervision-marker, AIS-marker are described in ES 201 803-2-3 [6]. The POH-header and payload are transported in one section holding a complete VC-2 super-frame.

Each section is prefixed by a PS-marker, holding the channel end-to-end performance supervision, and also acting as a section delimiter. The justification is performed by prefixing 2, 1 or 0 Idle markers before the section and its PS-marker, thus giving one justification point on each VC-2 super-frame.

NOTE: The PS-marker of the first section shall include the correct idle marker count of the frequency justification opportunity that just occurred. This is a direct consequence of the DCAP-0 definitions. Similarly, PS-markers for other sections should have zero as their idle marker count values.

8.2 Data slot mapping

The 428 octets of each section are divided into one section beginning slot and 53 section data slots. The section data slot holds 8 octets of data while the section beginning slot holds 4 data octets, 3 reserved octets and 1 non-data octet. The non-data octet of the section-beginning slot is used to identify which of the section beginning slots that holds the V5 octet of the transported VC-2. The section is thus synchronous to the transported VC-2.

8.2.1 Section beginning

The section beginning slots have 1 non-data octet (bit 63 down to 56). One octet is used for identifying the initial segment. The initial segment is encoded as the bit-string 01010101 (bit 63 down to bit 56). The lower 7 bits (bit 62 down to bit 56) of the octet is those used to transport an alternating bit pattern such that majority decisions can be performed. Thus, if 4 or more bits indicate initial segment, then the initial segment pattern is detected, else it is not detected. The highest bit (bit 63) of the initial segment identifier octet is reserved. It shall be set to 0 by the transmitter and shall not be interpreted by the receiver. The three reserved octets shall have all their bits set to 0 by the transmitter and shall not be interpreted by the receiver.

In total 25 bits are reserved and should not be interpreted. The checksum shall however be calculated regardless of the use, i.e. no special measures are required to hide the reserved bits from the checksum calculation.

The 4 data octets (bit 31 down to 0) hold data octets from the VC-2 datastream. If the section beginning is the initial section beginning, the V5 octet of the POH header shall be found in bit 31 down to bit 24 and bit 23 down to bit 0 shall hold the 3 octets immediately after V5 according to normal SDH multiplexing rules (EN 300 417-4-1 [3]).

A frame synchronization state machine continuously monitors the initial segment frame pattern. The state machine has two states, In Frame (IF) and Out Of Frame (OOF). If the state machine is in the OOF state and detects the frame pattern in two sections, being one super-frame apart (i.e. X sections) then the state machine shall enter the In Frame state. If the state machine is in the IF state and has failed to detect the frame pattern in the expected segment for a total of 5 super-frames, the state machine shall enter the Out Of Frame state.

8.2.2 Section data

In a section data slot bit 63 down to bit 0 shall hold the next 8 octets of the VC-2 octet stream, beginning with the first octet mapped into bit 63 down to bit 56, and then octet per octet until bit 7 down to 0 have been mapped.

8.3 VC-2 mapping

The VC-2 will be converted into 1 section, holding 428 octets. The first section for VC-2 super-frame will start on the V5 octet, followed by the octets in normal SDH multiplex order. The section containing the V5 will be marked with a frame marker.

9 Mapping of SDH VC-12 over DTM

The SDH VC-12 (EN 300 417-4-1 [3]) is mapped onto the DTM DCAP-0 ES 201 803-2-3 [6] format, providing means to transport the VC-12 data, VC-12 super-frame alignment, SSF and providing performance supervision. Each VC12 super-frame (500 us) contains 140 octets with 35 octets of data per frame, including the POH header. See table 13 for VC-12 mapping characteristics.

9.1 DCAP-0 slot elements

The DCAP-0 elements of 64 bit data slot, Idle-marker, Performance Supervision-marker, AIS-marker are described in ES 201 803-2-3 [6]. The POH-header and payload are transported in one section holding a complete VC-12 super-frame.

Each section is prefixed by a PS-marker, holding the channel end-to-end performance supervision, and also acting as a section delimiter. The justification is performed by prefixing 2, 1 or 0 Idle markers before the section and its PS-marker, thus giving one justification point on each VC-12 super-frame.

NOTE: The PS-marker of the first section shall include the correct idle marker count of the frequency justification opportunity that just occurred. This is a direct consequence of the DCAP-0 definitions. Similarly, PS-markers for other sections should have zero as their idle marker count values.

9.2 Data slot mapping

The 140 octets of each section are divided into one section beginning slot and 17 section data slots. The section data slot holds 8 octets of data while the section beginning slot holds 4 data octets, 3 reserved octets and 1 non-data octet. The non-data octet of the section-beginning slot is used to identify which of the section beginning slots that holds the V5 octet of the transported VC-12. The section is thus synchronous to the transported VC-12.

9.2.1 Section beginning

The section beginning slots have 1 non-data octet (bit 63 down to 56). One octet is used for identifying the initial segment. The initial segment is encoded as the bit-string 01010101 (bit 63 down to bit 56). The lower 7 bits (bit 62 down to bit 56) of the octet is those used to transport an alternating bit pattern such that majority decisions can be performed. Thus, if 4 or more bits indicate initial segment, then the initial segment pattern is detected, else it is not detected. The highest bit (bit 63) of the initial segment identifier octet is reserved. It shall be set to 0 by the transmitter and shall not be interpreted by the receiver. The three reserved octets shall have all their bits set to 0 by the transmitter and shall not be interpreted by the receiver.

In total 25 bits are reserved and should not be interpreted. The checksum shall however be calculated regardless of the use, i.e. no special measures are required to hide the reserved bits from the checksum calculation.

The 4 data octets (bit 31 down to 0) hold data octets from the VC-12 datastream. If the section beginning is the initial section beginning, the V5 octet of the POH header shall be found in bit 31 down to bit 24 and bit 23 down to bit 0 shall hold the 3 octets immediately after V5 according to normal SDH multiplexing rules (EN 300 417-4-1 [3]).

A frame synchronization state machine continuously monitors the initial segment frame pattern. The state machine has two states, In Frame (IF) and Out Of Frame (OOF). If the state machine is in the OOF state and detects the frame pattern in two sections, being one super-frame apart (i.e. X sections) then the state machine shall enter the In Frame state. If the state machine is in the IF state and has failed to detect the frame pattern in the expected segment for a total of 5 super-frames, the state machine shall enter the Out Of Frame state.

9.2.2 Section data

In a section data slot bit 63 down to bit 0 shall hold the next 8 octets of the VC-12 octet stream, beginning with the first octet mapped into bit 63 down to bit 56, and then octet per octet until bit 7 down to 0 have been mapped.

9.3 VC-12 mapping

The VC-12 will be converted into 1 section, holding 140 octets. The first section for VC-12 super-frame will start on the V5 octet, followed by the octets in normal SDH multiplex order. The section containing the V5 will be marked with a frame marker.

10 Mapping of SDH VC-11 over DTM

The SDH VC-11 (EN 300 417-4-1 [3]) is mapped onto the DTM DCAP-0 ES 201 803-2-3 [6] format, providing means to transport the VC-11 data, VC-11 super-frame alignment, SSF and providing performance supervision. Each VC11 super-frame (500 us) contains 104 octets with 26 octets of data per frame, including the POH header. See table 13 for VC-11 mapping characteristics.

10.1 DCAP-0 slot elements

The DCAP-0 elements of 64 bit data slot, Idle-marker, Performance Supervision-marker, AIS-marker are described in ES 201 803-2-3 [6]. The POH-header and payload are transported in one section holding a complete VC-11 super-frame.

Each section is prefixed by a PS-marker, holding the channel end-to-end performance supervision, and also acting as a section delimiter. The justification is performed by prefixing 2, 1 or 0 Idle markers before the section and its PS-marker, thus giving one justification point on each VC-11 super-frame.

NOTE: The PS-marker of the first section shall include the correct idle marker count of the frequency justification opportunity that just occurred. This is a direct consequence of the DCAP-0 definitions. Similarly, PS-markers for other sections should have zero as their idle marker count values.

10.2 Data slot mapping

The 104 octets of each section are divided into one section beginning slot and 13 section data slots. The section data slot holds 8 octets of data while the section beginning slot holds 0 data octets, 7 reserved octets and 1 non-data octet. The non-data octet of the section-beginning slot is used to identify which of the section beginning slots that holds the V5 octet of the transported VC-11. The section is thus synchronous to the transported VC-11.

10.2.1 Section beginning

The section beginning slots have 1 non-data octet (bit 63 down to 56). One octet is used for identifying the initial segment. The initial segment is encoded as the bit-string 01010101 (bit 63 down to bit 56). The lower 7 bits (bit 62 down to bit 56) of the octet is those used to transport an alternating bit pattern such that majority decisions can be performed. Thus, if 4 or more bits indicate initial segment, then the initial segment pattern is detected, else it is not detected. The highest bit (bit 63) of the initial segment identifier octet is reserved. It shall be set to 0 by the transmitter and shall not be interpreted by the receiver. The seven reserved octets shall have all their bits set to 0 by the transmitter and shall not be interpreted by the receiver.

In total 57 bits are reserved and should not be interpreted. The checksum shall however be calculated regardless of the use, i.e. no special measures are required to hide the reserved bits from the checksum calculation.

If the section beginning is the initial section beginning, the V5 octet of the POH header shall be found in bit 63 down to bit 56 in the following data slot and bit 55 down to bit 0 shall hold the 7 octets immediately after V5 according to normal SDH multiplexing rules (EN 300 417-4-1 [3]).

A frame synchronization state machine continuously monitors the initial segment frame pattern. The state machine has two states, In Frame (IF) and Out Of Frame (OOF). If the state machine is in the OOF state and detects the frame pattern in two sections, being one super-frame apart (i.e. X sections) then the state machine shall enter the In Frame state. If the state machine is in the IF state and has failed to detect the frame pattern in the expected segment for a total of 5 super-frames, the state machine shall enter the Out Of Frame state.

10.2.2 Section data

In a section data slot bit 63 down to bit 0 shall hold the next 8 octets of the VC-11 octet stream, beginning with the first octet mapped into bit 63 down to bit 56, and then octet per octet until bit 7 down to 0 have been mapped.

10.3 VC-11 mapping

The VC-11 will be converted into 1 section, holding 104 octets. The first section for VC-11 super-frame will start on the V5 octet, followed by the octets in normal SDH multiplex order. The section containing the V5 will be marked with a frame marker.

11 Grouped mapping of virtual containers

The grouped mapping allows a multiple of a virtual container (VC-11, VC-12, VC-2, VC-3 or VC-4) to be mapped into the same channel. For concatenated virtual containers it is convenient to group all the concatenated virtual containers into the same channel. It is not possible to group different types of virtual containers into the same channel.

NOTE: In order to group virtual containers of different types, the use of the generic Tunnel service (as described in ES 201 803-2-3 [6] clause 10) is recommended.

11.1 Grouped mapping

The grouped mapping is achieved through the use of the time slot layer tunnel switching ES 201 803-2-3 [6] (i.e. the TST trail termination and TST/TS adaptation function). For the mapping of a VC-n the number of slots required is N as specified in table 13. For the transport of X grouped VC-n virtual containers is X*N slot required. These slots are divided into continuous groups of X slots, each group is assigned a group number ranging from 0 to N-1. Slot 0 of the channel is assigned to be slot 0 of group 0. The slots of a group are assigned as linear and monotonic increase from the first slot of that group (slot 0). The first free slot in the channel after a complete group is assigned to the first slot of the next group. An example for 5 grouped VC-11 is found in table 14.

Table 14: Example of 5 VC-11 in a grouped mapping

Channel slot	Group	Group slot
0	0	0
1	0	1
2	0	2
3	0	3
4	1	0
5	1	1
6	1	2
7	1	3
8	2	0
9	2	1
10	2	2
11	2	3
12	3	0
13	3	1
14	3	2
15	3	3
16	4	0
17	4	1
18	4	2
19	4	3

The grouped mapping thus creates a virtual time division multiplex structure where the virtual slots as N slots wide. Any request or change of capacity must be a multiple of N for the type of VC-n specified for the channel. See clause 12 for details.

This mapping can be described by an equation giving the channel slot number Sc (0 to X×N-1) from the group number G (0 to X-1) and the basic mapping slot number Sb (0 to N-1). N is the number of slots per basic mapping.

$$Sc = G \times N + Sb$$

11.2 Separate or common phase

The virtual containers grouped into a single channel may be either having separate or common phase. Virtual containers having separate phase is individually phase and frequency adjusted. Virtual containers having common phase is phase aligned such that their section beginning occurs in the same frame and group slot.

NOTE 1: For VC-3 and VC-4 there is no super-frame spanning over multiple DTM frames, so the section beginning occurs in every DTM frame. This effectively reduces the requirement to only require the same group slot.

NOTE 2: For VC-11, VC-12 and VC-2 there is a super-frame spanning over multiple DTM frames, so for the section beginnings to be phase aligned they must appear in the same DTM frame and then within that DTM frame they also need to have the section beginning in the same group slot for all the grouped virtual containers.

The separate phase grouped virtual containers can carry individual channels as well as virtual concatenated virtual containers (i.e. VC-n-Xv).

The common phase grouped virtual containers can carry virtual concatenated virtual containers (i.e. VC-n-Xv) which is phase aligned and linearly concatenated virtual containers (i.e. VC-n-Xl).

NOTE 3: The linearly concatenated virtual containers are a variant of the virtual containers essentially being a mixture of contiguous concatenated and virtually concatenated virtual containers. The concatenation operates according to virtual concatenation rules, but with the exception that all the virtual containers is phase aligned to the first virtual container, much like in contiguous concatenation.

12 Channel creation information

When creating the channel, additional information may be sent along the channel setup signalling to further detail the channel characteristics to the receiving application. The additional information required to be sent for the SDH over DTM mapping during channel creation is the type of mapping, i.e. the type of virtual container and wither it is ungrouped or grouped. Further, if the channel is a grouped variant of the virtual container specified, it is required to specify wither it is separate or common phase.

For the SDH over DTM application, two octets are transmitted as the channel creation information. The first octet specifies the virtual container base type as specified in table 15.

Table 15: Virtual Container base type

Base type	Virtual Container	Allowed Mapping types
0	VC-11	0,1,2
1	VC-12	0,1,2
2	VC-2	0,1,2
3	VC-3	0,1,2
4	VC-4	0,1,2
5	VC-4-4c	0
6	VC-4-16c	0
7	VC-4-64c	0
8	VC-4-256c	0
9 to 255	reserved	N.A.

The second octet specifies the ungrouped/grouped type as specified in table 16.

Table 16: Mapping type

Mapping type	Meaning
0	Ungrouped (single VC-n)
1	Grouped - separate phase
2	Grouped - common phase
3 to 255	Reserved

There is no grouped mapping for VC-4-Xc defined, so only the ungrouped mapping type is allowed as defined in table 15.

NOTE: The hierarchical grouping is deemed unnecessary. Either use virtual or linear concatenation of grouped mapped VC-4 or use contiguous concatenation of VC-4-Xc.

The value of X for grouped VC-n is encoded in the number of slots the channel required. For grouped VC-n, where the slot number is defined to be an even integer X, X is found by dividing the channel capacity (in slots) with the number of slots N as indicated by the virtual container base type and table 13 for that virtual container. Any X not being an integer is an error and channel establishment or change of capacity shall be refused.

12.1 Historical encoding of channel characteristics

Older non-grouping implementations of SDH over DTM do not transmit the channel creation information. They use the number of slots for the channel to distinguish between the VC-n and VC-4-Xc cases as being defined in table 13. Such encoding of ungrouped VC-n and VC-4-Xc is depreciated, but should be tolerated by new implementations for the case where no channel creation information is attached to the channel creation message.

Future revisions of the SDH over DTM mapping does not guarantee that virtual channels be distinct by number of slots, in which case tolerance for this case is no longer possible due to the ambiguity. Then must all applications transmit the correct channel creation information and none should tolerate the old mapping.

Annex A (informative): Recommendation on Mapping of PDH over DTM

The SDH virtual containers VC-11, VC-12, VC-2, VC-3 and VC-4 support the transport of P11x (1 544 kb/s), P12x (2 048 kb/s), P21 (6 312 kb/s), P22 (8 448 kb/s), P31 (34 368 kb/s), P32 (44 736 kb/s) and P4 (139 264 kb/s) PDH signals. These PDH signals can be mapped onto the SDH virtual containers prior to these virtual containers being mapped onto DTM channels. There exists a PDH mapping onto DTM for all these speeds, using the 1 UI adjustment capable DCAP-2. The 64 UI adjustments for VC-n are intended for efficient mapping of data and not for overlay PDH signals. Thus, it is recommended that the PDH signals be mapped according to the PDH over DTM mapping rather than indirectly through the VC-n.

NOTE: While the preference is to use the direct PDH over DTM mapping, VC-n indirect mapping is possible given that care in frequency justification in relation to jitter and wander requirements is taken. However, such mapping is not guaranteed to be supported by other implementations of PDH over DTM mappings.

History

Document history		
V1.1.1	November 2003	Publication
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