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Dynamic synchronous Transfer Mode (DTM);
Part 3: Physical protocol

Reference

DES/TM-01089

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Contents

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Foreword

This ETSI Standard (ES) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

The present document is part 3 of a multi-part deliverable covering Dynamic synchronous Transfer Mode (DTM), as identified below:

Part 1: "System description";

Part 2: "System characteristics";

Part 3: "Physical protocol";

Part 4: "Mapping of DTM frames into SDH containers";

Part 5: "Mapping of PDH over DTM";

Part 6: "Mapping of SDH over DTM";

Part 7: "Ethernet over DTM Mapping";

Part 8: "Mapping of Frame relay over DTM";

Part 9: "Mapping of ATM over DTM";

Part 10: "Routeing and switching of IP flows over DTM";

Part 11: "Mapping of video streams over DTM";

Part 12: "Mapping of MPLS over DTM";

Part 13: "System description of sub-rate DTM";

Part 14: "Network management".

Introduction

Dynamic synchronous Transfer Mode (DTM) is a time division multiplex and a circuit-switched network technology that combines switching and transmission.

Part 1 describes the general properties of DTM and the DTM service over a unidirectional data channel. The overall system architecture is described and fundamental functions are identified.

Part 2 includes system aspects that are mandatory or optional for nodes from different vendors to interoperate. The interworking granularity should be at node level, such that nodes from different vendors can interoperate with regard to well-defined functions.

The present document (Part 3) specifies the physical layer for physical links based on 8B10B encoding.

Part 4 describes how DTM frames are mapped into SDH containers.

The transport of various tributary signals is specified for PDH (Part 5), SDH (Part 6), Ethernet (Part 7), Frame Relay (Part 8), ATM (Part 9), IP (Part 10), MPLS (Part 11) and video streaming (Part 12).

Part 13 describes sub-rate DTM.

Part 14 describes management aspects.

1 Scope

The present document:

- establishes a system for mapping DTM frames on 8B10B coding using a sublayer stack;
- specifies the characteristics of critical parameters for an 8B10B based physical interface;
- gives guidelines for the dependence on the IEEE 802.3 Gigabit Ethernet standard;
- gives terms and definitions for message encoding;
- gives terms and definitions for the frame format;
- gives terms and definitions for the sync transport;
- gives terms and definitions for the sync and physical link status.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication and/or edition number or version number) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

Referenced documents which are not found to be publicly available in the expected location might be found at http://docbox.etsi.org/Reference.

[1] ETSI TR 101 287: "Services and Protocols for Advanced Networks (SPAN); Terms and definitions".

[2] IEEE 802.3: "IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications".

[3] ITU-T Recommendation G.805: "General functional architecture of transport networks".

[4] ITU-T Recommendation G.806: "Characteristics of Transport Equipment - Description Methodology and Generic Functionality".

[5] ANSI X3.230-1994: "Information Technology - Fibre Channel - Physical and Signalling Interface (FC-PH)".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

8B10B code: line code format using 10 binary symbols to encode 8 bit data or 12 control codes

Access Point (AP): "reference point" that consists of the pair of co-located "unidirectional access" points, and therefore represents the binding between the trail termination and adaptation functions (adopted from ITU-T Recommendation G.805)

Adapted Information (AI): information passing across an AP (see also ITU-T Recommendation G.805), (adopted from ITU-T Recommendation G.806)

Alarm Indication Signal (AIS): special marker sent in a data slot to mark the lack of transported data as a result of a defect in the transmission path

Channel: set of slots allocated from one source access node to one or more destination access nodes in a network

Characteristic Information (CI): Signal with a specific format, which is transferred on "network connections". The specific formats will be defined in the technology specific Recommendations. The characteristic information is the information passing across a CP or TCP (adopted from ITU-T Recommendations G.805 and G.806).

Connection Point (CP): reference point where the output of a trail termination source or a connection is bound to the input of another connection, or where the output of a connection is bound to the input of a trail termination sink or another connection (adopted from ITU-T Recommendation G.806)

code group: single 8B10B entity taking 10 bits of transmission symbols, encoded in one of two disparities and taking on any of 256 data values or 12 special codes

comma character: 7 transmission symbols long sequence, existing in 8B10B code groups, acting as synchronization pattern for the 10-symbol boundary alignment in the PMA

Comma Detect (COM_DET): signal which when asserted indicates the detection of a comma character in the received stream and that the serial to parallel converter has been realigned to a new 10-symbol boundary

data ordered set: data ordered set containing 64 transported data bits

data slot: time slot in the TDM frame used for channel data or channel special code-groups (i.e. one of the Idle, PS or AIS ordered sets)

defect: The density of anomalies has reached a level where the ability to perform a required function has been interrupted. Defects are used as input for performance monitoring, the control of consequent actions, and the determination of fault cause (adopted from ITU-T Recommendation G.806).

disparity: The accumulated DC offset as a result of sent coding being used to select codes to avoid DC drift of line code. Residue disparity after an 8B10B code can take two values (+1 or –1).

Enable Comma Detect (EN_CDET): signal which when asserted enables the comma detect alignment in the PMA sublayer

fill: special ordered set sent in the interframe gap in order to mark the explicit end of frame as well as to provide a distinctly different ordered set to that of the SOF ordered set

frame: set of slots forming an entity that is transmitted on a physical medium repeatedly every 125 μs (nominally), i.e. 8 000 frames/second (in-between each frame is the gap transmitted)

Frame Error (FE): signal that is asserted when the SOF ordered set does not occur at a slot count, from the previous valid SOF ordered set, lower or equal to the fe_{high}

Frame Synchronization State Machine: state machine that monitors and determines the state of frame synchronization

gap: time period of variable length in-between the end of one frame and the beginning of the following frame (the gap is filled with fill ordered sets)

idle: special marker sent in a data slot to mark the lack of transported data in the slot

Loss Of Frame defect (dLOF): signal which when asserted indicates that there is no frame boundary synchronization, it is de-asserted when frame boundary synchronization is attained

Loss Of Slot Synchronization anomaly (nLOSS): signal which when asserted indicates that there is no slot boundary synchronization, it is de-asserted when slot boundary synchronization is attained

Management Information (MI): signal passing across an access point (adopted from ITU-T Recommendation G.806)

Management Point (MP): Reference point where the output of an atomic function is bound to the input of the element management function, or where the output of the element management function is bound to the input of an atomic function. The MP is not the TMN Q3 interface (adopted from ITU-T Recommendation G.806).

medium: transmission path along which a signal propagates, such as a wire pair, coaxial cable, waveguide, optical fibre or radio path

ordered set: grouping of 4 or 8 code groups

Ordered Set Fail anomaly (nOSF): signal updated for each received slot, it is asserted if the decoding of received symbols for the slot forms an illegal combination

Physical Coding Sublayer (PCS): upper sublayer of the physical layer responsible for mapping of ordered sets, line coding, line decoding and receiver state machines

physical link: unidirectional connection between the transmitter of one physical interface and the receiver of another physical interface

Physical Media Attachment (PMA): middle sublayer of the physical layer responsible for clock recovery, 10 symbol alignment, serial-parallel and parallel-serial conversion

Physical Media Dependent (PMD): lower sublayer of the physical layer responsible for conversion to and from the transport medium and related signal conditioning

Performance Supervision (PS): special marker sent with the data containing per channel performance supervision information

Server Signal Fail (SSF): signal fail indication output at the CP of an adaptation function (adopted from ITU-T Recommendation G.806)

Signal Fail (SF): A signal indicating the associated data has failed in the sense that a near-end defect condition (not being the degraded defect) is asserted (adopted from ITU-T Recommendation G.806).

slot: time slot within a frame, capable of transporting 64 bit of data or a number of special codes

NOTE: A slot contains 8 code groups.

Slot Synchronization State Machine: state machine that monitors and judges the state of slot boundary synchronization

Start Of Frame (SOF): ordered set that marks the end of the gap and beginning of the frame

symbol: transmission modulation unit over the underlying transmission medium

Trail Signal Fail (TSF): signal fail indication output at the AP of a termination function (adopted from ITU-T Recommendation G.806)

transmission cycle: full frame to frame cycle, it contains a frame and an interframe gap

Unit Interval (UI): Nominal difference in time between consecutive significant instants of a signal. One unit interval is one cycle time of the clock signal (adopted from TR 101 287).

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

A	Adapted function
AGC	Automatic Gain Control
AI	Adapted Information
AIS	Alarm Indication Signal
AM	Administrative Mode
AP	Access Point
aSSF	Server Signal Fail action
aTSF	Trail Signal Fail action
BPn	ByPass layer type n
BPnP	ByPass layer type n Protection
CGn	Code Groupe type n
CH	CHannel layer
CHP	CHannel layer Protection
CI	Characteristic Information
CK	ClocK
CP	Connection Point
D	Data
DC	Direct Current
dLOF	Loss Of Frame defect
dLOS	Loss Of Signal defect
EN	ENable
FE	Frame Error
FS	Frame Start signal
LOF	Loss of Frame
LOSS	Loss Of Slot Synchronization
MP	Management Point
NACT	Not ACTive
PCS	Physical Coding Sublayer
PL	Physical Link layer
PLn	Physical Link layer type n
PM	Port Mode
PS	Performance Supervision
RD	Running Disparity
Sk	Sink
Sn	SDH higher order VC-n layer (n = 3,4,4-Xc)
So	Source
SOF	Start Of Frame
SSF	Server Signal Fail
TS	Time Slot layer
TSF	Trail Signal Fail
TSP	Time Slot layer Protection
TST	Time Slot layer Tunnel
UI	Unit Interval

4 Overview

DTM is a TDM (Time Division Multiplex) and a circuit-switched network technology that combines switching and transport. The present document describes a DTM physical interface using 8B10B encoded physical links of the line rates 1,0 Gbps (Gigabit Ethernet rate).

The DTM Physical Link layer type 1 and Media layer type 1 (see figure 1) are based on the Gigabit Ethernet [2] interface.

The Media layer type 1 contains the Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) parts of the Gigabit Ethernet standard. The PMD is modelled into the Media layer type 1 Trail Termination (M1_TT) while the PMA is modelled into the Media layer type 1 to Physical Link layer type 1 Adaptation function (M1/PL1_A).

The PMA-10 interface of Gigabit Ethernet is thus available in the Physical Link layer type 1 Connection Point (PL1_CP).

The Physical Coding Sublayer (PCS) is divided into the Physical Link layer type 1 Trail Termination (PL1_TT) and the Physical Link layer type 1 to Bypass layer type 1 Adaptation function (PL1/BP1_A). The 8B10B-encoding/decoding process is modelled into the PL1_TT while the slot adaptation (encoding and decoding of ordered sets) is in PL1/BP1_A.

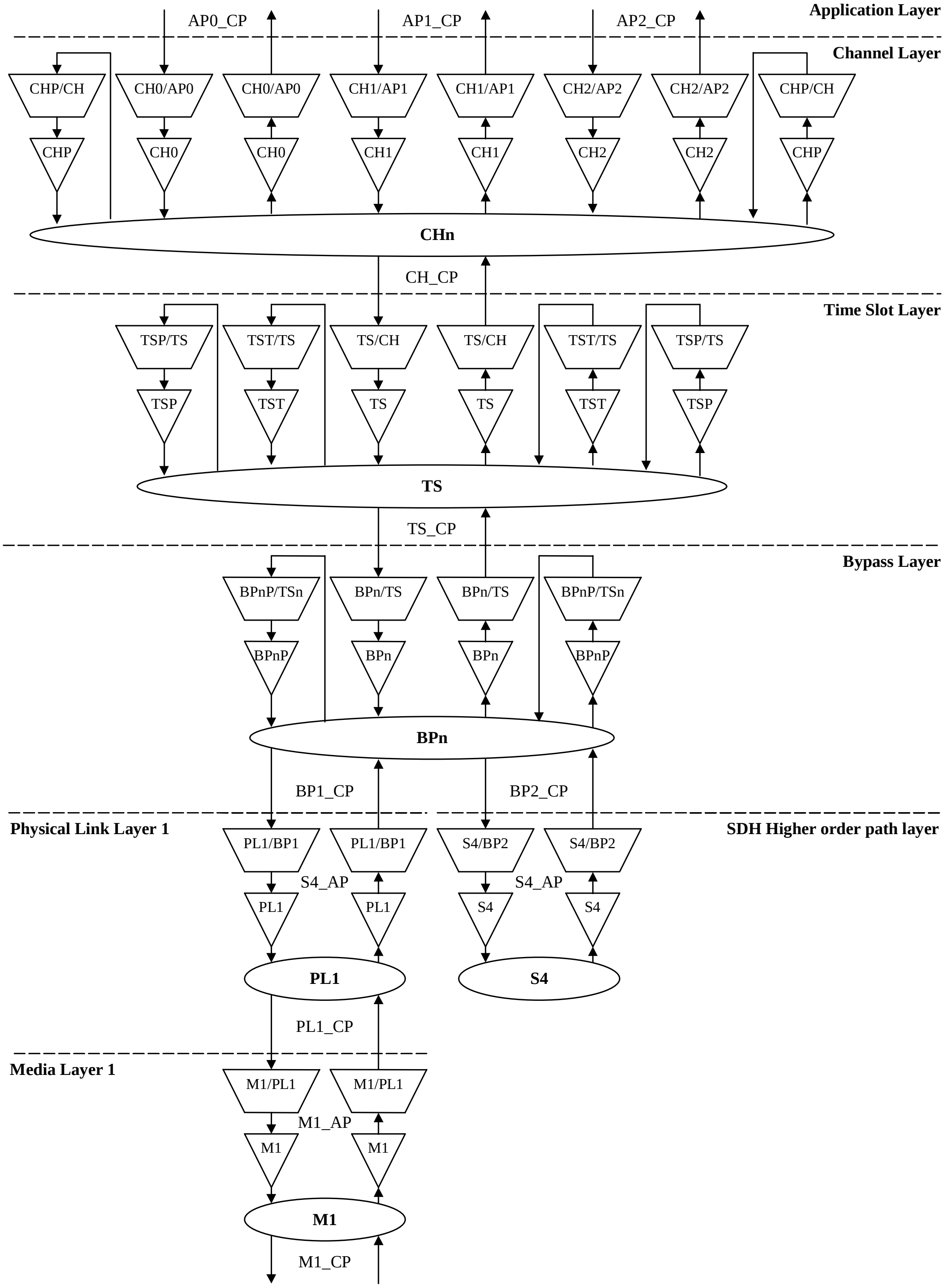

Figure 1: Transport Network Reference Model for DTM

5 Media layer type 1

The DTM Media layer type 1 (M1) (see figure 2) will provide the optical physical interface used for the 8B10B encoded code groups of the DTM Physical layer type 1 (PL1). The bit clock transfer and recovery is provided. Code group alignment is performed.

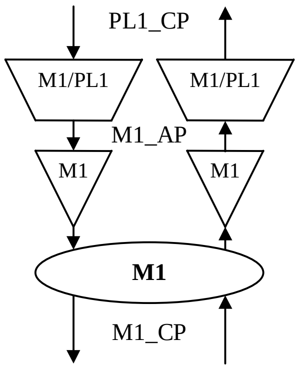

Figure 2: DTM Media layer type 1 atomic functions

The Characteristic Information (M1_CI) at the M1_CP is a digital optically coded signal of defined power, symbol rate, pulse width and wavelength. A range of such characteristic information is defined in clause 7.

The Adapted Information (M1_AI) at the M1_AP is a digital signal of defined symbol rate as defined in clause 7.

5.1 Connection function

Not applicable. There are no connection functions defined for this layer.

5.2 Termination functions

5.2.1 Media layer type 1 Trail Termination Source M1_TT_So

Symbol

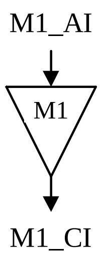

Figure 3: DTM Media Trail Termination Source

Interfaces

Table 1: M1_TT_So Input and output signals

Input(s)	Output(s)
M1_AI_D	M1_CI_D

Processes

The termination function conditions the data at M1_AP for transmission over the optical medium and presents it at the M1_CP.

Optical characteristics: The function shall generate optical signals that meet the characteristics as defined by the Physical Medium Dependent sublayer as found in clause 7.

Defects

None

Consequent actions

None

Defect correlation

None

Performance monitoring

None

5.2.2 Media layer type 1 Trail Termination Sink M1_TT_Sk

Symbol

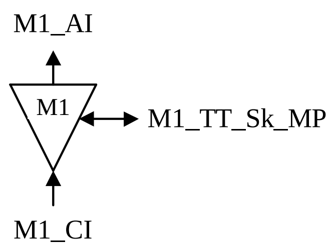

Figure 4: DTM Media Trail Termination Sink

Interfaces

Table 2: M1_TT_Sk Input and output signals

Input(s)	Output(s)
M1_CI_D	M1_AI_D
M1_TT_Sk_MP_PM	M1_AI_TSF
	M1_TT_Sk_MI_cLOS

Processes

The termination function conditions and formats the signal from the M1_CP and deliver a digital signal to the M1_AP.

The optical level is being monitored by the Automatic Gain Control (AGC) of the signal conditioning subsystem. The signal level is monitored and when the level goes below the threshold (as specified in [2], clauses 38 and 39) the Loss Of Signal defect (dLOS) is activated.

Optical characteristics: The function shall detect optical signals that meet the characteristics as in clause 7.

The operation of Port Mode is described in [4], clause 6.1.

Defects

dLOS: The Loss Of Signal defect (dLOS) is detected according to clause 7.

Consequent actions

The Trail Signal Fail action (aTSF) is asserted when the Loss Of Signal defect (dLOS) is asserted.

aTSF ← dLOS

Defect correlation

The Loss Of Signal cause (cLOS) is asserted when the Loss Of Signal defect (dLOS) is asserted and the Monitoring (MON) is asserted.

cLOS ← dLOS and MON

Performance monitoring

None.

5.3 Adaptation function

5.3.1 Media layer type 1 to Physical layer type 1 Adaptation Source M1/PL1_A_So

Symbols

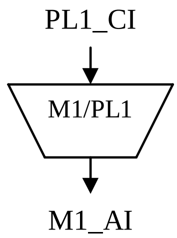

Figure 5: DTM Media Adaptation function Source

Interfaces

Table 3: M1/PL1_A_So Input and output signals

Input(s)	Output(s)
PL1_CI_D	M1_AI_D
PL1_CI_CK	

Processes

This function limits the output jitter on PL1_CI_CK to less than 0,1 UI as specified in clause 8 while increasing the frequency into the symbol rate of M1_AI_D.

The data at PL1_CI_D is being serialised into M1_AI_D according to clause 8.

Defects

None.

Consequent actions

None.

Defect correlation

None.

Performance monitoring

None.

5.3.2 Media layer type 1 to Physical layer type 1 Adaptation Sink M1/PL1_A_Sk

Symbols

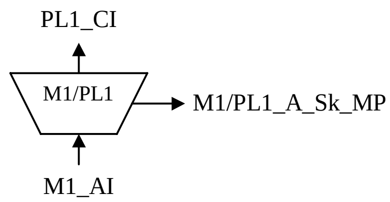

Figure 6: DTM Media Adaptation function Sink

Interfaces

Table 4: M1/PL1_A_Sk Input and output signals

Input(s)	Output(s)
M1_AI_D	PL1_CI_D
M1_AI_TSF	PL1_CI_CK
PL1_CI_EN_FS	PL1_CI_FS
	PL1_CI_SSF
	M1/PL1_A_Sk_MP_cLOF

Processes

The bit clock is being reconstructed from the incoming data stream. This process has the characteristics as specified in clause 8.

The bit alignment is found by the search of the comma sequence (1111100). The alignment synchronization is enabled by the CI_EN_FS and when enabled will the CI_FS be asserted for each detected comma sequence. The alignment process, EN_FS and FS are being defined in clause 9.6.1.

The M1_AI_D is serial to parallel converted into the ten bits format of PL1_CI_D. The characteristic of the parallel interface is defined in clause 8.

Defects

None.

Consequent actions

The Server Signal Fail action (aSSF) is asserted when the Trail Signal Fail (AI_TSF) is asserted.

aSSF ← AI_TSF

Defect correlation

None.

Performance monitoring

None.

5.4 Sublayer functions

There are no sublayer functions applicable to this layer.

6 Physical Link layer type 1

The DTM Physical Link layer type 1 (see figure 7) will provide the transport of DTM Bypass layer type 1 frames using 8B10B encoding similar to that of Fibre Channel [5] and Gigabit Ethernet [2]. It will encode the frame and slots into 8B10B code groups, which are sent over the DTM Media layer type 1. The DTM synchronization signal is transported using the start of frame marker.

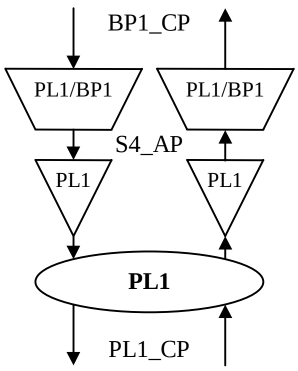

Figure 7: DTM Physical Link layer type1 atomic functions

The Characteristic Information (PL1_CI) at the PL1_CP contains a 10 bit code group signal in CI_D which is synchronous to the CI_CK. The characteristic information is defined in clause 9.

The Adapted Information (M1_AI) at the M1_AP contains a 8 + 1 bit code group signal in AI_D which is synchronous to the AI_CK. In the receiving end, the additional signals of PL1_AI_EN_FS and PL1_AI_FS are used for attaining code group alignment. The detailed description of these signals is defined in clause 9.

6.1 Connection function

Not applicable. There are no connection functions defined for this layer.

6.2 Termination function

6.2.1 Physical Link layer type 1 Trail Termination Source PL1_TT_So

Symbol

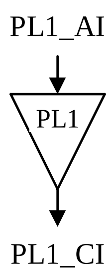

Figure 8: DTM Physical Link Trail Termination source

Interfaces

Table 5: PL1_TT_So Input and output signals

Input(s)	Output(s)
PL1_AI_D	PL1_CI_D
PL1_AI_CK	PL1_CI_CK

Processes

The 8B10B encoding is being performed according to clause 9.5.2.

Defects

None.

Consequent actions

None.

Defect correlation

None.

Performance monitoring

None.

6.2.2 Physical Link layer type 1 Trail Termination Sink PL1_TT_Sk

Symbol

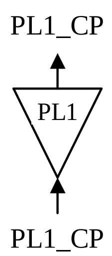

Figure 9: DTM Physical Link Trail Termination sink

Interfaces

Table 6: PL1_TT_Sk Input and output signals

Input(s)	Output(s)
PL1_CI_D	PL1_AI_D
PL1_CI_CK	PL1_AI_CK
PL1_CI_FS	PL1_AI_FS
PL1_CI_SSF	PL1_AI_CGF
PL1_AI_EN_FS	PL1_AI_TSF

Processes

The 8B10B decoding is being performed according to clause 9.5.2.

The detection of incorrect code groups is performed according to clause 9.4.4.

Anomalies

nCGF: Code Group Fail anomaly (nCGF) detection according to clause 9.4.4.

Defects

None.

Consequent actions

The Code Group Fail action (aCGF) is asserted when the Code Group Fail anomaly (nCGF) is asserted.

aCGF ← dCGF

The Trail Server Failure action (aTSF) is asserted when the Server Signal Fail (CI_SSF) is asserted.

aTSF ← CI_SSF

Defect correlation

None.

Performance monitoring

None.

6.3 Adaptation function

6.3.1 Physical Link layer type 1 to Bypass layer type 1 Adaptation Source PL1/BP1_A_So

Symbol

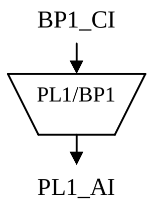

Figure 10: DTM Physical link Adaptation function source

Interfaces

Table 7: PL1/BP1_A_So Input and output signals

Input(s)	Output(s)
BP1_CI_D	PL1_AI_D
BP1_CI_CK	PL1_AI_CK
BP1_CI_FS	

Processes

The mapping of data, special ordered sets (Idle, PS and AIS), Fill generation and frame synchronization signal into code groups according to clause 9.5.

Defects

None.

Consequent actions

None.

Defect correlation

None.

Performance monitoring

None.

6.3.2 Physical Link layer type 1 to Bypass layer type 1 Adaptation Sink PL1/BP1_A_Sk

Symbol

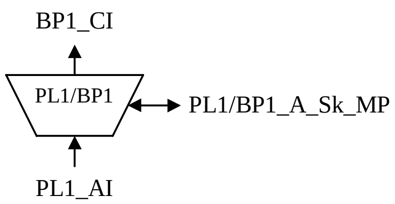

Figure 11: DTM Physical link Adaptation function sink

Interfaces

Table 8: PL1/BP1_A_Sk Input and output signals

Input(s)	Output(s)
PL1_AI_D	BP1_CI_D
PL1_AI_CK	BP1_CI_CK
PL1_AI_FS	BP1_CI_FS
PL1_AI_CGF	BP1_CI_SSF
PL1_AI_TSF	PL1_AI_EN_FS
PL1/BP1_A_Sk_MP_AM	PL1/BP1_A_Sk_MP_aTSF
PL1/BP1_A_Sk_MP_PM	PL1/BP1_A_Sk_MP_cOSF
PL1/BP1_A_Sk_MP_1second	PL1/BP1_A_Sk_MP_cLOF
	PL1/BP1_A_Sk_MP_pN_EBC
	PL1/BP1_A_Sk_MP_pN_LOF

Processes

The mapping of code groups into data, special ordered sets (Idle, PS and AIS) in BP1_CI_D format, frame synchronization detection signal (dFS) and Fill detection and removal (see clause 9.5). The Ordered Set Fail anomaly (nOSF) detection will detect code group arrangements which fail to result in valid ordered sets (see clause 9.5.2).

The frame error detection builds upon detecting the relative position of a received frame synchronization ordered set (dFS) and the previous frame synchronization ordered set (see clause 9.1).

The slot synchronization achieves and maintains synchronization to slot (see clause 9.6.2).

The frame synchronization state is being maintained and resulting in the loss of frame synchronization detection (see clause 9.6.3).

The AIS insertion into BP1_CI_D instead of received slots upon AIS defect (see [4], clause 6.3). The inserted AIS payload shall be according to ES 201 803-2-3 (see bibliography).

Anomalies

nOSF: The Ordered Set Fail anomaly (nOSF) detection according to clause 9.5.2, except for the nCGF.

nFE: The Frame Error anomaly (nFE) detection according to clause 9.1.

nFS: The Frame Start signal (nFS) detection according to clause 9.5.2.

nLOSS: The Loss Of Slot Synchronization anomaly (nLOSS) detection according to clause 9.6.2.

Defects

dLOF: The Loss Of Frame signal defect (dLOF) detection according to clause 9.6.3.

Consequent actions

The Server Signal Fail action (aSSF) is activated if the Trail Signal Fail (AI_TSF) or the Loss Of Frame signal defect (dLOF) is asserted.

aSSF ← dLOF or AI_TSF

The Enable 10-bit Frame Start action (aEN_FS) is asserted when the Loss of Frame signal defect (dLOF) is asserted.

aEN_FS ← dLOF

The Trail Signal Fail action (aTSF) is activated if the Trail Signal Fail (AI_TSF), the Loss Of Frame signal defect (dLOF) or Administrative Not Active (NACT) is asserted.

aTSF ← dLOF or AI_TSF or NACT

Defect correlation

The Ordered Set Fail cause (cOSF) is activated if Ordered Set Fail anomaly (nOSF) or Code Group Fail (AI_CGF) is asserted, the Trail Signal Fail (AI_TSF) is de-asserted and that Monitoring (MON) is asserted.

cOSF ← (nOSF or AI_CGF) and (not AI_TSF) and MON

The Loss Of Frame signal cause (cLOF) is activated if Loss Of Frame signal defect (dLOF) is asserted, the Trail Signal Fail (AI_TSF) is de-asserted and that Monitoring (MON) is asserted.

cLOF ← dLOF and (not AI_TSF) and MON

Performance monitoring

pN_EBC ← ∑ (nOSF or AI_CGF)

pN_LOF ← ∑ dLOF

6.4 Sublayer functions

There are no sublayer functions applicable to this layer.

7 Physical Medium Dependent (PMD) sublayer

The Physical Medium Dependent (PMD) sublayer is directly related to 1000BASE-X PMD sublayer (as described in [2], clauses 38 and 39).

8 Physical Medium Attachment (PMA) sublayer

The Physical Medium Attachment (PMA) sublayer is directly related to 1000BASE-X PMA sublayer (as described in [2], clause 36.3).

9 Physical Coding Sub layer (PCS)

9.1 TDM structure

The DTM TDM structure (figure 12) differentiates itself from classical TDM systems in that it has a TDM frame separated by a variable length gap. The DTM frame starts with a frame start pattern and is followed by data timeslots numbered relative the frame start. After the data time slots follows the gap encoded with a fill pattern in order to ensure continuity of clock recovery, state of AGC and a pattern distinct from that of the frame start pattern. The TDM frame is repeated in a mesochronous manner at nominally 125 us cycle time achieving a frame frequency of 8 kHz.

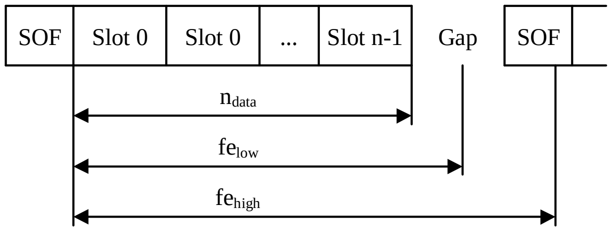

Figure 12: DTM TDM frame and interframe structure

The performance and characteristics of the 8B10B encoded physical interface is given in table 9.

Table 9: Performance table of physical interface

Description	Symbol	Value 1G	Unit
Symbol rate	R	1,25 ± 100 ppm	GBd
Bit rate	C	1,0	Gb/s
Slot rate	f_{slot}	15,625	MHz
Nominal frame rate	f_{frame}	8 000	Hz
Nominal slot count	n_{slot}	1 953,125	slots/frame
Slot length	t_{slot}	64	ns/slot
SOF length	n_{sof}	1	slots/frame
Data slot count	n_{data}	1 940	slots/frame
Frame length	n_{frame}	1 941	slots/frame
Nominal gap	n_{gap}	24	½ slot/frame
Link bit rate	C_{data}	993,28	Mb/s
FE low threshold	fe_{low}	1 950	slots/frame
FE high threshold	fe_{high}	1 957	slots/frame

The bit rate (C) is a function of the symbol rate on the fibre (R) since 10 binary symbols is being used to transmit 8 data bits. This relation comes from the use of the 8B10B line encoding. Thus:

$$C = R\frac{8}{10}$$

The slot speed (f_{slot}) is a function of the bit rate (C) since it takes 64 bits to build up a slot, thus:

$$f_{slot} = \frac{C}{64}$$

The nominal slot count (n_{slot}) is a strict function of the slot rate (f_{slot}) and the frame rate (f_{frame}), thus:

$$n_{slot} = \frac{f_{slot}}{f_{frame}}$$

The maximum bit rate available for channel traffic (including signalling) is strictly related to the number of data slots (n_{data}) and thus the bit rate (C_{data}) becomes:

$$C_{data} = n_{data} \times 64b \times 8k/s = n_{data} \times 512kb/s$$

There are nominally n_{frame} slots per frame on the physical link used for data transport. Their slot number is 0 to n_{frame}-1. These slot numbers are counted from the last Start of Frame (SOF) ordered set on the physical link starting with the slot following the SOF.

The slots after n_{frame} to the next SOF ordered set are assigned to the interframe gap after a frame and will be encoded with FILL ordered sets. The gap region has a variable length and is being ended by a transmission of the next SOF ordered set.

The fe_{low} value defines the minimum number of slots from (and including) the SOF ordered set of a frame to (but not including) the SOF ordered set of the following frame. A SOF ordered set arriving with a lower amount of slots from the previous SOF ordered set is to be interpreted as a Ordered Set Fail anomaly (nOSF).

The fe_{high} value defined the maximum number of slots from (and including) the SOF ordered set of a frame to (but not including) the SOF ordered set of the following frame. If a SOF ordered set does not occur at a slot count, from the previous valid SOF ordered set, lower or equal to the fe_{high}, then the nFE signal is asserted.

The Frame Error anomaly (nFE) signal is asserted when a SOF ordered set have not been received before fe_{high}.

9.2 8B10B transmission code

A transmission code is used to improve the transmission characteristics of information transferred across the physical link. The encoding defined by the transmission code ensures that sufficient transitions are presented in the bit stream to make clock recovery possible at the receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some of the special code-groups of the transmission code contain a distinct and easily recognisable bit pattern that assists a receiver in achieving code-group alignment on the incoming bit stream. The 8B10B transmission code specified for use in the present document has a high transition density, is a run-length-limited code, and is DC-balanced. The transition density of the 8B10B symbols range from 3 to 8 transitions per symbol.

The definition of the 8B10B transmission code in the present document is identical to that specified in [5], clause 11.

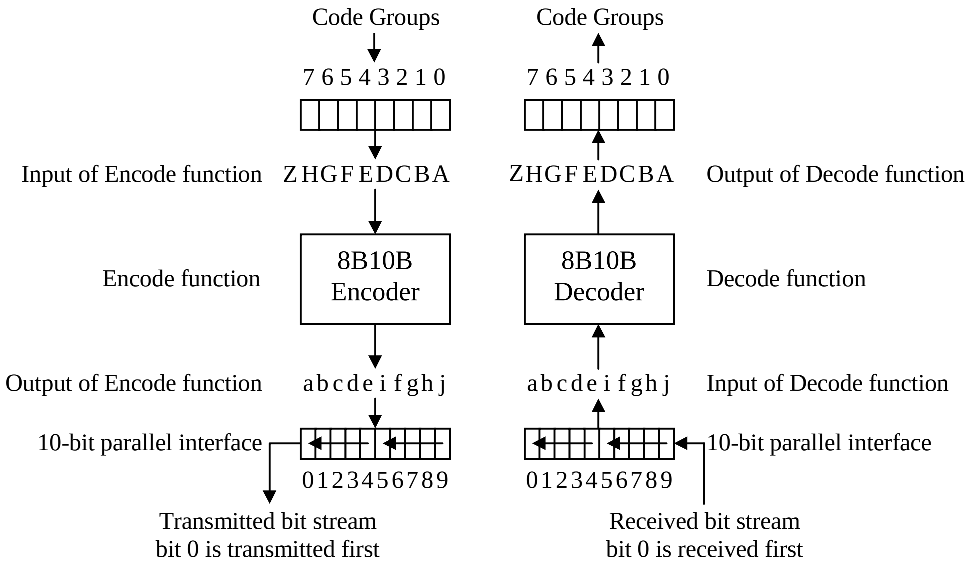

Figure 13: Mapping between of Code Groups and transmitted bits

9.2.1 Notation conventions

8B10B transmission code uses letter notation for describing the bits of an unencoded information octet and a single control variable. Each bit of the unencoded information octet contains either a binary zero or a binary one. A control variable, Z, has either the value D or the value K. When the control variable associated with an unencoded information octet contains the value D, the associated encoded code-group is referred to as a data code-group. When the control variable associated with an unencoded information octet contains the value K, the associated encoded code-group is referred to as a special code-group.

The bit notation of A, B, C, D, E, F, G and H for an unencoded information octet is used in the description of the 8B10B transmission code. The bits A, B, C, D, E, F, G and H are translated to bits a, b, c, d, e, i, f, g, h and j of 10 bit transmission code-groups. 8B10B code group bit assignments are illustrated in figure 13. Each valid code group has been given a name using the following convention: /Dx.y/ for the 256 valid code groups and /Kx.y/ for special control code groups, where x is the decimal value of bits EDCBA, and y is the decimal value of bits HGF.

9.3 Transmission order

9.3.1 Bit order within code group

Within the definition of the 8B10B transmission code, the bit positions of the code-group are labelled a, b, c, d, e, i, f, g, h and j. Bit 'a' shall be transmitted first, followed by bits 'b', 'c', 'd', 'e', 'i', 'f', 'g', 'h' and 'j' in that order (note that bit 'i' shall be transmitted between bit 'e' and bit 'f', rather than in the order that would be indicated by the letters of the alphabet). The code group bit transmission order is illustrated in figure 13.

9.3.2 Code group order within ordered set

Within ordered sets (as specified in table 12), code groups are transmitted sequentially in decreasing code-group order, i.e. CG7, CG6, CG5, CG4, CG3, CG2, CG1 and at last CG0. For ordered set having only the length of 4 code groups (i.e. FILL) is only CG7 to CG4 defined and sent. The ordered set code-group transmission is illustrated in figure 14.

```
   6         5         4         3         2         1         0
3210987654321098765432109876543210987654321098765432109876543210
```

HGFEDCBA CG 7	HGFEDCBA CG 6	HGFEDCBA CG 5	HGFEDCBA CG 4	HGFEDCBA CG 3	HGFEDCBA CG 2	HGFEDCBA CG 1	HGFEDCBA CG 0

Figure 14: Sequencing of data bits into code groups

9.3.3 Ordered set order within TDM frame cycle

Each TDM frame starts with a Start Of Frame (SOF) ordered set. The SOF ordered set is defined in clause 9.5.2.

After the SOF a fixed number of data slots follow where each data slot can contain a Data, Idle, AIS or PS ordered set. There are n_{frame} data-slots in each frame. The Data, Idle, AIS and PS ordered sets are defined in clause 9.5.2 and the number of data slots per frame is defined in clause 9.1.

After the data slots follow an interframe gap, containing a variable number of Fill ordered sets. The Fill ordered set is defined in 9.5.2 and the interframe gap timing is defined in clause 9.1.

9.4 Code groups

9.4.1 Valid and invalid code groups

Table 10 extracted from [2] defines the valid data code groups (D code groups) of the 8B10B transmission code. Table 11 (table 36-2 in [2] modified) defines the valid special code groups of the code. The tables are used for both generating valid code groups (encoding) and checking the validity of received code groups (decoding). In the tables, each octet entry has two columns that represent two (not necessarily different) code groups. The two columns correspond to the valid code group based on the current value of the running disparity (Current RD – or Current RD +). Running disparity is a binary parameter with either the value negative (-) or the value positive (+). Annex C provides several 8B10B transmission code running disparity calculation examples.

Table 10: Valid data code groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD -	Current RD +
			abcdei fghj	abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001
D28.1	3C	001 11100	001110 1001	001110 1001

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101
D10.2	4A	010 01010	010101 0101	010101 0101
D11.2	4B	010 01011	110100 0101	110100 0101
D12.2	4C	010 01100	001101 0101	001101 0101
D13.2	4D	010 01101	101100 0101	101100 0101
D14.2	4E	010 01110	011100 0101	011100 0101
D15.2	4F	010 01111	010111 0101	101000 0101
D16.2	50	010 10000	011011 0101	100100 0101
D17.2	51	010 10001	100011 0101	100011 0101
D18.2	52	010 10010	010011 0101	010011 0101
D19.2	53	010 10011	110010 0101	110010 0101
D20.2	54	010 10100	001011 0101	001011 0101
D21.2	55	010 10101	101010 0101	101010 0101
D22.2	56	010 10110	011010 0101	011010 0101
D23.2	57	010 10111	111010 0101	000101 0101
D24.2	58	010 11000	110011 0101	001100 0101
D25.2	59	010 11001	100110 0101	100110 0101
D26.2	5A	010 11010	010110 0101	010110 0101
D27.2	5B	010 11011	110110 0101	001001 0101
D28.2	5C	010 11100	001110 0101	001110 0101
D29.2	5D	010 11101	101110 0101	010001 0101
D30.2	5E	010 11110	011110 0101	100001 0101
D31.2	5F	010 11111	101011 0101	010100 0101
D0.3	60	011 00000	100111 0011	011000 1100
D1.3	61	011 00001	011101 0011	100010 1100
D2.3	62	011 00010	101101 0011	010010 1100
D3.3	63	011 00011	110001 1100	110001 0011
D4.3	64	011 00100	110101 0011	001010 1100
D5.3	65	011 00101	101001 1100	101001 0011
D6.3	66	011 00110	011001 1100	011001 0011
D7.3	67	011 00111	111000 1100	000111 0011
D8.3	68	011 01000	111001 0011	000110 1100
D9.3	69	011 01001	100101 1100	100101 0011
D10.3	6A	011 01010	010101 1100	010101 0011
D11.3	6B	011 01011	110100 1100	110100 0011
D12.3	6C	011 01100	001101 1100	001101 0011
D13.3	6D	011 01101	101100 1100	101100 0011
D14.3	6E	011 01110	011100 1100	011100 0011
D15.3	6F	011 01111	010111 0011	101000 1100
D16.3	70	011 10000	011011 0011	100100 1100
D17.3	71	011 10001	100011 1100	100011 0011
D18.3	72	011 10010	010011 1100	010011 0011
D19.3	73	011 10011	110010 1100	110010 0011
D20.3	74	011 10100	001011 1100	001011 0011
D21.3	75	011 10101	101010 1100	101010 0011
D22.3	76	011 10110	011010 1100	011010 0011
D23.3	77	011 10111	111010 0011	000101 1100
D24.3	78	011 11000	110011 0011	001100 1100
D25.3	79	011 11001	100110 1100	100110 0011
D26.3	7A	011 11010	010110 1100	010110 0011

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D27.3	7B	011 11011	110110 0011	001001 1100
D28.3	7C	011 11100	001110 1100	001110 0011
D29.3	7D	011 11101	101110 0011	010001 1100
D30.3	7E	011 11110	011110 0011	100001 1100
D31.3	7F	011 11111	101011 0011	010100 1100
D0.4	80	100 00000	100111 0010	011000 1101
D1.4	81	100 00001	011101 0010	100010 1101
D2.4	82	100 00010	101101 0010	010010 1101
D3.4	83	100 00011	110001 1101	110001 0010
D4.4	84	100 00100	110101 0010	001010 1101
D5.4	85	100 00101	101001 1101	101001 0010
D6.4	86	100 00110	011001 1101	011001 0010
D7.4	87	100 00111	111000 1101	000111 0010
D8.4	88	100 01000	111001 0010	000110 1101
D9.4	89	100 01001	100101 1101	100101 0010
D10.4	8A	100 01010	010101 1101	010101 0010
D11.4	8B	100 01011	110100 1101	110100 0010
D12.4	8C	100 01100	001101 1101	001101 0010
D13.4	8D	100 01101	101100 1101	101100 0010
D14.4	8E	100 01110	011100 1101	011100 0010
D15.4	8F	100 01111	010111 0010	101000 1101
D16.4	90	100 10000	011011 0010	100100 1101
D17.4	91	100 10001	100011 1101	100011 0010
D18.4	92	100 10010	010011 1101	010011 0010
D19.4	93	100 10011	110010 1101	110010 0010
D20.4	94	100 10100	001011 1101	001011 0010
D21.4	95	100 10101	101010 1101	101010 0010
D22.4	96	100 10110	011010 1101	011010 0010
D23.4	97	100 10111	111010 0010	000101 1101
D24.4	98	100 11000	110011 0010	001100 1101
D25.4	99	100 11001	100110 1101	100110 0010
D26.4	9A	100 11010	010110 1101	010110 0010
D27.4	9B	100 11011	110110 0010	001001 1101
D28.4	9C	100 11100	001110 1101	001110 0010
D29.4	9D	100 11101	101110 0010	010001 1101
D30.4	9E	100 11110	011110 0010	100001 1101
D31.4	9F	100 11111	101011 0010	010100 1101
D0.5	A0	101 00000	100111 1010	011000 1010
D1.5	A1	101 00001	011101 1010	100010 1010
D2.5	A2	101 00010	101101 1010	010010 1010
D3.5	A3	101 00011	110001 1010	110001 1010
D4.5	A4	101 00100	110101 1010	001010 1010
D5.5	A5	101 00101	101001 1010	101001 1010
D6.5	A6	101 00110	011001 1010	011001 1010
D7.5	A7	101 00111	111000 1010	000111 1010
D8.5	A8	101 01000	111001 1010	000110 1010
D9.5	A9	101 01001	100101 1010	100101 1010
D10.5	AA	101 01010	010101 1010	010101 1010
D11.5	AB	101 01011	110100 1010	110100 1010
D12.5	AC	101 01100	001101 1010	001101 1010
D13.5	AD	101 01101	101100 1010	101100 1010
D14.5	AE	101 01110	011100 1010	011100 1010
D15.5	AF	101 01111	010111 1010	101000 1010
D16.5	B0	101 10000	011011 1010	100100 1010
D17.5	B1	101 10001	100011 1010	100011 1010
D18.5	B2	101 10010	010011 1010	010011 1010
D19.5	B3	101 10011	110010 1010	110010 1010
D20.5	B4	101 10100	001011 1010	001011 1010
D21.5	B5	101 10101	101010 1010	101010 1010
D22.5	B6	101 10110	011010 1010	011010 1010
D23.5	B7	101 10111	111010 1010	000101 1010
D24.5	B8	101 11000	110011 1010	001100 1010

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D25.5	B9	101 11001	100110 1010	100110 1010
D26.5	BA	101 11010	010110 1010	010110 1010
D27.5	BB	101 11011	110110 1010	001001 1010
D28.5	BC	101 11100	001110 1010	001110 1010
D29.5	BD	101 11101	101110 1010	010001 1010
D30.5	BE	101 11110	011110 1010	100001 1010
D31.5	BF	101 11111	101011 1010	010100 1010
D0.6	C0	110 00000	100111 0110	011000 0110
D1.6	C1	110 00001	011101 0110	100010 0110
D2.6	C2	110 00010	101101 0110	010010 0110
D3.6	C3	110 00011	110001 0110	110001 0110
D4.6	C4	110 00100	110101 0110	001010 0110
D5.6	C5	110 00101	101001 0110	101001 0110
D6.6	C6	110 00110	011001 0110	011001 0110
D7.6	C7	110 00111	111000 0110	000111 0110
D8.6	C8	110 01000	111001 0110	000110 0110
D9.6	C9	110 01001	100101 0110	100101 0110
D10.6	CA	110 01010	010101 0110	010101 0110
D11.6	CB	110 01011	110100 0110	110100 0110
D12.6	CC	110 01100	001101 0110	001101 0110
D13.6	CD	110 01101	101100 0110	101100 0110
D14.6	CE	110 01110	011100 0110	011100 0110
D15.6	CF	110 01111	010111 0110	101000 0110
D16.6	D0	110 10000	011011 0110	100100 0110
D17.6	D1	110 10001	100011 0110	100011 0110
D18.6	D2	110 10010	010011 0110	010011 0110
D19.6	D3	110 10011	110010 0110	110010 0110
D20.6	D4	110 10100	001011 0110	001011 0110
D21.6	D5	110 10101	101010 0110	101010 0110
D22.6	D6	110 10110	011010 0110	011010 0110
D23.6	D7	110 10111	111010 0110	000101 0110
D24.6	D8	110 11000	110011 0110	001100 0110
D25.6	D9	110 11001	100110 0110	100110 0110
D26.6	DA	110 11010	010110 0110	010110 0110
D27.6	DB	110 11011	110110 0110	001001 0110
D28.6	DC	110 11100	001110 0110	001110 0110
D29.6	DD	110 11101	101110 0110	010001 0110
D30.6	DE	110 11110	011110 0110	100001 0110
D31.6	DF	110 11111	101011 0110	010100 0110
D0.7	E0	111 00000	100111 0001	011000 1110
D1.7	E1	111 00001	011101 0001	100010 1110
D2.7	E2	111 00010	101101 0001	010010 1110
D3.7	E3	111 00011	110001 1110	110001 0001
D4.7	E4	111 00100	110101 0001	001010 1110
D5.7	E5	111 00101	101001 1110	101001 0001
D6.7	E6	111 00110	011001 1110	011001 0001
D7.7	E7	111 00111	111000 1110	000111 0001
D8.7	E8	111 01000	111001 0001	000110 1110
D9.7	E9	111 01001	100101 1110	100101 0001
D10.7	EA	111 01010	010101 1110	010101 0001
D11.7	EB	111 01011	110100 1110	110100 1000
D12.7	EC	111 01100	001101 1110	001101 0001
D13.7	ED	111 01101	101100 1110	101100 1000
D14.7	EE	111 01110	011100 1110	011100 1000
D15.7	EF	111 01111	010111 0001	101000 1110
D16.7	F0	111 10000	011011 0001	100100 1110
D17.7	F1	111 10001	100011 0111	100011 0001
D18.7	F2	111 10010	010011 0111	010011 0001
D19.7	F3	111 10011	110010 1110	110010 0001
D20.7	F4	111 10100	001011 0111	001011 0001
D21.7	F5	111 10101	101010 1110	101010 0001
D22.7	F6	111 10110	011010 1110	011010 0001

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj
D23.7	F7	111 10111	111010 0001	000101 1110
D24.7	F8	111 11000	110011 0001	001100 1110
D25.7	F9	111 11001	100110 1110	100110 0001
D26.7	FA	111 11010	010110 1110	010110 0001
D27.7	FB	111 11011	110110 0001	001001 1110
D28.7	FC	111 11100	001110 1110	001110 0001
D29.7	FD	111 11101	101110 0001	010001 1110
D30.7	FE	111 11110	011110 0001	100001 1110
D31.7	FF	111 11111	101011 0001	010100 1110

Table 11: Valid special code groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD - abcdei fghj	Current RD + abcdei fghj	Notes
K28.0	1C	000 11100	001111 0100	110000 1011	1
K28.1	3C	001 11100	001111 1001	110000 0110	1 and 2
K28.2	5C	010 11100	001111 0101	110000 1010	1
K28.3	7C	011 11100	001111 0011	110000 1100	1
K28.4	9C	100 11100	001111 0010	110000 1101	
K28.5	BC	101 11100	001111 1010	110000 0101	2
K28.6	DC	110 11100	001111 0110	110000 1001	1
K28.7	FC	111 11100	001111 1000	110000 0111	1 and 2
K23.7	F7	111 10111	111010 1000	000101 0111	1
K27.7	FB	111 11011	110110 1000	001001 0111	1
K29.7	FD	111 11101	101110 1000	010001 0111	1
K30.7	FE	111 11110	011110 1000	100001 0111	1
NOTE 1: Reserved and not valid DTM code groups. Included for completeness. NOTE 2: Contains a comma.					

9.4.2 Running disparity rules

After powering on, the transmitter shall assume the negative value for its initial running disparity. Upon transmission of any code group, the transmitter shall calculate a new value for its running disparity based on the contents of the transmitted code group.

After powering on, the receiver should assume either the positive or negative value for its initial running disparity. Upon the reception of any code group, the receiver determines whether the code group is valid or invalid and calculates a new value for its running disparity based on the contents of the received code group.

The following rules for running disparity shall be used to calculate the new running disparity value for code groups that have been transmitted (transmitter's running disparity) and that have been received (receiver's running disparity).

Running disparity for a code group is calculated on the basis of sub-blocks, where the first six bits (abcdei) form one sub-block (six-bit sub-block) and the second four bits (fghj) form the sub-block (four-bit sub-block). Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the last code group. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the code-group is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1) Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the six-bit sub-block if the six-bit sub-block is 000111, and it is positive at the end of the four-bit sub-block if the four-bit sub-block is 0011.

2) Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the six-bit sub-block if the six-bit sub-block is 111000, and it is negative at the end of the four-bit sub-block if the four-bit sub-block is 1100.

3) Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

NOTE: All sub-blocks with equal numbers of zeros and ones are disparity neutral. In order to limit the run length of zeros or ones between sub-blocks, the 8B10B transmission code rules specify that sub-blocks encoded as 000111 or 0011 are generated only when the running disparity at the beginning of the sub-block is positive; thus, running disparity at the end of these sub-blocks is also positive. Likewise, sub-blocks containing 111000 or 1100 are generated only when the running disparity at the beginning of the sub-block is negative; thus, running disparity at the end of these sub-blocks is also negative.

9.4.3 Generating code groups

The appropriate entry in either table 10 or table 11 is found for each octet for which a code group is to be generated (encoded). The current value of the transmitter's running disparity shall be used to select the code group from its corresponding column. For each code group transmitted, a new value of the running disparity is calculated. This new value is used as the transmitter's current running disparity for the next octet to be encoded and transmitted.

9.4.4 Checking the validity of received code groups

The column in tables 10 and 11 corresponding to the current value of receiver's running disparity is searched for the received code group:

1) If the received code group is found in the proper column, according to the current running disparity, the code group is considered valid and, for data code groups, the associated data octet determined (decoded).

2) If the received code group is not found in that column, the code group is considered invalid.

3) If the received code group is one of the special code groups which are reserved and not valid in DTM, the code group is considered invalid.

Independent of the code group's validity, the received code group is used to calculate a new value of running disparity. The new value is used as the receiver's current running disparity for the next received code group.

NOTE: Detection of an invalid code group does not necessarily indicate that the code group in which the invalid code group was detected is in error. Invalid code groups may result from a prior error which altered the running disparity of the bit stream but which did not result in a detectable error at the code group in which the error occurred. Appendix C provides examples of this error.

The number of invalid code groups detected is proportional to the bit error rate (BER) of the physical link.

The Code Group Fail anomaly (nCGF) signal is asserted for a slot whenever the 8B10B decoder is unable to decode a 10 bit word to a valid code-group.

9.5 Ordered sets

Eight ordered sets, consisting of a combination of special and data code groups are defined. Ordered sets which include /K28.5/ provide the ability to obtain bit and code group synchronization and establish ordered set alignment (see clause 9.6). Ordered sets provide for the delineation of a frame and synchronization between the transmitter and receiver circuits at opposite ends of a physical link. Table 12 lists the defined ordered sets.

9.5.1 Ordered set rules

Ordered sets are specified according to the following rules:

1) Ordered sets consist of either four or eight code groups.

2) The first code group (CG7) of all non-data ordered sets is always a special code group.

3) The first code group (CG7) of the data ordered set is always a data code group.

4) The second code group of all ordered sets is always a data code group. The second code group provides a high bit transition density.

Table 12 lists the defined ordered sets.

9.5.2 Mapping between ordered sets and code groups

The SOF, Data, PS, AIS and Idle ordered sets is built out of 8 code groups. The FILL ordered set take up 4 code groups.

These ordered sets should be mapped into the D/Kxx.y format as described in table 12. The Idle and Fill ordered sets attain a different mapping depending on the disparity (marked with the addition of an pos or neg marker, see further on disparity in clause 9.4.2) output of the code group encoded prior to the coding of the full ordered set.

Table 12: Ordered sets

Ordered set	CG 7	CG 6	CG 5	CG 4	CG 3	CG 2	CG 1	CG 0
SOF (FILL + SOF Normal Class 1)	K28.5	D21.4	D21.6	D21.6	K28.5	D21.5	D23.1	D23.1
Data	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y
PS (Receiver Ready)	K28.4	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y
AIS	K28.5	D5.4	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y	Dxx.y
IDLE pos (Idle)	K28.5	D21.5	D21.5	D21.5	K28.5	D21.4	D21.5	D21.5
IDLE neg (Idle)	K28.5	D21.4	D21.5	D21.5	K28.5	D21.4	D21.5	D21.5
FILL pos (EOF Normal)	K28.5	D21.5	D21.6	D21.6				
FILL neg (EOF Normal)	K28.5	D21.4	D21.6	D21.6				

In table 12, the corresponding Fibre Channel ordered sets (if exist) are given within parenthesis.

The Start of Frame (SOF) ordered set is sent at the start of a new frame. In the receiver will the decoded SOF set the Frame Start signal (nFS) asserted.

After a frame has been transmitted, the encoder transmits FILL ordered set. There is always FILL ordered sets sent between the frames for absorbing jitter in the network. The FILL ordered sets set the disparity to negative before a new frame is started.

For 64-bit data, Dxx.y is being sent in all code groups. The data bit 63 down to 0 (Code Group 7 to 0) is the data-payload.

For the Idle-marker, the Idle ordered set is transmitted. There are two disparity variants of the Idle ordered set for disparity handling. The Idle marker is only sent within a frame in place of data.

For the PS-marker, the PS ordered set is transmitted. The data bit 55 down to 0 (Code Groups 6 to 0) is the PS-payload.

For the AIS-marker, the AIS ordered set is transmitted. The data bit 47 down to 0 (Code Groups 5 to 0) is the AIS-payload.

The code group K28.5 in the beginning of each ordered set is a comma character and is used for synchronising the receiver and to achieve 10-bit alignment of at the PMA service interface.

The Ordered Set Fail anomaly (nOSF) signal is asserted for a slot whenever:

a) The Code Group Fail anomaly (nCGF) signal was asserted for any of ordered sets in the slot position.

b) The mapping of code-groups into slot format according to table 12 fails.

c) The detection of a FILL ordered set in the data slot range according to clause 9.1.

d) The detection of a SOF ordered set in a slot position lower than FE_{low} (before the gap) according to clause 9.1.

e) The detection of a ordered set other than SOF and FILL in a slot position above that of FE_{low} (in the gap) according to clause 9.1.

9.5.3 /K28.5/ code group considerations

The /K28.5/ special code group is chosen as the first code group of all ordered sets (except for Data and PS-marker) that are signalled repeatedly and for the purpose of allowing a receiver to synchronize to the incoming bit stream, for the following reasons:

1) Bits abcdeif make up a comma. The comma can be used to easily find and verify code group and ordered set boundaries of the rx_bit stream.

2) Bits ghj of the encoded code group present the maximum number of transitions, simplifying receiver acquisition of bit synchronization.

9.5.4 Comma considerations

The seven bit comma string is defined as either b"0011111" (comma+) or b"1100000" (comma-). The Idle and Fill ordered sets are specified to ensure that comma+ is transmitted with either equivalent or greater frequency than comma- for the duration of their transmission. This is done to ensure compatibility with common components.

The comma contained within the /K28.1/, /K28.5/ and /K28.7/ special code groups is a singular bit pattern, which in the absence of transmission errors, cannot appear in any other location of a code group and cannot be generated across the boundaries of any two adjacent code groups.

9.6 Alignment synchronization

When receiving a bit stream alignment to the bit stream must be accomplished through synchronization processes. Three levels of alignment synchronization are needed for a 8B10B encoded DTM transmission:

- Code group boundary synchronization in bit stream.
- Ordered set (Slot) boundary synchronization in code group stream.
- Frame boundary synchronization in ordered set stream.

9.6.1 Code group boundary synchronization

The code group boundary synchronization is achieved by the use of the comma string, which through the encoding is ensured to exist only one alignment form, which exists in 3 special code groups, but not in any sequential combination of legal code groups. The code group boundary synchronization is performed in the deserialisation block, which converts the received bit stream into 10 bit code group words.

In order to prohibit incorrect re-alignments due to bit errors (which would cause excessive error propagation) the alignment is controlled by a control signal. This control signal, PL1_AI_EN_FS (traditionally referred to as EN_CDET for Enable Comma Detect), is controlled by the higher levels of synchronization.

When a comma+ string (b"0011111") is detected in the bit stream, and the PL1_AI_EN_FS is asserted, then shall the deserialiser block realign such that the first bit of the comma (first "0" of "0011111") will align to bit a (bit 0) of the deserialiser). Upon realignment shall the PL1_AI_FS signal (traditionally referred to as COM_DET for Comma Detect) be put asserted in order to indicate realignment to the higher layer synchronization.

9.6.2 Ordered set boundary synchronization

The ordered set boundary synchronization is achieved by the use of the Fill ordered set, and is maintained by monitoring the failures of the ordered set decoding.

The state machine described in figure 15 detects the if the receiver gains or looses slot boundary synchronization with the incoming bit stream. This is done by checking for faults in the decoded data stream indicated by the nOSF signal. The machine is stepped per slot received from the decoder.

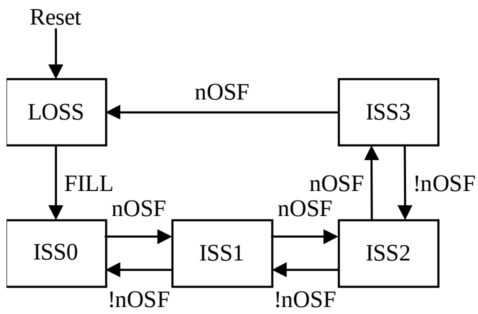

Figure 15: Slot Sync State Machine

The initial state is the Loss Of Slot Synchronization (LOSS) state.

The Loss Of Slot Synchronization state (LOSS) will be maintained until a Fill ordered set has been detected by the ordered set decoder. When the Fill ordered set has been received, the state is changed to the ISS 0.

The In Slot Sync state 0 (ISS0) will be maintained until nOSF goes asserted. When nOSF goes asserted, the state is changed to the ISS1.

When in the In Slot Sync state 1 (ISS1) if nOSF is asserted will the next state be ISS2, else will the next state be ISS0.

When in the In Slot Sync state 2 (ISS2) if nOSF is asserted will the next state be ISS3, else will the next state be ISS1.

When in the In Slot Sync state 3 (ISS3) if nOSF is asserted will the next state be LOSS, else will the next state be ISS2.

When the state machine is in the LOSS state shall the Loss Of Slot Synchronization anomaly (nLOSS) be asserted, else it shall be de-asserted.

9.6.3 Frame boundary synchronization

The frame boundary synchronization (see figure 16) is achieved by successfully received 4 full frames and upon loss of ordered set synchronization or frame error, looses frame synchronization.

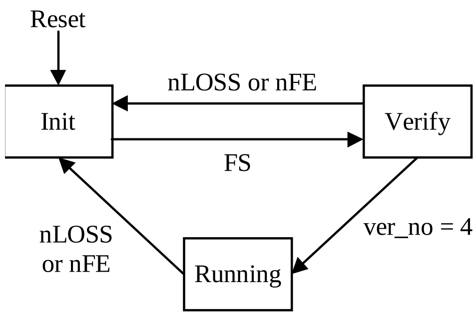

Figure 16: Frame Synchronization State Machine

The initial state is the Init state.

When in the Init state a FS is detected, the next state shall be the Verify state and the verification counter shall be reset to 0.

When in the Verify state a FS is detected, the verification counter (ver_no) is to be increased by one. If the counter reaches the value of 4, then shall the next state be the Running state else, if either nLOSS or nFE goes asserted, then shall the next state be the Init state.

When in the Running state and either nLOSS or nFE goes asserted, then shall the next state be the Init state.

The Loss Of Frame defect (dLOF) is asserted when the state machine is in either the Init or the Verify states. The dLOF signal is de-asserted when the state machine is in the Running state.

The PL1_AI_EN_FS signal is asserted when the state machine is in either the Init or the Verify states. The PL1_AI_EN_FS signal is de-asserted when the state machine is in the Running state. This will enable the alignment hunting when frame synchronization has not been achieved, and ensure to reduce the possibility of bit errors to cause loss of frame synchronization.

Annex A (informative): External dependencies

A.1 Conformity to IEEE 802.3

Only selected parts of [2] are being used and therefore only some parts of [2] are applicable for the 8B10B encoded physical interface. The full comparability map is found in table A.1.

Table A.1: Conformity to IEEE 802.3

IEEE 802.3 clause	Applicability	Description
36	Parts	Physical Coding Sub layer (PCS) and Physical Medium Attachment (PMA) sub layer, type 1000BASE-X
36.1	Parts with modifications	Overview
36.2	Parts with modifications	Physical Coding Sublayer (PCS)
36.3	Full	Physical Medium Attachment (PMA) sub layer
36.4	Parts with modifications	Comparability considerations
36.7	Parts with modifications	Protocol Implementation Conformance Statement (PICS) proforma for clause 36, Physical Coding Sub layer (PCS) and Physical Medium Attachment (PMA) sub layer, type 1000BASE-X
36B (informative)	Full	8B10B transmission code running disparity calculation examples
38	Full	Physical Medium Dependent (PMD) sub layer and baseband medium, type 1000BASE-LX (Long Wavelength Laser) and 1000BASE-SX (Short Wavelength Laser)
39	Full	Physical Medium Dependent (PMD) sub layer and baseband medium, type 1000BASE-CX

Annex B (normative): Jitter test pattern

This annex defines test patterns that allow DPP-8B10B PMDs to be tested for compliance while in a system environment. The patterns may be implemented at a bit, code-group, or frame level and may be used for transmitter testing. The receiver may not have the capability to accept these diagnostic sequences; however, system debug can be improved if a receiver is able to test one or more of these patterns and report bit error (e.g. 8B10B decoder errors) back to the user.

B.1 High-frequency test pattern

The intent of this test pattern is to test random jitter (RJ) at a BER of 10^{-12}, and also to test the asymmetry of transition times. This high-frequency test pattern generates a one, or light on, for a duration of 1 bit time, followed by a zero, or light off, for a duration of 1 bit time. This pattern repeats continuously for the duration of the test.

EXAMPLE: 1010101010101010101010101010101010101010…

NOTE: This pattern can be generated by the repeated transmission of the D21.5 code group. Disparity rules are followed.

B.2 Low-frequency test pattern

The intent of this test pattern is to test low-frequency RJ and also to test PLL tracking error. This low frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 5 bit times. This pattern repeats continuously for the duration of the test.

EXAMPLE: 1111100000111110000011111000001111100000…

NOTE: This pattern can be generated by the repeated transmission of the K28.7 code group. Disparity rules are followed.

B.3 Mixed frequency test pattern

The intent of this test pattern is to test the combination of RJ and deterministic jitter (DJ). This mixed frequency test pattern generates a one, or light on, for a duration of 5 bit times, followed by a zero, or light off, for a duration of 1 bit times, followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 2 bit times followed by a zero for 5 bit times followed by a one for 1 bit time followed by a zero for 1 bit time followed by a one for 1 bit time followed by a zero for 2 bit times. This pattern repeats continuously for the duration of the test.

EXAMPLE: 11111010110000010100111110101100000101000…

NOTE: This pattern can be generated by the repeated transmission of the K28.5 code group. Disparity rules are followed.

B.4 Long continuous random test pattern

The long continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking that can be used for the measurement of jitter at either a component or system level.

NOTE: The derivation of this pattern may be found in ANSI FC-MJS "*Fibre Channel Jitter Working Group Technical Report" (see bibliography)*. This technical report modified the original RPAT as defined by Fibre Channel so that is would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an 802.3 frame.

The long continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in [2], clause 36 in the ordinary way. The contents of each packet are composed of the following octet sequences, as observed at the GMII, before 8B10B coding.

Each packet in the long continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 1 512 data octets (126 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

```
PREAMBLE/SFD:
    55 55 55 55 55 55 55 D5
MODIFIED RPAT SEQUENCE (LOOP 126 times)
    BE D7 23 47 6B 8F B3 14 5E FB 35 59
CRC
    94 D2 54 AC
IPG (TX_EN and TX_ER low)
    00 00 00 00 00 00 00 00 00 00 00 00
END
```

B.5 Short continuous random test pattern

The short continuous random test pattern is a random test pattern intended to provide broad spectral content and minimal peaking used for the measurement of jitter at either a component or system level.

NOTE: The derivation of this pattern may be found in ANSI FC-MJS "*Fibre Channel Jitter Working Group Technical Report" (see bibliography)*. This technical report modified the original RPAT as defined by Fibre Channel so that is would maintain its intended qualities but fit into a Fibre Channel frame. This annex uses similar modifications to fit the same RPAT into an 802.3 frame.

The short continuous random test pattern consists of a continuous stream of identical packets, separated by a minimum IPG. Each packet is encapsulated within SPD and EPD delimiters as specified in clause 36 in the ordinary way. The contents of each packet are composed of the following octet sequences, as observed at the GMII, before 8B10B coding.

Each packet in the short continuous random test pattern consists of 8 octets of PREAMBLE/SFD, followed by 348 data octets (29 repetitions of the 12-octet modified RPAT sequence), plus 4 CRC octets, followed by a minimum IPG of 12 octets of IDLE.

The format of this packet is such that the PCS will generate the following ordered sets for the IPG:
/T/ /R/ /I1/ /I2/ /I2/ /I2/ /I2/

```
PREAMBLE/SFD:
    55 55 55 55 55 55 55 D5
MODIFIED RPAT SEQUENCE (LOOP 29 TIMES)
    BE D7 23 47 6B 8F B3 14 5E FB 35 59
CRC
    2F E0 AA EF
IPG (TX_EN and TX_ER low)
    00 00 00 00 00 00 00 00 00 00 00 00
END
```

Annex C (informative): 8B10B transmission code running disparity calculation example

Detection of a invalid code-group in the 8B10B transmission code does not necessarily indicate that the code-group in which the error was detected was the one in which the error occurred. Invalid code-groups may result from a prior error which altered the running disparity of the bit stream but which did not result in a detectable error at the code-group in which the error occurred. The examples shown in tables C.1 and C.2 exhibit this behaviour. The example shown in table C.3 exhibits the case where a bit error in a received code-group is detected in that code-group, affects the next code-group, and error propagation is halted upon detection of running disparity error.

Table C.1: RD error detected two code-groups following error

		Code-Group		**Code-Group**		**Code-Group**	
Stream	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**
Transmitted code-group	-	D21.1	-	D10.2	-	D23.5	+
Transmitted bit stream	-	101010 - 1001	-	010101 - 0101	-	111010 + 1010	+
Received bit stream	-	101010 - 10**1**1 (see note 1)	+	010101 + 0101	+	111010 + 1010 (see note 2)	+
Received code-group	-	D21.0	+	D10.2	+	invalid code-group (see note 2)	+ (see note 3)

NOTE 1: Bit error introduced (1001 ⇒ 10**1**1).
NOTE 2: Nonzero disparity blocks must alternate in polarity (+ ⇒ -). In this case, RD does not alternate (+ ⇒ +), the received code-group is not found in the Current RD+ column in either table 11 or table 12, and an invalid code-group is recognised.
NOTE 3: Running disparity is calculated on the received code-group regardless of the validity of the received code-group. Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e. equivalent to the receiving bit stream had an error not occurred).

Table C.2: RD error detected in next code-group following error

		Code-Group		**Code-Group**		**Code-Group**	
Stream	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**
Transmitted code-group	-	D21.1	-	D23.4	-	D23.5	+
Transmitted bit stream	-	101010 - 1001	-	111010 - 0010	-	111010 + 1010	+
Received bit stream	-	101010 - 10**1**1 (see note 1)	+	111010 + 0010 (see note 2)	-	111010 + 1010 (see note 2)	+
Received code-group	-	D21.0	+	invalid code-group (see note 2)	-	D23.5	+

NOTE 1: Bit error introduced (1001 ⇒ 10**1**1).
NOTE 2: Nonzero disparity blocks must alternate in polarity (+ ⇒ -).

Table C.3: A single bit error affects two received code-groups

		Code-Group		Code-Group		Code-Group	
Stream	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**	**RD**
Transmitted code-group	-	D3.6	-	K29.7	-	K23.7	-
Transmitted bit stream	-	110001 - 0110	-	101110 - 1000	-	111010 + 1000	-
Received bit stream	-	110001 - 011**1** (see note 1)	+ (see note 2)	101110 + 1000 (see note 3)	-	111010 + 1000	-
Received code-group	-	invalid code-group (see note 4)	+	invalid code-group (see note 5)	-	K23.7	-

NOTE 1: Bit error introduced (0110 ⇒ 011**1**).

NOTE 2: Nonzero disparity blocks must alternate in polarity (+ ⇒ -). Received RD differs from transmitted RD.

NOTE 3: Nonzero disparity blocks must alternate in polarity (- ⇒ +). Invalid code-group due to RD error since RD remains at +.

NOTE 4: Received code-group is not found in either table 11 or table 12.

NOTE 5: Nonzero disparity blocks prevent the propagation of errors and normalize running disparity to the transmitted bit stream (i.e. equivalent to the receiving bit stream had an error not occurred).

Annex D (informative): Bibliography

ANSI FC-MJS: "Fibre Channel - Methods for Jitter Specification".

ETSI ES 201 803-2-3: "Dynamic synchronous Transfer Mode (DTM); Part 2: System characteristics; Sub-part 3: Transport network and channel adaption aspects".

ETSI ES 201 803-1: "Dynamic synchronous Transfer Mode (DTM); Part 1: System description".

History

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