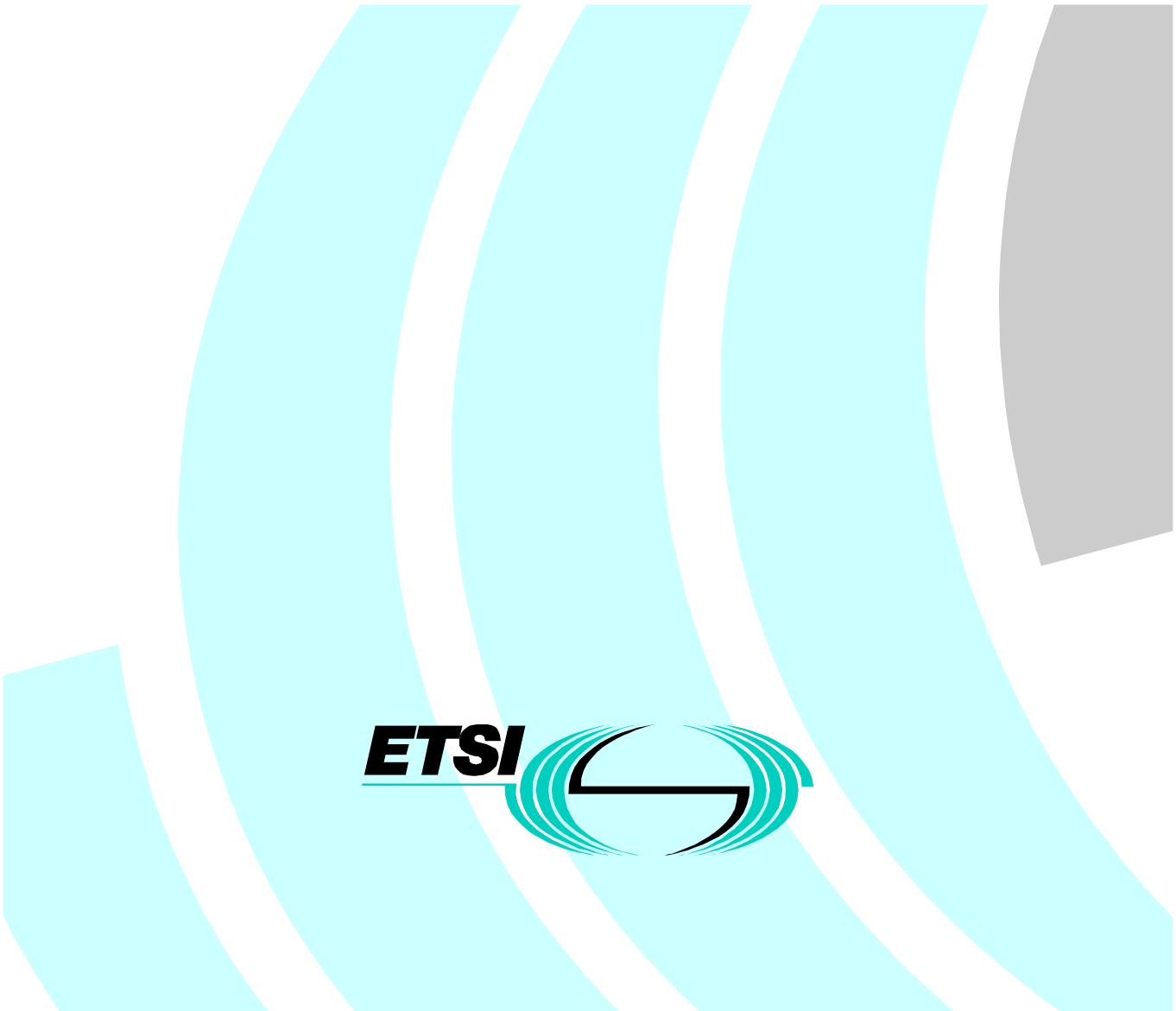
EN 300 462-5-1 V1.1.2 (1998-05)

European Standard (Telecommunications series)

Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment



Reference
REN/TM-03017-5-1 (4a199idc.PDF)

Keywords
synchronization, timing, transmission

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Contents

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Foreword

This European Standard (Telecommunications series) has been produced by the Transmission and Multiplexing (TM) Technical Committee.

The present document has been produced to provide requirements for synchronization networks that are compatible with the performance requirements of digital networks. It is one of a family of documents covering various aspects of synchronization networks:

Part 1-1:	"Definitions and terminology for synchronization networks";
Part 2-1:	"Synchronization network architecture";
Part 3-1:	"The control of jitter and wander within synchronization networks";
Part 4-1:	"Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment";
Part 4-2:	"Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment Implementation Conformance (ICS) Statement";
Part 5-1:	**"Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment";**
Part 6-1:	"Timing characteristics of primary reference clocks";
Part 6-2:	"Timing characteristics of primary reference clocks Implementation Conformance (ICS) Statement";
Part 7-1:	"Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications".

Parts 1-1, 2-1, 3-1 and 5-1 have previously been published as ETS 300 462 Parts 1, 2, 3 and 5, respectively.

Additionally, parts 4-1 and 6-1 completed the Voting phase of the Two Step Approval procedure as ETS 300 462 Parts 4 and 6, respectively.

It was decided to prepare ICS proformas for several of the parts and this necessitated a re-numbering of the individual document parts. It was also decided to create a new part 7-1.

This in turn led to a need to re-publish new versions of all six parts of the original ETS. At the same time, the opportunity was taken to convert the document type to EN.

This has involved no technical change to any of the documents. However part 5-1 has been modified, due to editorial errors which appeared in ETS 300 462-5.

Transposition dates	
Date of adoption of this ETS:	16 August 1996
Date of latest announcement of this ETS (doa):	31 December 1996
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	30 June 1997
Date of withdrawal of any conflicting National Standard (dow):	30 June 1997

NOTE: The above transposition table is the original table from ETS 300 462-5 (September 1996, see History).

1 Scope

This European Standard (Telecommunications series) outlines requirements for timing devices used in synchronising network equipment that operates according to the principles governed by the Synchronous Digital Hierarchy (SDH). These requirements apply under the normal environmental conditions specified for SDH equipment. Typical SDH equipment contains a slave clock linked to a master, or a primary reference clock. The logical function of the SEC is described in figure 2 of EN 300 462-2-1 [3]. In general the SDH Equipment Clock (SEC) will have multiple reference inputs. In the event that all links between the master and the slave clock fail, the equipment should be capable of maintaining operation (holdover) within the prescribed performance limits contained within the present document.

Slave clocks used in SDH equipment shall meet specific requirements in order to comply with the jitter specifications given in ETS 300 417-1-1 [9] for plesiochronous tributaries.

The case where clock performance is required in SDH equipment is outside the scope of the present document, see EN 300 462-4-1 [10].

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, subsequent revisions do apply.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] ETS 300 019: "Equipment Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment".

[2] EN 300 462-1-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1-1: Definitions and terminology for synchronization networks".

[3] EN 300 462-2-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2-1: Synchronisation network architecture".

[4] ITU-T Recommendation G.823: "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".

[5] EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[6] ITU-T Recommendation G.703: "Physical/electrical characteristics of hierarchical digital interfaces".

[7] ITU-T Recommendation G.825: "The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)".

[8] ITU-T Recommendation Q.551: "Transmission characteristics of digital exchanges".

[9] ETS 300 417-1-1 (1996): "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 1-1: Generic processes and performance".

[10] EN 300 462-4-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4-1: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of the present document, the definitions given in EN 300 462-1-1 [2] apply.

3.2 Abbreviations

For the purposes of the present document, the abbreviations given in EN 300 462-1-1 [2], together with the following, apply:

MTIE	Maximum Time Interval Error
NE	Network Element
PDH	Plesiochronous Digital Hierarchy
PLL	Phase Locked Loop
ppm	parts per million
PRC	Primary Reference Clock
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SSU	Synchronisation Supply Unit
STM-N	Synchronous Transport Module N
TDEV	Time Deviation
UI	Unit Interval
UIpp	Unit Interval peak to peak
VCO	Voltage Controlled Oscillator

4 Frequency accuracy

Under free-running conditions, the SEC output frequency accuracy shall be within 4,6 ppm with regard to a reference traceable to a clock as specified in EN 300 462-6-1 [5].

NOTE: The time interval for this accuracy specification is for further study.

5 Pull-in and pull-out ranges

The minimum pull-in range shall be $\pm$ 4,6 ppm, whatever the internal oscillator frequency offset may be. The Pull-out range is for further study. A value of $\pm$ 4,6 ppm has been proposed.

6 Noise generation

The noise generation of a SEC represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures Maximum Time Interval Error (MTIE) and Time Deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10 Hz, first order, low-pass measurement filter, at a maximum sampling time t_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

6.1 Wander in locked mode

When the SEC is in the locked mode of operation, the MTIE and TDEV measured using the synchronised clock configuration defined in figure 1a of EN 300 462-1-1 [2] shall have the limits in tables 1 and 2, if the temperature is constant (± 1 K).

Table 1: Wander in locked mode for constant temperature specified in MTIE

Requirement	Observation interval
40 ns	$0,1 < \tau \leq 1$ s
$40\ \tau^{0,1}$ ns	$1 < \tau \leq 100$ s
$25\ \tau^{0,2}$ ns	$100 < \tau \leq 1\ 000$ s

Table 2: Wander in locked mode for constant temperature specified in TDEV

Requirement	Observation interval
3,2 ns	$0,1 < \tau \leq 25$ s
$0,64\ \tau^{0,5}$ ns	$25 < \tau \leq 100$ s
6,4 ns	$100 < \tau \leq 1\ 000$ s

The model used to derive these numbers is described in (informative) annex C. The resultant requirements are shown by the thick solid lines in figures 1 and 2.

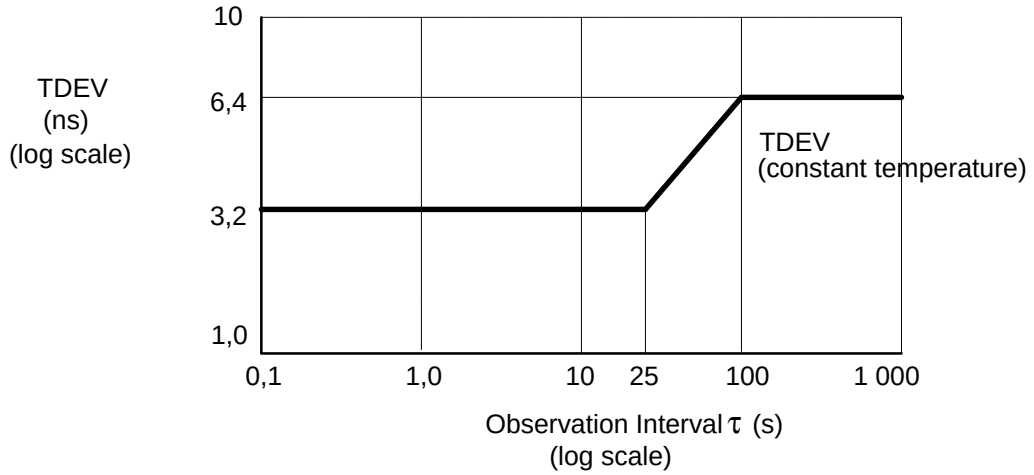


Figure 1: TDEV as a function of an observation period τ

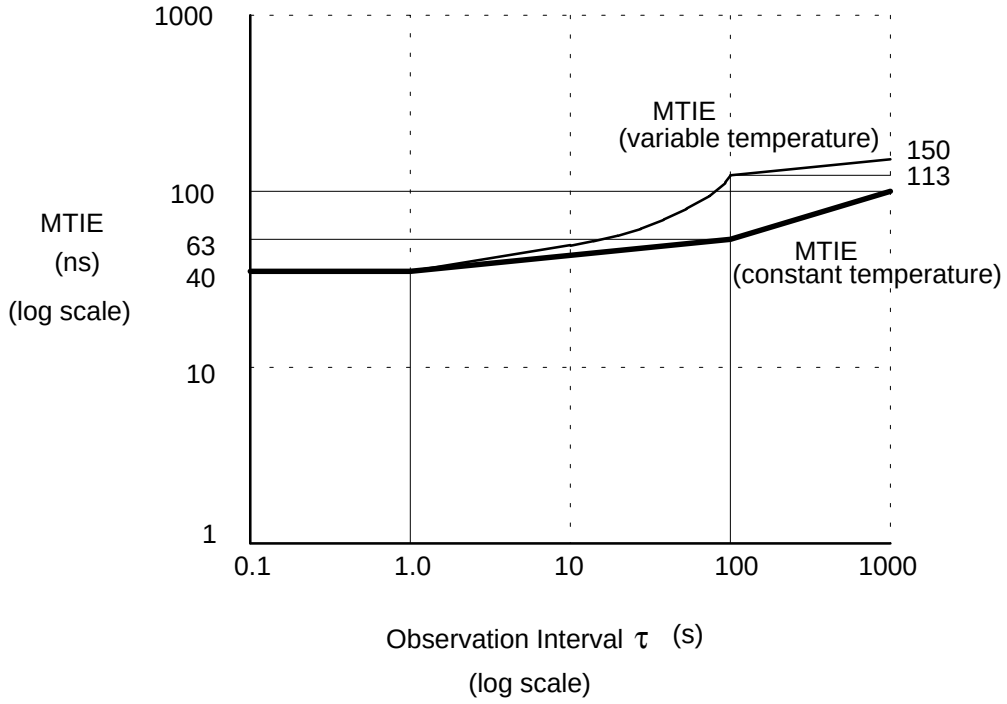


Figure 2: MTIE as a function of an observation period τ

When temperature effects are included of which the limits and rate of change are defined in ETS 300 019 [1], the allowance for the total MTIE contribution of a single SEC increases by the values in table 3.

Table 3: Additional wander in locked mode for variable temperature specified in MTIE

Requirement	Observation interval
0,5 τ ns	τ ≤ 100 s
50 ns	τ > 100 s

The resultant requirement is shown by the upper solid line in figure 2.

6.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently the non-locked wander effects are included in subclause 9.1.

6.3 Jitter

While most specifications in the present document are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation specifications shall utilize existing specifications that are currently specified differently for different interface rates. These requirements are stated separately for the interfaces identified in clause 10. To be consistent with other jitter requirements the specifications are in Unit Interval peak to peak (UIpp), where the Unit Interval (UI) corresponds to the reciprocal of the bit rate of the interface.

Due to the stochastic nature of jitter, the peak-to-peak values given in this clause eventually are exceeded. The requirements shall therefore be fulfilled with a probability of 99 %.

6.3.1 Output jitter at a 2 048 kHz and 2 048 kbit/s interface

In the absence of input jitter, the intrinsic jitter at a 2 048 kHz or 2 048 kbit/s output interface as measured over a 60 seconds interval shall not exceed 0,05 UIpp when measured through a band-pass filter with corner frequencies at 20 Hz and 100 kHz each with a first order 20 dB/decade roll-off characteristic.

6.3.2 Output jitter at a Synchronous Transport Module N (STM-N) interface

In the absence of input jitter at the synchronization interface, the intrinsic jitter at optical STM-N output interfaces as measured over a 60 seconds interval shall not exceed the limits given in table 4. The allowed jitter on an STM-1 electrical interface is for further study.

Table 4: Output jitter requirements for STM-N optical interfaces

Interface	Measuring filter (Hz)	Peak-to-peak amplitude (UI)
STM-1	500 to 1,3 M	0,50
	65 k to 1,3 M	0,10
STM-4	1 k to 5 M	0,50
	250 k to 5 M	0,10
STM-16	5 k to 20 M	0,50
	1 M to 20 M	0,10

for STM-1: 1 UI = 6,43 ns;

for STM-4: 1 UI = 1,61 ns;

for STM-16: 1 UI = 0,40 ns.

7 Noise tolerance

Noise tolerance of an SEC indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

- maintaining the clock within prescribed performance limits. The exact performance limits are for further study;
- not causing any alarms;
- not causing the clock to switch reference;
- not causing the clock to go into holdover.

In general, the noise tolerance is the same as the network limit for the synchronization interface in order to maintain acceptable performance. The jitter and wander tolerances given in subclauses 7.1 and 7.2 represent the worst levels that a synchronization carrying interface should exhibit. The requirements in subclause 7.1 have been derived by combining the most stringent requirements from each specific data interface and presenting them as a single specification which defines the performance of the SDH Equipment Clock (SEC). It is not expected that every synchronization interface should tolerate the full requirements in figure 3. Consequently when testing a specific interface (e.g. an STM-N), the interface is also bound by the jitter and wander tolerance limits defined in ITU-T Recommendations G.823 [4] and G.825 [7].

7.1 Jitter tolerance

The lower limits of maximum tolerable input jitter for signals carrying synchronization to SECs is given in figure 3 and table 5.

Table 5: Lower limit of maximum tolerable input jitter

Requirement	Frequency interval
250 ns	$1 < f \leq 19$ Hz
$4\,900\ f^{-1}$ ns	$19 < f \leq 49$ Hz
100 ns	$49 < f \leq 10^5$ Hz

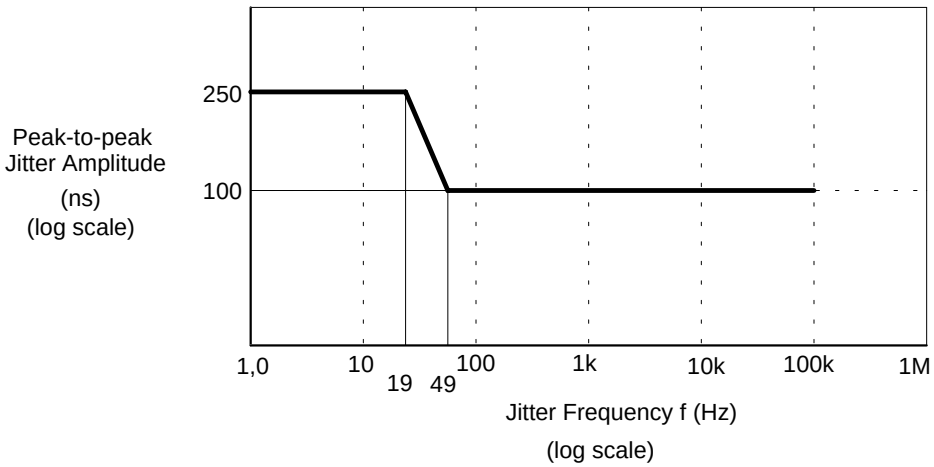


Figure 3: Lower limit of maximum tolerable input jitter

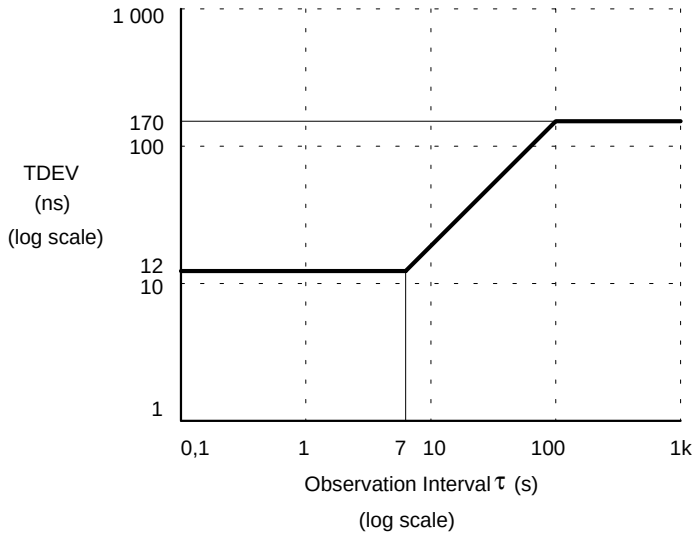
7.2 Wander tolerance

The clock shall tolerate (i.e. shall give no indication of improper operation) input wander as specified in figures 4 and 5 (and tables 6 and 7 respectively). The templates in these figures are intended to represent the cumulative network wander at the SEC input, i.e. for synchronization inputs the required wander tolerance should at least be equal to the network limit.

MTIE and TDEV are measured through an equivalent 10 Hz, first order, low-pass measurement filter, at a maximum sampling time t_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

Table 6: Input wander tolerance specified in TDEV

Requirement	Observation interval
12 ns	$0{,}1 < \tau \leq 7$ s
$1{,}7\tau$ ns	$7 < \tau \leq 100$ s
170 ns	$100 < \tau \leq 1\,000$ s

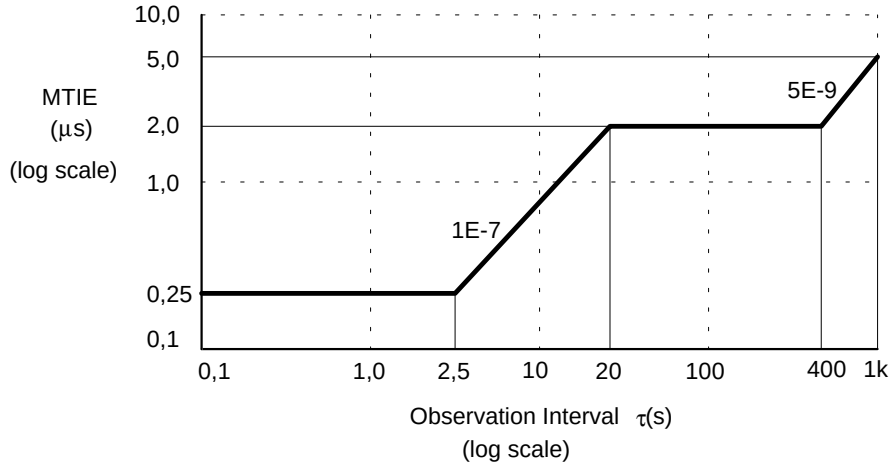


NOTE: The TDEV signal used for a conformance test should be generated by adding white, gaussian noise sources, of which each has been filtered to obtain the proper type of noise process with the proper amplitude. Annex C gives an example of a set-up to generate white and flicker phase noise.

Figure 4: Input wander tolerance (TDEV)

Table 7: Lower limit of maximum tolerable input jitter

Requirement	Observation interval
0,25 µs	0,1 < τ ≤ 2,5 s
0,1 τ µs	2,5 < τ ≤ 20 s
2 µs	20 < τ ≤ 400 s
0,005 τ µs	400 < τ ≤ 1 000 s



NOTE: The numbers next to the sloped regions indicate the relative frequency offset.

Figure 5: Input wander tolerance (MTIE)

While suitable test signals that check conformance to the masks in figure 5 are being studied, test signals with a sinusoidal phase variation can be used, according to the levels in figure 6.

Table 8: Input wander tolerance specified in sinusoidal input wander

Requirement	Frequency interval
0,0016 f^{-1} µs	0,00032 < f ≤ 0,0008 Hz
2 µs	0,0008 < f ≤ 0,016 Hz
0,032 f^{-1} µs	0,016 < f ≤ 0,13 Hz
0,25 µs	0,13 < f ≤ 10 Hz

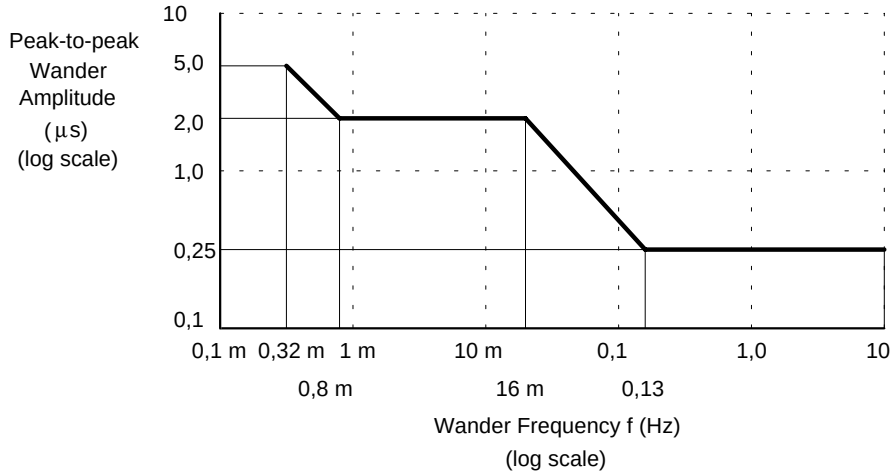


Figure 6: Lower limit of maximum tolerable sinusoidal input wander

8 Transfer characteristic

The transfer characteristic of the synchronous equipment clock determines its properties with regard to the transfer of excursions of the input phase relative to the carrier phase. The SEC can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The minimum and maximum allowed bandwidths for this low-pass filter behaviour are based on the considerations described in annex A and are specified as follows:

a) the minimum bandwidth of an SEC is 1 Hz;

b) the maximum bandwidth of an SEC is 10 Hz.

In the pass band the phase gain of the SEC is smaller than 0,2 dB (2,3 %). The above applies to a linear SEC model. However, this model should not restrict implementation. Measurement methods to determine clock transfer characteristics are described in annex B.

9 Transient response and holdover performance

The specifications in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g. short interruptions, switching between different synchronization signals, etc.) that result in phase transients at the SEC output (see clause 10). The ability to withstand specified disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

To ensure transmission integrity it is recommended that all the phase movements at the output of the SEC stay within the level described in the following clauses.

9.1 Short-term phase transient response

This specification reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously or shortly after the detection of the failure (e.g. in cases of autonomous restoration). In such cases the reference is lost for at most 15 s. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements:

The phase error should not exceed $\Delta\Phi + 5 \times 10^{-8} \times S$ seconds over any period S up to 15 s. $\Delta\Phi$ represents two phase jumps that may occur during the transition into and out of the holdover state. Each phase jump should not exceed 120 ns with a temporary offset of no more than 7,5 ppm.

The resultant overall specification is summarized in figure 7. Background information on the requirements that led to this specification are provided in annex A.

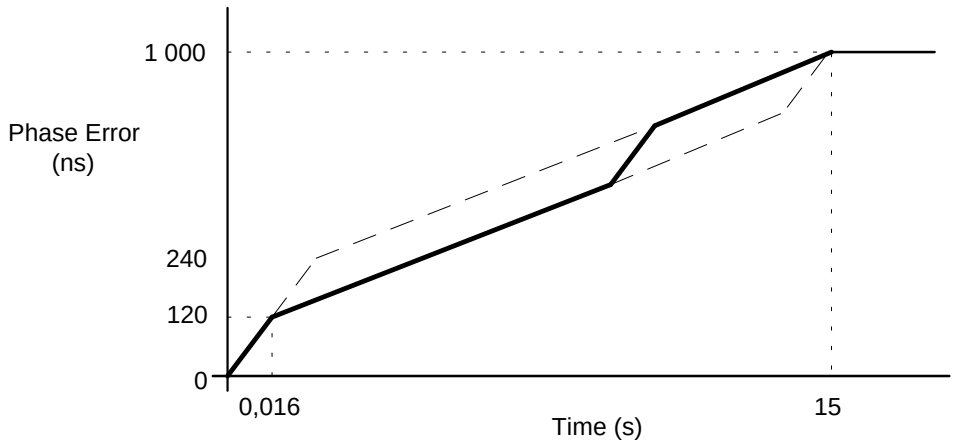


Figure 7: Maximum phase transient at the output due to reference switching

This figure is intended to depict the worst case phase movement attributable to an SEC reference clock switch. Clocks may change state more quickly than is shown here.

The figure shows two phase jumps in the clock switching transient. The first jump reflects the initial response to a loss of the synchronization reference source and subsequent entry into hold-over. The magnitude of this jump corresponds to a frequency offset less than 7,5 ppm for a duration less than 16 ms. After 16 ms, the phase movement is restricted to lie underneath the line with a slope of 5×10^{-8} in order to constrain pointer activity. The second jump, which is to take place within 15 s after entering holdover, accounts for the switching to the secondary reference. The same requirements are applicable for this jump. After the second jump the phase error should remain constant and smaller than 1 μs.

NOTE: Output phase excursion, when switching between references which are not traceable to the same Primary Reference Clock (PRC), are for further study.

In cases where the input synchronization signal is lost for more than 15 s, the specifications in subclause 9.2 apply.

9.2 Long-term phase transient response (holdover)

This specification bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

When a SEC loses its reference, it is said to enter the hold-over state. The phase error, ΔT, at the output of the SEC relative to the input at the moment of loss of reference should not, over any period of $S > 15$ s, exceed the following limit:

$$\Delta T(S) = \{(\boldsymbol{a_1} + \boldsymbol{a_2})\, S + 0{,}5\, \boldsymbol{b}\, S^2 + \boldsymbol{c}\}$$

where : $\boldsymbol{a_1} = 50$ ns/s (see note 1);

$\boldsymbol{a_2} = 2\,000$ ns/s (see note 2);

$\boldsymbol{b} = 1{,}16 \times 10^{-4}$ ns/s^2 (see note 3);

$\boldsymbol{c} = 120$ ns (see note 4).

NOTE 1: The frequency offset $\boldsymbol{a_1}$ represents an initial frequency offset corresponding to 5×10^{-8} (0,05 ppm).

NOTE 2: The frequency offset $\boldsymbol{a_2}$ accounts for temperature variations after the clock went into holdover and corresponds to 2×10^{-6} (2 ppm). If there are no temperature variations, the term $\boldsymbol{a_2}\, S$ should not contribute to the phase error.

NOTE 3: The drift $\boldsymbol{b}$ is caused by ageing: $1{,}16 \times 10^{-4}$ ns/s^2 corresponds to a frequency drift of 1×10^{-8} /day (0,01 ppm/day). This value is derived from typical ageing characteristics after 10 days of continuous operation. It is not intended to measure this value on a per day basis as the temperature effect will dominate.

NOTE 4: The phase offset $\boldsymbol{c}$ takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

This limit is subject to a maximum frequency offset of $\pm$ 4,6 ppm. The behaviour for $S < 15$ s is defined in subclause 9.1. The resultant overall requirement for constant temperature (i.e. the temperature effect is negligible) is summarized in figure 8.

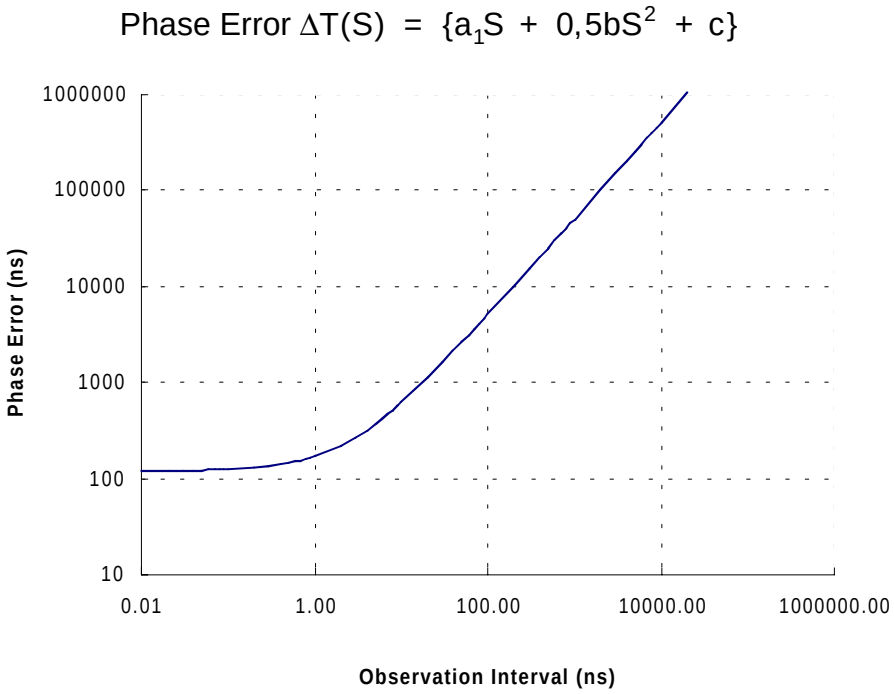


Figure 8: Permissible phase error for a SEC under holdover operation at constant temperature

9.3 Phase response to input signal interruptions

For short term interruptions on synchronization input signals, that do not cause reference switching, the output phase variation shall not exceed 120 ns, with a maximum frequency offset of 7,5 ppm for a maximum of 16 ms.

9.4 Phase discontinuity

In cases of infrequent internal testing or other internal disturbances (but excluding major hardware failures, e.g. those that would give rise to clock equipment protection switches) within the SDH equipment clock, the following conditions should be met:

- the phase variation over any period S up to 0,016 s should not exceed 7500 x S ns;
- the phase variation over any period from 16 ms up to 2,4 s should not exceed 120 ns;
- for periods greater than 2,4 s, the phase variation for each interval of 2,4 s should not exceed 120 ns with a temporary offset of no more than 7,5 ppm up to a total amount of 1 μs.

10 Interfaces

The requirements in the present document are related to reference points internal to the equipment or Network Element (NE) in which the clock is embedded and are therefore not necessarily available for measurement or analysis by the user. Therefore the performance of the SEC is not specified at these internal reference points, but rather at the external interfaces of the equipment, that are used for synchronization. The input and output interfaces specified for SDH equipment in which the SEC may be contained are:

- 2 048 kHz external interfaces according to ITU-T Recommendation G.703/§10 [6];
- 2 048 kbit/s interfaces according to ITU-T Recommendation G.703/§6 [6];
- STM-N traffic interfaces.

Note that all of the above interfaces may not be implemented on all equipment. These interfaces should comply with the additional jitter, wander and frequency accuracy requirements as defined in the present document.

Annex A (informative): Considerations on bandwidth requirements

A.1 Introduction

In locked mode a SEC will generally mimic the behaviour of an analogue, ideal, 2nd order phase locked loop. This allows us to use the terms (equivalent) 3 dB bandwidth and (equivalent) damping factor, as they are used in analogue Phase Locked Loop (PLL) theory, irrespective of the fact that in the implementation of a SEC, digital and/or non-linear techniques may be used.

In this annex the considerations on the choice of equivalent bandwidth are discussed, given the constraints imposed by the stated requirements and assumptions.

A.2 Relevant network requirements and assumptions

A.2.1 ITU-T Recommendation G.825 STM-N jitter acceptance

Table 2 of ITU-T Recommendation G.825 [7] states that the tolerance for jitter on the STM-4 signal decreases linearly along a 7,5 ppm slope between A2 (0,25 μs) and A3 (1,5 UI) levels. The STM-4 case is the most restrictive in this respect. In the cases of STM-1 and STM-16 the specifications are 15,2 ppm and 9,5 ppm respectively.

This requirement leads directly to an upper limit for the SEC bandwidth. When the SEC switches reference it will experience a phase jump on its input, because in general the phases of the various references are uncorrelated. Such jumps may lead to a phase jump on the output with a magnitude of at most 120 ns. The jumps are shown in figure A.2. Their magnitude of 120 ns is between the A2 and A3 levels in table 2 of ITU-T Recommendation G.825 [7] and hence the 7,5 ppm limit applies. In other words it shall take at least 16 ms to reach the 120 ns phase offset at the output. A time constant of 16 ms corresponds to a bandwidth of at most 10 Hz in a PLL model with a reasonable damping factor (e.g. larger than 3).

A.2.2 Wander accumulation in a synchronization distribution chain

The choice of bandwidth for the SEC needs to consider the worst case synchronization reference chain as specified in figure 5 of EN 300 462-2-1 [3]. To limit the wander accumulation, the bandwidth ratio between the SEC and the Synchronisation Supply Unit (SSU) shall be large enough. An upper limit for the bandwidth of an SSU like clock is given in ITU-T Recommendation Q.551 [8] to be 0,1 Hz. This assumption leads to the consideration that the SEC bandwidth should be at least 1 Hz. If the SSU/SEC bandwidth ratio is sufficiently large, only a fraction of the chain according to figure A.1 has to be considered for the noise contribution of the SECs to the noise at the output of the synchronization chain.

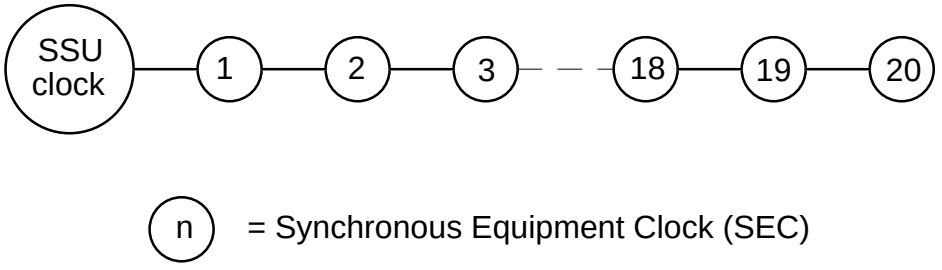


Figure A.1: Synchronisation reference chain

Simulations have been carried out using standard clock recovery device models. The simulation results show that the output noise is predominantly determined by the SEC, and that increasing the bandwidth of the SEC significantly reduces the jitter and wander produced by the chain. This leads to a minimum bandwidth requirement in the order of 1 Hz.

A.2.3 Phase transients due to automatic timing restoration

The reference chain of figure 5 of EN 300 462-2-1 [3] shows that a path carrying synchronization through the network may contain up to 10 SSUs and 60 SECs. Since the wander on such a synchronization distribution trail is limited to 5 µs (determined by the network limit for wander at SEC outputs with an observation interval of 86 400 seconds) it is necessary to limit phase transients that are the consequence of automatic timing restoration in a chain of SECs.

A value of 1 µs is assumed as the upper limit for such a phase transient. Moreover, if phase transients stay below 1 µs, the SEC chain shows the same MTIE performance as a single SSU. Such a practice avoids the risk that the downstream SSU generates an alarm or performs reference switching due to a bad input, since it may be assumed that SSUs in general can accept the 1 µs transients that may be generated by the upstream SSU.

From the 1 µs requirement a lower limit of the SEC bandwidth can be deduced, by considering the restoration time of a SEC chain and the holdover accuracy of the SEC. Given that two phase jumps with a contribution of 120 ns each may be needed to switch to and from holdover, there are 15 s to operate with an inaccuracy of 50 ns/s (0,05 ppm) and still stay within the 1 µs phase transient limit (see figure A.2, based on figure 7 of the present document).

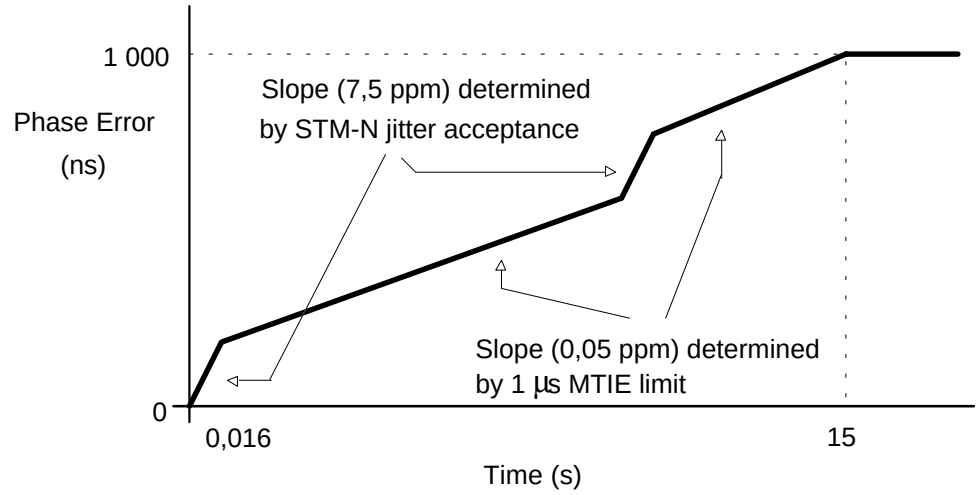


Figure A.2: SEC output phase under reference switching

This imposes a trade-off between the processing time of the synchronization status messages that trigger the timing restoration, and the bandwidth of the SECs. Simulations have shown that to allow for switching processing times in the order of 200 ms - 600 ms a minimum bandwidth of the SEC of 1 Hz is required.

This simulation was done on the longest chain (20) of SECs in a ring. The 1 000 ns phase transient limit is reached only in one SEC of the ring when the failure is located in a specific location on the ring. Furthermore, the simulation assumed that each switch in each node gives rise to the maximum phase step of + 120 ns.

A.3 Conclusion

In summary the requirements listed above lead to the following bandwidth constraints for the SEC in table A.1.

Table A.1: SEC bandwidth constraints

Requirement	Resulting SEC bandwidth constraint (Hz)
ITU-T Recommendation G.825 [7] STM-N jitter acceptance	< 10
Wander accumulation in a synchronization distribution chain; SSU/SEC bandwidth ratio	> 1
Wander accumulation in a synchronization distribution chain; SEC accumulation	> 1
1 µs maximum phase transients due to automatic timing restoration	> 1

From this it is concluded that the bandwidth of the SEC should be in the range 1 Hz to 10 Hz.

Annex B (informative): Measurement methods for transfer characteristics

To measure the transfer characteristics of the SEC several equivalent measurement methods are listed. The difficulty in measuring the phase transfer characteristic is that the (phase) signals that are transferred through the clock have to be substantially larger than the internally generated phase noise. This may require large input phase deviations, which may cause overflow of the phase detector or may throw the SEC into holdover. Such events would make the measurement worthless. Depending on the particular implementation of an SEC, different methods of measuring may be appropriate to measure the transfer characteristic. Relevant factors are the amount of internally generated phase noise, the amount of internally generated frequency noise, the size of the phase step that the phase detector can absorb and the conditions that throw the clock into holdover (which possibly can be switched off).

Five methods are suggested to measure the transfer characteristics of the SEC, but it should be noted that it may be possible to pass one method and not another. This requires further study. The most appropriate may be chosen.

a) phase step at the input;

b) frequency step at the input;

c) sinusoidal signals at the input;

d) white phase noise at the input (frequency domain);

e) white phase noise at the input (time domain).

NOTE: All values mentioned in this annex are proposed values and are subject to further study.

B.1 Phase step response

This method is suitable for designs that can accept large phase transients or have a low internal noise level. As an input signal a "sloped" phase step is proposed, according to figure B.1. The size of the phase step, ΔT, shall be larger than 20 times the internal phase noise, X, over the measurement time T to overcome the internal noise (X = MTIE(T)). The rise-time τ is chosen to be at least 10 times faster than the fastest desired result.

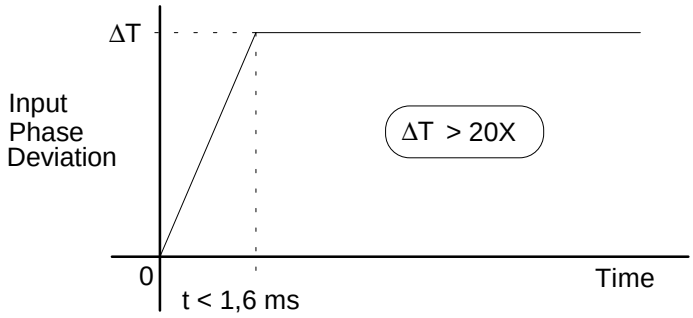


Figure B.1: Phase step to be applied at the input

The resultant output mask is given in figure B.2. The steep slope corresponds with a 10 Hz equivalent bandwidth and the faint slope with a 1 Hz equivalent bandwidth. There is room for 0,2 dB overshoot
($\cong$ 2,3 %), corresponding to an equivalent damping factor $\varsigma > 3$.

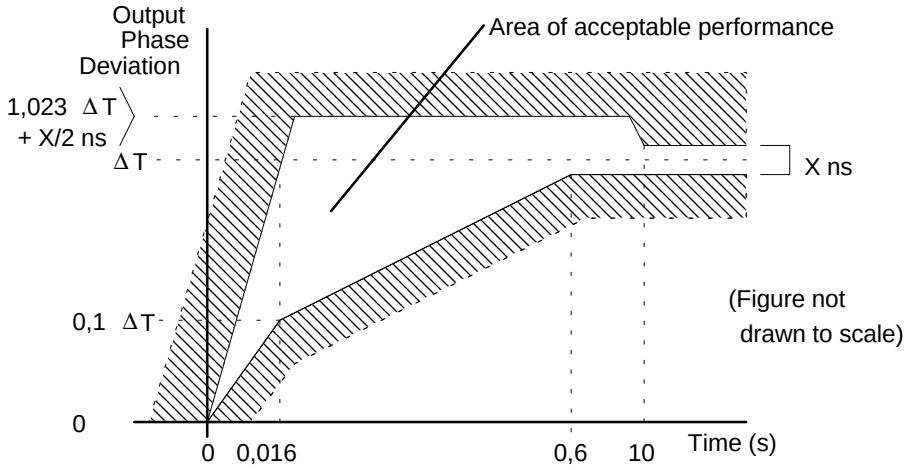


Figure B.2: Response to a phase step at the input

B.2 Frequency step response

This method may in some designs avoid throwing the SEC in holdover or overflowing the phase detector. If the maximum instantaneous frequency deviation of the SEC is Y ppm, then a frequency step $\Delta f = 20Y$ is adequate to determine the frequency step response. The resulting frequency response is given by figure B.3.

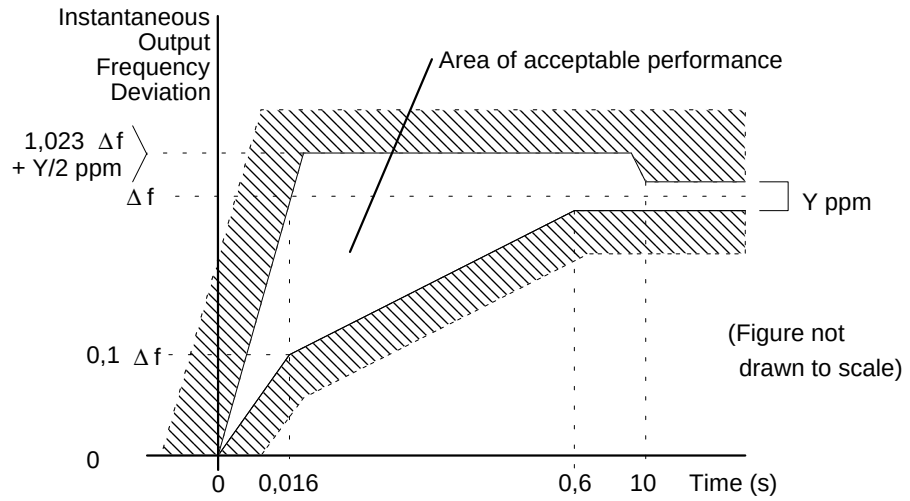


Figure B.3: Response to a frequency step at the input

B.3 Sinusoidal phase response

Designs that are largely of linear nature can be tested by measuring the response to sinusoidal phase variations. This has the advantage that the output can be measured in a frequency selective way. Consequently, the internal noise of the clock is not a big contributor. The transfer characteristics can be directly measured in the frequency domain. The response is shown in figure B.4.

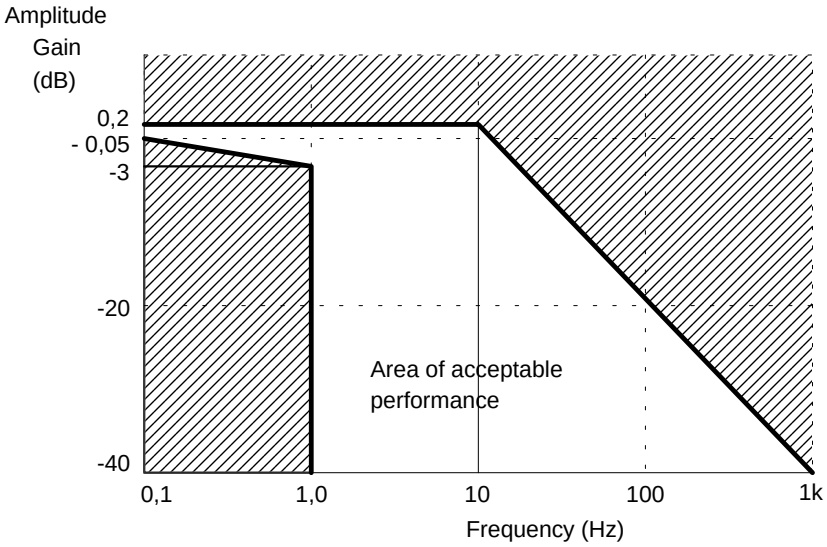


Figure B.4: Response to sinusoidal jitter input

B.4 White phase noise response (frequency domain)

The response to white phase noise (flat between 0,1 Hz and 100 Hz) can also be used to characterize the response of the SEC. The output noise level is measured in a frequency selective way while the input is kept constant. This means that non-linear effects are also captured which makes this method also suitable for non-linear applications. However the applied noise level needs to be considerably larger than the internally generated amount of noise. The output shall satisfy figure B.5.

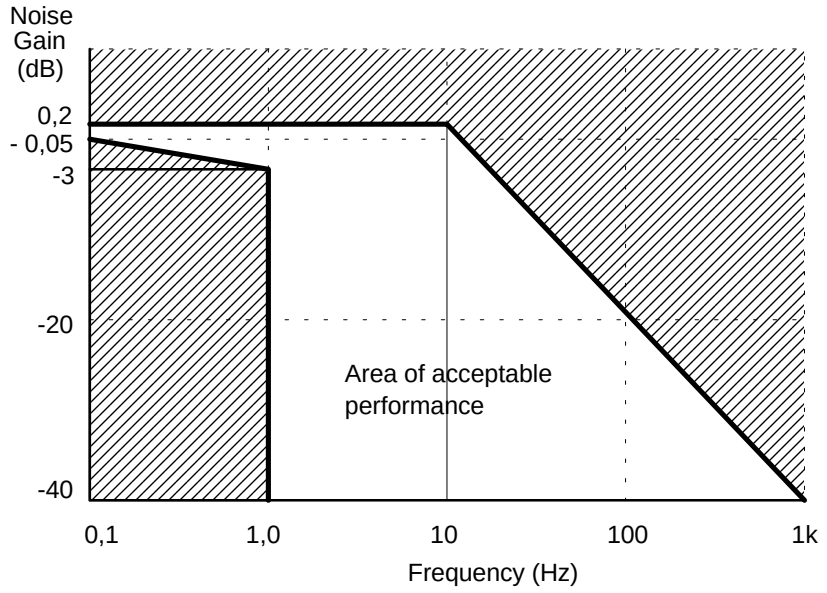


Figure B.5: Response to white phase noise at the input

B.5 White phase noise response (time domain)

The response to white phase noise (flat between 0,1 Hz and 100 Hz) can also be used to charaterize the response of an SEC in the time domain, using a set-up as in figure B.6.

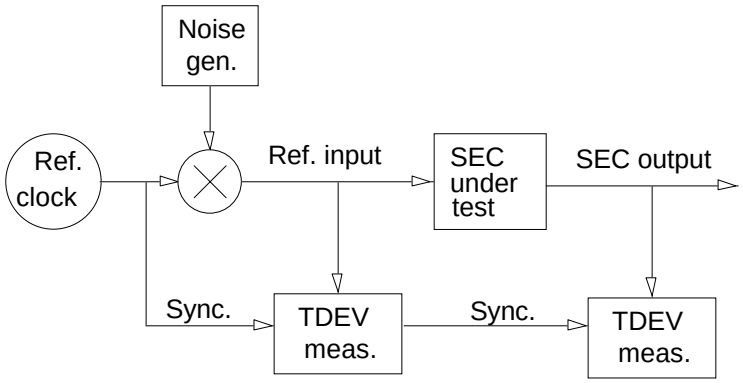


Figure B.6: Measurement set-up for TDEV transfer characteristics

The plots of the TDEV input and output curves should look something like figure B.7. The usefulness of this method and the exact relationship between the cut-off point in figure B.7 and the actual bandwidth of the clock need more study. The advantage of this method is that no noise source has to be used that produces noise with a prescribed TDEV characteristic.

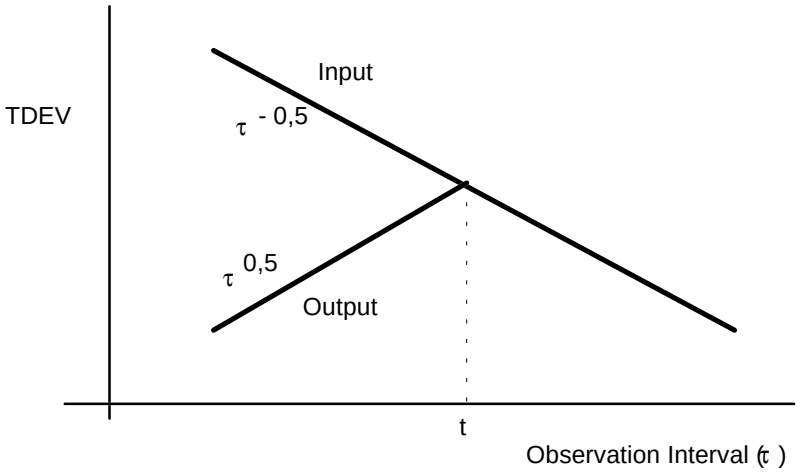


Figure B.7: Input and Output TDEV curves for transfer measurement

Annex C (informative): Information on the SEC noise model

The model of the SEC given below is derived from the well known PLL block schematic of which the most important output noise sources (white phase noise and flicker phase noise) have been extracted and been modelled on their own. The upper noise source, together with the filter bank A, which has approximately a $f^{-0,5}$ behaviour in the frequency range of interest, generates the flicker phase noise and the lower noise source generates the white phase noise. Gain blocks I and II are used to control the relative strength of both sources. Filters B and C model the filtering by the PLL itself (first order low-pass and high-pass filters, respectively between 1 Hz and 10 Hz).

This simplified clock model reflects the impact of sources injecting noise in the loop of the PLL at points before the Voltage Controlled Oscillator (VCO) and at points after the VCO.

All MTIE and TDEV curves that can be generated with this model by varying gain I, gain II and β fall below the MTIE and TDEV curves given in figures 1 and 2. The consistency between TDEV and MTIE mask is achieved by making reference to a completely defined model of the power spectral density of the phase noise at the output of the PLL.

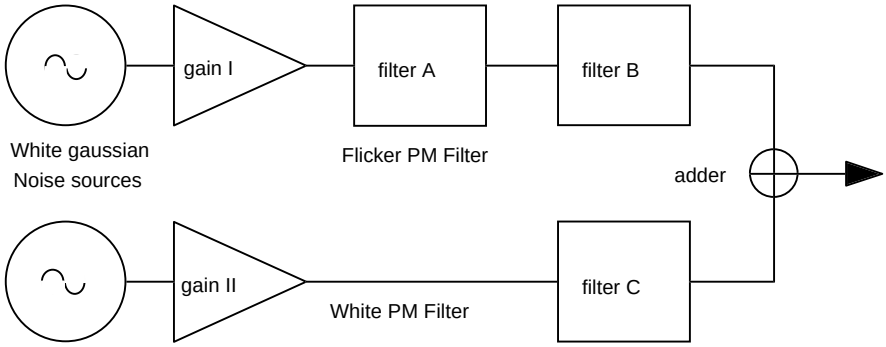


Figure C.1: Simple model for SEC noise generation

Noise sources: Gaussian random samples with zero mean and unit standard deviation (ns).

Where:

$$FilterA = \prod_{n=1}^{8} \frac{1}{\sqrt{7}} \times \frac{s + \alpha_n \sqrt{7}}{s + \alpha_n}$$

$$FilterB = \frac{\beta}{s + \beta}$$ (Low Pass filter)

$$FilterC = \frac{s}{s + \beta}$$ (High Pass filter)

$$\frac{\alpha_{n+1}}{\alpha_n} = 7$$

$\alpha_8 = 2\ \pi$ x 6,72

$\beta = 2\ \pi$ x 1 ... $2\ \pi$ x 10

gain I = 0,3.....3,0 (provisional value)

gain II = 0,275 ..... 0,875 (provisional value)

Bibliography

- EN 300 462-3-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks".

History

Document history				
Edition 1	May 1995	Public Enquiry as ETS 300 462-5	PE 84:	1995-05-22 to 1995-09-15
Edition 1	May 1996	Vote as ETS 300 462-5	V 102:	1996-05-06 to 1996-08-09
Edition 1	September 1996	Publication as ETS 300 462-5		
V1.1.2	May 1998	Publicaton (Converted to EN 300 462-5-1)		

ISBN 2-7437-2202-9
Dépôt légal : Mai 1998