EN 300 462-4-1 V1.1.1 (1998-05)

European Standard (Telecommunications series)

**Transmission and Multiplexing (TM);
Generic requirements for synchronization networks;
Part 4-1: Timing characteristics of slave clocks
suitable for synchronization supply to
Synchronous Digital Hierarchy (SDH)
and Plesiochronous Digital Hierarchy (PDH) equipment**

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Contents

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Foreword

This European Standard (Telecommunications series) has been produced by the Transmission and Multiplexing (TM) Technical Committee.

The present document has been produced to provide requirements for synchronization networks that are compatible with the performance requirements of digital networks. It is one of a family of documents covering various aspects of synchronization networks:

Part 1-1: "Definitions and terminology for synchronization networks";

Part 2-1: "Synchronization network architecture";

Part 3-1: "The control of jitter and wander within synchronization networks";

Part 4-1: "Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment";

Part 4-2: "Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment Implementation Conformance (ICS) Statement";

Part 5-1: "Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment";

Part 6-1: "Timing characteristics of primary reference clocks";

Part 6-2: "Timing characteristics of primary reference clocks Implementation Conformance (ICS) Statement";

Part 7-1: "Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications".

Parts 1-1, 2-1, 3-1 and 5-1 have previously been published as ETS 300 462 Parts 1, 2, 3 and 5, respectively.

Additionally, parts 4-1 and 6-1 completed the Voting phase of the Two Step Approval procedure as ETS 300 462 Parts 4 and 6, respectively.

It was decided to prepare ICS proformas for several of the parts and this necessitated a re-numbering of the individual document parts. It was also decided to create a new part 7-1.

This in turn led to a need to re-publish new versions of all six parts of the original ETS. At the same time, the opportunity was taken to convert the document type to EN.

This has involved no technical change to any of the documents. However part 5-1 has been modified, due to editorial errors which appeared in ETS 300 462-5.

National transposition dates	
Date of adoption of this EN:	22 May 1998
Date of latest announcement of this EN (doa):	31 August 1998
Date of latest publication of new National Standard or endorsement of this EN (dop/e):	28 February 1998
Date of withdrawal of any conflicting National Standard (dow):	28 February 1998

1 Scope

This European Standard (Telecommunications series) outlines requirements for timing devices called Synchronization Supply Units (SSUs) used in synchronizing network equipment in the Synchronous Digital Hierarchy (SDH) transport network and the Public Switched Telephone Network (PSTN) network.

NOTE 1: The requirements in the present document apply under environmental conditions according to one of the environmental classes defined in ETS 300 019 [1], unless stated otherwise. The manufacturer will need to specify to which specific environmental class an equipment belongs.

A description of the Synchronization Supply Unit (SSU) logical function is given in figure 1 in EN 300 462-2-1 [3]. In general, the SSU will have multiple timing reference inputs and in the event that all timing references fail, the SSU should be capable of maintaining operation (holdover) within prescribed performance limits as detailed in the present document. The requirements laid down in the present document decribe the minimum performance of an SSU applied as a transit node clock. It is recognized that local node clock applications for SSU's exist, requiring different parameters. Those are for further study.

NOTE 2: There can be situations in which more stringent requirements are applicable, for instance, in cases where an SSU has only one independent reference (e.g. due to limitations in the network topology).

The SSU function can be implemented in a separate piece of equipment called a Stand-Alone Synchronization Equipment (SASE) or it can form a logical function of another equipment such as a telephony exchange or an SDH cross-connect.

The requirements specified in the present document refer to the design of new synchronization networks and consequently they do not necessarily represent the performance of existing synchronization networks and equipment.

A timing device within SDH equipment can also conform to EN 300 462-5-1 [5].

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, subsequent revisions do apply.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] ETS 300 019: "Equipment Engineering (EE); Environmental conditions and environmental tests for telecommunications equipment".

[2] EN 300 462-1-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1-1: Definitions and terminology for synchronization networks".

[3] EN 300 462-2-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2-1: Synchronization network architecture".

[4] EN 300 462-3-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks".

[5] EN 300 462-5-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[6] EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[7] ETS 300 166: "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2 048 kbit/s-based pleisiochronous or synchronous digital hierarchies".

[8] ITU-T Recommendation G.825: "The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)".

[9] ITU-T Recommendation G.823: "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".

3 Definitions, abbreviations and symbols

3.1 Definitions

For the purposes of the present document, the definitions given in EN 300 462-1-1 [2] apply.

3.2 Abbreviations

For the purposes of the present document, the abbreviations given in EN 300 462-1-1 [2], together with the following, apply:

MTIE Maximum Time Interval Error
NE Network Element
PDH Plesiochronous Digital Hierarchy
PLL Phase Locked Loop
ppm parts per million
PSTN Public Switched Telephone Network
SASE Stand Alone Synchronization Equipment
SDH Synchronous Digital Hierarchy
SEC SDH Equipment Clock
SSU Synchronization Supply Unit
STM-N Synchronous Transport Module-N
TDEV Time DEViation
UI Unit Interval
UIpp Unit Interval peak to peak
VCO Voltage Controlled Oscillator

3.3 Symbols

For the purposes of the present document, the following symbols apply:

K Kelvin
τ Tau

4 Frequency accuracy

The long term frequency accuracy normally applies when operating in long term free running conditions. Since the SSU is a slave clock, then the normal operating modes are either locked or holdover. The frequency accuracy specification in holdover mode is specified in clause 9.

5 Pull-in and pull-out ranges

The minimum pull-in range shall be ± 0,01 ppm, whatever the internal oscillator frequency offset may be. The pull-out range is for further study.

6 Noise generation

The noise generation of an SSU represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures Maximum Time Interval Error (MTIE) and Time Deviation (TDEV) are useful for characterization of noise generation performance.

For observation intervals, τ, between 0,1 s and 10 000 s, MTIE and TDEV are measured through an equivalent 10 Hz, first order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period, T, for TDEV is twelve times the observation interval ($T = 12\tau$). Further guidance is provided in clause A.2 of EN 300 462-3-1 [4].

6.1 Wander in locked mode

When the SSU is in the locked mode of operation, the MTIE and TDEV measured using the synchronized clock configuration defined in figure 1a) of EN 300 462-1-1 [2] shall have the limits in tables 1 and 2, if the temperature is constant (± 1 K).

Table 1: Wander in locked mode for constant temperature specified in TDEV

Requirement	Observation interval
3 ns	$0,1 < \tau \leq 25$ s
$0,12\tau$ ns	$25 < \tau \leq 100$ s
12 ns	$100 < \tau \leq 10\,000$ s

Table 2: Wander in locked mode for constant temperature specified in MTIE

Requirement	Observation interval
24 ns	$0,1 < \tau \leq 9$ s
$8\tau^{0,5}$ ns	$9 < \tau \leq 400$ s
160 ns	$400 < \tau \leq 10\,000$ s

The model used to derive these numbers is described in (informative) annex A. The resultant requirements are shown by the thick solid lines in figures 1 and 2.

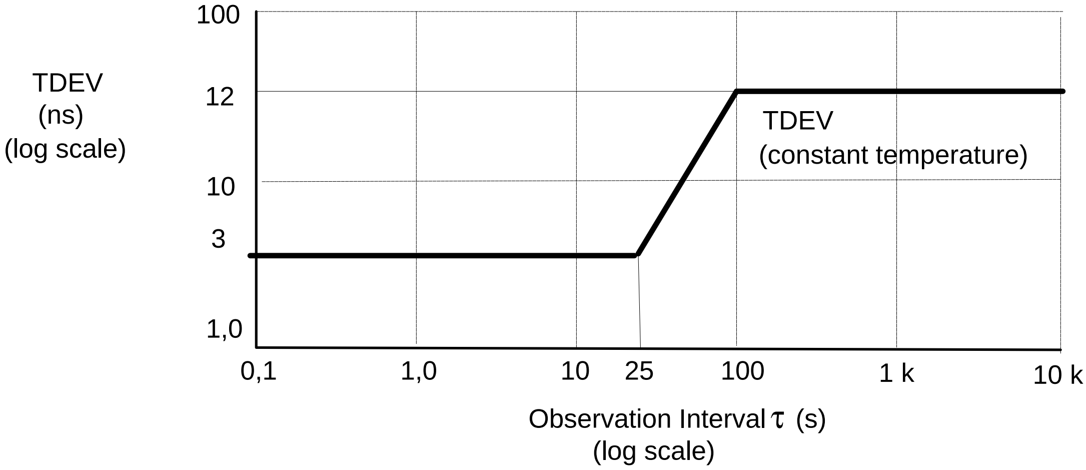


Figure 1: TDEV as a function of an observation interval τ

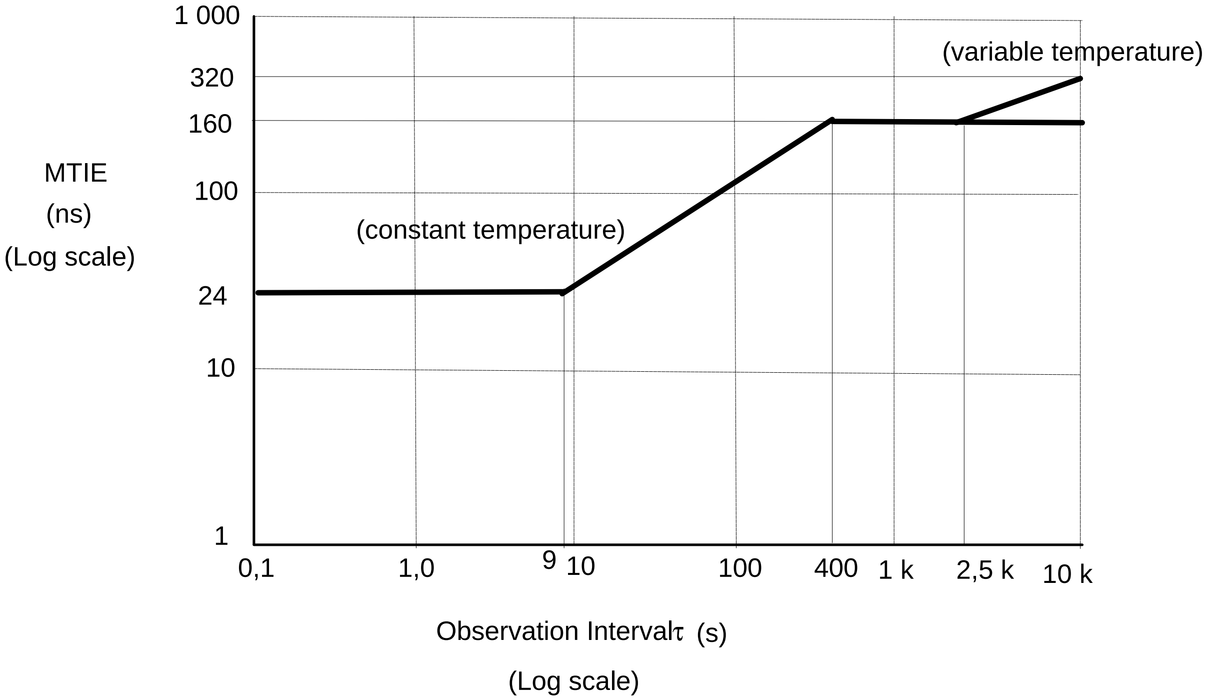


Figure 2: MTIE as a function of an observation interval τ

When temperature effects are included of which the limits and rate of change are defined in ETS 300 019 [1], corresponding to the environmental class to which the equipment belongs, the allowance for the total MTIE contribution of a single SSU is given by the values in table 3.

Table 3: Total wander in locked mode for variable temperature specified in MTIE

Requirement	Observation interval
$3,2 \times \tau^{0,5}$	2 500 to 10 000 s

NOTE: For observation intervals greater than 10 000 s the MTIE is expected not to exceed 320 ns.

The resultant requirement is shown by the upper solid line in figure 2.

6.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently the non-locked wander effects are included in subclause 9.2.

6.3 Jitter

While most specifications in the present document are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation specifications shall utilize existing specifications that are currently specified differently for different interface rates. These requirements are stated separately for the interfaces identified in clause 10. To be consistent with other jitter requirements the specifications are in Unit Interval peak to peak (UIpp), where the Unit Interval (UI) corresponds to the reciprocal of the bit rate of the interface.

Due to the stochastic nature of jitter, the peak-to-peak values given in this clause eventually are exceeded. The requirements shall therefore be fulfilled with a probability of 99 %.

6.3.1 Output jitter at a 2 048 kHz and 2 048 kbit/s interface

In the absence of input jitter, the intrinsic jitter at a 2 048 kHz or 2 048 kbit/s output interface as measured over a 60 seconds interval shall not exceed 0,05 UIpp when measured through a band-pass filter with corner frequencies at 20 Hz and 100 kHz each with a first order 20 dB/decade roll-off characteristic.

6.3.2 Output jitter at a Synchronous Transport Module N (STM-N) interface

In the absence of input jitter at the synchronization interface, the intrinsic jitter at STM-N output interfaces as measured over a 60 seconds interval shall not exceed the limits given in table 4.

Table 4: Output jitter requirements for STM-N interfaces

Interface	Measuring filter (Hz)	Peak-to-peak amplitude (UI)
STM-1 electrical	500 to 1,3 M	0,50
	65 k to 1,3 M	0,075
STM-1 optical	500 to 1,3 M	0,50
	65 k to 1,3 M	0,10
STM-4	1 k to 5 M	0,50
	250 k to 5 M	0,10
STM-16	5 k to 20 M	0,50
	1 M to 20 M	0,10
NOTE: for STM-1: 1 UI = 6,43 ns; for STM-4: 1 UI = 1,61 ns; for STM-16: 1 UI = 0,40 ns.		

7 Noise tolerance

Noise tolerance of an SSU indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

- maintaining the clock within prescribed performance limits in locked mode of operation;
- not causing any alarms;
- not causing the clock to switch reference;
- not causing the clock to go into holdover.

In general, the noise tolerance is the same as the network limit for the synchronization interface in order to maintain acceptable performance. The jitter and wander tolerances given in subclauses 7.1 and 7.2 represent the worst levels that a synchronization carrying interface should exhibit.

NOTE: Clocks may be used to monitor, in-service, the phase noise on an incoming timing reference signal. For such purposes different observation intervals and sampling times can be used. Guidance is provided in clause A.2 of EN 300 462-3-1 [4].

The requirements in subclause 7.1 have been derived by combining the most stringent requirements from each specific data interface and presenting them as a single specification which defines the performance of the SSU. It is not expected that every synchronization interface should tolerate the full requirements in figure 3. Consequently when testing a specific interface (e.g. an STM-N), the interface is also bound by the jitter and wander tolerance limits defined in ITU-T Recommendations G.823 [9] and G.825 [8].

For observation intervals of 0,1 s to 10 000 s, MTIE and TDEV shall be measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period T for TDEV is twelve times the observation interval τ.

7.1 Jitter tolerance

The lower limits of maximum tolerable input jitter for signals carrying synchronization to SSUs is given in table 5 and figure 3.

Table 5: Lower limit of maximum tolerable input jitter

Requirement	Frequency interval
750 ns	0,001 kHz < f ≤ 2,4 kHz
$1,8 \times 10^6 f^{-1}$ ns	2,4 < f ≤ 18 kHz
100 ns	18 < f ≤ 100 kHz

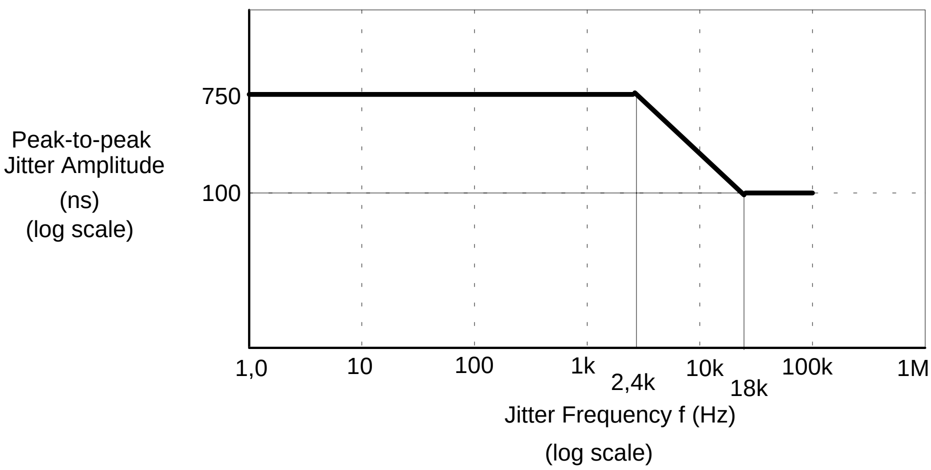


Figure 3: Lower limit of maximum tolerable input jitter

7.2 Wander tolerance

The clock shall tolerate (i.e. shall give no indication of improper operation) input wander as specified in figures 4 and 5 (tables 6 and 7 respectively). The templates in these figures are intended to represent the cumulative network wander at the SSU clock input, i.e. for synchronization inputs the required wander tolerance is equal to the maximum expected network limit in the field.

For observation intervals of 0,1 s to 10 000 s, MTIE and TDEV shall be measured through an equivalent 10 Hz , first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period T for TDEV is twelve times the observation interval τ.

Table 6: Input wander tolerance specified in TDEV

Requirement	Observation interval
34 ns	$0,1 < \tau \leq 20$ s
$1,7\tau$ ns	$20 < \tau \leq 100$ s
170 ns	$100 < \tau \leq 1\,000$ s
$5,4\tau^{0,5}$ ns	$1\,000 < \tau \leq 10\,000$ s

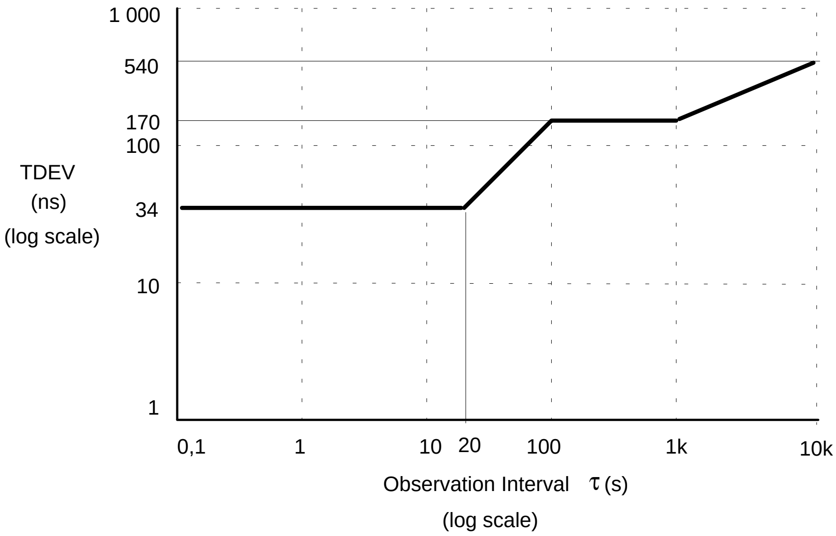
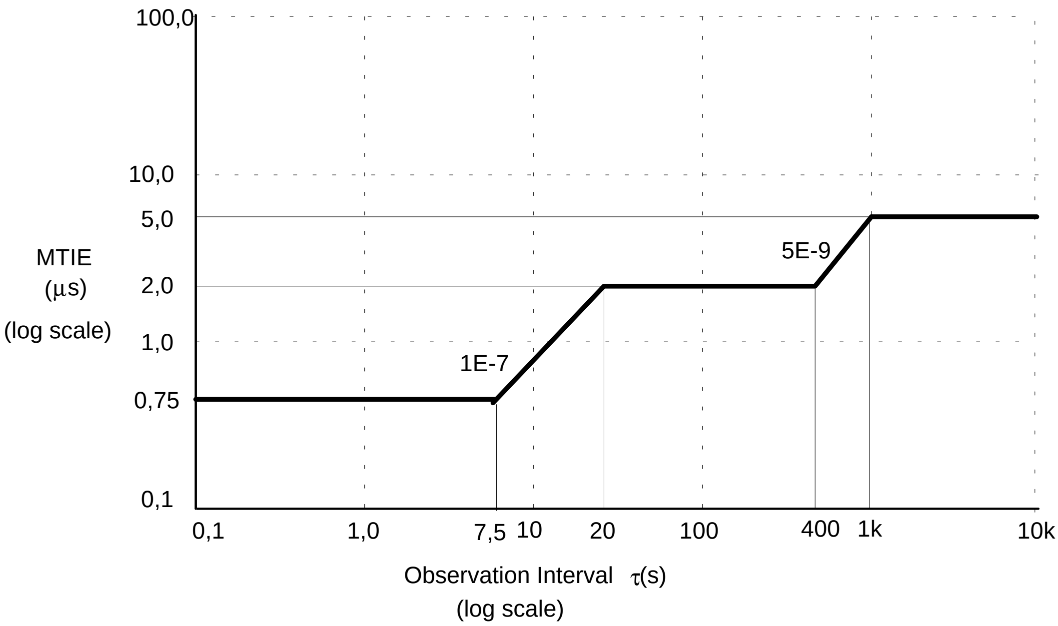


Figure 4: Input wander tolerance (TDEV)

Table 7: Input wander tolerance (MTIE)

Requirement	Observation interval
0,75 µs	$0,1 < \tau \leq 7,5$ s
$0,1\tau$ µs	$7,5 < \tau \leq 20$ s
2 µs	$20 < \tau \leq 400$ s
$0,005\tau$ µs	$400 < \tau \leq 1\,000$ s
5 µs	$1\,000 < \tau \leq 10\,000$ s



NOTE: The numbers next to the sloped regions indicate the relative frequency offset.

Figure 5: Input wander tolerance (MTIE)

While suitable test signals that check conformance to the masks in figure 5 are being studied, test signals with a sinusoidal phase variation can be used, according to the levels in table 8 and figure 6.

Table 8: Input wander tolerance specified in sinusoidal input wander

Requirement	Frequency interval
5 μs	0,000 012 < f ≤ 0,00 032 Hz
0,0 016 f^{-1} μs	0,00 032 < f ≤ 0,0 008 Hz
2 μs	0,0 008 < f ≤ 0,016 Hz
0,032 f^{-1} μs	0,016 < f ≤ 0,043 Hz
0,75 μs	0,043 < f ≤ 1 Hz

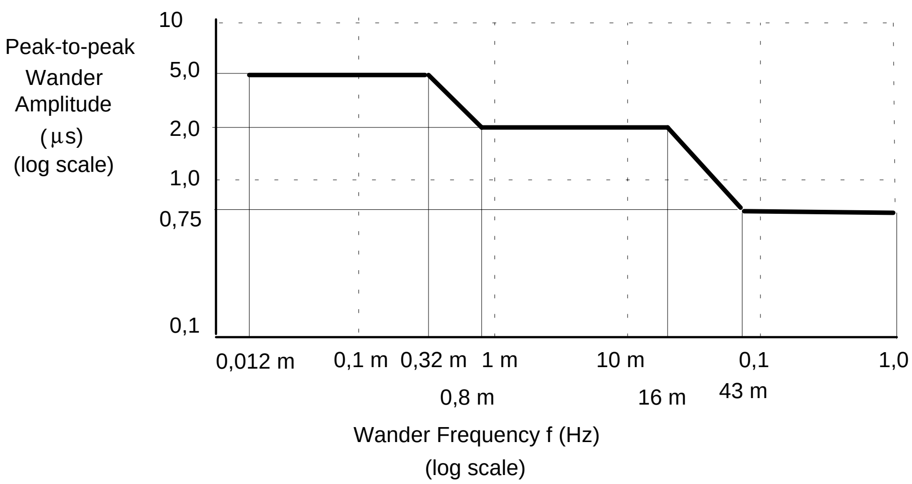


Figure 6: Lower limit of maximum tolerable sinusoidal input wander

8 Transfer characteristic

The transfer characteristic of the SSU determines its properties with regard to the transfer of excursions of the input phase relative to the phase modulation. Noise transfer can be described in two ways:

a) the SSU can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The allowed bandwidth for this low-pass filter behaviour is:

- the maximum bandwidth of an SSU is 3 mHz;
- there is no limit specified for the minimum bandwidth.

In the pass band the phase gain of the SSU shall be smaller than 0,2 dB (2,3 %).

b) noise transfer describes the amount of noise impairment observed at the output, as a result of noise introduced at the input of the clock. The SSU clock, when subjected to a wideband noise signal shaped as prescribed in subclause 7.2 (i.e. the TDEV input tolerance specification), shall produce an output signal that lies within the limits specified in table 9 and figure 7. The model that can be used to derive these numbers is described in annex A.

NOTE: The output wander mask includes both intrinsic noise and pass-band phase gain.

Guidance on the measurement techniques for these requirements is given in annex B of EN 300 462-5-1 [5].

For observation intervals of 0,1 s to 10 000 s, MTIE and TDEV shall be measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period T for TDEV is twelve times the observation interval τ.

Table 9: Output wander mask specified in TDEV

Requirement	Observation interval
3 ns	$0,1 < \tau \leq 13,1$ s
$0,0176\tau^2$ ns	$13,1 < \tau \leq 100$ s
176 ns	$100 < \tau \leq 1000$ s
$5,58\tau^{0,5}$ ns	$1000 < \tau \leq 10000$ s

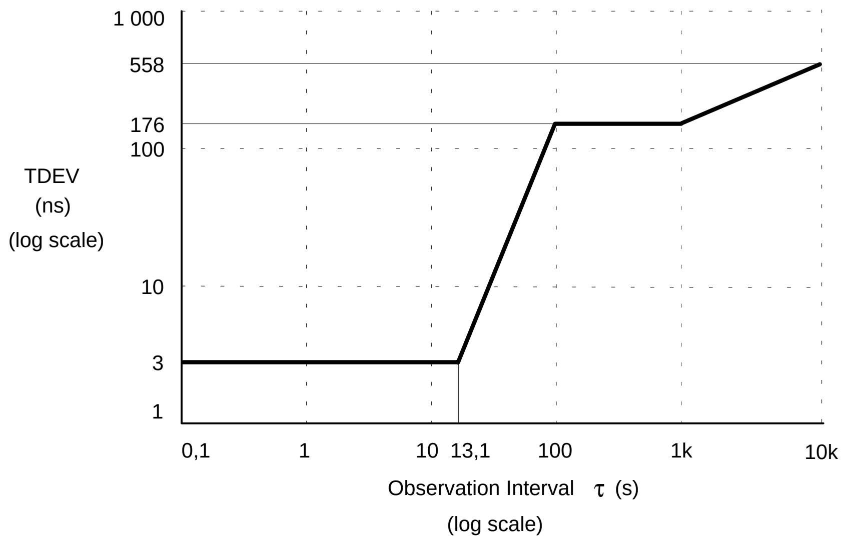


Figure 7: Output wander mask (TDEV)

9 Transient response and holdover performance

The specifications in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g. short interruptions, switching between different synchronization signals, etc.) that result in phase transients at the SSU output (see clause 10). The ability to withstand specified disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

To ensure transmission integrity it is recommended that all the phase movements at the output of the SSU stay within the level described in the following clauses.

9.1 Phase response during input reference switching

This specification reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously or shortly after the detection of the failure (e.g. in cases of autonomous restoration). The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements.

The phase error should not exceed 240 ns over the period T_y between the loss of reference and locking to an alternative reference. During T_y two phase jumps are allowed that may occur upon loss of the current reference and the locking to a new reference. Each phase jump should not exceed 60 ns, with a temporary offset of no more than 7,5 ppm. During the rest of the duration of T_y, the frequency offset shall not exceed 5×10^{-10}.

The resultant overall specification is summarized in figure 8.

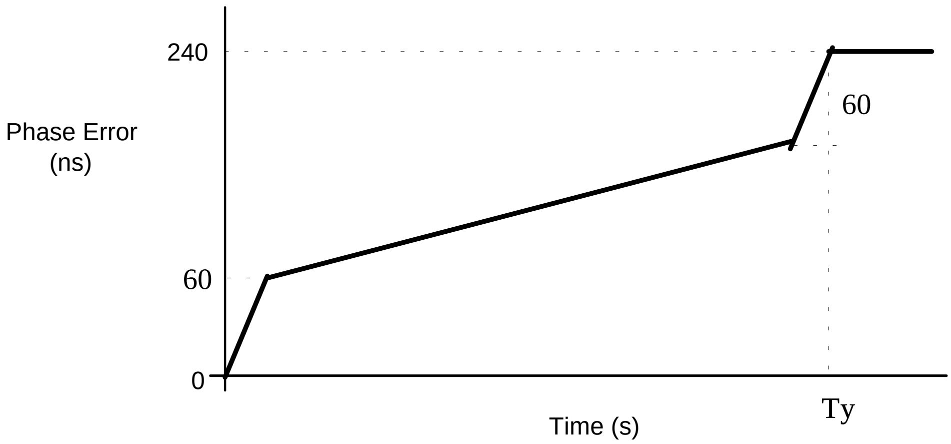


Figure 8: Maximum phase transient at the output due to reference switching

This figure is intended to depict the worst case phase movement attributable to an SSU reference clock switch. Clocks may change state more quickly than is shown here.

NOTE: Output phase excursions, when switching between references which are not traceable to the same clock, are for further study.

9.2 Phase response during hold-over operation

This specification bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

When an SSU loses its reference, it is said to enter the hold-over state. The phase error, ΔT, at the output of the SSU relative to the input at the moment of loss of reference should not exceed the following limit:

$$\Delta T(S) = \{(\boldsymbol{a_1} + \boldsymbol{a_2})\,S + 0{,}5\,\boldsymbol{b}\,S^2 + \boldsymbol{c}\} \text{ (see note 5)}$$

where: $\boldsymbol{a_1}$ = 0,5 ns/s (see note 1);

a_2 = 2,0 ns/s (see note 2);

b = 2,3 x 10^{-6} ns/s^2 (see note 3);

c = 60 ns (see note 4).

The frequency offset a_1 represents an initial frequency offset corresponding to 5 x 10^{-10} (0,0005 ppm).

The frequency offset a_2 accounts for temperature variations after the clock went into holdover and corresponds to 2 x 10^{-9} (0,002 ppm). If there are no temperature variations, the term a_2 S should not contribute to the phase error.

The drift b is caused by ageing: 2,3 x 10^{-6} ns/s^2 corresponds to a frequency drift of 2 x 10^{-10} /day (0,0002 ppm/day). This value is derived from typical ageing characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis as the temperature effect will dominate.

The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state. During this transition, the temporary frequency offset on SDH output interfaces shall not exceed 7,5 ppm.

During the period of holdover, with the exception of the period of transition into holdover (see note 4), the temporary frequency offset after S seconds shall not exceed (a_1 + a_2 + b S).

The resultant overall requirement at constant temperature (i.e. the temperature effect is negligible) is summarized in figure 9.

$$\text{Phase Error } \Delta T(S) = \{a_1 S + 0{,}5 b S^2 + c\}$$

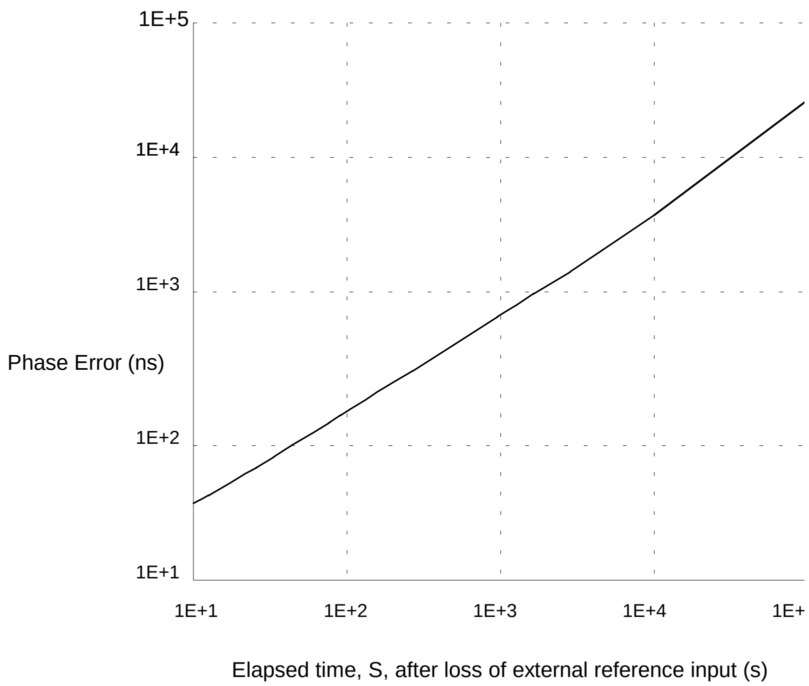


Figure 9: Permissible phase error for an SSU under holdover operation at constant temperature

9.3 Phase response to input signal interruptions

To be defined.

9.4 Phase discontinuity

In cases of infrequent internal testing or other internal disturbances (including major hardware failures, that would give rise to clock equipment protection switches) within the SSU, the following conditions should be met on 2 Mbit/s and 2 MHz synchronization output interfaces:

- the phase variation over any period S up to 1 ms should not exceed 60 ns;
- the phase variation over any period S up to 4 s should not exceed 120 ns;
- for periods greater than 4 s, the phase variation should not exceed a total amount of 240 ns.

In case the SSU is built-in into an SDH equipment, the following condition should be met on any STM-N output interface:

- the temporary frequency offset shall never exceed 7,5 ppm.

10 Interfaces

The requirements in the present document are related to reference points internal to the equipment or Network Element (NE) in which the clock is embedded and are therefore not necessarily available for measurement or analysis by the user. Therefore the performance of the SSU is not specified at these internal reference points, but rather at the external interfaces of the equipment, that are used for synchronization. The input and output interfaces are:

- 2 048 kHz external interfaces according to ETS 300 166 [7];
- 2 048 kbit/s interfaces according to ETS 300 166 [7];
- STM-N traffic interfaces.

NOTE: All of the above interfaces may not be implemented on all equipment. These interfaces should comply with the additional jitter, wander and frequency accuracy requirements as defined in the present document.

Annex A (informative): Information on the SSU noise model

The model of the SSU given below is derived from the well known Phase Locked Loop (PLL) block schematic of which the most important output noise sources (white phase noise and flicker phase noise) have been extracted and been modelled on their own. This simplified clock model reflects the impact of sources injecting noise in the loop of the PLL at points before the Voltage Controlled Oscillator (VCO) and at points after the VCO. It is used to derive an MTIE mask consistent with the TDEV limits for the SSU noise generation requirements in figure 1.

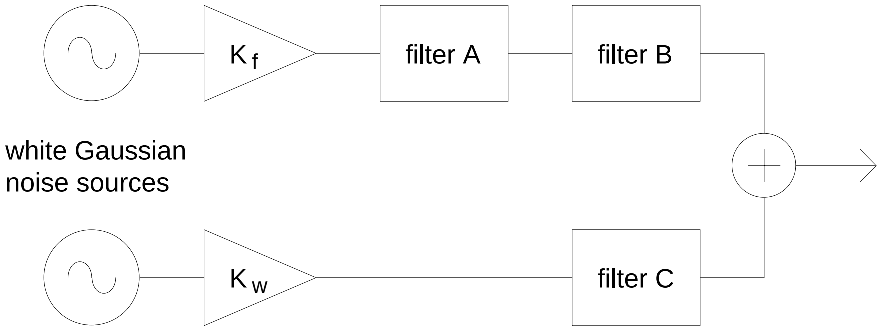


Figure A.1: SSU clock model

In detail, given the schematic in figure A.1:

- noise sources give Gaussian random samples with zero mean, and standard deviation $\sigma_n = 1\text{ ns}$; noise bandwidth is assumed to be $B_n = 5\text{ Hz}$, corresponding to 0,1 s sampling time for independent samples;

- filter A models flicker noise spectral shaping in the frequency range of interest:

$$H_A(s) = \prod_{n=1}^{8} \frac{1}{\sqrt{7}} \times \frac{s + \alpha_n \sqrt{7}}{s + \alpha_n} \qquad \alpha_{n+1} = 7\alpha_n \qquad \alpha_8 = 2\pi \times 6{,}72 \text{ rad / s}$$

- filter B models clock low pass filtering of flicker phase noise before the VCO (*B* is the clock bandwidth):

$$H_B(s) = \frac{\beta}{s + \beta} \qquad \beta = 2\pi \times B$$

- filter C models clock high pass filtering of white phase noise after the VCO (*B* is the clock bandwidth):

$$H_C(s) = \frac{s}{s + \beta} \qquad \beta = 2\pi \times B$$

- flicker noise gain K_f, white noise gain K_w and clock bandwidth *B* settings are responsible for the actual TDEV and MTIE noise characteristics.

Moving from this model, simple analytical relationships can be established between the model parameters K_f, K_w and *B*, and the asymptotical behaviours of TDEV and MTIE, if some approximations are introduced:

- in the frequency range of interest, filter A effectively models a flicker phase noise spectrum shaping, that is:

$$H_A(s) \approx \sqrt{\frac{2\pi f_0}{s}} \qquad f_0 = \alpha_1 / (2\pi \times \sqrt[4]{7}) \approx 5\ \mu\text{Hz}$$

- given the noise band-limited spectral characteristics, the following asymptotic TDEV evaluation can be carried out:

$$\mathrm{TDEV}(\tau) \approx \sqrt{\frac{8\tau^2}{3}\int_0^\infty S_x(f)\frac{\sin^6(\pi f\tau)}{(\pi f\tau)^2}df}$$

being $S_x(f)$ the single-sided power spectrum density of the phase noise expressed in time units and τ the observation interval;

- MTIE is statistically 2σ-estimated as four times the corresponding TIE standard deviation (TIErms), which means that 95 % of MTIE measured values would keep below this estimated value:

$$\mathrm{MTIE}(\tau) \approx 4\sqrt{4\int_0^\infty S_x(f)\sin^2(\pi f\tau)df}$$

Given these assumptions, the following approximate asymptotical estimates for TDEV and MTIE result:

formula applicability	TDEV	MTIE
white noise ($B\tau \to 0$)	$0{,}71\times\frac{K_\mathrm{w}\sigma_\mathrm{n}}{\sqrt{B_\mathrm{n}\tau}}$	$7{,}1\times K_\mathrm{w}\sigma_\mathrm{n}$
white noise ($B\tau \to \infty$)	$0{,}36\times\frac{K_\mathrm{w}\sigma_\mathrm{n}}{\sqrt{B_\mathrm{n}\tau\times B\tau}}$	$7{,}1\times K_\mathrm{w}\sigma_\mathrm{n}$
flicker noise ($B\tau \to 0$)	$3{,}5\times K_\mathrm{f}\sigma_\mathrm{n}\sqrt{\frac{f_0}{B_\mathrm{n}}}\times B\tau$	$25\times K_\mathrm{f}\sigma_\mathrm{n}\sqrt{\frac{f_0}{B_\mathrm{n}}}\times\sqrt{\log\left(\frac{1}{B\tau}\right)-0{,}92}\times B\tau$
flicker noise ($B\tau \to \infty$)	$1{,}1\times K_\mathrm{f}\sigma_\mathrm{n}\sqrt{\frac{f_0}{B_\mathrm{n}}}$	$5{,}6\times K_\mathrm{f}\sigma_\mathrm{n}\sqrt{\frac{f_0}{B_\mathrm{n}}}\sqrt{\log(B\tau)+2{,}42}$

Moreover, it can be calculated that the two asymptotical expressions ($B\tau \to 0$ and $B\tau \to \infty$) for flicker noise meet at $B\tau \approx 0{,}3$ and $B\tau \approx 0{,}13$ for TDEV and MTIE, respectively; the TDEV expressions for white noise meet at $B\tau \approx 0{,}26$ while MTIE is hardly influenced by $B\tau$, provided that $B_\mathrm{n} >> B$.

From a practical point of view it is very useful to relate model parameters B, K_f, and K_W to characteristic features of TDEV curves: assuming $\tau_0 = 0{,}1\mathrm{s}$, $B_\mathrm{n} = 5$ Hz , and $\sigma_\mathrm{n} = 1$ ns in the above equations the following simple formulas are derived:

$$\mathrm{TDEV}(\tau_0) = K_w \quad [\mathrm{ns}] \qquad \text{for B} \leq 1 \text{ Hz}$$

$$\mathrm{TDEV}(\infty) = 1{,}075\times10^{-3}K_f \quad [\mathrm{ns}]$$

$$\tau_\mathrm{c} = 0{,}3\sqrt{1+\frac{1}{B^2}} \qquad [\mathrm{s}]$$

The resulting asymptotic TDEV behaviour is shown in figure A.2.

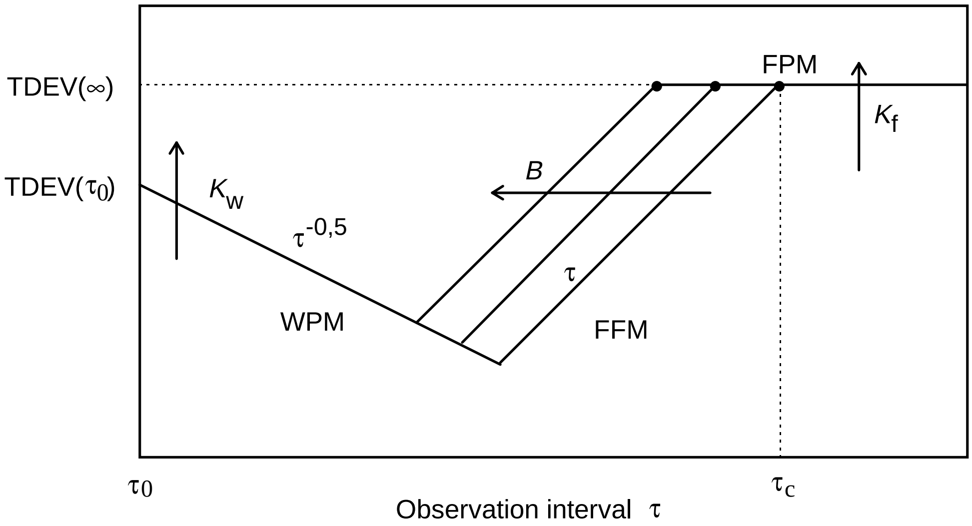


Figure A.2: Asymptotic TDEV behaviour of the SSU model

Assuming the TDEV mask in figure 1 of the main body, model parameters can be calculated to completely define a clock model compliant with the mask itself: from the 12 ns TDEV plateau and from the breakpoint at 100 s, $K_f \approx 11\,000$ and $B \approx 3$ mHz can be estimated, whereas, considering white phase noise dominating at lower observation intervals, the TDEV 3 ns level is consistent with $K_w \approx 3$ (the $B\tau \to 0$ expression applies).

Given these values for the K_f, K_w and B parameters and the approximate expressions above, the asymptotic TDEV and MTIE curves in figure A.3 result: modelled TDEV confirms compliance with the proposed TDEV mask (also reported in figure A.3), while modelled MTIE is used as a basis to consistently define the proposed MTIE mask, shown in figure A.3 as well.

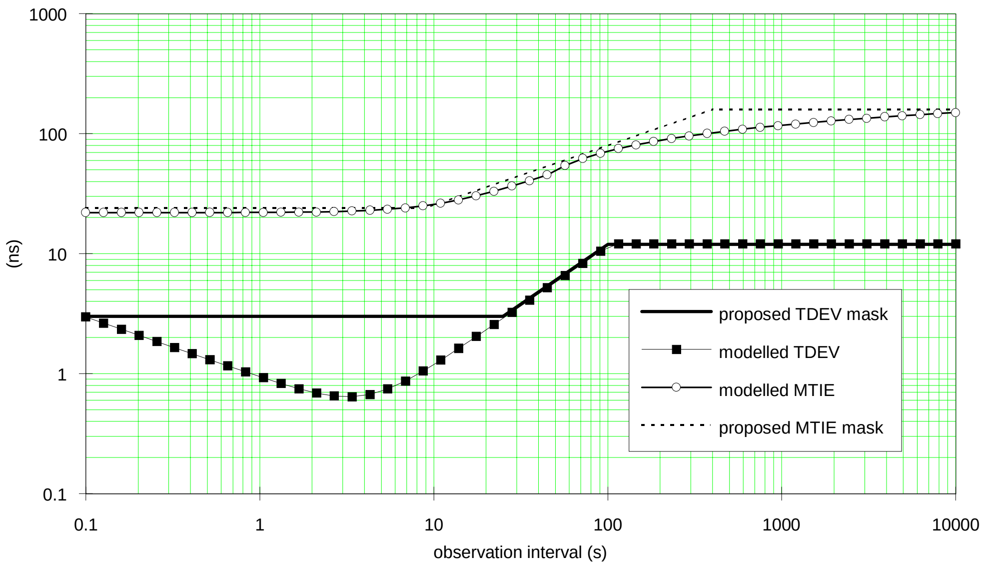


Figure A.3: Consistency between proposed masks and modelled asymptotic expressions

Annex B (informative): Measurement method for combined noise transfer and noise generation

Methods suitable for testing the requirements of clause 8 (a) are described in annex B in EN 300 462-5-1 [5]. The measurement method recommended here directly tests conformance with the noise transfer specification of clause 8 (b) by applying the TDEV input noise tolerance limit, figure 4, as the test signal. The output TDEV characteristic is then directly compared against the specification limit, figure 7.

The measurement set-up is shown in figure B.1.

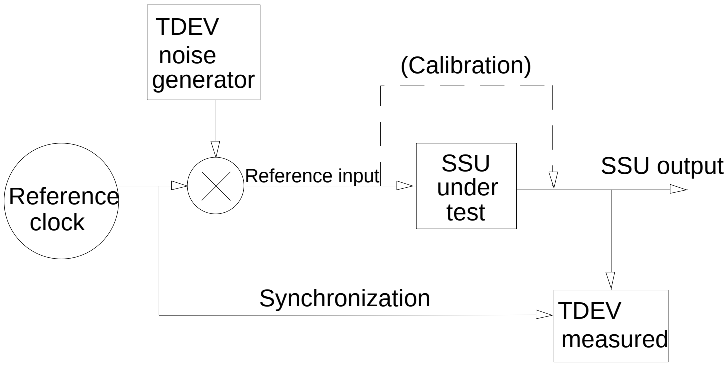


Figure B.1: Measurement set-up for TDEV noise transfer characteristics

To ensure sufficiently accurate, robust and consistent measurements, the following principles should be applied:

1) The test signal should be deterministic, yet sufficiently noise-like over a short observation interval.

2) The noise generator should produce a test signal within ± 20 % of the input noise tolerance specification - subclause 7.2, figure 4.

3) At large values of τ, the TDEV results should match the TDEV output mask within ± 2 % of the specification - clause 8, figure 7.

In order to achieve the above levels of accuracy, normalization and calibration techniques should be applied. In general, the following procedure is recommended:

1) Perform a calibration measurement sequence, without the SSU under test - TDEV(calibration). This obtains the raw test signal characteristics.

2) Calculate a correction factor with respect to the required input wander tolerance specification - TDEV(reference). This now represents the ideal test signal.

3) Measure TDEV(dat) of the SSU under test under the same conditions as the calibration sequence.

4) Normalize TDEV(dat) using TDEV(reference) - obtaining TDEV(measured).

5) TDEV(measured) may now be directly compared with the noise transfer specification limit.

B.1 Functional model of TDEV noise generator

The noise generator shown in figure B.1 can be described by the functional diagram in figure B.2. It does not imply a specific implementation, but defines the key characteristics that should be observed in order to meet the measurement objectives above. A suitable noise generator can, for example, be constructed with a PRBS sequence of 2^{32} - 1, generated at 6,4 kHz.

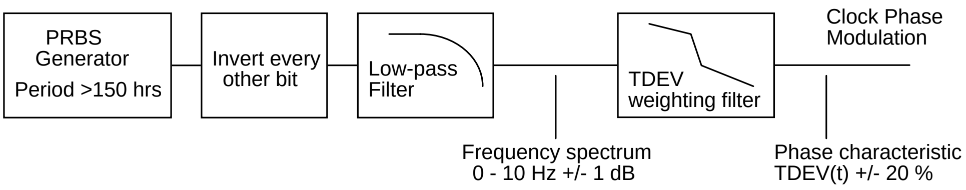


Figure B.2: Functional model of TDEV noise generator

Bibliography

- ITU-T Recommendation Q.551: "Transmission characteristics of digital exchanges".
- ETS 300 417-1-1: "Transmission and Multiplexing (TM); Generic functional requirements for Synchronous Digital Hierarchy (SDH) equipment; Part 1-1: Generic processes and performance".
- ITU-T Recommendation G.810: "Definitions and terminology for synchronization networks".
- ITU-T Recommendation G.811: "Timing requirements at the outputs of primary reference clocks suitable for plesichronous operation of international digital links".
- ITU-T Recommendation G.812: "Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links".
- ITU-T Recommendation G.813: "Timing characteristics of SDH equipment slave clocks (SEC)".

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