Recommendation T/CD 02-02 E
(Ostende 1979, revised at Cannes 1983)
concerning the Specification of engineering requirements for a synchronous digital multiplexer operating at 64 kbit/s using a 10-bit (8+2) envelope structure

Recommendation proposed by Working Group T/WG 10 "Data Communications" (CD)

Text of the revised Recommendation adopted by the "Telecommunications" Commission:

"The Conference of European Post and Telecommunications Administrations,

Considering

— that CCITT Recommendation X.51 describes the standard for a synchronous digital multiplexer operating at 64 kbit/s using a 10-bit (8+2) envelope structure and envelope interleaving;

— that GT/CD has studied the harmonization of multiplexing equipment for data communication under the auspices of Question CD 1.

Recommends

— that the attached specification of engineering requirements for a synchronous digital multiplexer as annexed to this Recommendation should be taken into account by all CEPT Administrations when implementation of such a piece of equipment is being planned by Administrations."

Administrations are free to stipulate additional requirements, and also which of the optional requirements, if any, are to be provided.

Note 1: The specification is the subject of continuing study and possible amendment.
Note 2: The Annex is an integral part of the Recommendation.

1. GENERAL

This Specification describes the characteristics of a synchronous digital multiplexer operating at a multiplexed bit stream having a gross bit rate of 64 kbit/s. The fundamental multiplex structure shall have a gross bit rate of 60 kbit/s and shall utilize padding techniques for transmission on 64 kbit/s national or international bearers.

The tributary channels shall have gross bit rates between 0.75 and 12 kbit/s, organized in 10-bit (8+2) envelopes.

2. TRIBUTARY CHANNEL DATA SIGNALLING RATES

The signal elements of each individual channel shall be assembled in 10-bit envelopes, in which bit 1 is a status bit (S), bit 2 is an envelope alignment bit (A), and bits 3 ... 10 are information bits (I_n); see Figure 1 (T/CD 02-02).

S	A	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8

Figure 1 (T/CD 02-02). 10-bit envelope.

A status bit is associated with each envelope and in conjunction with the associated 8-bit data byte conveys call control or channel status information.

The envelope alignment bit steadily alternates between ONE and ZERO condition from one envelope to the other.

The net bit rate of the tributary channels shall be 600 bit/s, 2,400 bit/s, 4,800 bit/s and 9,600 bit/s, in accordance with user classes 3, 4, 5 and 6 of CCITT Recommendation X.1.

The addition of the status and the envelope alignment bits results in the following gross bit rates and consequent maximum number of respective tributary channels in one multiplex system:

Net bit rate of tributary	Gross bit rate channels	Maximum number of tributary channels in fundamental multiplex structure
600	750	80
2,400	3,000	20
4,800	6,000	10
9,600	12,000	5

Table 1 (T/CD 02-02).

Both structures suitable for handling homogeneous (with respect to gross bit rates) mixes of tributary channels and structures for handling heterogeneous mixes of tributary channels are required, with the constraint that the division of any 12 kbit/s tributary channels of the multiplex shall be homogeneous providing either two 6 kbit/s, four 3 kbit/s or sixteen 750 bit/s tributary channels.

3. INTERFACES

There are five different interfaces defined in the multiplexor system, see Figure 2 (T/CD 02-02).

3.1. Tributary interfaces

3.1.1. *External tributary interface*

Two main variants of this interface exist.

i) When the Tributary interface conversion unit is an integral part of the multiplexor, the interface will be a physical two wire or four wire interface, carrying baseband or voiceband signals. These signals will be specified in the Tributary interface conversion unit specification.

ii) When external transmission equipment is used, such as individual voiceband modems for different tributary gross bit rates, the interface will be a digital modem interface and the Tributary interface conversion unit consists of a modem adaptor.

Both variants can exist in the same multiplexor depending on the transmission requirements of the individual channels.

3.1.2. *Internal tributary interface*

The internal tributary interface is defined by the functional interchange circuits as given in Table 2 (T/CD 02-02).

The functional interchange circuits may or may not be accessable as a physical interface, according to the requirements of the individual Administration.

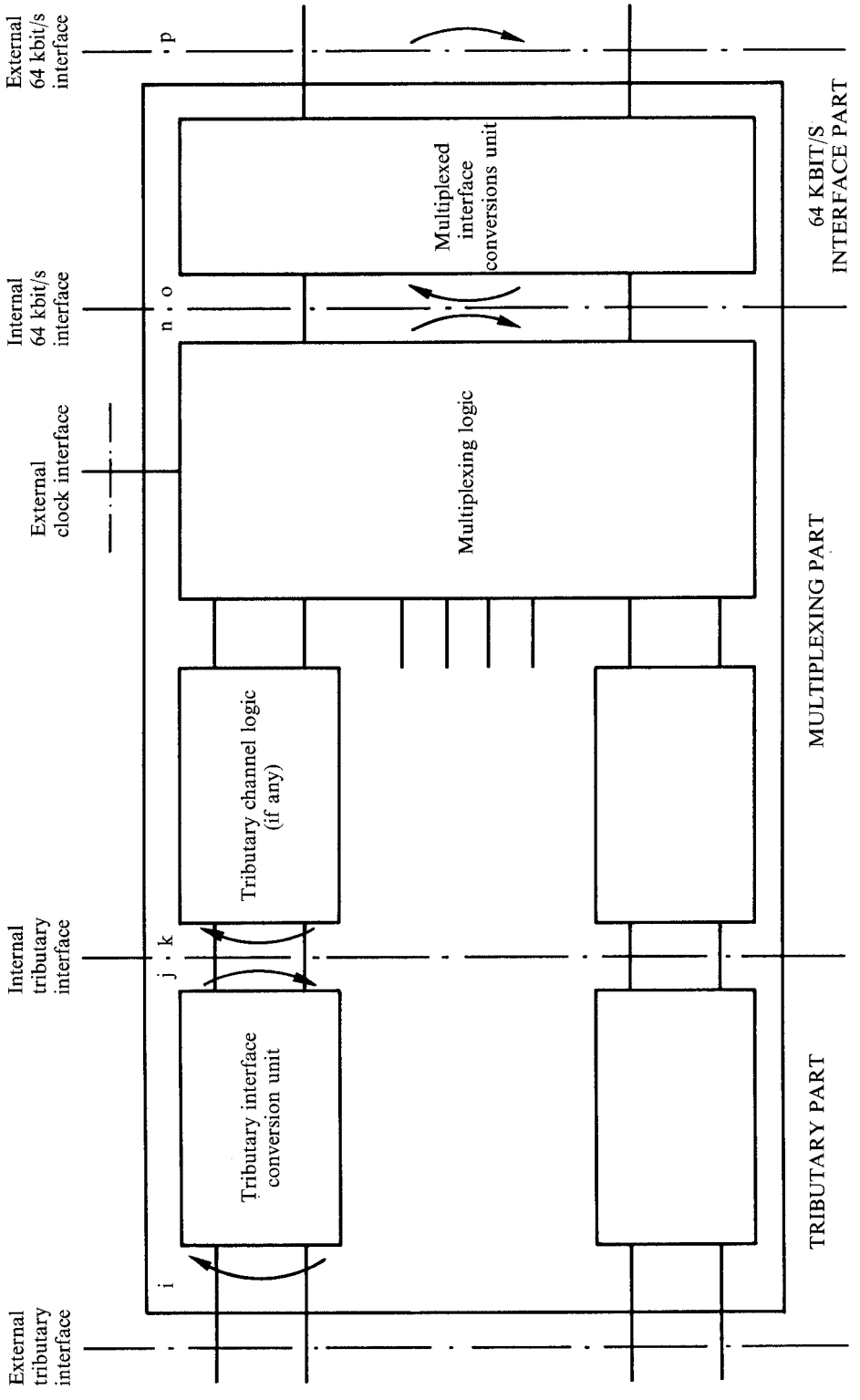


Figure 2 (T/CD 02-02). Functional structure and interfaces of 64 kbit/s data multiplexor system.

Interchange circuit designation	Interchange circuit name	Direction from mux.	Direction to mux.
G	Signal ground or common return		
TT	Tributary channel transmitted data	X	
TR	Tributary channel received data		X
TST	Tributary channel transmitter signal element timing (optional) [1]	X	
TSR	Tributary channel receiver signal element timing (optional) [1]		X
TLC	Loop No. 5 control (optional)	X	
TA	Received line signal level detector (optional)		X

Table 2 (T/CD 02-02). Interchange circuits at the internal tributary interface.

Notes:

[1] In those implementations where a centralized timing source supplies both, the multiplex equipment and the Tributary interface conversion units external to the multiplex equipment, there are no timing interchange circuits at this interface. In this case the receive tributary channel buffers are situated in the external Tributary interface conversion units.

[2] The speed on this interface is equal to the gross bit rate, the data being organized in 10-bit envelopes.

[3] The electrical characteristics of this interface are under study.

[4] The definitions of the interchange circuits are under study.

3.2. 64 kbit/s interfaces

3.2.1. *External 64 kbit/s interface*

Three main variants of this interface exist.

i) A digital interface for direct connection to codirectional or contradirectional interfaces, as defined for access to PCM equipment in CCITT Recommendations G.703 and G.732 paragraphs 5.1. and 5.2.

ii) A digital modem interface according to CCITT Recommendation X.27 (V.11).

iii) An analogue line interface as defined by the Multiplexed interface conversion unit, cf. Figure 2 (T/CD 02-02).

The Multiplexed interface conversion unit of the multiplexor, corresponding to variants i) and ii) above would be PCM or modem adaptors.

In variant iii) the Multiplexed interface conversion unit would be either a 64 kbit/s baseband transmission equipment or a groupband modem, both designed to be integrated parts of the data multiplexor.

3.2.2. *Internal 64 kbit/s interface*

The internal 64 kbit/s interface is defined by the functional interface circuits as given in Table 3 (T/CD 02-02).

The electrical characteristics of the interface could be defined by the logic circuits used and are left for further study.

The functional interchange circuits may or may not be accessable as a physical interface.

Interchange circuit designation	Interchange circuit name	Direction from mux.	Direction to mux.
G	Signal ground or common return		
MT	Multiplex channel transmitted data	X	
MR	Multiplex channel received data		X
MST1	Multiplex channel transmitter signal element timing, mux. source (optional)	X	
MST2	Multiplex channel transmitter signal element timing, 64 kbit/s bearer source (optional)		X
MSR	Multiplex channel receiver signal element timing		X
MLC	Multiplex channel loop No. X control (optional)	X	
MLI	Multiplex channel loop No. X indicator (optional)		
MA	Multiplex channel received line signal level detector (optional)		X

Table 3 (T/CD 02-02). Interchange circuits at the internal 64 kbit/s interface.

Note: The definitions of the interchange circuits are under study.

3.3. **External clock interface** (optional)

In cases where a clock source external to the multiplexor system is used, the following interchange circuits shall be provided between the multiplexor equipment and the external clock equipment or a clock distribution equipment (see Table 4 / T/CD 02-02).

Interchange circuit designation	Interchange circuit name	Direction from mux.	Direction to mux.
G	Signal ground or common return		
CEI	Clock, envelope, incoming		X
CEO	Clock, envelope, outgoing[1)]	X	

Table 4 (T/CD 02-02). Interchange circuits at the external clock interface.

Notes:

[1)] If interchange circuit CEI is not available, the envelope timing signal has to be detected inside the multiplexor equipment from the incoming 64 kbit/s multiplexed data stream.
In order to provide external tributary transmission equipment with an envelope timing signal, an external clock distribution equipment is inserted between the multiplexor (interchange circuit CEO) and the external tributary transmission equipment and provides for the distribution of the envelope timing signal.

[2)] The electrical characteristics at this interface could be in accordance with CCITT Recommendation X.27 (V.11).

[3)] The multiplexor equipment has an internal clock source which can be synchronized from the 64 kbit/s bearer via interchange circuit MST2. This internal clock source shall guarantee the operation in case of failure of the external clock source, at least to be capable of sending the control informations.

[4)] The definitions of the interchange circuits are under study.

4. METHOD OF FRAMING

4.1. Overall structure

The residual 4 kbit/s capacity obtained by carrying the fundamental 60 kbit/s multiplex on the 64 kbit/s bearer shall be distributed so that a padding bit is inserted after each group of 15 bits from the fundamental multiplex (see also Figure 2 (T/CD 02-02)).

The frame length shall be 2,560 bits in the case of a synchronized bearer, i.e. 2,400 bits or 240 envelopes from the fundamental multiplex interleaved with 160 padding bits.

When justification is used (for national purposes) in the case of a non-synchronized bearer the last padding bit in the frame can be deleted or an extra padding bit added when needed, resulting in a variable frame length of $2{,}560 \pm 1$ bit. (This can allow a maximum speed tolerance of approximately ± 4 parts in 10^4.)

The padding bits shall contain the framing pattern, justification service digits and housekeeping signalling (alarms, etc.).

4.2. Framing

4.2.1. *Frame alignment patterns*

The frame alignment method is based on the use of four equidistantly distributed frame alignment patterns written into the padding bits, dividing the frame into four subframes. Each subframe alignment pattern starts with the 14-bit pattern:

1 1 1 1 1 0 0 1 1 0 1 0 1 0

followed by a 2-bit subframe identifier unique to the subframe, i.e.:

SF1 = 00, SF2 = 01, SF3 = 10, SF4 = 11

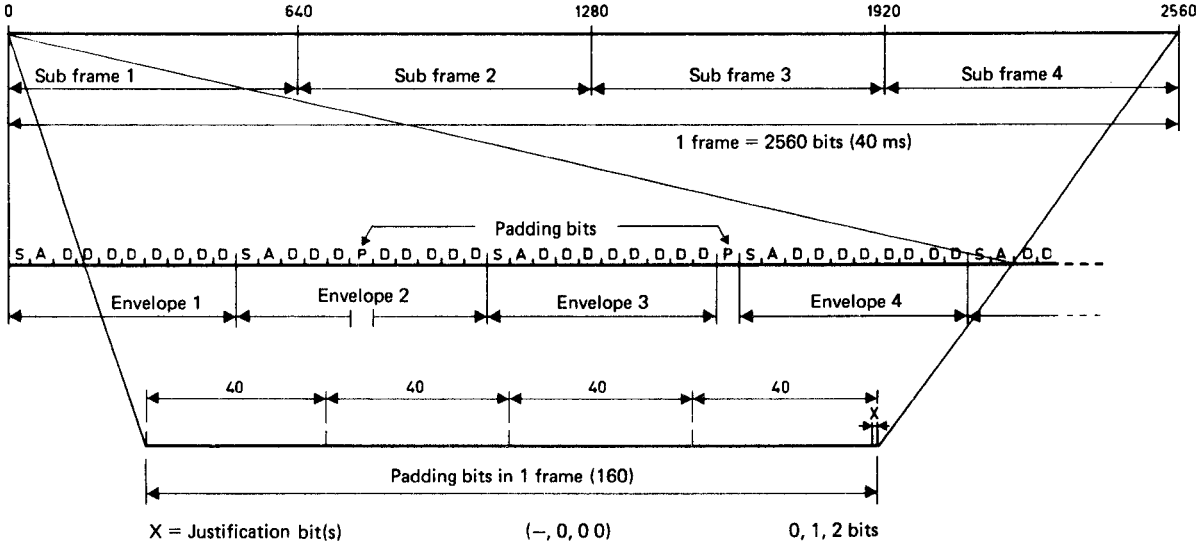


Figure 3 (T/CD 02-02). Multiplex frame structure.

4.2.2. *Framing strategy*

4.2.2.1. Loss of frame alignment

The criterion for loss of frame alignment shall be three consecutive frame alignment patterns including subframe identifier in error.

The frame alignment shall also be considered lost if the first received frame alignment pattern including subframe identifier after reframing is in error.

4.2.2.2. Reframing

The criterion for reframing shall be the detection of one valid frame alignment pattern.

4.2.2.3. Reframing procedure

After loss of frame alignment
— the outgoing envelopes shall be set to all ONES;
— the state shall be signalled to the distant end, and
— a parallel hunt for a valid frame alignment pattern shall be started.

After a valid frame alignment pattern is found
— the two following padding bits shall be accepted as subframe identifiers and be used to set the frame and subframe counter(s) as applicable;
— the blocking of the outgoing data channels shall be removed, and
— the signalling of out of frame alarm to the distant end shall be terminated.

5. JUSTIFICATION

Justification can be required for national purposes.

To achieve this, plus minus justification shall be used in which four repeated justification service signals occupy the three bits immediately following each subframe identifier. The last padding bit of the frame is used as a justification digit.

The repeated justification service signals are:
010 no justification (i.e. one padding bit at end of frame);
100 one justification bit has been added (i.e. two padding bits at end of frame);
001 the justification bit has been deleted (i.e. no padding bit at end of frame).

In evaluating the signals in one frame a majority decision of the four received signals is used. In case of no majority, no justification shall be assumed.

If framing is lost, no justification shall be assumed before reframing has occured.

6. HOUSEKEEPING SIGNALS AND FUNCTIONS

The padding bits not used for framing and justification shall be available for housekeeping information signals, for both international and national use. The definition and allocation of some of the available housekeeping bits is left for further study. The following allocation shall be used.

6.1. International housekeeping bits

Eight bits A, B, C, D, E, F, G, and H are allocated for international housekeeping signals.

The bit A is used to convey to the distant end alarm indications detected at the local end corresponding to:

— absence of incoming pulses,
— loss of frame alignment;

and the bit A shall be assigned such that:

— A equals ONE means no alarm,
— A equals ZERO means alarm.

The other bits B, C, D, E, F, G, and H are reserved to convey further international housekeeping signals. The exact use is under study. Pending the result of the study these bits shall be set to binary ONE.

6.2. Cyclic error-control

A cyclic error-control to be used end-to-end on the international 64 kbit/s link is included as an option. The multiplex frame (2,560 bits) is divided modulo 2 by the polynomial $x^{16} + x^{12} + x^5 + 1$ and the resulting reminder (16 bits), the check bits, are sent in the next frame, four bits in each subframe. An error is detected at the receiving end by comparing the check bits generated locally by dividing the received multiplex frame with the same polynomial, and the check bits received in the following frame. The error detection shall be blocked in the out-of-frame state.

6.3. National housekeeping signals

A total of 48 housekeeping bits, 12 in each subframe, remains for national housekeeping signals, of which the following are provided:

Network status	1- 4 bits
Multiplex channel allocation (depending on number of speed classes and coding)	5-10 bits
Internal and external alarms	1- 4 bits

* These signals could possibly be extended for international use. Housekeeping bits not used in one network shall be set to binary ONE. For international use multiplexers shall be able to ignore information on national housekeeping bits. The use of national housekeeping bits has to be in accordance with the requirements of the individual Administration.

7. ALLOCATION AND USE OF PADDING BITS (40 bits) IN ONE SUBFRAME (640 bits) FOR FRAMING, JUSTIFICATION AND HOUSEKEEPING

The allocation of padding bits in one subframe numbered P1 to P40 is described below and shown in Figure 3 (T/CD 02-02).

P1-P4	International housekeeping bits A, B, C and D	
P5-P8	Error check bits	4 bits
P9-P20	National housekeeping bits	12 bits
P21-P34	Framing pattern Code 1 1 1 1 1 0 0 1 1 0 1 0 1 0	14 bits
P35-P36	Subframe identifier Code 00, 01, 10 or 11	2 bits

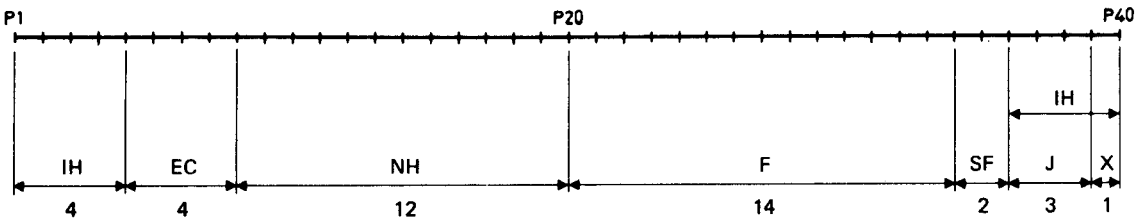
For P37-P40 two alternatives exist:

I. Synchronous transmission bearer

P37-P40	International housekeeping bits E, F, G, and H	

II. Asynchronous transmission bearer

P37-P39	Justification service signals Code 001, 010, 100	3 bits
P40(P41)	Justification bit(s) 0, 1, 2 bit(s) Code —, 0, 00 Only the justification bit(s) in the last subframe (SF4) is used for justification	



IH	= international housekeeping	4+4 bits
EC	= error-control	4 bits
NH	= national housekeeping	12 bits
F	= frame alignment pattern	14 bits
SF	= subframe identifier	2 bits
J	= justification service signals	3 bits
X	= justification bit	1 bit

Figure 4 (T/CD 02-02). Allocation of padding bits in one subframe (40 bits).

8. TESTING AND MEASURING REQUIREMENTS

This item is currently under study (see also Appendices 1 and 2).

9. FAULT CONDITIONS AND CONSEQUENT ACTIONS

9.1. Fault conditions

The muldex equipment shall detect the following fault conditions:

i) Failure of power supply.
ii) Failure of timing source.
iii) Loss of envelope alignment at a tributary channel interface.
iv) Loss of frame alignment at the 64 kbit/s interface.
v) An alarm signal, received from the associated muldex equipment at the distant end of a 64 kbit/s link, indicating a fault at the associated muldex equipment (see paragraph 9.3. Use of housekeeping bits).
vi) Loss of incoming signal at a tributary channel interface.

The following conditions, currently under study, may also be recognized as fault conditions and may require subsequent actions:

vii) In the event of a muldex equipment including an error monitor for the examination of the incoming 64 kbit/s composite signals; an alarm could be raised if a certain specific error rate threshold has been exceeded.
viii) An alarm may be required to indicate internal buffer overflows.
ix) In the event of a muldex equipment being designed with the capability of checking parity errors, an alarm may be required if such errors are identified.
x) Other hardware alarms, e.g. channel card not fully inserted.
xi) Loss of incoming signal from line (groupband modem case circuit 109).
xii) Detection of AIS at the internal 64 kbit/s interface.

9.2 Consequent actions

When a fault condition has been detected, appropriate actions shall be taken as specified in Table 5 (T/CD 02-02).

When the Alarm indication signal (AIS, see *Note 1*) has been detected at the internal 64 kbit/s interface, the local prompt alarm shall optionally be inhibited. Moreover, AIS or a signal according to X.21/71 shall be sent on all tributary channels.

Notes:

1) The Alarm indication signal (AIS) consists of a continuous stream of binary ONEs.

2) The alarm is conveyed to the remote end by setting the 'A' bit of each transmitted frame to binary ZERO condition.

3) When the prompt alarm is not inhibited, the AIS or subsequent loss of frame alignment is regarded as a service alarm, indicating that the data service is interrupted.

4) It is for further study whether the service alarm, detected by means of AIS, should be conveyed in a separate housekeeping bit, e.g. bit B, to the far end.

10. PERFORMANCE

The following characteristics should be defined:
— error performance between the internal 64 kbit/s interface and the internal tributary interface, expressed as percentage of error free seconds;
— timing jitter acceptable at the input of the internal interfaces;
— maximum transmission delay.

Appropriate values are not available at present and further studies are necessary.

11. POWER SUPPLY UNIT

The power supply unit shall be in accordance with the appropriate CEPT specification, and shall be compatible with power supply interfaces in accordance with CEPT Recommendation T/TR 02-02.

12. CONSTRUCTION

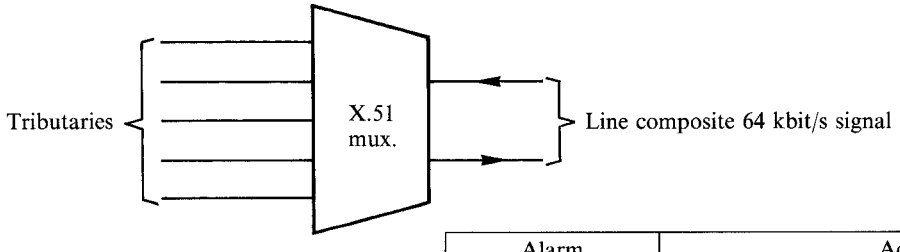
The equipment practice utilised shall comply with the appropriate CEPT specification and shall be compatible with Type B racks in accordance with CEPT Recommendation T/TR 02-01.

13. SPECIFIC DESIGN REQUIREMENTS

The equipment shall be modular in construction, the modules, each of which may consist of one or more cards, shall be as shown in Figure 2 (T/CD 02-02).

14. ENVIRONMENTAL REQUIREMENTS

The equipment shall be suitable for the environmental conditions described in CEPT Recommendation T/TR 02-03.



		Alarm		Action	
Equipment part	Fault conditions	Deferred	Prompt	Towards tributary	Towards composite signal
Central part	Power and timing failures	—	Yes	—	—
Receiving side from tributaries	Loss of envelope alignment	—	Yes	—	Alarm signal on the relevant tributary channel
	Loss of signal from modem	—	Yes	—	Alarm signal on the relevant tributary channel (could be the same)
Receiving side from composite signal	Loss of frame alignment	—	Yes	AIS on all tributaries or signal according to X.21/71	Alarm indication to DSE (within mux. housekeeping bit)
	Loss of incoming signal (detected by line terminal equipment)	—	—	AIS (from line terminal equipment)	

Table 5 (T/CD 02-02). Fault conditions and consequent actions.

Appendix 1

MONITORING AND REMOTE CONTROL BY INBAND SIGNALLING

Fault monitoring facilities

In the event of a fault condition in one tributary channel this shall be signalled to the nearest network control station by conveying particular envelopes, where the envelope alignment bit keeps continuously alternating between ONE and ZERO status, the status bit is kept in the ZERO status, and the information bits are set to patterns conforming to the fault condition.

The following particular fault indicating envelopes are provided:

Signal to be conveyed	Status bit (S)	Envelope alignment bit (A)	Information bits (I_n) 1 2 3 4 5 6 7 8
Loss of envelope alignment (LEA)	0	1010 ...	0 0 1 0 1 0 1 1
Uncontrolled not ready (UCNR) and network out of service (NOS), respectively	0	1010 ...	0 0 0 0 0 0 0 0
Symmetry fault	0	1010 ...	0 1 1 1 1 1 1 0

"Symmetry fault" means that channel allocation or number of channel cards or other parameters are different in both multiplexers.

Table 1. Particular fault indicating envelopes.

Remote control facilities

Facilities have to be provided in the muldex equipment for remote control of test loops in the network from and by network node control centres.

With the aid of a Remote loop control/monitor equipment (RLCME), connected to the muldex equipment, particular remote control envelopes can be injected into the individual tributary channels, and particular monitoring envelopes, generated by various network components, can be detected and decoded.

The following remote control signals are provided:

Signal to be conveyed	Status bit (S)	Envelope alignment bit (A)	Information bits (I_n) 1 2 3 4 5 6 7 8
Loop No. k	0	1010 ...	0 0 1 0 1 0 0 1
Loop No. g	0	1010 ...	0 0 0 0 1 1 1 1

Table 2. Particular remote control envelopes.

When the control envelope for loop No. g is detected, a control signal is fed to the analogue line signal conditioning device to close the loop.

In order to avoid a "loop hook-up" condition between two muldex equipments, the muldex equipment, detecting the "Close loop No. k" or "Close loop No. g" control envelope on the incoming multiplex bitstream, clamps the first information bit (I_1) of the returned signal envelope to binary 1.

So the following acknowledge envelopes arise:

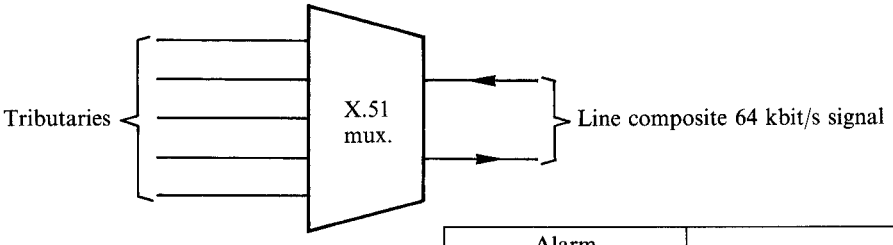
Acknowledge signal	Status bit (S)	Envelope alignment bit (A)	Information bits (I_n) 1 2 3 4 5 6 7 8
Loop No. k acknowledge	0	1010 ...	1 0 1 0 1 0 0 1
Loop No. g acknowledge	0	1010 ...	1 0 0 0 1 1 1 1

Table 3. Particular acknowledge envelopes.

The acknowledge envelopes are detected in the remote loop control/monitor equipment and serve as indication whether or not the looped connection is ready for service.

Remote control signal inhibition

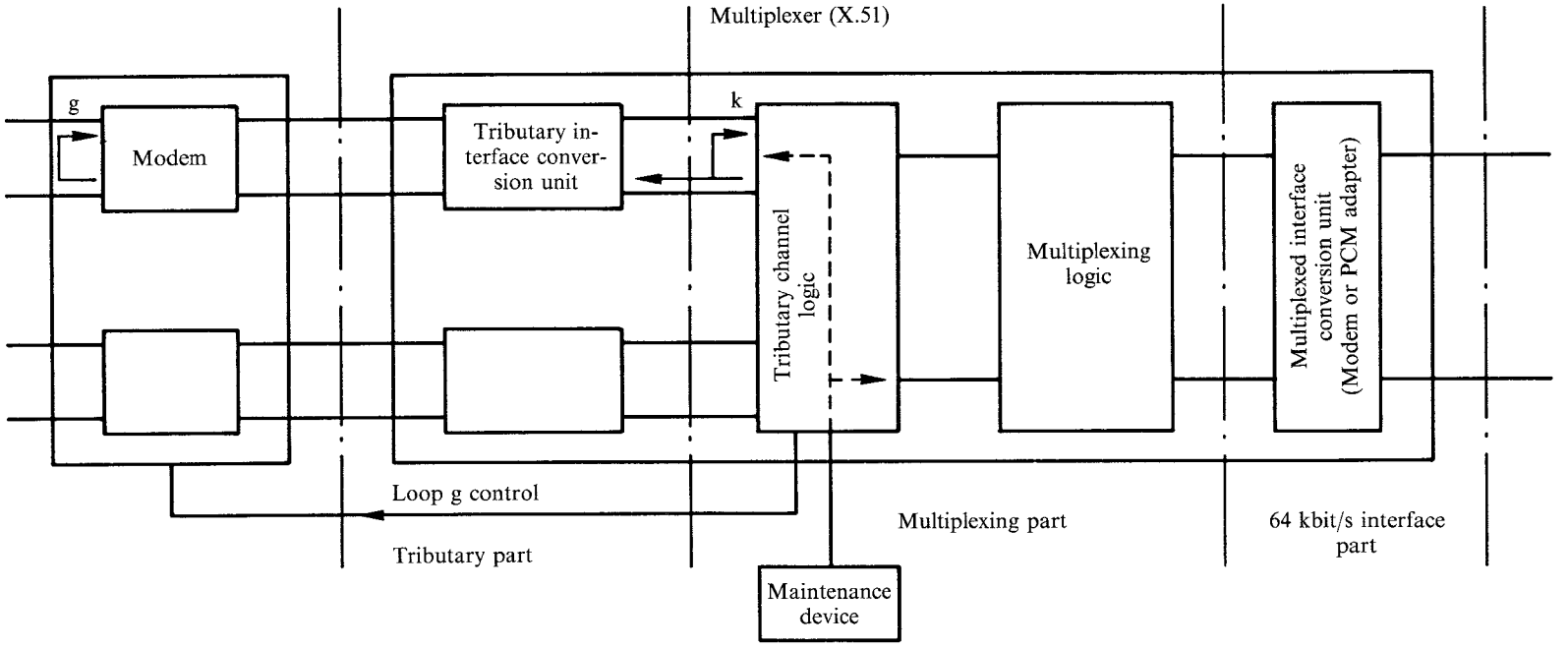
Means have to be provided in the muldex equipment to inhibit the detection of control and monitoring loops and their consequent actions in cases of interworking with multiplex equipment of networks using testing and measuring facilities other than described before (e.g. according to Appendix 2 below). This may be the case in international connexions.



		Alarm		Action	
Equipment part	Fault conditions	Deferred	Prompt	Towards tributary	Towards composite signal
Central part	Power failure		X	—	—
	Internal hardware failure		X	"Clear inhibition" signal* followed by "NOS" (see Table 1)	Housekeeping bit P1 in 0 condition
Receiving side from tributaries	Loss of envelope alignment	X	X	Remote side: "Loss of envelope" signal or "NOS" signal (see Table 1)	Signal envelope in the time slots of affected channel "Loss of envelope" (see Table 1)
Receiving side from composite signal	Loss of frame alignment	X	X	"Clear inhibition" signal* followed by "NOS" signal	Housekeeping bit P1 in 0 condition
	Loss of carrier	X	X		Housekeeping bits P1 and P19 in 0 condition
Channel part	Loss of symmetry, i.e. the channel card is not properly inserted or falsely programmed compared to the far end or vice versa	X	X	"NOS" signal	Signal envelope in the time slots of affected channel "symmetry fault" (see Table 1)

* SA $I_1..I_8$ for a selectable period of time (e.g. 1.8 s) to protect connections against short breaks on the bearer circuit.
X.21: 0 01.. 1 ("Ready").
X.71: 1 01.. 1 ("DTE Waiting").

Table 4 to Appendix 1. Fault monitoring (Inband).



Comments on the loops:

Loop g is an automatically controlled analogue line loop possibly activated at the local or remote side.

Loop k is an automatically controlled digital loop possibly activated at the local or remote side.

Because the loops are controlled by inband signal envelopes the channels are tested by supervision of the acknowledge envelopes.

Figure 1. Implemented loops.

Padding bit	To network management center	From network management center
P1	Service alarm	Service alarm
P2	Not allocated	Not allocated
P3	Not allocated	Not allocated
P4	Not allocated	Not allocated
P5	Cyclic error control	Cyclic error control
P6	Cyclic error control	Cyclic error control
P7	Cyclic error control	Cyclic error control
P8	Cyclic error control	Cyclic error control
P9	100 Baud channel (not in use)	Remote control signal inhibition
P10	100 Baud channel (not in use)	Remote control signal inhibition
P11	Fault monitoring	Network management signals
P12	Fault monitoring	Network management signals
P13	Fault monitoring	Network management signals
P14	Fault monitoring	Network management signals
P15		
⋮	Not allocated	Not allocated
P18		
P19	Loss of line signal at 64 kbit/s interface	Loss of line signal at 64 kbit/s interface
P20	Channel allocation information	Channel allocation information

not in use

Table 5. Housekeeping signals.

Test and maintenance facilities

1. *Switches*
   - selection of channel allocation;
   - external alarm cancellation.
2. *Indicators*
   - loss of central clock;
   - loss of envelope alignment (near end);
   - loss of envelope alignment (far end);
   - symmetry fault:
   - loop activated;
   - alarm at far end;
   - loss of line signal (far end);
   - loss of line signal (near end MA);
   - external alarm (important fault, near end);
   - external alarm (less important fault, near end or fault far end);
   - power alarm;
   - loss of envelope alignment (per channel indicated on channel card);
   - internal clock fault;
   - signal on interchange circuit MR missing;
   - signal on interchange circuit MSR missing;
   - loss of sync. (near end).
3. *Test points*
   - incoming central clock;
   - outgoing central clock;
   - loop control signal to modem rack;
   - incoming multiplexed channel information 60 kbit/s;
   - incoming padding information;
   - frame synchronisation pulses (trigger for oscilloscope, incoming);
   - outgoing multiplexed channel information;
   - outgoing padding information;
   - frame synchronisation pulses (outgoing);
   - fault in incoming sync. information;
   - MT;
   - MR;
   - MST1;
   - MSR;
   - TT;
   - TR.

Appendix 2

MONITORING AND REMOTE CONTROL BY OUTBAND SIGNALLING

Padding bit	Incoming padding bits	Outgoing padding bits
P1	Loss of frame sync. (far end)	Loss of frame sync. (near end)
P2	Not allocated	External alarm
P3	Not allocated	External alarm
P4	Not allocated	External alarm
P5	Cyclic error control	Cyclic error control
P6	Cyclic error control	Cyclic error control
P7	Cyclic error control	Cyclic error control
P8	Cyclic error control	Cyclic error control
P9	Loss of line signal at 64 kbit/s interface (far end)	Loss of line signal at 64 kbit/s interface (near end)
P10	Not allocated	Bit error (from cyclic error control)
P11	Origin = 0 if received from far end (no loops activated)	Origin = 1
P12] *Note 1*	Channel allocation	Buffer overflow/underflow at 64 kbit/s interface
P13]	Channel allocation	Parity alarm from buffer at the tributary interface
P14] *Note 2*	Loop order (line loop at the tributary interface)	Parity alarm from buffer at the 64 bit/s interface
P15]	Loop order (line loop at the tributary interface)	Parity alarm from register containing channel allocation information
P16	Not allocated	Parity alarm from loop order
P17	Not allocated	Not allocated
P18	Not allocated	Channel allocation manually selected
P19	Loop indication (64 kbit/s loop activated at the far end)	Loop indication (64 kbit/s loop activated at the near end)
P20	Blocked (indicates that the multiplexor is blocked for maintenance reasons at the far end)	Blocked (indicates a major fault in the multiplexor)

Table 1 to Appendix 2. Housekeeping signals.

Note 1: Two bits per subframe, totally 8 bits binary coded per frame, are used for channel allocation. 6 bits give the actival alternative out of 56, 2 bits are used as parity bits. The information is assumed valid if 3 consecutive frames contain identical information. The actual channel allocation number is signalled as indicated in the table below.

Table: Channel allocation information

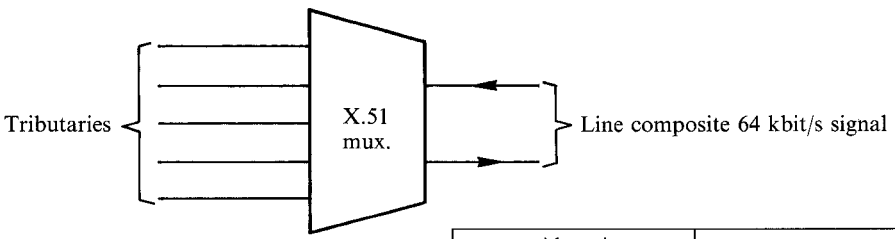
Subframe	1 = 00		2 = 01		3 = 10		4 = 11	
Padding bit	P12	P13	P12	P13	P12	P13	P12	P13
Information	p1	p0	MSB	I_5	I_4	I_3	I_2	LSB

p1 is parity bit (odd parity) for I_2, I_4 and MSB.
P0 is parity bit (odd parity) for LSB, I_3 and I_5.
MSB means most significant bit.
LSB means least significant bit.

Note 2: Two bits in each subframe, totally 8 bits binary coded per frame is used for loop order information to tributary interface conversion units. 7 bits give the multiple number within the multiplexor (0-79) of the tributary interface conversion unit as indicated in the table below. If two frames contain identical information, valid loop order is assumed.

Table: Loop order information

Subframe	1 = 00		2 = 01		3 = 10		4 = 11	
Padding bit	P14	P15	P14	P15	P14	P15	P14	P15
Information	p	MSB	I_6	I_5	I_4	I_3	I_2	LSB



Equipment part	Fault conditions	Alarm*		Action	
		Deferred	Prompt	Towards tributary	Towards composite signal
Central part	Power failure		X	—	—
	Internal hardware failure		X	—	Housekeeping bit P20 set to 0 condition
	Internal buffer overflows	X		—	Housekeeping bit P12 to binary 0
	Internal parity errors	X		—	Housekeeping bits P13, P14, P15 and P16 to binary 0
	External alarms		X	—	Housekeeping bits P2, P3 and P4 to binary 0
Receiving side from tributaries	Loss of envelope alignment		X	—	In all time, slots of affected channel(s) all bits to binary 1 condition (AIS)
	Loss of envelope alignment and loss of carrier		X	—	In all time, slots of affected channel(s) 0 0 1 1 0 0 0 0 0 0
Receiving side from composite signal	Loss of frame alignment		X	AIS on all tributary channels	Housekeeping bit P1 to binary 0 condition
	Loss of carrier		X	AIS on all tributary channels	Housekeeping bit P9 to binary 0 condition
	Cyclic error control	X		—	Housekeeping bit P10 to binary 0 during one frame period

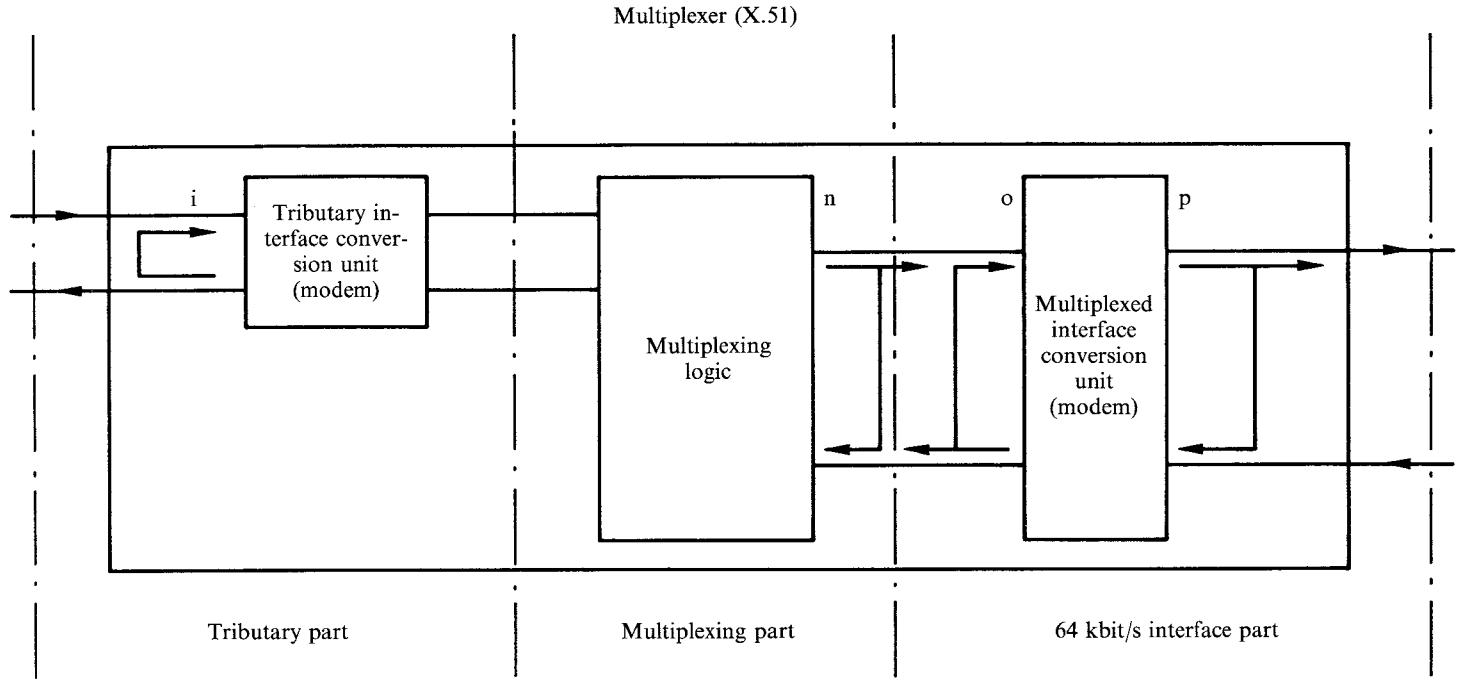
* All alarms are handled and presented by the remote DSE acting as an OMC. Deferred alarms are presented only if the alarm indication is received a number of times within.

Table 2 to Appendix 2. Fault monitoring.

Test and maintenance facilities

1. *Switches*
   — selection between manual (local) or automatic (remote) control of the channel allocation;
   — selection of actual channel allocation (active only if the switch for manual control is active);
   — loop control; loop n);
   — loop control; loop p);
   — LED test (if depressed all LEDs shall light up).

2. *Indicators*
   The following indicators (LEDs) are provided
   — loss of sync., far end (padding bit P1);
   — loss of line signal, far end (P9);
   — loss of sync., near end (P1);
   — loss of line signal, near end (P9);
   — overflow elastic buffer (P12), 64 kbit/s incoming;
   — overflow elastic buffer (P12), 64 kbit/s outgoing;
   — parity alarm in elastic buffer (P14), 64 kbit/s incoming;
   — parity alarm in elastic buffer (P14), 64 kbit/s outgoing;
   — bit error (P10);
   — channel allocation setting (6 LEDs);
   — transmission quality (circuit 110 from V.36 modem);



Comments on the loops:
Loop i is an analogue line loop which is remotely controlled by signalling on the padding bits.
Loop n is a digital loop which is manually controlled by a pushbutton on the multiplexer.
Loop o is a digital loop which is manually controlled by a pushbutton on the modem.
Loop p is an analogue line loop which is manually controlled by a pushbutton on the modem.
When loops n, o or p are aktivated the "line signal" is still conveyed to the "line" (echo-back-loop).

Figure 1. Implemented loops.

— loop 2, far end;
— loop 3, far end;
— loop 2, near end;
— loop 3, near end;
— multiplexor blocked (P20);
— clock alarm (P20);
— power alarm (subscriber modem rack) (P2);
— parity alarm from buffers at the tributary interface (P13).

3. *Test points*

A number of test points (short circuit proof) are provided for fault location purposes. The following test points could be mentioned

— incoming 64 kbit/s data;
— incoming 64 kbit/s timing;
— outgoing 64 kbit/s data;
— outgoing 64 kbit/s timing.