TECHNICAL BASIS for REGULATION

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Attachment requirements for Data Terminal Equipment (DTE) to connect to Packet Switched Public Data Networks (PSPDNs) for CCITT Recommendation X.25 interfaces at data signalling rates up to 1 920 kbit/s utilising interfaces derived from CCITT Recommendations X.21 and X.21bis

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Foreword

This draft Technical Basis for Regulation (TBR) has been produced by the Terminal Equipment (TE) Technical Committee of the European Telecommunications Standards Institute (ETSI) and is now submitted for National Consultation under the Public Enquiry phase of the ETSI standards approval procedure.

Annex D (informative) should be read prior to any detailed study of this draft TBR 2. It sets out the rationale and points of principle that are reflected throughout this draft TBR and is, therefore, useful in understanding the context used in its creation.

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1 Scope

This TBR specifies the technical characteristics (electrical and mechanical interface requirements, and access control protocol) to be provided by packet mode terminal equipment capable of connection to a dedicated interface of a Packet Switched Public Data Network (PSPDN) using CCITT Recommendation X.25 [1] to [3], making use of Link Access Procedure-Balanced (LAPB) and LAPB Extended modes of operation.

The objective of this TBR is to ensure that no disturbance occurs to the public network, and to ensure interworking between network and terminal so that calls can be routed successfully through the network, but without any guarantee of terminal operation and end-to-end operability across networks.

This TBR contains the minimum set of requirements derived from CCITT Recommendation X.25 [1] to [3], in accordance with prior European harmonization documents (NET 2). The requirements of this TBR are suitable for testing terminal equipment for connection to CCITT Recommendation X.25 (1980 [1], 1984 [2], and 1988 [3]) PSPDN terminal equipment that is capable of either originating only or terminating only, packet level modes of operation have been included. A Data Terminal Equipment (DTE) which satisfies the relevant technical requirements of this TBR may be connected to every PSPDN, use any of the essential (E) facilities and invoke any of the provided additional (A) facilities as given in CCITT Recommendation X.2 [4] and [5].

For each requirement in this TBR, a test is given including measurement methods. Requirements apply at the public network interface of the terminal equipment, which may be stimulated to perform tests by additional **equipment** if necessary. For the purposes of this TBR a terminal **equipment** comprises of that apparatus included between a PSPDN Network Termination Point (NTP), and the terminal equipment boundary point that delimits the Network to Transport layers as defined in CCITT Recommendation X.200, subclause 7.5. **Equipment** is taken to mean in this context as either software, firmware or hardware.

Where the packet terminal equipment supplied for test does not contain the functions of all three OSI (CCITT Recommendation X.200) Layers 1, 2 and 3, the terminals documentation and instructions for use shall state which additional **equipment** is required for compliance to this TBR and the additional **equipment** shall be submitted for test, as though all the functional layers were provided by the packet terminal equipment.

This TBR also gives guidance on appropriate standards relating to the essential requirements on safety. Terminal equipment may be subject to additional or alternative attachment requirements in other Common Technical Regulations (CTRs) depending on its functionality, in particular if it supports a service which is considered to be a justified case for regulation of terminal equipment interworking via the public telecommunications network.

The requirements and tests given in this TBR may be suitable for use in conjunction with other requirements not given in this TBR, for the approval of apparatus attaching to public data network interfaces, that are not PSPDN, using CCITT Recommendation X.21bis [6] interfaces for terminal attachments to leased circuits.

Operation at signalling rates in excess of 48 kbit/s and up to 1 920 kbit/s have been included, using interfaces derived from CCITT Recommendations X.21bis [6] and X.21 [7].

2 Normative references

This TBR incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this TBR only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation X.25 (1980): "Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for terminals operating in the packet mode and connected to public data networks by dedicated circuit".

[2] CCITT Recommendation X.25 (1984): "Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for terminals operating in the packet mode and connected to public data networks by dedicated circuit".

[3] CCITT Recommendation X.25 (1988): "Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for terminals operating in the packet mode and connected to public data networks".

[4] CCITT Recommendation X.2 (1984): "International data transmission services and optional user facilities in public data networks".

[5] CCITT Recommendation X.2 (1988): "International data transmission services and optional user facilities in public data networks".

[6] CCITT Recommendation X.21bis (1984): "Use on public data networks of data terminal equipment (DTE) which is designed for interfacing to synchronous V-series modems".

[7] CCITT Recommendation X.21 (1984): "Interface between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) for synchronous operation on public data networks".

[8] ISO 2110 (1980): "Data communication - 25-pin DTE/DCE interface connector and pin assignments".

[9] ISO/IEC 11569 (1992): "Data communication - 26-pin DTE/DCE interface connector and pin assignments".

[10] ISO 4902 (1980): "Data communication - 37-pin DTE/DCE interface connector and pin assignments".

[11] ISO 2593 (1984): "Data communication - 34-pin DTE/DCE interface connector and pin assignments".

[12] ISO 4903 Second edition (1989): "Data communication - 15-pin DTE/DCE interface connector and pin assignments".

[13] EN 45011 (1989): "General criteria for certification bodies operating product certification".

[14] ISO/IEC 9646 - 3 (1992): "Information technology - Open Systems Interconnection - Conformance testing methodology and framework - Part 3: The Tree and Tabular Combined Notation (TTCN)".

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purposes of this TBR, the definitions provided in CCITT Recommendations X.25 ([1], [2] and [3]) and X.2 ([4] and [5]) apply along with the following:

CCITT Recommendation X.25 ([1] to [3]) network: A PSPDN network which offers a CCITT Recommendation X.25 [1], [2] and [3] DTE/DCE interface providing the essential (E) facilities for user classes of service 8 to 11 as defined in CCITT Recommendation X.2, [4] and [5].

3.2 Symbols

For the purposes of this TBR, the following symbols apply:

A	Symbol 1
B	Symbol 2
C	Symbol 3

3.3 Abbreviations

For the purposes of this TBR, the following abbreviations apply:

DCE	Data Circuit Terminating Equipment
DTE	Data Terminal Equipment
FCS	Frame Check Sequence
GFI	General Format Identifier
hex	hexadecimal
IS	Initialisation Sequence
ISDN	Integrated Services Digital Network
LC	Logical Channel
LCN	Logical Channel Number
NTP	Network Termination Point
PSPDN	Packet Switched Public Data Network
PTI	Packet Type Identifier
PVC	Permanent Virtual Circuit
SVC	Switched Virtual Circuit (The term Virtual Call is used in CCITT Recommendation X.25 [1])
VS	Verification Sequence
LAPB	Link Access Procedure Balanced (Modulo 8 operation)
LAPB Extended	Link Access Procedure Balanced (Modulo 128 operation)
SABM	Set Asynchronous Balanced Mode
SABME	Set Asynchronous Balanced Mode Extended
SABM(E)	SABM or SABME
FRMR	Frame Reject
DM	Disconnected Mode
DISC	Disconnect
V0	is the open-circuit generator voltage
R0	is the total effective resistance associated with the generator, measured at the interchange point
C0	is the total effective capacitance associated with the generator, measured at the interchange point
V1	is the voltage at the interchange point with respect to common return
CL	is the total effective capacitance associated with the load, measured at the interchange point
RL	is the total effective resistance associated with the load, measured at the interchange point
EL	is the open-circuit load voltage (bias)

4 Safety

There are no safety technical requirements under this TBR.

NOTE: Safety requirements are imposed under the Low Voltage Directive (73/23/EEC) and articles 4(a) and 4(b) of Directive 91/263/EEC.

5 EMC

There are no EMC technical requirements under this TBR.

NOTE: General EMC requirements are imposed under the EMC Directive (89/336/EEC).

6 General requirements

6.1 Generator characteristics

All generator tests are defined as either one or two physical connection points A and B on the means provided for connection to the Data Circuit-terminating Equipment (DCE), to which the output of a terminal equipment generator is connected, and point C the physical connection to which the terminal equipment signal ground is connected.

6.1.1 Generator polarities

6.1.1.1 Signal condition "0"

When the signal condition 0 (space) for data circuits, or ON for control circuits, is transmitted, the output point A shall be positive with respect to point B for balanced generators or shall be positive with respect to point C for unbalanced generators.

6.1.1.2 Signal condition "1"

When the signal condition 1 (mark) for data circuits, or OFF for control circuits, is transmitted, the output point A shall be negative with respect to point B for balanced generators or shall be negative with respect to point C for unbalanced generators.

6.2 Receiver characteristics

6.2.1 Input voltage-current

All receiver tests are defined as either one physical connection point defined as point A' or two physical connection points defined as points A' and B'; on the means provided for connection to the DCE to which the input of a terminal equipment receiver is connected, and point C' the physical connection to which the terminal equipment signal ground is connected.

6.3 Physical Layer requirements

6.3.1 Interconnection requirements

The means for the connection of the DTE to the Network Termination Point (NTP) for test purposes shall be in accordance with either subclause 6.3.1.1 or subclause 6.3.1.2.

6.3.1.1 Integral connection

Where the apparatus is to connect directly to the NTP and the method of connection is by the use of an integral connection cable arrangement, the NTP end of the cable shall terminate on one of the connectors specified in subclause 6.3.2. Compliance with this requirement shall be determined by the supplier submitting for test, the DTE with its longest interconnection cable for connection to the NTP. This shall be based upon the Protocol Implementation Conformance Statement/Protocol Implementation eXtra Information for Testing (PICS/PIXIT) declaration and inspection with the requirements being met in subclause 6.4. Where the supplier only connects to the network with one fixed interconnection cable

arrangement then all references to the longest cable shall refer to the one fixed inter-connection cable declared for use.

6.3.1.2 Non-integral connection

Where the apparatus is to connect directly to the NTP and the method of connection is by the use of a non-integral connection cable arrangement, the supplier shall provide the DTE to NTP cable interconnection cable with the NTP end of the cable terminated with one of the connectors specified in subclause 6.3.2. Compliance with this requirements shall be determined by the supplier submitting for test, the DTE with the longest cable specified in the "DTE equipment documentation". This shall be based upon the PICS/PIXIT declaration and inspection with the requirements being met in subclause 6.4. The DTE equipment documentation shall state all cable lengths, their physical and electrical characteristics with identification of the interchange circuits and the connector type for the correct operation of the equipment; as if they had been supplied by an integral connection method, for use with the equipment. Where the supplier only intends that connection to the network is by the use of one fixed interconnection cable arrangement then all references to the longest cable shall refer to the one fixed interconnection cable declared for use in the "DTE equipment documentation".

6.3.2 Connector requirements and pin allocations

The interconnecting cables supplied with the DTE shall be terminated with a connector appropriate for the relevant service data rate for connection to the NTP in accordance with subclauses 6.3.2.1, 6.3.2.2, 6.3.2.3, 6.3.2.4 or 6.3.2.5.

6.3.2.1 ISO 2110 for attachment to CCITT Recommendation X.21bis and X.21 interfaces

Connector type and pin allocation for services up to 19,2 kbit/s using a CCITT Recommendation V.24 interface with CCITT Recommendation V.10 or V.28 electrical characteristics.

The connector implemented at the NTP end of the DTE to NTP interconnecting cable shall conform to ISO 2110 [8]. All implemented interchange circuits stated by the supplier shall be assigned as generators or loads, except for common return, to the connector pins indicated in Annex B, Clause B.1.

NOTE: This requirement is based upon CCITT Recommendation X.21bis [6], subclause 1.2.

Conformance shall be verified by inspection of the PICS and PIXIT declaration, a physical inspection of the connector and an attempt to mate the connector provided by the terminal equipment, to a DCE compliant connector with female contacts. Successful mechanical mating shall occur without any undue force and deformation of these mechanical surfaces.

Justification: Directive 91/263/EEC, Article 4(f).

6.3.2.2 ISO/IEC 11569 for attachment to CCITT Recommendation X.21bis and X.21 interfaces

Connector type and pin allocation for services up to 19,2 kbit/s using a CCITT Recommendation V.24 interface with CCITT Recommendation V.10 or V.28 electrical characteristics or for services up to 1 920 kbit/s with CCITT Recommendation V.11 electrical characteristics.

The connector implemented at the NTP end of the DTE to NTP interconnecting cable shall conform to ISO 11569 [9]. All implemented interchange circuits as stated by the supplier shall be assigned as generators or loads, except for common return, to the connector pins indicated in Annex B, Clause B.2.

NOTE: This requirement is based upon Draft ITU-T Recommendation X.21/X.21bis.

Conformance shall be verified by inspection of the PICS and PIXIT declaration, a physical inspection of the connector and an attempt to mate the connector provided by the terminal equipment, to a DCE compliant connector with female contacts. Successful mechanical mating shall occur without any undue force and deformation of these mechanical surfaces.

Justification: Directive 91/263/EEC, Article 4(f).

6.3.2.3 ISO 4902 for attachment to CCITT Recommendation X.21bis and X.21 interfaces

Connector type and pin allocation for services up to 1 920 kbit/s using a CCITT Recommendation V.36 interface with CCITT Recommendation V.11 or V.10 electrical characteristics.

The connector implemented at the NTP end of the DTE to NTP interconnecting cable shall conform to ISO 4902 [10]. All implemented interchange circuits as stated by the supplier shall be assigned as generators or loads, except for common return, to the connector pins indicated in Annex B, Clause B.3.

NOTE: This requirement is based upon CCITT Recommendation X.21bis [6], subclause 1.2.

Conformance shall be verified by inspection of the PICS and PIXIT declaration, a physical inspection of the connector and an attempt to mate the connector provided by the terminal equipment, to a DCE compliant connector with female contacts. Successful mechanical mating shall occur without any undue force and deformation of these mechanical surfaces.

Justification: Directive 91/263/EEC, Article 4(f).

6.3.2.4 ISO 2593 for attachment to CCITT Recommendation X.21bis and X.21 interfaces

Connector type and pin allocation for services up to 1 920 kbit/s using a CCITT Recommendation V.35 interface with CCITT Recommendations V.35 and V.28 or V.11 and V.10 electrical characteristics.

The connector implemented at the NTP end of the DTE to NTP interconnecting cable shall conform to ISO 2593 [11]. All implemented interchange circuits as stated by the supplier shall be assigned as generators or loads, except for common return, to the connector pins indicated in Annex B, Clause B.4.

NOTE: This requirement is based upon CCITT Recommendation X.21bis [6], subclause 1.2 and CCITT Recommendation V.36, subclause 10.1.2.

Conformance shall be verified by inspection of the PICS and PIXIT declaration, a physical inspection of the connector and an attempt to mate the connector provided by the terminal equipment, to a DCE compliant connector with female contacts. Successful mechanical mating shall occur without any undue force and deformation of these mechanical surfaces.

Justification: Directive 91/263/EEC, Article 4(f).

6.3.2.5 ISO 4903 for attachment to CCITT Recommendation X.21 interfaces

Connector type and pin allocation for services up to 1 920 kbit/s using a CCITT Recommendation X.24 interface with CCITT Recommendation V.11 electrical characteristics.

The connector implemented at the NTP end of the DTE to NTP interconnecting cable shall conform to ISO 4903 [12]. All implemented interchange circuits as stated by the supplier shall be assigned as generators or loads, except for common return, to the connector pins indicated in Annex B, Clause B.5.

NOTE: This requirement is based upon CCITT Recommendation X.21 [7], subclause 2.2.

Conformance shall be verified by inspection of the PICS and PIXIT declaration, a physical inspection of the connector and an attempt to mate the connector provided by the terminal equipment, to a DCE compliant connector with female contacts. Successful mechanical mating shall occur without any undue force and deformation of these mechanical surfaces.

Justification: Directive 91/263/EEC, Article 4(f).

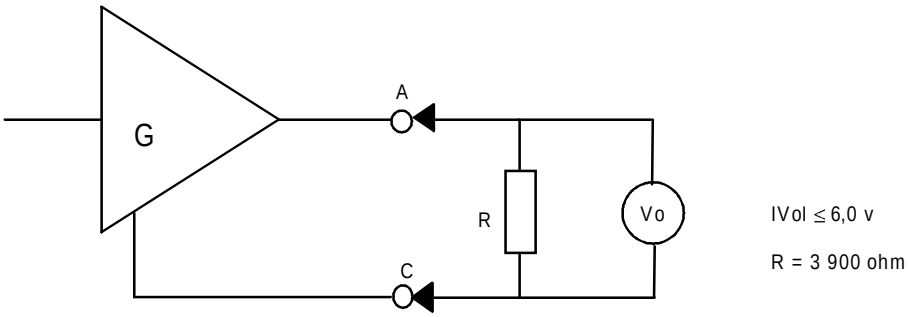
6.4 Layer 1 (electrical) requirements

6.4.1 Electrical requirements for attachment to CCITT Recommendation V.10 interchange circuits

Where an interface utilises different electrical characteristic on adjacent pins, which are not applicable to subclause 6.4.1, then those essential requirements given in subclauses 6.4.2, 6.4.3 or 6.4.4 shall apply.

6.4.1.1 Generator open circuit output voltage

When a 3 900 ohm non-reactive impedance is connected between points A and C, for each binary state the magnitude of the voltage between points A and C shall be less than or equal to 6,0 volts (see figure 1).



NOTE: This requirement is based upon CCITT Recommendation V.10 (1988), subclause 5.2.1 and NET 1, First Edition (1988), subclause 8.1.1.1, in order to determine the ability of terminal equipment to establish interworking with public networks under minimum load condition.

Figure 1

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.2.1.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.1.2 Generator terminated output voltage

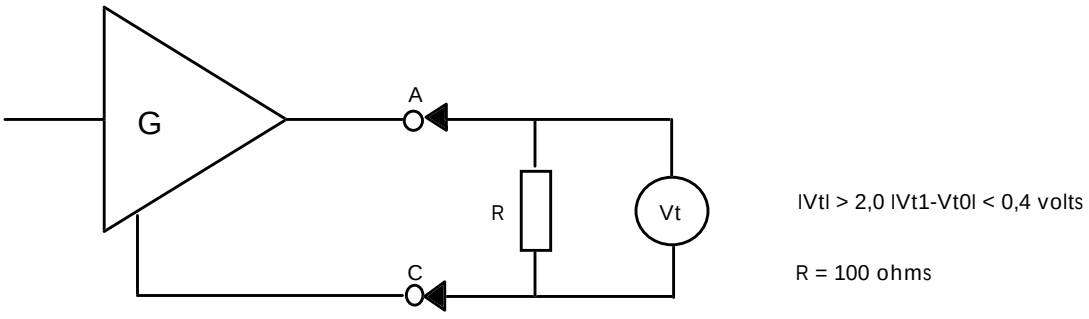
The output voltage of a generator when terminated with a 100 ohm non-reactive impedance connected in series between points A and C (see figure 2):

a) the magnitude of the voltage, for either binary state, between points A and C shall be greater than or equal to 2,0 volts;

b) the magnitude of the voltage, for either binary state, between points A and C shall be greater than or equal to 50 % of the voltage measured in the requirement stated in subclause 6.4.1.2 a);

c) the polarity of the differential voltage between points A and C for a particular binary state shall be the reverse of that for the other binary state;

d) the difference in the magnitudes of the voltages measured in either of the binary states as described in a) shall be less than 400 mV.



NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 5.2.2 and NET 1, First Edition (1988), subclause 8.1.1.1 in order to determine the ability of terminal equipment to establish interworking with public networks under an ideal load condition.

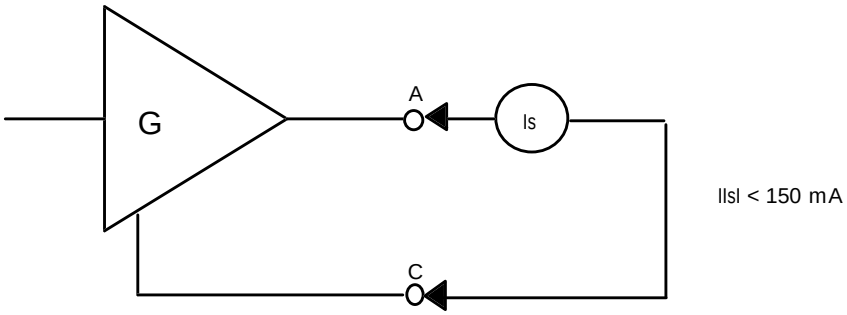
Figure 2

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.2.2.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.1.3 Generator output current limit

When the generator point A is short circuited to point C, the current flowing through point A shall not exceed 150 milliamperes, for either binary state (see figure 3):



NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 5.2.3 and NET 1, First Edition (1988), subclause 8.1.1.1 in order to determine the potential for harm to a public network interface by a terminal whose technical characteristics may cause misoperation or damage to that network by excessive electrical signals that would have no effect on humans and which fall outside the scope of Directive 73/23/EEC.

Figure 3

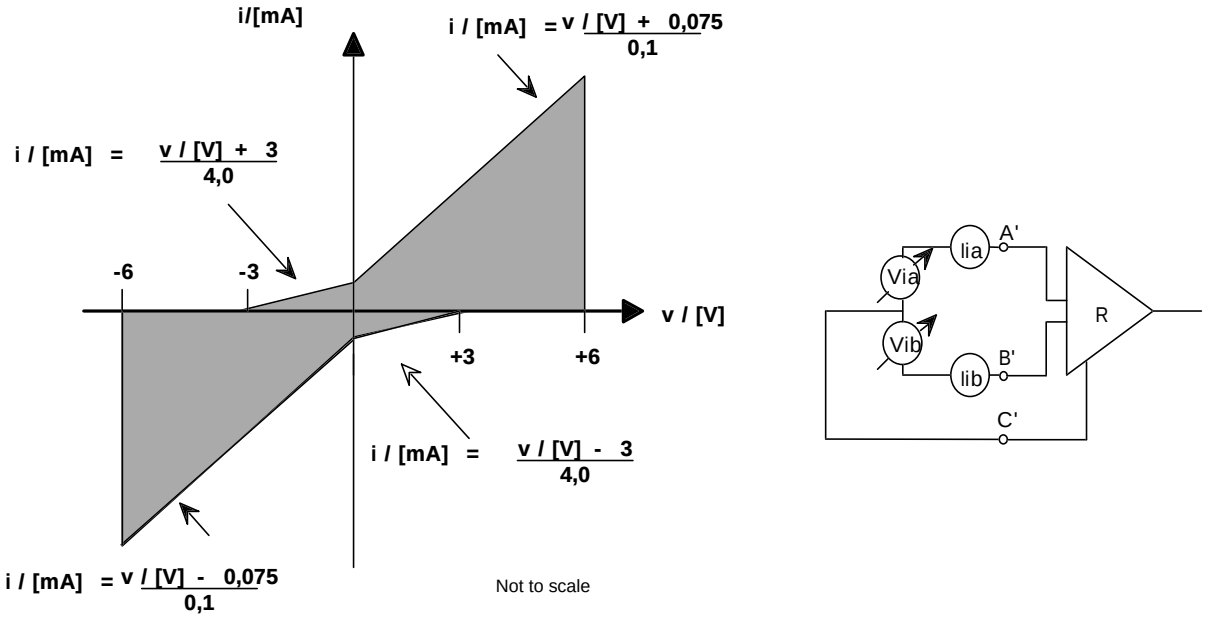
Compliance shall be verified in accordance with the test specified in Annex A, subclause A.2.3.

Justification: Directive 91/263/EEC, Article 4(d).

6.4.1.4 Receiver input voltage - current limit

The receiver, when a voltage source (Via) connected between points A' and C', is varied between -6,0 volts and +6,0 volts (whilst point B' is maintained at 0 volts), the current flow through point A', shall remain within the shaded range shown in figure 4.

A voltage source (Vib) connected between points B' and C', is then varied between -6,0 volts and +6,0 volts (whilst point A' is maintained at 0 volts), the current flow through point B' shall continue to remain within the shaded range shown in figure 4.



NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 6.2 and NET 1, First Edition (1988), subclause 8.1.1.1 in order to determine the ability of terminal equipment to establish interworking with public networks under minimum and maximum load conditions.

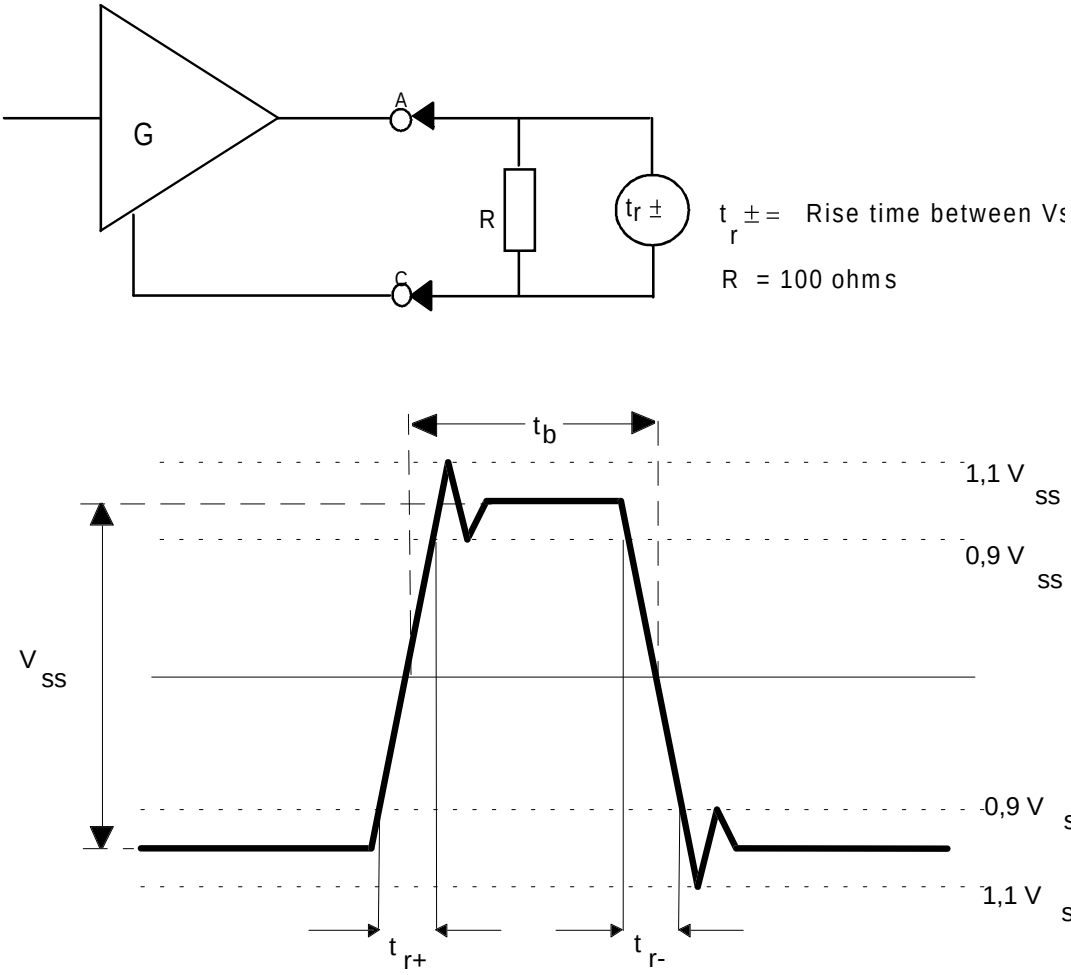
Figure 4

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.2.4.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.1.5 Generator output rise time

The generator, when connected to the test circuit shown in figure 5, during transitions from one binary state to the other, shall have the time taken for the differential voltage measured between points A and C to pass between points at which, for each binary state, it is 90 % of its steady state value, for data signalling rates up to 19,2 kbit/s, less than or equal to 0,3 of the nominal duration of a bit. For the purposes of this requirement, transient signals are ignored (see figure 5).



V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit for Tb ≥ 50 µs, Tr ≤ 0,3 Tb.

NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 5.3 and NET 1, First Edition (1988), subclause 8.1.1.1 in order to determine the ability of terminal equipment to establish interworking with public networks under ideal load conditions by determining the signal rise time between significant signal states.

Figure 5

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.2.5.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.2 Electrical requirements for attachment to CCITT Recommendation V.11 interchange circuits

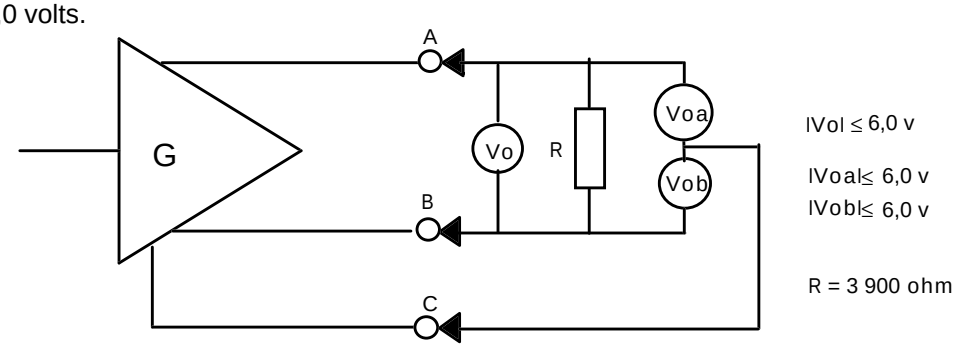
Where an interface utilises different electrical characteristic on adjacent pins, which are not applicable to subclause 6.4.2, then those essential requirements given in subclauses 6.4.1, 6.4.3 or 6.4.4 shall apply.

6.4.2.1 Generator open circuit output voltage

The open circuit generator voltage when terminated with a 3 900 ohm non-reactive impedance connected between points A and B for each binary state (see figure 6):

a) the magnitude of the voltage between points A and B shall be less than or equal to 6,0 volts;

b) the magnitude of the voltage between either points A or B and point C shall be less than or equal to 6,0 volts.



NOTE: This requirement is based upon CCITT Recommendation V.10 (1988), subclause 5.2.1 (1988) and NET 1, First Edition (1988), subclause 8.1.1.1 in order to determine the ability of terminal equipment to establish interworking with public networks under a minimum load condition.

Figure 6

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.3.1.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.2.2 Generator terminated output voltage

The output voltage of a generator when terminated with two 50 ohm non-reactive impedances connected in series between points A and B (see figure 7):

a) the magnitude of the voltage, for either binary state, between points A and B shall be greater than or equal to 2,0 volts;

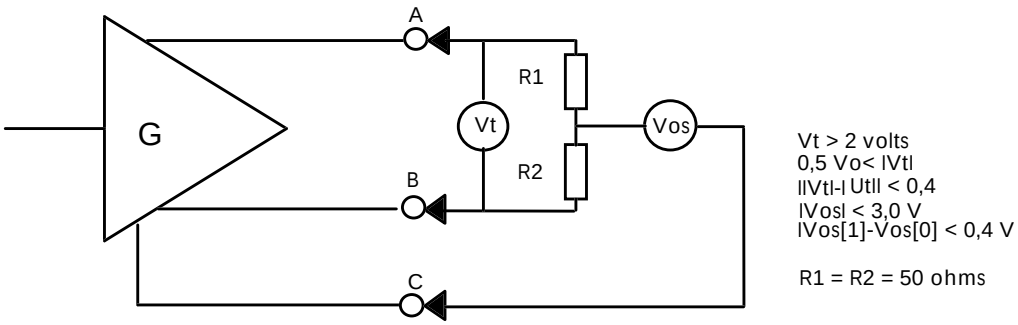
b) the magnitude of the voltage, for either binary state, between points A and B shall be greater than or equal to 50 % of the voltage measured in requirement a) of subclause 6.4.2.1;

c) the polarity of the differential voltage between points A and B for a particular binary state shall be the reverse of that for the other binary state;

d) the difference in the magnitudes of the voltages measured in either of the binary states in subclause 6.4.2.2, a) shall be less than 400 mV;

e) the magnitude of the voltage between the centre point of the two series connected 50 ohm impedances and point C shall be less than or equal to 3,0 volts for either binary state;

f) the difference in the magnitudes of the voltages measured in either of the binary states in subclause 6.4.2.2, e) shall be less than 400 mV.



NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 5.2.2 and NET 1, First Edition (1988), subclause 8.1.1.2 in order to determine the ability of terminal equipment to establish interworking with public networks under an ideal load condition.

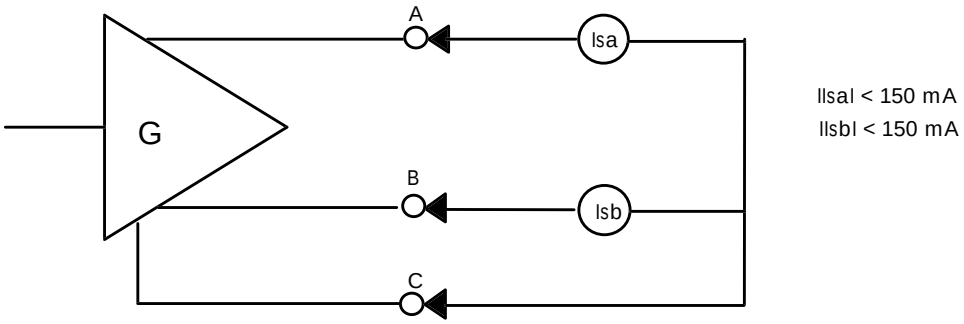
Figure 7

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.3.2.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.2.3 Generator output current limit

When the generator points A and B are both short circuited to point C, the currents flowing through point A and through point B shall not exceed 150 milliamperes, for either binary state (see figure 8):



NOTE: This requirement is based upon CCITT Recommendation V.10, subclause 5.2.3 and NET 1, First Edition (1988), subclause 8.1.1.2 in order to determine the potential for harm of a public network interface by a terminal whose technical characteristics may cause misoperation or damage to that network, by excessive electrical signals that would have no effect on humans which fall outside the scope of Directive 73/23/EEC.

Figure 8

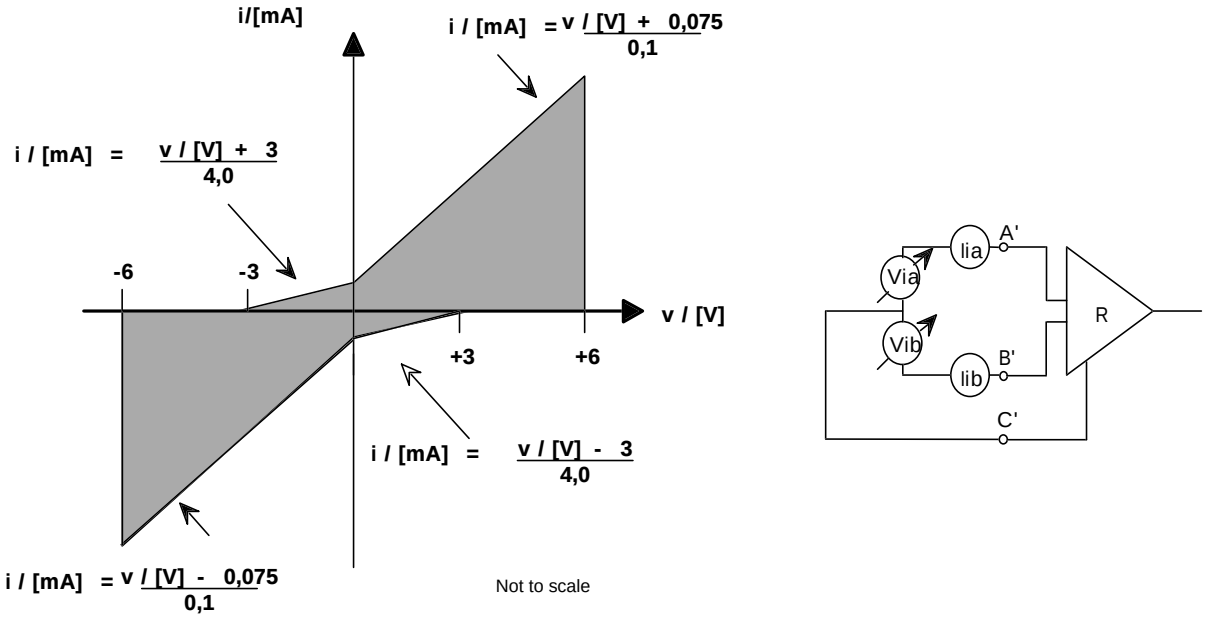
Compliance shall be verified in accordance with the test specified in Annex A, subclause A.3.3.

Justification: Directive 91/263/EEC, Article 4(d).

6.4.2.4 Receiver input voltage - current limit

The receiver, when a voltage source (Via) connected between points A' and C', is varied between -6,0 volts and +6,0 volts (whilst point B' is maintained at 0 volts), the current flow through point A' shall remain within the shaded range shown in figure 9.

A voltage source (Vib) connected between points B' and C', is then varied between -6,0 volts and +6,0 volts (whilst point A' is maintained at 0 volts), the current flow through point B' shall continue to remain within the shaded range shown in figure 9.



NOTE: This requirement is based upon CCITT Recommendation V.11, subclause 6.2 and NET 1, First Edition (1988), subclause 8.1.1.2 in order to determine the ability of terminal equipment to establish interworking with public networks under minimum and maximum load conditions.

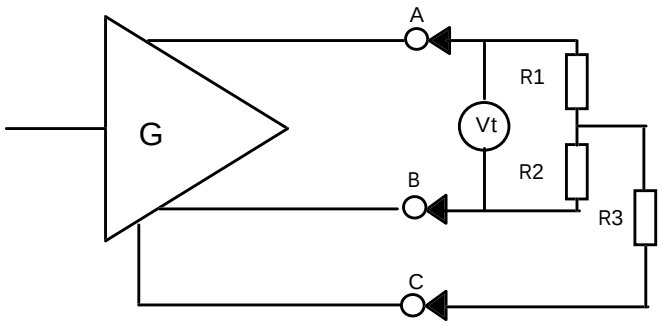
Figure 9

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.3.4.

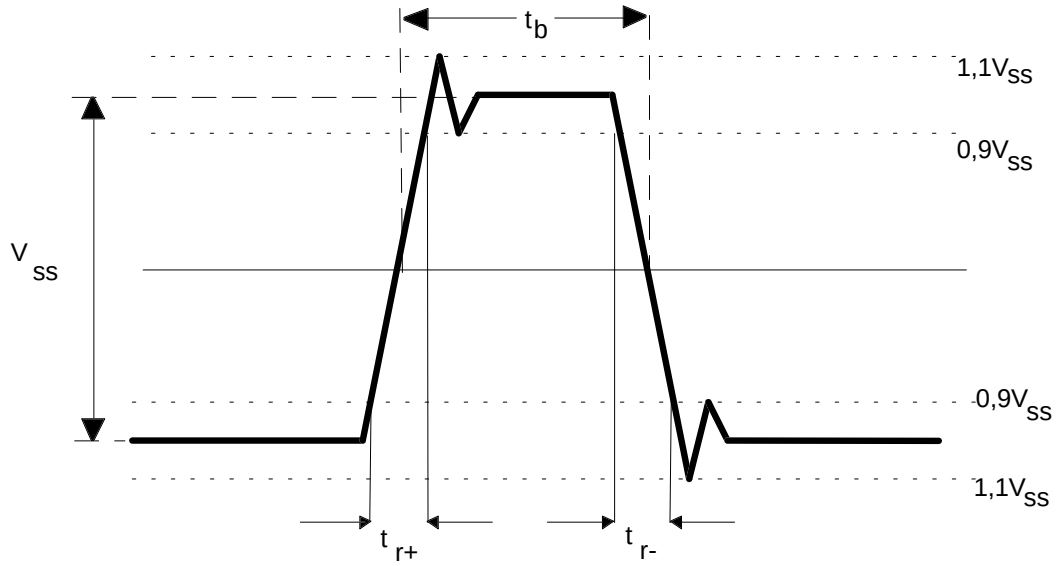
Justification: Directive 91/263/EEC, Article 4(f).

6.4.2.5 Generator output rise time

The generator when connected to the test circuit shown in test specification in Annex A, subclause A.3.6, during transitions from one binary state to the other, the time taken for the differential voltage measured between points A and B to pass between points at which, for each binary state, it is 90 % of its steady state value for data signalling rates up to 1 920 kbit/s, less than or equal to 0,3 of the nominal duration of a bit. For the purposes of this requirement, transient signals are ignored (see figure 10).



R1 = R2 = R3 = 50 ohms
R1 & R2 = matched



V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit for Tb ≥ 50 µs, Tr ≤ 0,3 Tb and for Tb < 50 µs, Tr ≤ 0,1 Tb.

NOTE: This requirement is based upon CCITT Recommendation V.11, subclause 5.3 and NET 1, First Edition (1988), subclause 8.1.1.2 in order to determine the ability of terminal equipment to establish interworking with public networks under ideal load conditions by determining the signal rise time between significant signal states.

Figure 10

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.3.5.

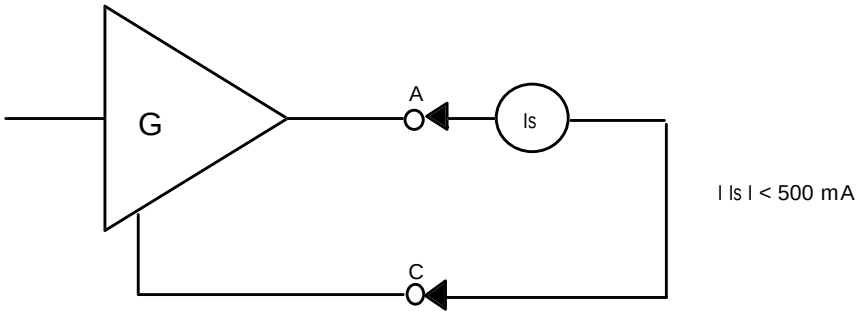
Justification: Directive 91/263/EEC, Article 4(f).

6.4.3 Electrical requirements for attachment to CCITT Recommendation V.28 interchange circuits

Where an interface utilises different electrical characteristics on adjacent pins, which are not applicable to subclause 6.4.3, then those essential requirements of subclauses 6.4.1, 6.4.2 or 6.4.4 shall apply.

6.4.3.1 Generator output current short circuit limit

The generator shall not be damaged and its output current shall not exceed 0,5 Amperes with a short circuit applied between the generator points A and C over a 60 second period (see figure 11).



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 4, first paragraph and NET 2, First Edition (1988), Annex B, subclauses B.1.1 and B.1.2 in order to determine the potential for harm of a public network interface by a terminal whose technical characteristics may cause misoperation or damage to that network, by excessive electrical signals that would have no effect on humans which fall outside the scope of Directive 73/23/EEC.

Figure 11

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.1.

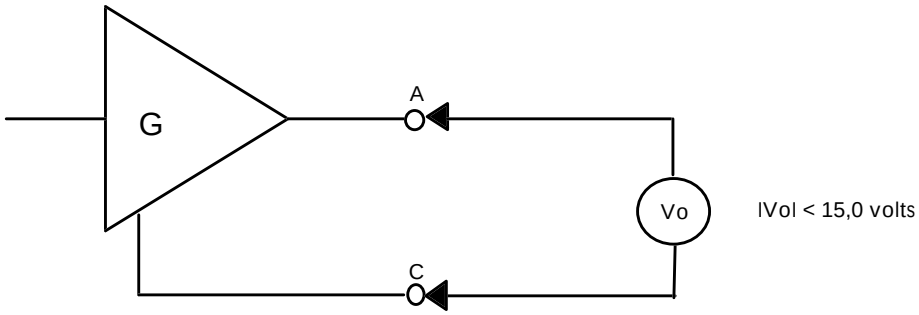
Justification: Directive 91/263/EEC, Article 4(d).

6.4.3.2 Generator open circuit output voltage limit

The open circuit voltage (see figure 12) shall not exceed either:

a) 15 volts between the generator points A and C; or

b) 25 volts between the generator points A and C.



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 4, second paragraph and NET 2, First Edition (1988), Annex B, subclause B.1.3 in order to determine the ability of terminal equipment to establish interworking with public networks under a minimum load condition. The inclusion of the 25 volt requirement is to allow for equipment practice that has not migrated to revised CCITT/ITU-T recommended limits.

Figure 12

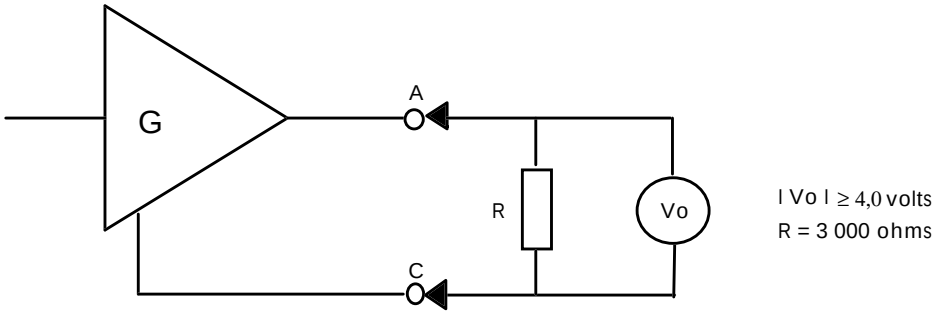
Compliance for generators declared as meeting a), shall be verified in accordance with the test specified in Annex A, subclause A.4.2. **and** the requirement specified in subclause 6.4.3.4 **shall not** apply.

Compliance for generators declared as meeting b) **shall meet** the requirement in subclause 6.4.3.4.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.3 Generator output voltage limit under maximum load

The output voltage shall be greater than or equal to 4,0 volts, when terminated in a 3 000 ohm non-reactive impedance between generator points A and C (see figure 13).



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 4, third paragraph and NET 2, First Edition (1988), Annex B, subclause B.1.4 in order to determine the ability of terminal equipment to establish interworking with public networks under a maximum load condition. The 4,0 volt limit is to allow for CCITT Recommendation V.28 to V.10 interworking where a V.10 generator has a volt of ≥ 4,0 volt into a 3 000 ohms load whereas a corresponding V.28 generator should work into a V.10 load of 3 077 ohms within the limits of 0,3 volt < Vin < 12,0 V.

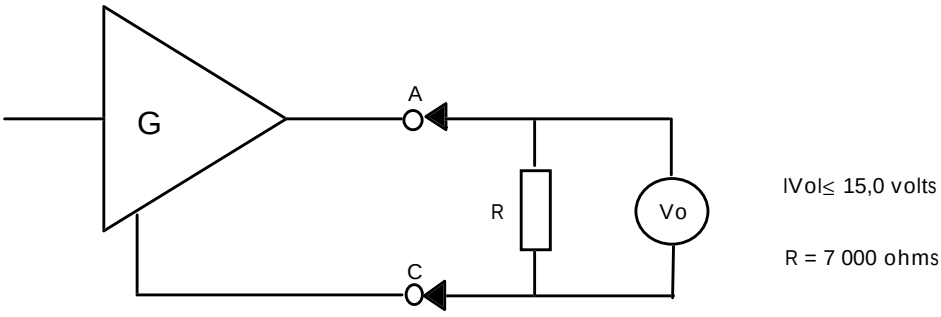
Figure 13

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.3.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.4 Generator output voltage limit under minimum load

The output voltage shall be less than or equal to 15 V when terminated in a 7 000 ohm non-reactive impedance between the generator points A and C (see figure 14).



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 4, third paragraph and NET 2, First Edition (1988), Annex B, subclause B.1.5 in order to determine the ability of terminal equipment to establish interworking with public networks under a minimum load condition.

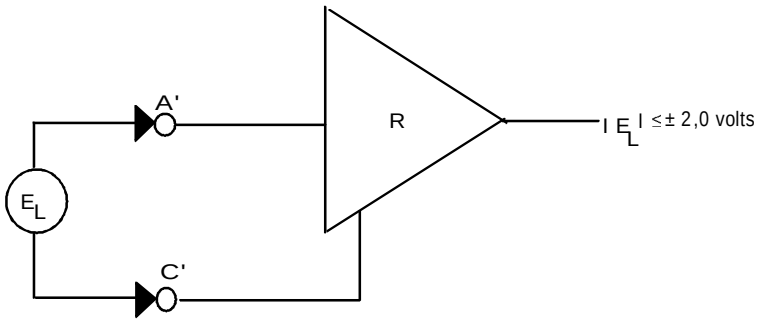
Figure 14

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.4.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.5 Receiver maximum open circuit voltage limit

The open circuit voltage of a receiver between points A' and C' shall be less than or equal to plus or minus 2,0 V when disconnected from a generator source (see figure 15).



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 3, third paragraph and NET 2, First Edition (1988), Annex B, subclause B.2.2. in order to determine the ability of terminal equipment to establish interworking with public networks by ensuring that the bias voltages acting upon a received signal do not shift the significant signal states to within the transition region.

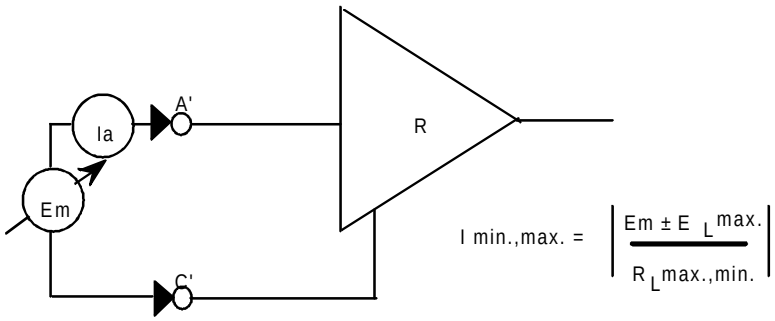
Figure 15

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.5.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.6 Receiver resistance

The receiver resistance shall have a minimum value of 3 000 ohms and a maximum value of 7 000 ohms between points A' and C'.



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 3, second paragraph and NET 2, First Edition (1988), Annex B, subclause B.3.1 in order to determine the ability of terminal equipment to establish interworking with public networks by determining the minimum and maximum load conditions of the receiver.

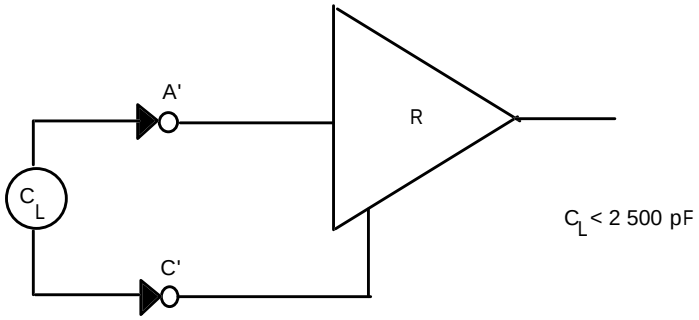
Figure 16

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.6.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.7 Receiver maximum shunt capacitance

The total effective shunt capacitance shall not exceed 2 500 pF between the receiver points A' and C' (see figure 17).



NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 3, fourth paragraph and NET 2, First Edition (1988), Annex B, subclause B.2.3 in order to determine the ability of terminal equipment to establish interworking with public networks by determining the maximum capacitive load conditions.

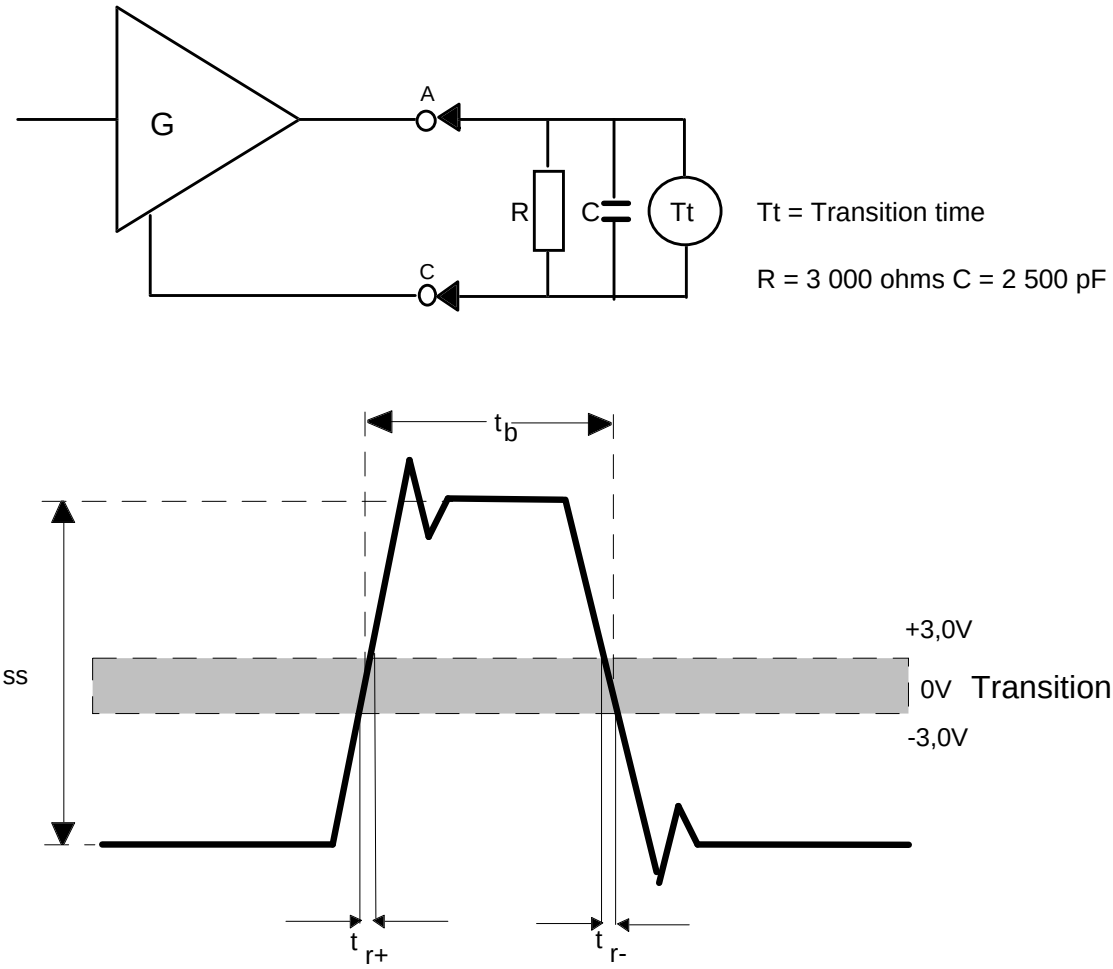
Figure 17

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.7.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.8 Generator maximum transition time

The time required for the binary signal to traverse the transition region during a change in signal state shall not exceed one millisecond or 3 % of the nominal element period, whichever is the lesser between the generator points A and C (see figure 18).



V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit.

NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 6, paragraph 4 and NET 2, First Edition (1988), Annex B, subclause B.3.2 in order to determine the ability of terminal equipment to establish interworking with public networks when the change between significant signalling states are subject to maximum load conditions. In demonstrating compliance with this requirement, CCITT Recommendation V.28, Clause 4, paragraphs 3 and 4 places upon a generator the worst case load condition of 3 000 ohms and 2 500 pF in parallel.

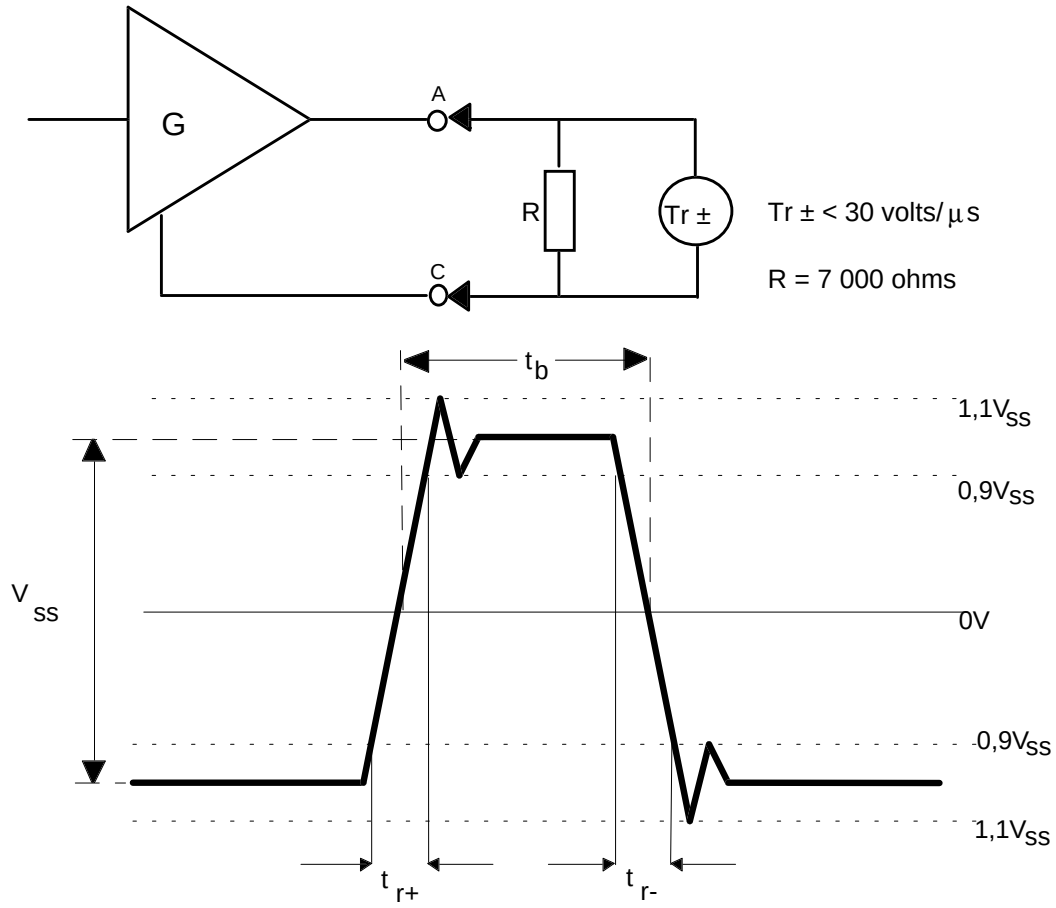
Figure 18

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.8.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.3.9 Generator maximum instantaneous rate of voltage change

The instantaneous rate of voltage change shall not exceed 30 v per microsecond within the 10 % to 90 % period of the transition region of a signal waveform, when terminated in a 7 000 ohm non-reactive impedance between the generator points A and C (see figure 19).



V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit.

NOTE: This requirement is based upon CCITT Recommendation V.28, Clause 6, paragraph 5 and NET 2, First Edition (1988), Annex B, subclause B.3.4 in order to determine the ability of terminal equipment to establish interworking with public networks (with fast signal transitions), without undue interference to adjacent signal transfer or signal control interface circuits.

Figure 19

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.4.9.

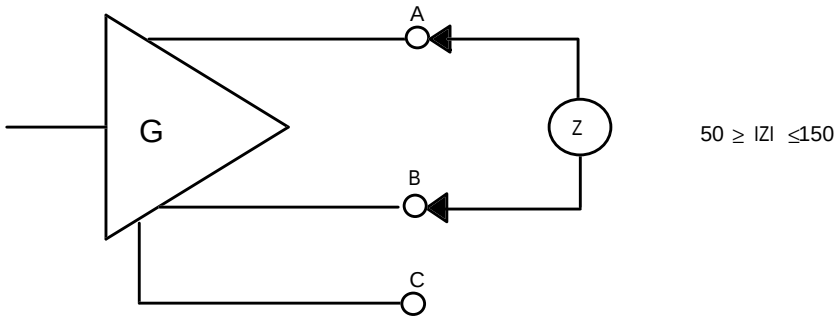
Justification: Directive 91/263/EEC, Article 4(f).

6.4.4 Electrical requirements for attachment to CCITT Recommendation V.35 interchange circuits

Where an interface utilises different electrical characteristics on adjacent pins, which are not applicable to subclause 6.4.4, then those essential requirements stated in subclauses 6.4.1 or 6.4.2 or 6.4.3 shall apply.

6.4.4.1 Generator source impedance

The source impedance shall be 100 ohms plus or minus 50 ohms between the generator points A and B (see figure 20).



NOTE: This requirement is based upon CCITT Recommendation V.35, Annex 2, subclause 2.3, paragraph (a) and NET 2, First Edition (1988), Annex C, subclause C.1.1 in order to determine the ability of terminal equipment to establish interworking with public networks within minimum and maximum source impedance conditions of a generator.

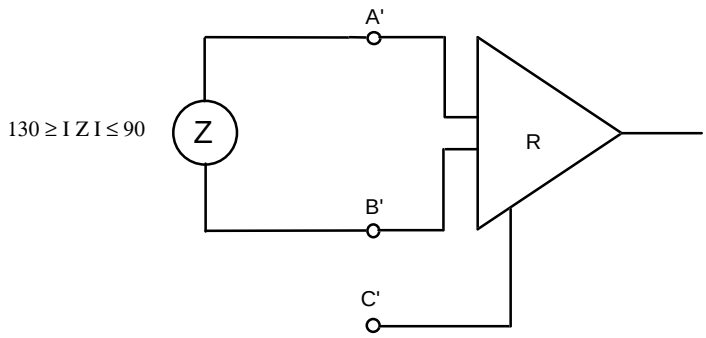
Figure 20

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.5.1.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.4.2 Receiver input impedance

The input impedance shall be 100 ohms plus 30 ohms or minus 10 ohms between the receiver points A' and B' (see figure 21).



NOTE: This requirement is based upon CCITT Recommendation V.35, Annex 2, subclause 2.4, paragraph (a) and NET 2, First Edition (1988), Annex C, subclause C.3.1 in order to determine the ability of terminal equipment to establish interworking with public networks under minimum and maximum impedance conditions for a load. CCITT Recommendation V.35 specifies a limit of 100 ohms ± 10 ohms at the receiver chip interface (this is substantially resistive in the frequency range of operation), without any cable considerations being specified. The above requirement has been varied from the CCITT Recommendation V.35 value, to give an allowance for the longest interconnection means to the DCE.

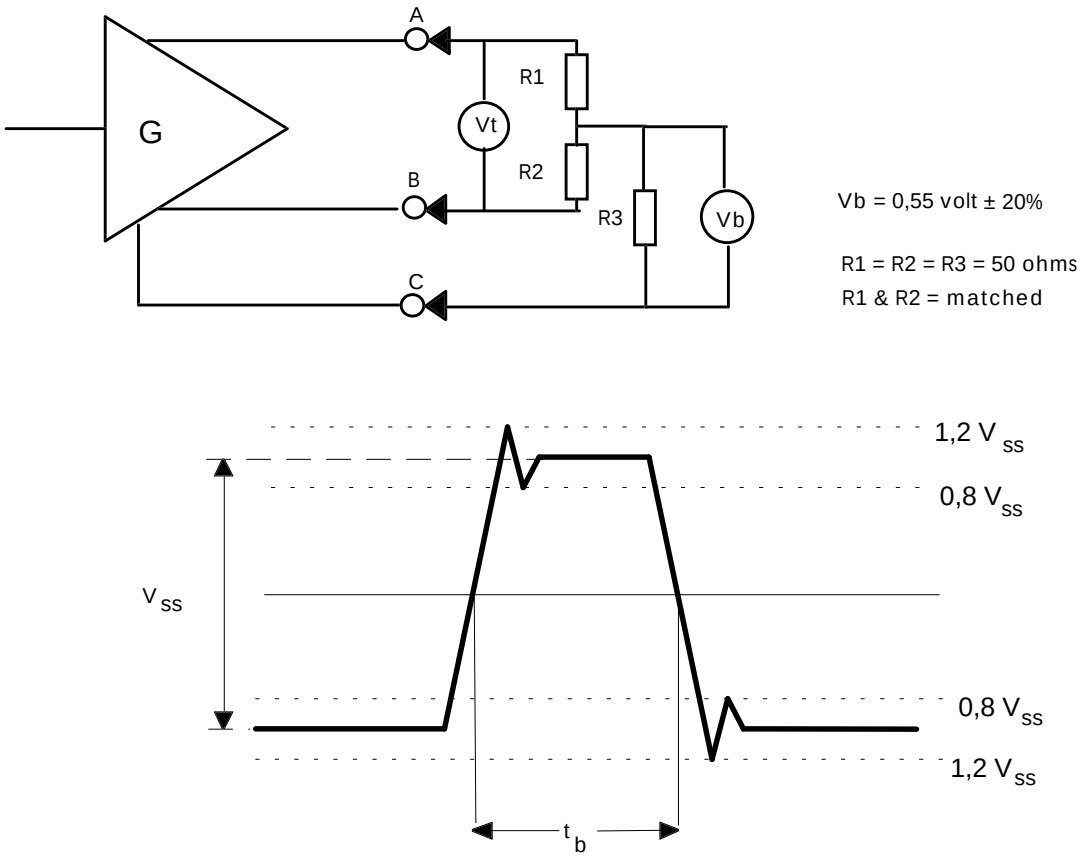
Figure 21

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.5.2.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.4.3 Generator output signal balance

A generator terminated with a 100 ohm non-reactive impedance shall have a terminal-to-terminal voltage of 0,55 volt ± 20 % across points A and B when A is positive to B when binary 0 is transmitted and the conditions are reversed to transmit binary 1 (see figure 22).



V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit.

NOTE: This requirement is based upon CCITT Recommendation V.35, Annex 2, subclause 2.3, paragraph (c) and NET 2, First Edition (1988), Annex C, subclause C.1.3 in order to determine the ability of terminal equipment to establish interworking with public networks under ideal load conditions by verifying the amount of differential balance presented by the generator.

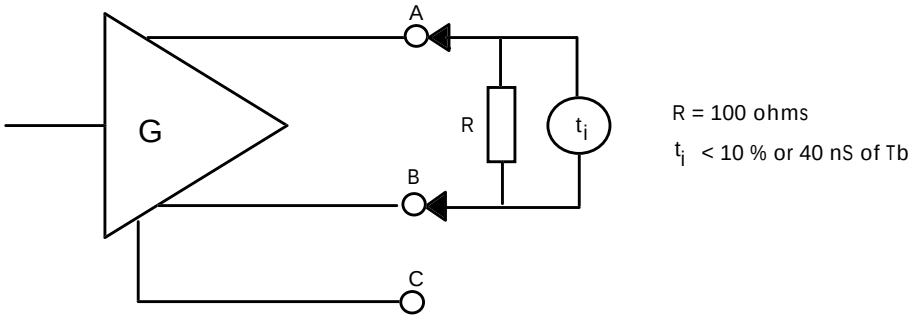
Figure 22

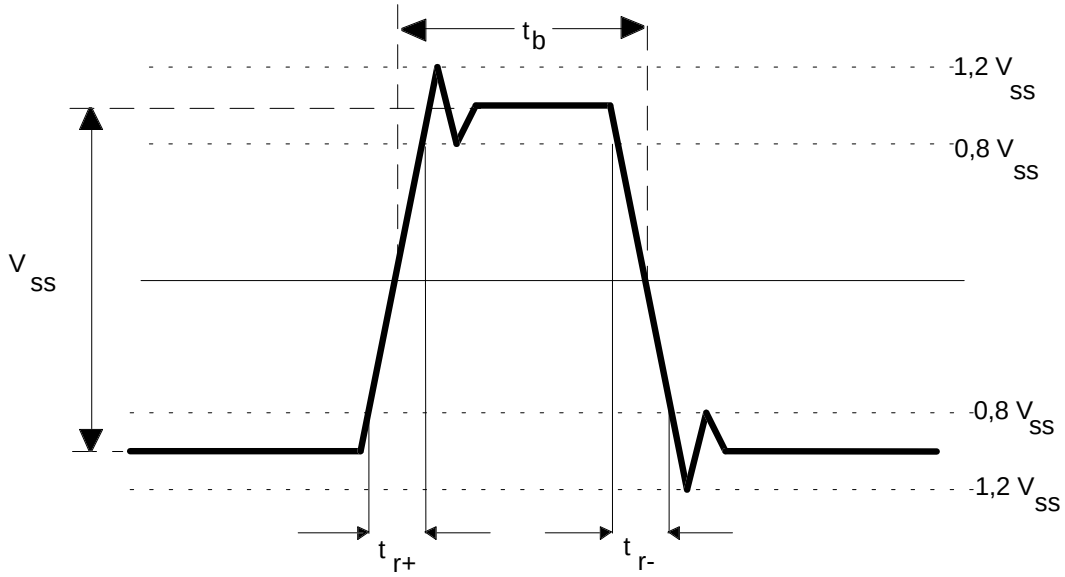
Compliance shall be verified in accordance with the test specified in Annex A, subclause A.5.3.

Justification: Directive 91/263/EEC, Article 4(f).

6.4.4.4 Generator maximum transition time

A generator terminated with a 100 ohm non-reactive impedance shall have a transition time of less than 10 % or 40 nS of the nominal duration of a signal element, whichever is the greater, between points A and B (see figure 23).





V_{SS} = Voltage difference between steady-state signal conditions.
Tb = Nominal duration of a bit Tr ≤ 40 ns Tb or Tr ≤ 0,1 Tb.

NOTE: This requirement is based upon CCITT Recommendation V.35, Annex 2, subclause 2.3, paragraph (d) and NET 2, First Edition (1988), Annex C, subclause C.1.4 in order to determine the ability of terminal equipment to establish interworking with public networks under ideal load conditions. The 1 % limit recommended in CCITT Recommendation V.35 has been relaxed to 10 %, in order to align with CCITT Recommendation V.11 rise times, for similar data rates using the ISO 2593 [11] connector. The lower limit of 40 nS remains unchanged.

Figure 23

Compliance shall be verified in accordance with the test specified in Annex A, subclause A.5.4.

Justification: Directive 91/263/EEC, Article 4(f).

6.5 Layer 2 (link layer) requirements for attachment to CCITT Recommendation X.25 interfaces

Compliance to Layer 2 (link layer) shall be determined by measurement for each declared port type, intended for operation, by the application of the test procedures specified in Annex A, Clause A.6.

6.5.1 Link set-up

The DTE shall reach the information transfer phase by one or more link set-up methods using either DTE or DCE initiated Set Asynchronised Balanced Mode (SABM) or Set Asynchronised Balanced Mode Extended (SABME) start, DTE initiated Disconnect (DISC) start or DCE solicited Disconnected code (DM) start.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.4.4.1 and NET 2, First Edition (1988), subclause 9.1.

Compliance shall be verified in accordance with meeting the requirements given in subclauses 6.5.2, 6.5.3, 6.5.4, 6.5.5, 6.5.6, 6.5.7 and 6.5.8 only.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.2 Window rotation

The DTE in the information transfer phase shall operate using either Modulo 8 or Modulo 128 sequence numbering.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.3.2.2.1 and NET 2, First Edition (1988), subclause 9.3.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.1.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.3 Timer recovery procedures

The DTE in the information transfer phase shall recover from lost frames by initiating its timer recovery procedures.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclauses 2.2.7, 2.4.8.1 and 2.4.8.4 and NET 2 First Edition (1988), subclause 9.4.1.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.2.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.4 Incorrect Frame Check Sequence (FCS)

The DTE in the information transfer phase shall discard all frames containing an incorrect FCS.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.2.7 and NET 2, First Edition (1988), subclause 9.5.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.3.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.5 Frame abort

The DTE shall discard received aborted frames.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.3.5.2 and NET 2, First Edition (1988) subclause 9.6.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.5.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.6 Reject procedure

The DTE in the information transfer phase shall recover from loss of received information frames by using the reject procedure according to the value of the P-bit. The DTE in the information transfer phase upon receiving a reject frame shall react according to the reject procedure.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.3.4.4 and NET 2, First Edition (1988), subclause 9.8.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.6.

Justification: Directive 91/263/EEC, Article 4(f).

6.5.7 Flow control

The DTE in the information transfer phase shall implement the flow control mechanisms for Modulo 8 or Modulo 128.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 2.4.8.6 and NET 2, First Edition (1988), subclause 9.9.

Compliance shall be verified in accordance with Annex A, subclause A.6.2.7.

Justification: Directive 91/263/EEC, Article 4(f).

6.6 Layer 3 (packet layer) requirements for attachment to CCITT Recommendation X.25 interfaces

Compliance to Layer 3 (packet layer) shall be determined by measurement; using only one port type implemented by the terminal equipment, by the application of the test procedures specified in Annex A, Clause A.7. The declaration in the PICS/PIXIT shall be on the basis that the requirements in subclauses 6.6.1 to 6.6.5 are compliant for all port types tested under subclause 6.5 and not just the port type used for demonstrating compliance with subclause 6.6.

6.6.1 Restart

The DTE in information transfer phase shall be able to handle the first restart procedure, when initiated by the network, by initialising or re-initialising the packet level.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclauses 5.5 and 5.2.1 and NET 2, First Edition (1988), subclause 10.1.

Compliance shall be verified in accordance with meeting the requirements given in subclauses 6.6.2, 6.6.3, 6.6.4, 6.6.5 and 6.6.6 as declared.

Justification: Directive 91/263/EEC, Article 4(f).

6.6.2 Incoming call

With a Logical Channel in state p1, the DTE shall respond to DCE incoming call packets and shall enter state p4 and d1, except where the DTE is declared as not supporting incoming call operation then it shall reject an incoming call packet.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 4.1.3 and NET 2, First Edition (1988) subclause 10.5.

Compliance shall be verified in accordance with Annex A, subclause A.7.2.2.

Justification: Directive 91/263/EEC, Article 4(f).

6.6.3 Call request

The DTE with a logical channel set to state p1 shall send call request packets on that channel and shall enter state p4 and d1, except where the DTE is declared as not supporting outgoing call operation.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 4.1.2 and NET 2, First Edition (1988), subclause 10.6.

Compliance shall be verified in accordance with Annex A, subclause A.7.2.3.

Justification: Directive 91/263/EEC, Article 4(f).

6.6.4 Call clearing

With a Logical Channel in state p4 the DTE shall initiate and/or respond to call clearing procedures.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclauses 4.1.7 and 5.2.3 and NET 2, First Edition (1988), subclause 10.7.

Compliance shall be verified in accordance with Annex A, subclause A.7.2.4.

Justification: Directive 91/263/EEC, Article 49(f).

6.6.5 Call collision

The DTE shall correctly handle "call collision packets".

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclause 4.1.6 and NET 2, First Edition (1988), subclause 10.8.

Compliance shall be verified in accordance with Annex A, subclause A.7.2.5.

Justification: Directive 91/263/EEC, Article 4(f).

6.6.6 Permanent Virtual Circuit (PVC) operation

Where the DTE is declared as supporting Permanent Virtual Circuit (PVC) operation, it shall enter the data transfer state without using the call set up procedure.

NOTE: This requirement is based upon CCITT Recommendation X.25 [1] to [3], subclauses 4.2 and 5.5 and NET 2, First Edition (1988), subclause 10.1.

Compliance shall be verified in accordance with Annex A, subclause A.7.2.6.

Justification: Directive 91/263/EEC, Article 4(f).

Annex A (normative): TBR 2 Test specifications & procedures

A.1 Conditions of test

A.1.1 Environment for tests

Where the applicant has not declared in the PICS/PIXIT as to what environmental limits the apparatus is intended to operate within, then all tests shall be performed at an ambient temperature in the range 15°C to 35°C and at a relative humidity in the range of 25 % to 75 %, except where the applicant has declared alternative operating limits that the apparatus has been designed for. Testing shall take account of those declared limits, even though they may fall outside the scope of the ranges quoted above.

A.1.2 Power supply limitations

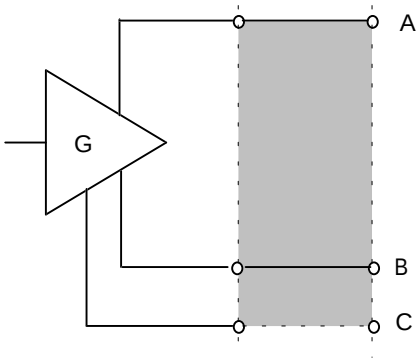
For apparatus that is directly powered from the mains supply all tests shall be carried out within 5 % of the normal operating voltage. If apparatus is powered by other means and those means are not supplied as part of the apparatus, e.g. batteries, stabilised ac supplies, dc, etc., all tests shall be carried out within the power supply limit declared by the supplier. If the power supply is ac the tests shall be conducted within 4 % of the stated frequency as declared by the supplier.

A.1.3 Test state

All requirements apply and tests are carried out with the terminal in the "power on" state unless otherwise stated.

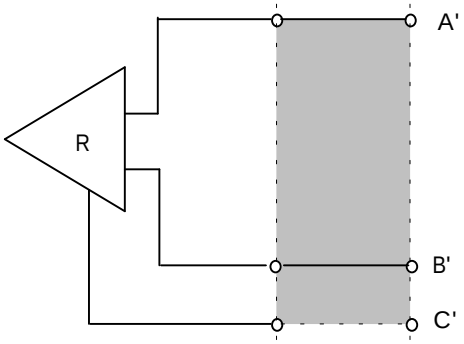
A.1.4 Test point

Tests shall be carried out at the point of connection to the DCE provided by the integral or non-integral connection means provided by the terminal equipment for connecting to the DCE. In order to demonstrate compliance with Annex A the supplier shall provide a completed PICS/PIXIT, as shown in Annex C, with a declaration on the connections supported by the DTE to NTP(DCE) interconnection cable means. Non-integral interconnection means shall prove that it can meet the requirements through the test procedures and specifications via the use of a test cable supplied by the equipment manufacturer or the supplier intending to place the terminal upon the market. The test cable shall meet the specifications given in the DTE equipment documentation as intended for use.



A and B = interchange points
C = zero volt reference
to interchange points

NOTE 1: The shaded area denotes an interconnection means, e.g. interface and connect



A' and B' = interchange points
C' = zero volt reference
to interchange points

NOTE 2: The shaded area denotes an interconnection means, e.g. interface and connecI

Figure A.1

A.1.5 Bit patterns

It may be necessary in certain instances for the tester to send specified bit patterns to the terminal equipment to ensure that a particular state is maintained. The applicant shall inform the test authority of such cases and specify the nature of the bit patterns to be sent.

A.1.6 Signal Element Timing

It is necessary for the terminal equipment to be supplied with Signal Element Timing as defined in CCITT Recommendation X.25 [1] to [3] at the data signalling rate at which the test is to be performed. For some terminal equipment it may be necessary to provide Signal Element Timing in order to carry out tests for steady state conditions.

A.1.7 Interchange circuits presented

The tester shall assume that the interchange circuits are presented on the means for connection to the DCE on the poles of the connector as specified in Annex B.

A.1.8 Condition and operation

When checking compliance with the requirements of subclauses 6.5 and 6.6, the tester shall present interchange conditions and operations in accordance with CCITT Recommendation X.25 [1] to [3]. The definitions of conditions and operations used in subclauses 6.5 and 6.6 as well as its associated compliance tests shall, unless otherwise stated, be in accordance with CCITT Recommendation X.25 [1] to [3].

A.1.9 Data signalling rates

Except where stated otherwise, the tests shall be conducted at the highest declared data signalling rate stated by the applicant. This information shall be declared by completing the PICS/PIXIT form contained in Annex C. The declaration will be on the basis that all these requirements are compliant at all data signalling rates for each port type so declared, and not just the port or port types selected for demonstrating compliance with this TBR. The declarer shall therefore ensure that the terminal equipment meets all the requirements as if they had been conducted at all the lower data signalling rates for all ports or port types.

A 1.10 Test equipment and measurement tolerances

Unless otherwise specified, test equipment used to measure voltage, current and resistance shall meet the test measurement criteria of EN 45011 [13] and shall be within a 1 % tolerance. It shall be necessary for voltmeters to have a minimum internal resistance of 5 Mohms and ammeters to have internal resistances of less than 0,5 ohms. Where oscilloscopes are used for waveform measurements, they should have a slewing rate of ≥ 50 volts per µSec and an input impedance of ≥ 5 Mohms. Tolerances on test measurements; unless otherwise specified, shall be made within an accuracy of 1 % for all voltage, current and resistance measurements specified in the test specifications in Clauses A.2 to A.5.

A.2 Test specifications for attachment to CCITT Recommendation V.10 interchange circuits

A.2.1 Generator open circuit voltage limit

Test purpose:

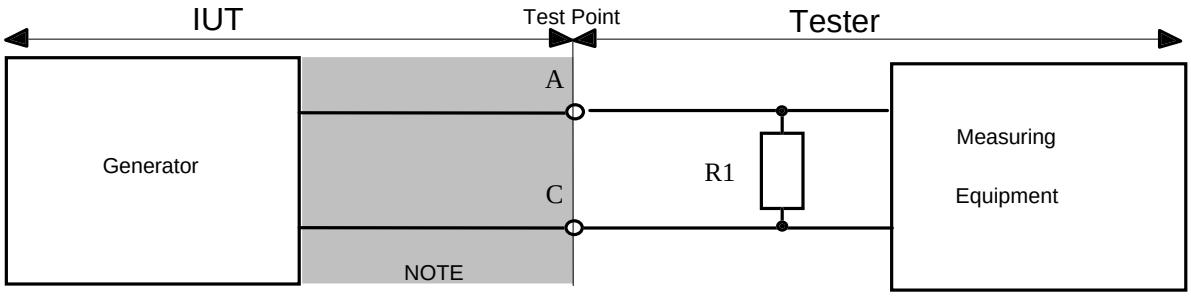
This test is to demonstrate compliance with the requirements of subclause 6.4.1.1.

Test considerations:

Where for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating, but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 3 900 ohm non-reactive impedance (R1) shall be connected between points A and C. A device for measuring dc voltage is connected across points A and C. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.2

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

The magnitude of the recorded output voltage for each applicable generator between point A and point C, shall be less than or equal to 6,0 volts for each of the binary states.

A.2.2 Generator terminated output voltage limit

Test purpose:

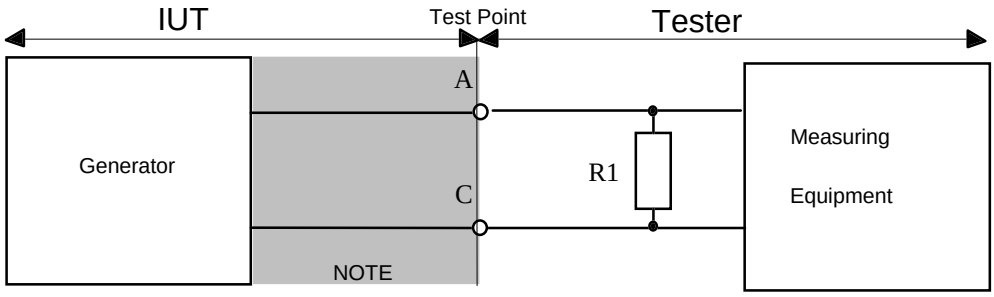
This test is to demonstrate compliance with the requirements of subclause 6.4.1.2.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating, but in this case the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 100 ohm non-reactive impedance (R1) shall be connected between points A and C. A device for measuring dc voltage is connected across points A and C. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.3

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

a) The voltage measured (Vt) shall be greater than or equal to 2 volts.

b) The voltage measured (V_t) shall be greater than or equal to 50 % of the voltage (Vo) measured in Annex A, subclause A.2.1.

c) For each of the binary states, the polarity of the voltage measured between points A and B shall be the opposite of that measured in the other binary state.

d) The difference in magnitude of voltages measured in each binary states shall be less than 0,4 volt.

A.2.3 Generator output current limit

Test purpose:

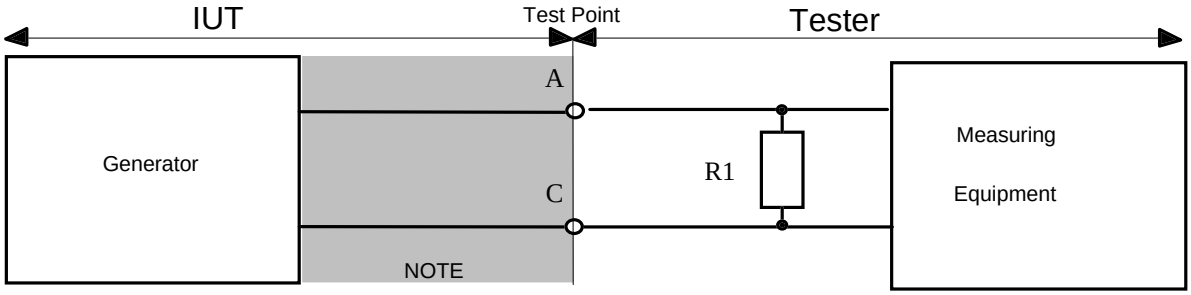
This test is to demonstrate compliance with the requirements of subclause 6.4.1.3.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions, can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 0,5 ohm non-reactive impedance (R1) is connected between points A and B. A device for measuring dc voltage is connected between points A and C. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.4

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The terminal shall stimulated to generate each of the binary states as applicable for the generator under test. When the short circuit is applied, wait 1 second before measuring the dc voltage between points A and C. Calculate, over a 60 second period the maximum current that flows during any 1 second interval. The test shall be repeated for each generator to be tested.

Expected results:

For either binary state, the currents calculated for each device shall not exceed 150 milliamperes.

A.2.4 Load receiver input voltage - current limit

Test purpose:

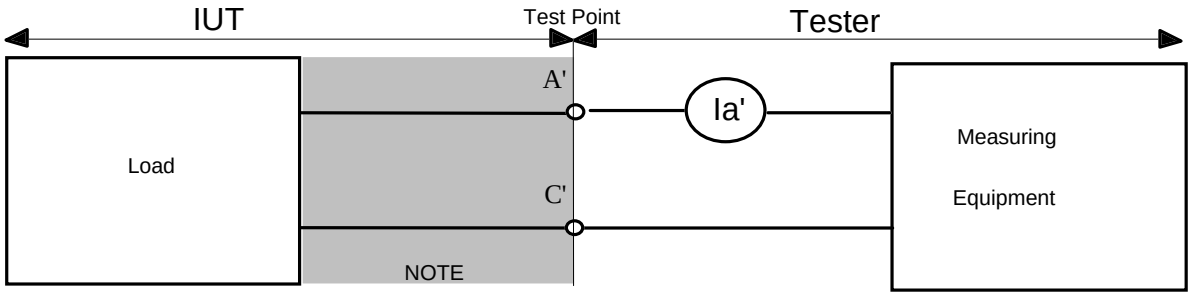
This test is to demonstrate compliance with the requirements of subclause 6.4.1.4.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions, can disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A device for measuring direct current and a source of dc voltage are connected in series between point A' and point C'. The output of the voltage source connected between point A' and C' is referred to as V_{ia}. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.5

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The voltage source (Via) shall be varied so that the magnitude of the voltage between points A' and C' is varied between -6,0 volts and +6,0 volts in 1,0 volt intervals. (The Via source is set so as to allow for any bias voltages present between points A' and C'). Measure the current at each interval.

Expected results:

The current flowing through point A' shall remain within the shaded range shown in figure 4, subclause 6.4.1.4.

A.2.5 Generator output rise time between significant signal states

Test purpose:

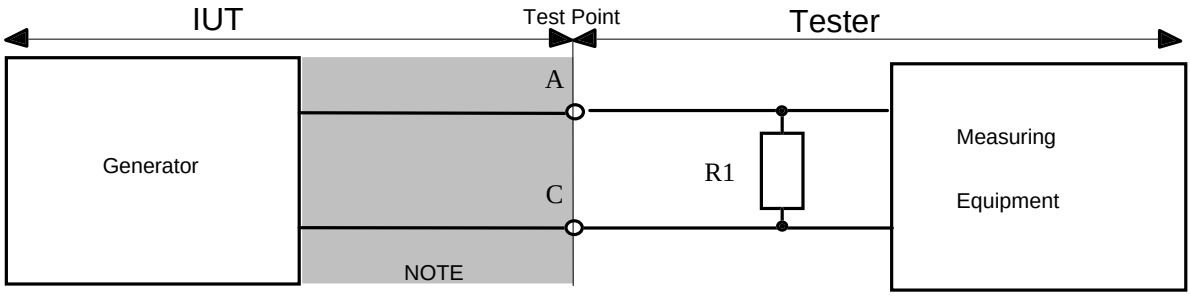
This test is to demonstrate compliance with the requirements of subclause 6.4.1.5.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 100 ohm non-reactive impedance (R1) shall be connected between points A and C. A device capable of measuring a differential voltage is connected between points A and C. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.6

IUT interface state:

The IUT shall be powered with a binary 1:1 bit pattern or with the DTE data stream set to Hex 7E/flags.

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition, shall be measured. The test shall be repeated with the polarity of the transition reversed.

Expected results:

For data signalling rates less than 20 kbit/s, the time measured shall be less than or equal to the 0,3 of the nominal duration of a bit.

For data signalling rates greater than or equal to 20 kbit/s, the time measured shall be less than or equal to 0,1 of nominal duration of a bit.

A.3 Test specifications for attachment to CCITT Recommendation V.11 interchange circuits

A.3.1 Generator open circuit voltage limit

Test purpose:

This test is to demonstrate compliance with the requirements of subclause 6.4.2.1.

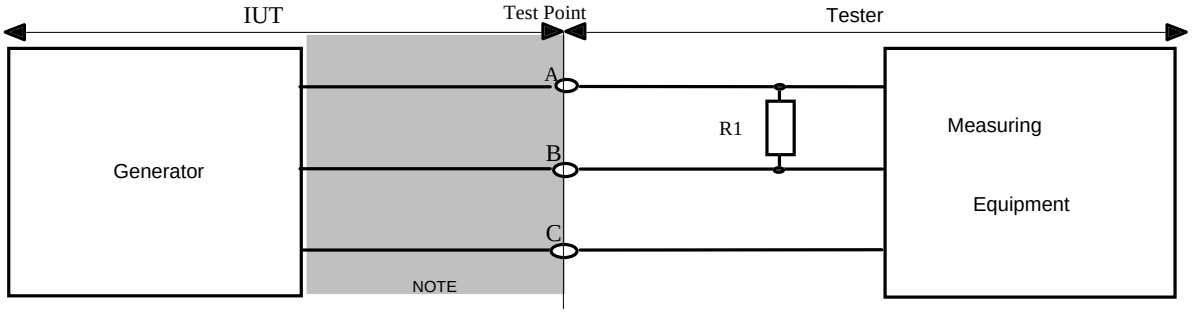
Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions shall be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.

A 3 900 ohm non-reactive impedance (R1) is connected between points A and B. A device for measuring dc voltage (Vo) is connected between points A and B. A device for measuring dc voltage (Voa) is connected between points A and C. A device for measuring dc voltage (Vob) is connected between points B and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.7

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The terminal is caused to generate each of the binary states for the generator under test. The test shall repeated for each generator to be tested. The dc voltage shall be measured between points A and B. The dc voltage shall be measured between points A and C. The dc voltage shall be measured between points B and C.

Expected results:

The magnitudes of the voltages measured between points A and B, points A and C and points B and C shall each be less than or equal to 6,0 volts for each binary state.

A.3.2 Generator terminated output voltage limit

Test purpose:

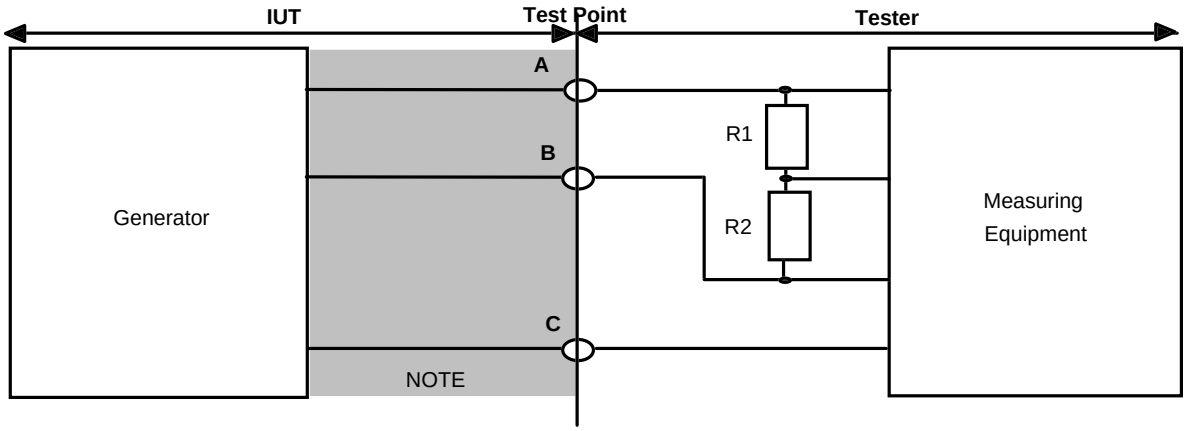
This test is to demonstrate compliance with the requirements of subclause 6.4.2.2.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions shall be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

For the tests of a) to d) in the requirements, two 50 ohm (R1 and R2), non-reactive impedances shall be connected in series between points A and B. A device for measuring dc voltage shall also be connected between points A and B. For the tests of e) and f) in the requirements, two 50 ohm (R1 and R2), non-reactive impedances shall be connected in series between points A and B. A device for measuring dc voltage is connected the centre point of the two 50 ohm impedances and point C. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.8

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The terminal is caused to generate each of the binary states for the generator under test. The test shall be repeated for each generator to be tested.

Expected results:

a) The voltage measured (Vt) shall be greater or equal to 2 volts.

b) The voltage measured (V_t) shall be greater or equal to 50 % of the voltage measured above.

c) For each of the binary states, the polarity of the voltage measured between points A and B shall be the opposite of that measured in the other binary state.

d) The differences in magnitudes of voltages measured in each binary states shall be less than 0,4 volt.

e) The voltage measured (Vos) shall be less than or equal to 3,0 volts.

f) The differences in magnitudes of voltages measured in each binary states shall be less than 0,4 volt.

A.3.3 Generator output current limit

Test purpose:

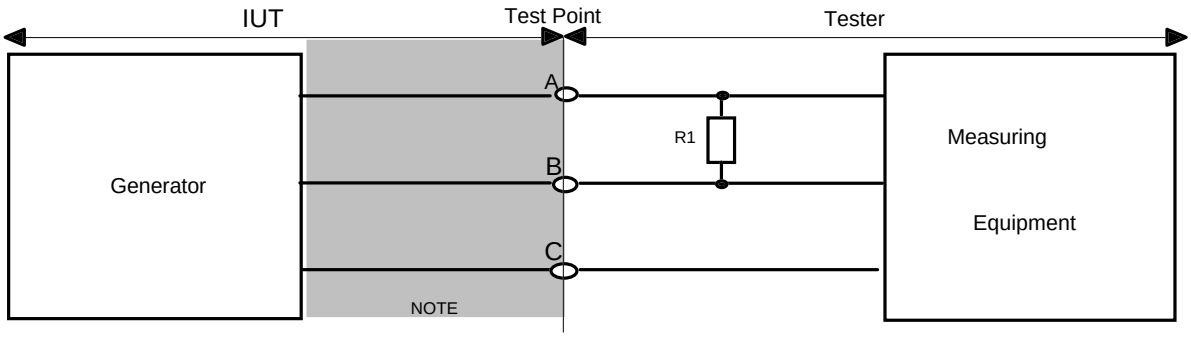
This test is to demonstrate compliance with the requirements of subclause 6.4.2.3.

Test considerations:

Where, for the purposes of testing, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 0,5 ohm non-reactive impedance (R1) shall be connected between points A and B. A device for measuring dc voltage shall be connected between points A and B. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.9

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The terminal is caused to generate each of the binary states for the generator under test. The test shall be repeated for each generator to be tested. When the short circuited is applied, wait 1 second before measuring the dc voltage between points A and B. Calculate over a 60 second period the maximum current that flows during any 1 second interval.

Expected results:

For either binary state, the currents calculated for each device shall not exceed 150 milliamperes.

A.3.4 Load receiver input voltage - current limit

Test purpose:

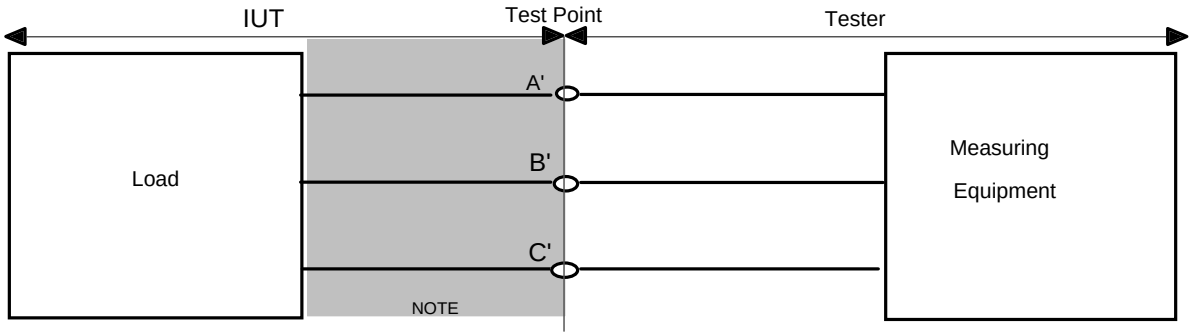
This test is to demonstrate compliance with the requirements of subclause 6.4.2.4.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A device for measuring direct current and a source of dc voltage shall be connected in series between point A' and point C' and another device for measuring direct current and a source of dc voltage shall be connected in series between point B' and point C' The output of the voltage source connected between point A' and C' is referred to as V_{ia} and that of the voltage source connected between point B' and point C' as Vib. Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.10

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The voltage source (Via) is varied so that the magnitude of the voltage between points A' and C' is varied between -6,0 volts and +6,0 volts in 1,0 volt intervals, while Vib is held at 0 volt. (The Via source shall be set so as to allow for any bias voltages present between points A' and C') Measure the current at each interval.

The voltage source (Vib) is varied so that the magnitude of the voltage between points B' and C' is varied between -6,0 volts and +6,0 volts in 1,0 volt intervals, while Via is held at 0 volt. (The Vib source shall be set so as to allow for any bias voltages present between points B' and C'). Measure the current at each interval.

Expected results:

The current flowing through point A' shall remain within the shaded range shown in figure 9.

The current flowing through point B' shall remain within the shaded range shown in figure 9.

A.3.5 Generator output rise time between significant signal states

Test purpose:

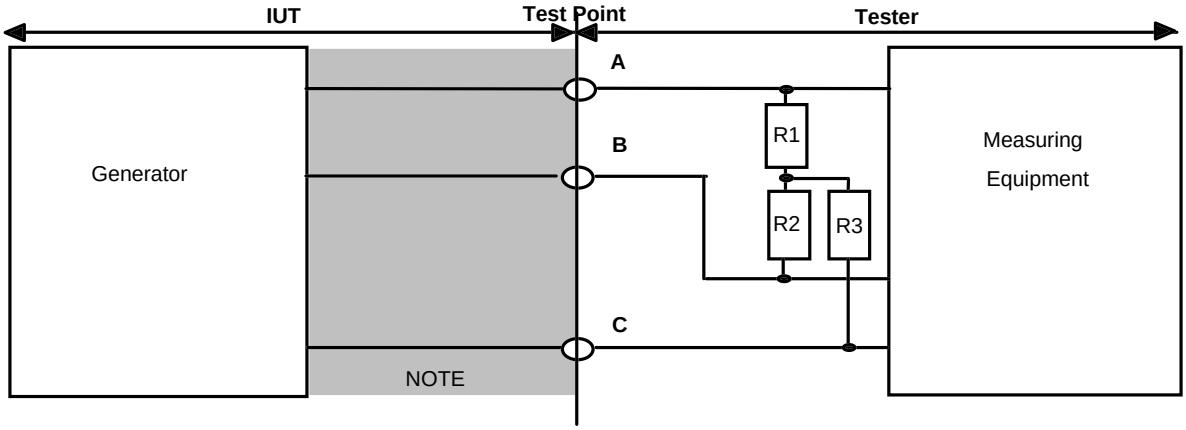
This test is to demonstrate compliance with the requirements of subclause 6.4.2.5.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

Point C shall be taken as Circuit 102a for ISO 4902 [10] and Circuit 102 for ISO 4903 [12] implementations. The resistors R_1, R2 and R3 are all 50 ohm non-reactive. A device capable of measuring a differential voltage (Vt) shall be connected between points A and B.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.11

IUT interface state:

The IUT shall be powered with binary 1:1 bit pattern or with the DTE data stream set to Hex 7E/flags.

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition, shall be measured. The test shall be repeated with the polarity of the transition reversed.

Expected results:

For data signalling rates less than 20 kbit/s, the time measured shall be less than or equal to 0,3 of the nominal duration of a bit.

For data signalling rates greater than or equal to 20 kbit/s, the time measured shall be less than or equal to 0,1 of nominal duration of a bit.

A.4 Test specifications for attachment to CCITT Recommendation V.28 interchange circuits

A.4.1 Generator output current and short circuit protection

Test purpose:

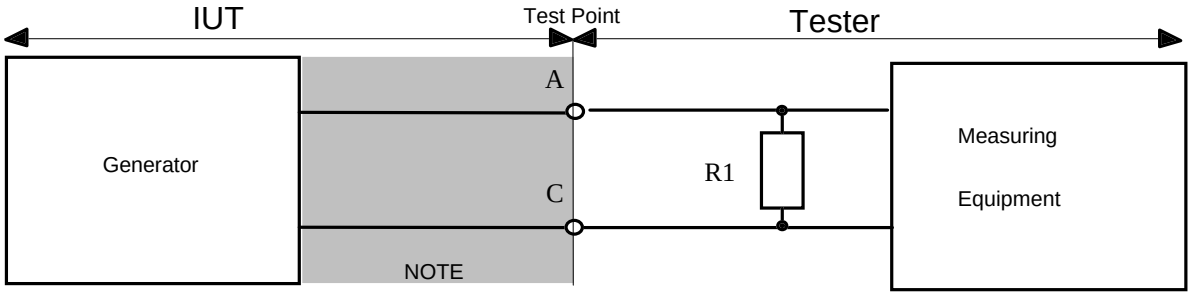
This test is to demonstrate compliance with the requirements of subclause 6.4.3.1.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT for supply with the equipment.

Test configuration:

A 0,5 ohm non-reactive impedance (R1) shall be connected between points A and C. A device for measuring dc voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.12

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The terminal shall be stimulated to generate each of the binary states as applicable for the generator under test. When the short circuited is applied, wait 1 second before measuring the dc voltage between points A and C. Calculate over a 60 second period the maximum current that flows during any 1 second interval. The test shall be repeated for each generator to be tested.

Expected results:

For either binary state, the currents calculated for each device shall not exceed 0,5 amperes and the generator shall not have sustained damaged if it then complies with the requirements of subclauses 6.4.3.3 and 6.4.3.4 after this test procedure.

A.4.2 Generator output voltage

Test purpose:

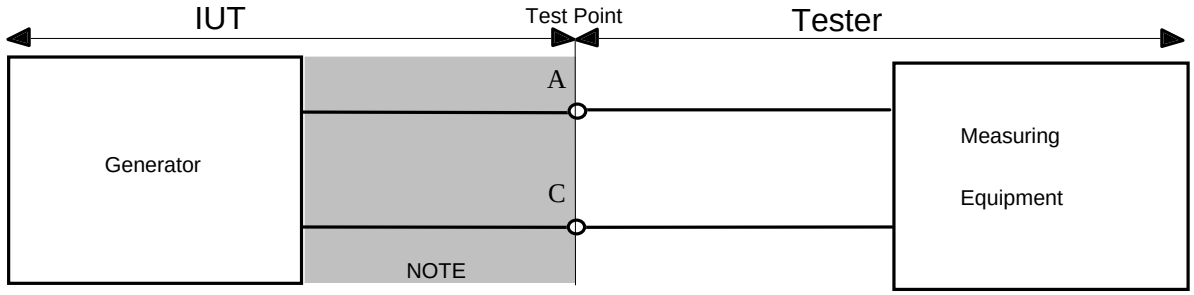
This test is to demonstrate compliance with the requirements of subclause 6.4.3.2.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT for supply with the equipment.

Test configuration:

A device for measuring dc voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.13

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

The magnitude of the recorded output voltage for each applicable generator between point A and point C, shall be less than or equal to 15,0 volts.

A.4.3 Generator output voltage under maximum load conditions

Test purpose:

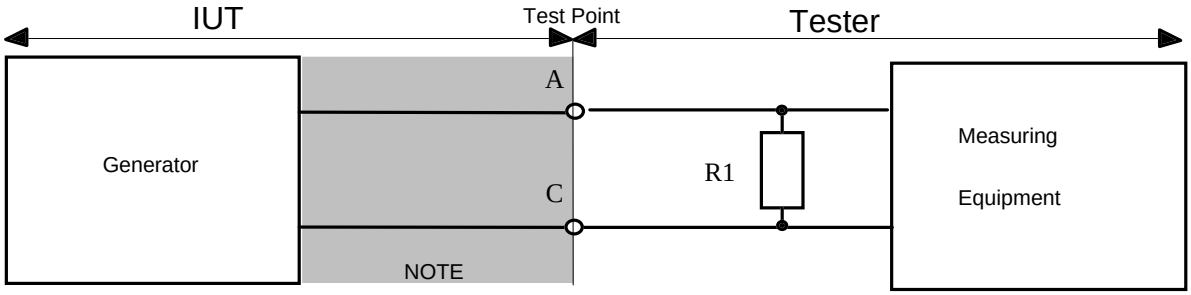
This test is to demonstrate compliance with the requirements of subclause 6.4.3.3.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 3 000 ohm non-reactive impedance (R1) shall be connected between points A and C. A device for measuring dc voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.14

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

The magnitude of the recorded output voltage for each applicable generator between point A and C shall not be less than 4,0 volts for each binary state.

A.4.4 Generator output voltage under minimum load conditions

Test purpose:

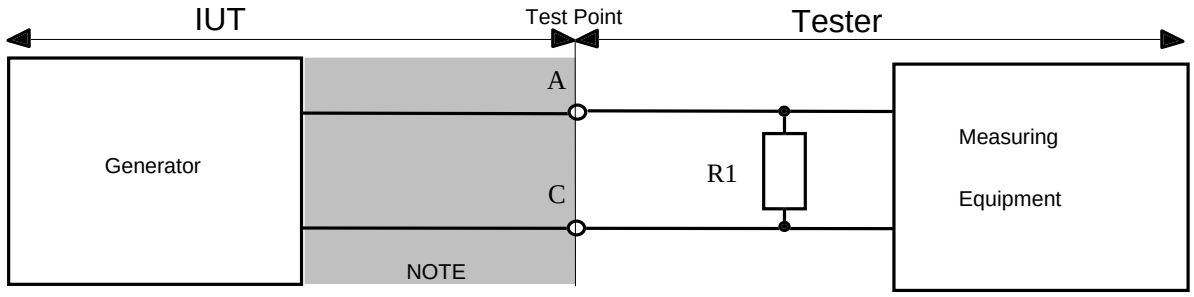
This test is to demonstrate compliance with the requirements of subclause 6.4.3.4.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT for supply with the equipment.

Test configuration:

A 7 000 ohm non-reactive impedance (R1) shall be connected between points A and C. A device for measuring dc voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.15

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

The magnitude of the recorded output voltage for each applicable generator between point A and C shall not exceed 15,0 volts for each binary state.

A.4.5 Load maximum open circuit voltage

Test purpose:

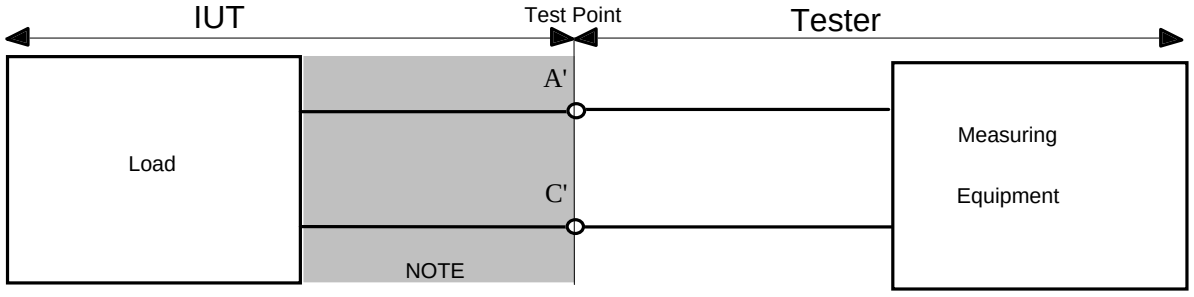
This test is to demonstrate compliance with the requirements of subclause 6.4.3.5.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT for supply with the equipment.

Test configuration:

A device for measuring dc voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.16

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The IUT shall be stimulated to generate each of the binary states as applicable for the generator under test and the results shall be recorded. The test shall then be repeated for each generator to be tested.

Expected results:

The open circuit voltage (El) shall not exceed ± 2 volts when disconnected from the generator. Compliance to this requirement shall be met if, after applying this test configuration, the open circuit voltage (El) is not exceeded.

A.4.6 Load resistance

Test purpose:

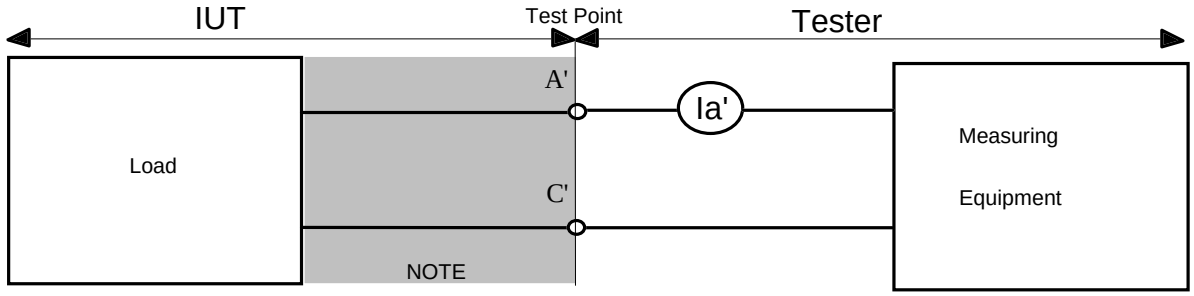
This test is to demonstrate compliance with the requirements of subclause 6.4.3.6.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT for supply with the equipment.

Test configuration:

A device for measuring direct current and a source of dc voltage shall be connected in series between point A' and point C'. The output of the voltage source connected between point A' and C' is referred to as V_{ia}.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.17

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The voltage source (Via) is varied so that the magnitude of the voltage between points A' and C' is varied between -15,0 volts to -3,0 volts and +3,0 volts to -15,0 volts in 1,0 volt intervals. (The Via source shall be set so as to allow for any bias voltages present between points A' and C'). Measure the current and calculate the load resistance at each interval.

Expected results:

The load resistance (R_L) shall have a minimum value of 3 000 ohms and a maximum value of 7 000 ohms.

A.4.7 Maximum load shunt capacitance

Test purpose:

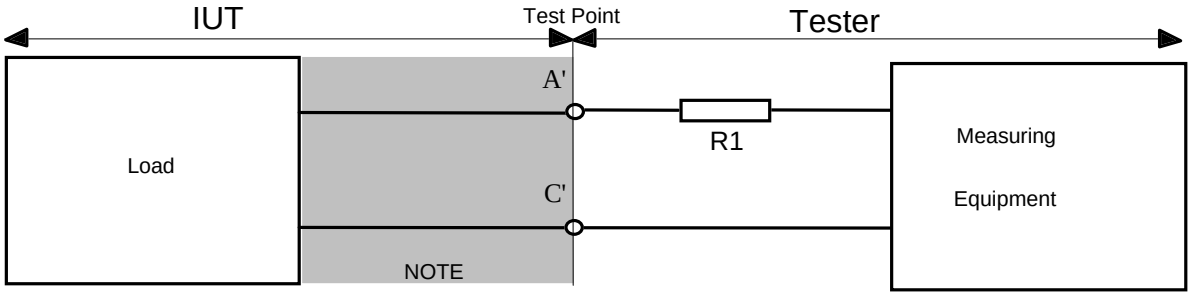
This test is to demonstrate compliance with the requirements of subclause 6.4.3.7.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 1 200 ohm non-reactive impedance (R1) shall be connected in series between point A' and a function generator output point that supplies a V_{SS} signal equal to 14,0 volts at 9 600 bit/s with respect to point C'. A device for measuring differential voltage shall be connected across points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.18

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

A function generator supplies a V_{SS} signal of 9 600 bit/s at 14,0 volts between significant signal states to the 1 200 ohm non-reactive resistor. A device for measuring the voltage between points A' and C' shall record the value of the load voltage (Vload). The actual equivalent load resistance (Rload) can then be calculated from the formula given below. During the transition from one binary state to the other, the time that elapses between the differential voltage changing between -1,0 volt and +1,0 volt or between +1,0 volt and -1,0 volt of its steady state value for the binary state that existed prior to this transition, shall be measured. Using the value of Rload found by calculation, and measuring the time taken for the signal to pass between +1,0 volt and -1,0 volt or -1,0 volt and +1,0 volt, the effective capacitance (C_L) can then be calculated as follows:

$$Rload = \frac{1200.Vload}{14,0 - Vload}$$

$$C = T / Rload \, Ln \frac{Vload - v1}{Vload - v2}$$

where T = Transition time from v1 (–1,0 volt) to v2 (+1,0 volt)

Expected results:

The total effective capacitance (C_L) shall be less than or equal to 2 500 picofarads.

NOTE: Annex D (informative) gives a similar approach by using the measurement of time delay between ± 3,0 volts and the use of a time delay/capacitance chart that is calculated for any function generator. Views are sought on both methods as to which approach should be adopted.

A.4.8 Generator maximum transition time on data interchange circuits

Test purpose:

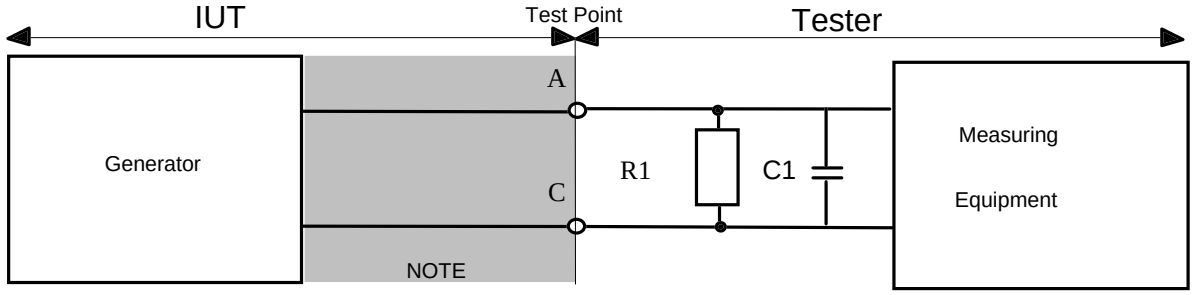
This test is to demonstrate compliance with the requirements of subclause 6.4.3.8.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions, can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 3 000 ohm non-reactive impedance (R1) shall be connected in parallel with a 2 500 pF capacitor between points A and C. A device capable of measuring a differential voltage shall be connected between points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.19

IUT interface state:

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition, shall be measured. The test shall be repeated with the polarity of the transition reversed.

Expected results:

For data signalling rates less than 20 kbit/s, the time measured shall be less than or equal to 1,0 millisecond or 3 % of the nominal duration of a bit.

A.4.9 Generator maximum instantaneous rate of voltage change

Test purpose:

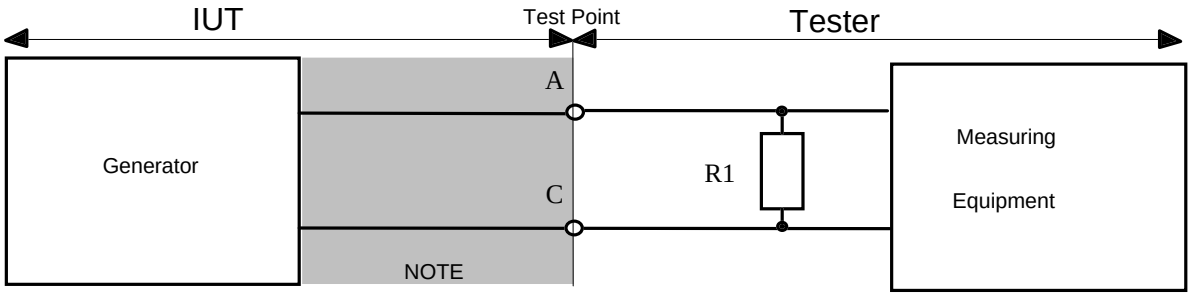
This test is to demonstrate compliance with the requirements of subclause 6.4.3.9.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 7 000 ohm non-reactive impedance (R1) shall be connected between points A and C. A device capable of measuring a differential voltage shall be connected between points A and C.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.20

IUT interface state:

The IUT shall be powered with binary 1:1 bit pattern or with the DTE data stream set to hex 7E/flags.

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition. Determine over all 1,0 volt integration period the worst value. The test shall be repeated with the polarity of the transition reversed.

Expected results:

It shall not be possible for an interchange circuit to produce an instantaneous rate of voltage change of more than 30 volts per microsecond, for data signalling rates less than 20 kbit/s.

A.5 Test specifications for attachment to CCITT Recommendation V.35 interchange circuits

A.5.1 Generator source impedance

Test purpose:

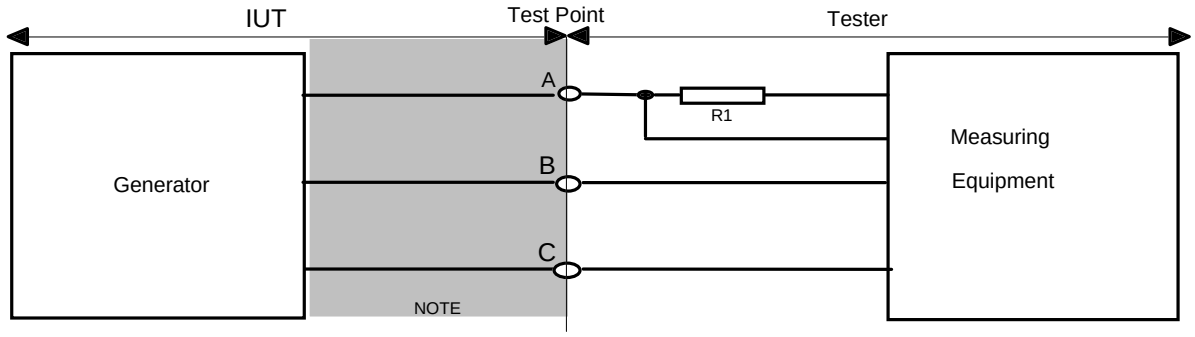
This test is to demonstrate compliance with the requirements of subclause 6.4.4.1.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 50 ohm non-reactive impedance (R1) shall be connected in series between point A and a function generator output point that supplies a 24 kHz sine wave signal with a peak to peak voltage of 550 millivolts with respect to point B (ensuring the function generator is decoupled from dc voltages). A device for measuring ac voltage shall be connected across points A and B and another device for measuring ac voltage is connected across R1.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.21

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The Function Generator supplies a 24 kHz sine wave with a peak-to-peak voltage in the range 550 mV to point A via R1. Measure V1 across R1 (the known 50 ohm resistor) and record the result. Measure V2 across the unknown source impedance and calculate the impedance using the formula below:

$$\frac{V2}{V1} \text{ x } R1 = Z \text{ (Z = (Numerical Value) (E + X) x R1 ohms)}$$

Expected results:

The generator source impedance shall be equal to or greater than 50 ohms and equal to or less than 150 ohms.

NOTE: Annex D (informative) contains an alternative test method that uses a dc measurement technique. Views are sought as to which method should be adopted.

A.5.2 Input impedance

Test purpose:

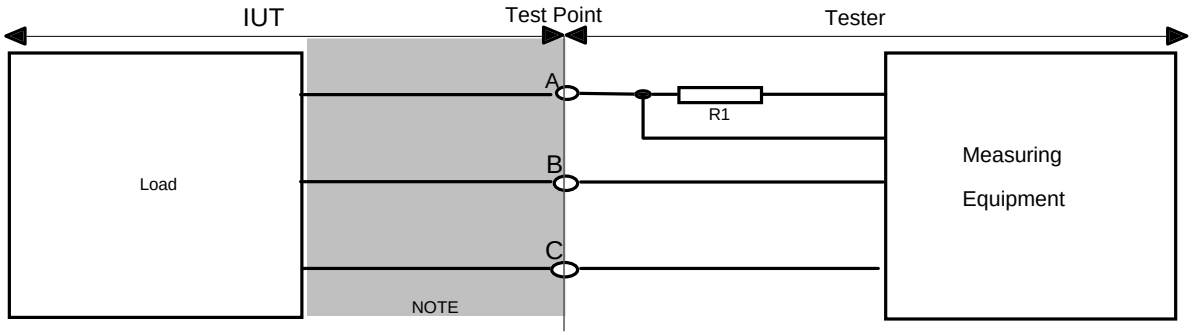
This test is to demonstrate compliance with the requirements of subclause 6.4.4.2.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 50 ohm non-reactive impedance (R1) shall be connected in series between point A and a function generator output point that supplies a 24 kHz sine wave signal with a peak-to-peak voltage of 550 millivolts with respect to point B. A device for measuring ac voltage shall be connected across points A and B and another device for measuring ac voltage shall be connected across R1.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.22

IUT interface state:

The IUT shall be powered.

Test stimulus and action:

The Function Generator supplies a 24 kHz sine wave with a peak-to-peak voltage in the range 550 mV to point A' via R1. Measure V1 across R1 (the known 50 ohm resistor) and record the result. Measure V2 across the unknown source impedance and calculate the impedance using the formula below.

$$\frac{V2}{V1} \times R1 = Z \text{ (Z = (Numerical Value) (E + X) x R1 ohms)}$$

Expected results:

The load impedance shall be equal to or greater than 90 ohms and equal to or less than 130 ohms.

NOTE: The use of a sine wave source is intended to minimise the measurement error that could result from a square wave source method. No significant differences in results should occur with the interface operating at binary 0 or with a 1:1 bit pattern provided that the function generator source is adequately decoupled from dc voltages.

A.5.3 Generator output signal balance

Test purpose:

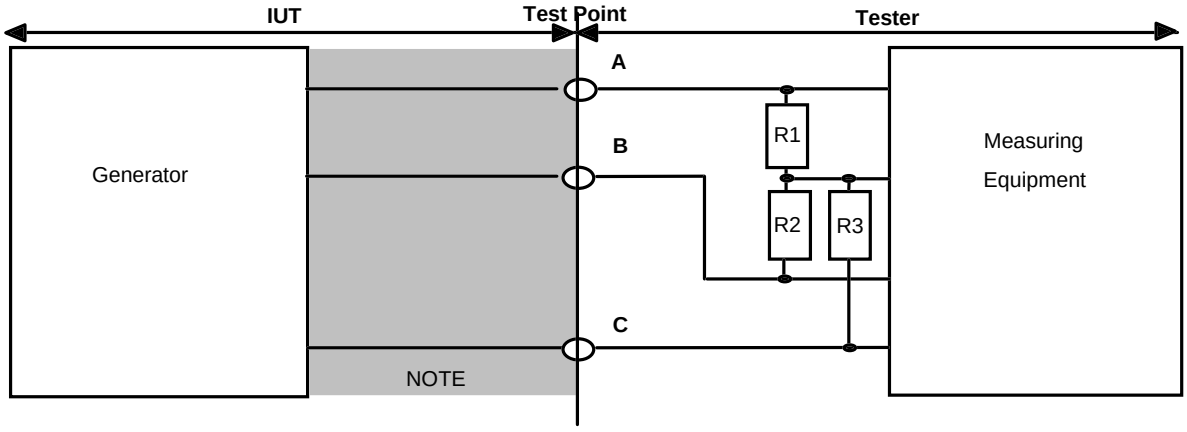
This test is to demonstrate compliance with the requirements of subclause 6.4.4.3.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

The resistors R_1, R2 and R3 are all 50 ohm non-reactive. A device capable of measuring a differential voltage (Vt) shall be connected between points A and B.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.23

IUT interface state:

The IUT shall be powered with binary 1:1 bit pattern or with the DTE data stream set to Hex 7E/flags.

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition, shall be measured. The test shall be repeated with the polarity of the transition reversed.

Expected results:

The generator, when terminated with a 100 ohms non-reactive load, shall have a terminal-to-terminal voltage of 0,55 volt ± 20 %.

A.5.4 Generator rise time

Test purpose:

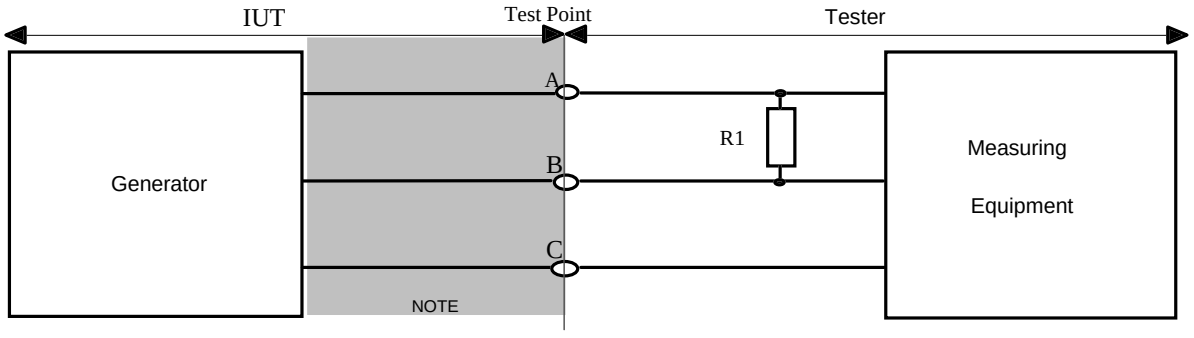
This test is to demonstrate compliance with the requirements of subclause 6.4.3.4.

Test considerations:

Where, for the purposes of the test, two or more circuits are identically implemented, the test need only be carried out on one of them. Where for a particular terminal equipment, a particular generator output state is not relevant for a specific interchange circuit, there is no requirement for that generator output state to be tested in respect of that interchange circuit. The tests are more easily performed using signals that do not make transitions from one binary state to another whilst measurement is in progress. However, these tests may be carried out using other signal patterns which the terminal is capable of generating but, in this case, the effects of transient signal conditions can be disregarded. The test shall be performed using the longest interface cable declared in the PICS/PIXIT, for supply with the equipment.

Test configuration:

A 100 ohm non-reactive impedance (R1) shall be connected between points A and B. A device capable of measuring a differential voltage shall be connected between points A and B.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure A.24

IUT interface state:

The IUT shall be powered with binary 1:1 bit pattern or with the DTE data stream set to Hex 7E/flags.

Test stimulus and action:

During the transition from one binary state to the other, the time that elapses between the differential voltage reducing to 90 % of its steady state value for the binary state that existed prior to this transition, and its reaching 90 % of the steady state value that is attained following this transition, shall be measured. The test shall be repeated with the polarity of the transition reversed.

Expected results:

The generator, when terminated with a 100 ohms resistive load, shall have a rise time of less than 10 % of the nominal duration of a signal element or 40 nS, whichever is the greater.

A.6 Layer 2 - link layer test specifications

A.7 Layer 3 - packet layer test specifications

Annex B (informative): References to other standards

B.1 Pin allocation using interface connector according to ISO 2110

Connector type and pin allocation to ISO 2110 [8] for services up to 19,2 kbit/s using a CCITT Recommendation V.24 interface with either CCITT Recommendation V.10 or V.28 electrical characteristics.

Table B.1: Pin allocation using interface connector according to ISO 2110

Item No	Pin Allocation	ISO reference	CCITT reference	Status Note
1	Circuit 102 on pin 7	ISO 2110	--	1
2	Circuit 103 on pin 2	ISO 2110	V.28	1
3	Circuit 104 on pin 3	ISO 2110	V.28	1
4	Circuit 105 on pin 4	ISO 2110	V.28/V.10	1
5	Circuit 106 on pin 5	ISO 2110	V.28/V.10	2
6	Circuit 107 on pin 6	ISO 2110	V.28/V.10	2
7	Circuit 108/1 on pin 20	ISO 2110	V.28/V.10	2
8	Circuit 109 on pin 8	ISO 2110	V.28/V.10	2
9	Circuit 114 on pin 15 ISO 2110	ISO 2110	V.28	1
10	Circuit 115 on pin 17 ISO 2110	ISO 2110	V.28	1
11	Circuit 140 on pin 21 ISO 2110	ISO 2110	V.28/V.10	2
12	Circuit 141 on pin 18 ISO 2110	ISO 2110	V.28/V.10	2
13	Circuit 142 on pin 25 ISO 2110	ISO 2110	V.28/V.10	2

NOTE 1: Primary circuits that shall be implemented as data transfer functions are given the category "mandatory essential" (me).

NOTE 2: Secondary circuits that, if implemented as data control functions, are given the category "optionally essential" (oe).

B.2 Pin allocation using interface connector according to ISO/IEC 11569

Connector type and pin allocation to ISO/IEC 11569 [9] for services up to 19,2 kbit/s using a CCITT V.24 interface with either CCITT Recommendation V.10 or V.28 electrical characteristics or for services up to 1 920 kbit/s with CCITT Recommendation V.11 electrical characteristics.

Table B.2: Pin allocation using interface connector according to ISO/IEC 11569

Item No	Pin Allocation	V.10/V.11* >20kbit/s (NOTE 3)	V.28 X.21bis (NOTE 3)	Reference	Status Note
1	1	Shield	Shield	ISO/IEC 11569	--
2	2	103A	103	ISO/IEC 11569	NOTE 1
3	3	104A	104	ISO/IEC 11569	NOTE 1
4	4	105A/133A	105	ISO/IEC 11569	NOTE 1
5	5	106A	106	ISO/IEC 11569	NOTE 2
6	6	107	107	ISO/IEC 11569	NOTE 2
7	7	102A	102	ISO/IEC 11569	NOTE 1
8	8	109	109A	ISO/IEC 11569	NOTE 2
9	9	115B	F	ISO/IEC 11569	NOTE 2
10	10	109B	F	ISO/IEC 11569	NOTE 2
11	11	113B	F	ISO/IEC 11569	NOTE 2
12	12	114B	F	ISO/IEC 11569	NOTE 1
13	13	106B	F	ISO/IEC 11569	NOTE 2
14	14	103B	F	ISO/IEC 11569	NOTE 1
15	15	114A	114	ISO/IEC 11569	NOTE 1
16	16	104B	F	ISO/IEC 11569	NOTE 1
17	17	115A	115	ISO/IEC 11569	NOTE 1
18	18	141	141	ISO/IEC 11569	NOTE 2
19	19	105B/133B	F	ISO/IEC 11569	NOTE 1
20	20**	108	108	ISO/IEC 11569	NOTE 2
21	. 21	140	140	ISO/IEC 11569	NOTE 2
22	22	107	107	ISO/IEC 11569	NOTE 2

(continued)

Table B.2: Pin allocation using interface connector according to ISO/IEC 11569 (concluded)

Item No	Pin Allocation	V.10/V.11* >20 kbit/s (NOTE 3)	V.28 X.21bis (NOTE 3)	Reference	Status Note
23	23	102A	102	ISO/IEC 11569	NOTE 1
24	24	109A	109	ISO/IEC 11569	NOTE 2
25	25	115B	F	ISO/IEC 11569	NOTE 2
26	26	NC	NC	ISO/IEC 11569	--

NOTE 1: Primary circuits that shall be implemented as data transfer functions are given the category "mandatory essential" (me).

NOTE 2: Secondary circuits that, if implemented as data control functions, are given the category "optionally essential" (oe).

NOTE 3: Where the circuit numbers are followed by an **A** or a **B** it indicates both sides of a balanced electrical circuit. This type of circuit should have both sides (the A and B) assigned to a twisted pair in the interconnecting cable to minimise cross talk.

F = Contact reserved for international use.
NC = No connection.
* = At present there is no pin assignment for V.10/V.11 Circuit 102 only 102A and 102B.
** = Pin 20 may be either circuit 108/1 or 108/2.

B.3 Pin allocation using interface connector according to ISO 4902

Connector type and pin allocation to ISO 4902 [10] for services up to 1 920 kbit/s using a CCITT Recommendation V.36 interface with CCITT Recommendation V.11 electrical characteristics.

Table B.3: Pin allocation using interface connector according to ISO 4902

Item No	Pin Allocation	ISO reference	CCITT reference	Status Note
1	Circuit 102 on pin 19	ISO 4902	--	NOTE 1
2	Circuit 102a on pin 37	ISO 4902	--	NOTE 1
3	Circuit 102b on pin 20	ISO 4902	--	NOTE 1
4	Circuit 103 A-Wire on pin 4	ISO 4902	V.11	NOTE 1
5	Circuit 103 B-Wire on pin 22	ISO 4902	V.11	NOTE 1
6	Circuit 104 A-Wire on pin 6	ISO 4902	V.11	NOTE 1
7	Circuit 104 B-Wire on pin 24	ISO 4902	V.11	NOTE 1
8	Circuit 105 A-Wire on pin 7	ISO 4902	V.10/V.11	NOTE 1
9	Circuit 105 B-Wire on pin 25	ISO 4902	V.10/V.11	NOTE 1
10	Circuit 106 A-Wire on pin 9	ISO 4902	V.10/V.11	NOTE 2
11	Circuit 106 B-Wire on pin 27	ISO 4902	V.10/V.11	NOTE 2
12	Circuit 107 A-Wire on pin 11	ISO 4902	V.10/V.11	NOTE 2
13	Circuit 107 B-Wire on pin 29	ISO 4902	V.10/V.11	NOTE 2
14	Circuit 108/1A-Wire on pin12	ISO 4902	V.10/V.11	NOTE 2
15	Circuit 108/1B-Wire on pin 30	ISO 4902	V.10/V.11	NOTE 2
16	Circuit 109 A-Wire on pin 13	ISO 4902	V.10/V.11	NOTE 2
17	Circuit 109 B-Wire on pin 31	ISO 4902	V.10/V.11	NOTE 2
18	Circuit 114 A-Wire on pin 5	ISO 4902	V.11	NOTE 1
19	Circuit 114 B-Wire on pin 23	ISO 4902	V.11	NOTE 1
20	Circuit 115 A-Wire on pin 8	ISO 4902	V.11	NOTE 1
21	Circuit 115 B-Wire on pin 26	ISO 4902	V.11	NOTE 1

(continued)

Table B.3: Pin allocation using interface connector according to ISO 4902 (concluded)

Item No	Pin Allocation	ISO reference	CCITT reference	Status Note
22	Circuit 140 on pin 14	ISO 4902	V.10	NOTE 2
23	Circuit 141 on pin 10	ISO 4902	V.10	NOTE 2
24	Circuit 142 on pin 18	ISO 4902	V.10	NOTE 2

NOTE 1: Primary circuits that shall be implemented as data transfer functions, are given the category "mandatory essential" (me).

NOTE 2: Secondary circuits that if implemented as data control functions, are given the category "optionally essential" (oe).

B.4 Pin allocation using interface connector according to ISO 2593

Connector type and pin allocations (NOTE 3) to ISO 2593 [11] for services up to 1 920 kbit/s using a CCITT Recommendation V.35 interface with either CCITT Recommendation V.35 or V.11 electrical characteristics for data transfer functions and CCITT Recommendation V.28 for control functions.

Table B.4: Pin allocation using interface connector according to ISO 2593

item No	Pin Allocation	ISO reference	CCITT reference	Status Note
1	Circuit 102 A-Wire on B	ISO 2593	--	NOTE 1
2	Circuit 103 A-Wire on P	ISO 2593	V.35/V.11	NOTE 1
3	Circuit 103 B-Wire on S	ISO 2593	V.35/V.11	NOTE 1
4	Circuit 104 A-Wire on R	ISO 2593	V.35/V.11	NOTE 1
5	Circuit 104 B-Wire on T	ISO 2593	V.35/V.11	NOTE 1
6	Circuit 105 A-Wire on C	ISO 2593	V.10/V.28	NOTE 1
7	Circuit 106 A-Wire on D	ISO 2593	V.10/V.28	NOTE 2
8	Circuit 107 A-Wire on E	ISO 2593	V.10/V.28	NOTE 2
9	Circuit 108/1 A-Wire on H	ISO 2593	V.10/V.28	NOTE 2
10	Circuit 109 A-Wire on F	ISO 2593	V.10/V.28	NOTE 2
11	Circuit 114 A-Wire on Y	ISO 2593	V.35/V.11	NOTE 1
12	Circuit 114 B-Wire on AA	ISO 2593	V.35/V.11	NOTE 1
13	Circuit 115 A-Wire on V	ISO 2593	V.35/V.11	NOTE 1
14	Circuit 115 B-Wire on X	ISO 2593	V.35/V.11	NOTE 1
15	Circuit 140 A-Wire on N	ISO 2593	V.10/V.28	NOTE 2
16	Circuit 141 A-Wire on L	ISO 2593	V.10/V.28	NOTE 2
17	Circuit 142 A-Wire on NN	ISO 2593	V.10/V.28	NOTE 2

NOTE 1: Primary circuits that shall be implemented as data transfer functions, are given the category "mandatory essential" (me).
NOTE 2: Secondary circuits that, if implemented as data control functions, are given the category "optionally essential" (oe).
NOTE 3: *= all pin references are to the 1,6 mm dia. requirement.

B.5 Pin allocation using interface connector according to ISO 4903

Connector type and pin allocations to ISO 4903 [12] for services up to 1 920 kbit/s using a CCITT Recommendation X.24 interface with CCITT Recommendation V.11 electrical characteristics.

Table B.5: Pin allocation using interface connector according to ISO 4903

Item No	Pin Allocation	ISO Reference	Status Note
1	Signal Ground A-Wire on pin 8	ISO 4903	NOTE 1
2	Transmit A-Wire on pin 2	ISO 4903	NOTE 1
3	Transmit B-Wire on pin 9	ISO 4903	NOTE 1
4	Receive A-Wire on pin 4	ISO 4903	NOTE 1
5	Receive B-Wire on pin 11	ISO 4903	NOTE 1
6	Control A-Wire on pin 3	ISO 4903	NOTE 1
7	Control B-Wire on pin 10	ISO 4903	NOTE 1
8	Indication A-Wire on pin 5	ISO 4903	NOTE 2
9	Indication B-Wire on pin 12	ISO 4903	NOTE 2
10	Signal Element Timing A-Wire on pin 6	ISO 4903	NOTE 1
11	Signal Element Timing B-Wire on pin 13	ISO 4903	NOTE 1
12	Byte Timing A-Wire on pin 7	ISO 4903	NOTE 2
13	Byte Timing B-Wire on pin 14	ISO 4903	NOTE 2

NOTE 1: Primary circuits that shall be implemented as data transfer functions, are given the category "mandatory essential" (me).

NOTE 2: Secondary circuits that, if implemented as data control functions, are given the category "optionally essential" (oe).

Annex C (normative): PICS/PIXIT for CCITT Recommendation X.25 terminal equipments

PICS Cover page proforma

PICS **(Protocol Implementation Conformance Statement)** **FOR TBR 2,PHYSICAL LAYER**
Protocol supplier (IF NOT THE SYSTEM SUPPLIER) **Name :** **Contact :** **Street :** **Phone No :** **City :** **Telex No :** **Country :** **Fax No :**
REFERENCE PROTOCOL IDENTIFICATION **NAME:** **REFERENCE STANDARDS:** **NUMBER/REVISION DATE:** **ADDENDA APPLICABLE:**
DTE IDENTIFICATION: **NAME:** **VERSION No:**
DATE:

C.1 Introductory guidance to the PICS

To evaluate essential requirements of a particular implementation to a protocol standard, it is necessary to have a statement of which capabilities and options have been implemented for a given protocol. Such a statement is called a Protocol Implementation Conformance Statement (PICS). This annex contains PICS proformas for PSDN data terminal implementations stated to be conforming to TBR 2 at the physical layer.

The PICS proformas in this TBR shall be used to make this declaration.

The status attribute in the "STATUS" column reflects the conformance requirements defined in the referenced standards as follows:

me = mandatory essential. The item is specified as "mandatory essential", i.e. the capability is required to meet the referenced standard;

oe = optional essential. The item is specified as "optionally essential", i.e. the capability is not required to meet the referenced standard, but if it is implemented, it shall conform to the specifications;

- = (minus sign). Undefined or not applicable item.

The person who submits or applies a terminal for assessment against TBR 2 shall fill in one PICS proforma for each layer to be tested. The response to each question shall be placed in the right hand column called "ITEM IMPLEMENTED? Yes (=Y)/No (=N)". Each table row of this column is filled in as follows:

- for implemented items, a Y (or Yes) is entered;

- for not implemented items, a N (or No) is entered.

For each not implemented mandatory item the client shall give a justification, e.g. in the last PIXIT table entitled "Supplier's Additional Information". This table may be used by the client also to provide any other additional information.

C.2 Physical layer PICS

C.2.1 Access types

Table C.1: Access type

No	Item	Reference	Status	ITEM IMPLEMENTED
1	**Access via X.21**	**CCITT X.21**	**oe**	
2	**Access via X.21bis**	**CCITT X.21bis**	**oe**	

Table C.2: Connection arrangement between the terminal and the NTP

No	Item	Reference	Status	ITEM IMPLEMENTED
1	**Integral Connection**	**TBR 2 6.3.1.1**	**oe**	
2	**Non Integral Connection**	**TBR 2 6.3.1.2**	**oe**	

C.2.2 Interface connector types

Table C.3: Interface connector type

No	Item	Reference	Status	ITEM IMPLEMENTED
1	For X.21bis to ISO 2110 (25)	TBR 2 6.3.2.1	oe	
2	For X.21/X.21bis to ISO 11569 (26)	TBR 2 6.3.2.2	oe	
3	For X.21bis to ISO 2593 (34)	TBR 2 6.3.2.4	oe	
4	For X.21/X.21bis to ISO 4902 (37)	TBR 2 6.3.2.3	oe	
5	For X.21 to ISO 4903 (15)	TBR 2 6.3.2.5	oe	

C.2.3 Employed circuits

Table C.4: Circuits employed for CCITT Recommendation X.21 access

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Signal Ground	CCITT X.24	me	
2	Transmit	CCITT X.24	me	
3	Receive	CCITT X.24	me	
4	Control	CCITT X.24	me	
5	Indication	CCITT X.24	oe	
6	Signal Element Timing	CCITT X.24	me	
7	Byte Timing	CCITT X.24	oe	

Table C.5: Circuits employed for CCITT Recommendation X.21bis access

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Signal Ground 102	CCITT V.24	me NOTE 1	
2	DTE Common Return 102a	CCITT V.24	me NOTE 2	
3	DTE Common Return 102b	CCITT V.24	me NOTE 2	
4	Transmitted Data 103	CCITT V.24	me	
5	Received Data 104	CCITT V.24	me	
6	Request To Send 105	CCITT V.24	me	
7	Ready For Sending 106	CCITT V.24	oe	
8	Data Set Ready 107	CCITT V.24	oe	
9	Connect Data Set To Line 108/1	CCITT V.24	oe	
10	Data Channel Received Line Signal Detector 109	CCITT V.24	oe	
11	Transmit Signal Element Timing DCE 114	CCITT V.24	me	
12	Received Signal Element Timing DCE 115	CCITT V.24	me	
13	Loopback/Maintenance 140	CCITT V.24	oe	
14	Local Loopback 141	CCITT V.24	oe	
15	Test Indicator 142	CCITT V.24	oe	

NOTE 1: This circuit is neither a generator or a load.
NOTE 2: Mandatory for the 37 pin interface connector to ISO 4902 [10].

C.2.4 Pin allocations

Table C.6: Pin allocation using interface connector according to ISO 2110 (25 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Circuit 102 on Pin 7	ISO 2110	me	
2	Circuit 103 on Pin 2	ISO 2110	me	
3	Circuit 104 on Pin 3	ISO 2110	me	
4	Circuit 105 on Pin 4	ISO 2110	me	
5	Circuit 106 on Pin 5	ISO 2110	me	
6	Circuit 107 on Pin 6	ISO 2110	oe	
7	Circuit 108/1 on Pin 20	ISO 2110	oe	
8	Circuit 109 on Pin 8	ISO 2110	me	
9	Circuit 114 on Pin 15	ISO 2110	oe	
10	Circuit 115 on Pin 17	ISO 2110	oe	
11	Circuit 140 on Pin 21	ISO 2110	me	
12	Circuit 141 on Pin 18	ISO 2110	me	
13	Circuit 142 on Pin 25	ISO 2110	oe	

Table C.7: Pin allocation using interface connector according to ISO 11569 (26 pins)

Electrical Pin No	V.10 or V11/X.21 > 20 kbit/s NOTE 1	V.28/X.21bis < 20kbit/s NOTE 2	Reference	Status	Item Implemented Y(Yes)/N(No) V.10/V.11[ ] V.28 [ ]
1	Shield	Shield	ISO 11569	--	
2	103A	103	ISO 11569	me	
3	104A	104	ISO 11569	me	
4	105A/133A	105	ISO 11569	me	
5	106A	106	ISO 11569	oe	
6	107	107	ISO 11569	oe	
7	102A	102	ISO 11569	me	
8	109A	109	ISO 11569	oe	
9	115B	F	ISO 11569	--	
10	109B	F	ISO 11569	--	
11	113B	F	ISO 11569	oe	
12	114B	F	ISO 11569	me	
13	106B	F	ISO 11569	oe	
14	103B	F	ISO 11569	me	
15	114A	114	ISO 11569	me	
16	104B	F	ISO 11569	me	
17	115A	115	ISO 11569	me	
18	141	141	ISO 11569	oe	
19	105B/133B	F	ISO 11569	me	
20 (NOTE 3)	108	108	ISO 11569	oe	

(continued)

Table C.7: Pin allocation using interface connector according to ISO 11569 (26 pins) (concluded)

Electrical Pin No	V.10 or V.11/X.21 > 20 kbit/s NOTE 1	V.28/X.21bis < 20 kbit/s NOTE 2	Reference	Status	Item Implemented Y(Yes)/N(No) V.10/V.11[ ] V.28 [ ]
21	**140**	**140**	**ISO 11569**	**oe**	
22	**125**	**125**	**ISO 11569**	**oe**	
23	**102B**	**F**	**ISO 11569**	**me**	
24	**113A**	**F**	**ISO 11569**	**me**	
25	**142**	**142**	**ISO 11569**	**oe**	
26	**No Connection**	**No Connection**	**ISO 11569**	**--**	

NOTE 1: At present there is no pin assignment for V.10/V.11 Circuit 102 only Circuits 102A and 102B. A decision should be known by 8/93.
NOTE 2: F = Contact reserved for international use.
NOTE 3: Pin 20 may be either circuit 108/1 or 108/2.

Table C.8: Pin allocation using interface connector according to ISO 4902 (37 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Circuit 102 A-Wire on Pin 19	ISO 4902	me	
2	Circuit 102a A Wire on Pin 37	ISO 4902	me	
3	Circuit 102b B Wire on Pin 20	ISO 4902	me	
4	Circuit 103 A Wire on Pin 4	ISO 4902	me	
5	Circuit 103 B Wire on Pin 22	ISO 4902	me	
6	Circuit 104 A Wire on Pin 6	ISO 4902	me	
7	Circuit 104 B Wire on Pin 24	ISO 4902	me	
8	Circuit 105 A Wire on Pin 7	ISO 4902	me	
9	Circuit 105 B Wire on Pin 25	ISO 4902	me	
10	Circuit 106 A Wire on Pin 9	ISO 4902	oe	
11	Circuit 106 B Wire on Pin 27	ISO 4902	oe	
12	Circuit 107 A Wire on Pin 11	ISO 4902	oe	
13	Circuit 107 B Wire on Pin 29	ISO 4902	oe	
14	Circuit 108/1 A Wire on Pin 12	ISO 4902	oe	
15	Circuit 108/1 B Wire on Pin 30	ISO 4902	oe	
16	Circuit 109 A Wire on Pin 13	ISO 4902	oe	
17	Circuit 109 B Wire on Pin 31	ISO 4902	oe	
18	Circuit 114 A Wire on Pin 5	ISO 4902	me	
19	Circuit 114 B Wire on Pin 23	ISO 4902	me	
20	Circuit 115 A Wire on Pin 8	ISO 4902	me	
21	Circuit 115 B Wire on Pin 26	ISO 4902	me	
22	Circuit 140A Wire on Pin 14	ISO 4902	oe	
23	Circuit 141 A Wire on Pin 10	ISO 4902	oe	
24	Circuit 142 A Wire on Pin 18	ISO 4902	oe	

Table C.9: Pin allocation using interface connector according to ISO 2593 (34 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Circuit 102 A-Wire on Pin B	ISO 2593	me	
2	Circuit 103 A Wire on Pin P	ISO 2593	me	
3	Circuit 103 B Wire on Pin S	ISO 2593	me	
4	Circuit 104 A Wire on Pin R	ISO 2593	me	
5	Circuit 104 B Wire on Pin T	ISO 2593	me	
6	Circuit 105 A Wire on Pin C	ISO 2593	me	
7	Circuit 106 A Wire on Pin D	ISO 2593	oe	
8	Circuit 107 A Wire on Pin E	ISO 2593	me	
9	Circuit 108/1 A Wire on Pin H	ISO 2593	oe	
10	Circuit 109 A Wire on Pin F	ISO 2593	oe	
11	Circuit 114 A Wire on Pin Y	ISO 2593	me	
12	Circuit 114 B Wire on Pin AA	ISO 2593	me	
13	Circuit 115 A Wire on Pin V	ISO 2593	me	
14	Circuit 115 B Wire on Pin X	ISO 2593	me	
15	Circuit 140A Wire on Pin N	ISO 2593	oe	
16	Circuit 141 A Wire on Pin L	ISO 2593	oe	
17	Circuit 142 A Wire on Pin NN	ISO 2593	oe	
NOTE: The physical dimensions for the pin diameter refer to the 1,6 mm option under ISO 2593 [11].				

Table C.10: Pin allocation using interface connector according to ISO 4903 (15 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Signal Ground A Wire on Pin 8	ISO 4903	me	
2	Transmit A Wire on Pin 2	ISO 4903	me	
3	Transmit B Wire on Pin 9	ISO 4903	me	
4	Receive A Wire on Pin 4	ISO 4903	me	
5	Receive B Wire on Pin 11	ISO 4903	me	
6	Control A-Wire on Pin 3	ISO 4903	me	
7	Control B-Wire on Pin 10	ISO 4903	me	
8	Indication A Wire on Pin 5	ISO 4903	oe	
9	Indication B Wire on Pin 12	ISO 4903	oe	
10	Signal Element Timing A Wire on Pin 6	ISO 4903	me	
11	Signal Element Timing B Wire on Pin 13	ISO 4903	me	
12	Byte Timing A-Wire on Pin 7	ISO 4903	oe	
13	Byte Timing B Wire on Pin 14	ISO 4903	oe	
14	DTE Common Return on Pin 9	ISO 4903	oe	
15	DCE Common Return on Pin 10	ISO 4903	oe	

C.2.5 Electrical circuit characteristics

Table C.11: Electrical circuit characteristics using interface connector according to ISO 2110 (25pins)

No	Item	Reference	Status	Item Implemented V.28 [ ] / V.10 [ ]
1	Circuit 102 According to V.28	CCITT V.28	me	
2	Circuit 103 According to V.28	CCITT V.28	me	
3	Circuit 104 According to V.28	CCITT V.28	me	
4	Circuit 105 According to V.28/V.10	CCITT V.28/V.10	me	
5	Circuit 106 According to V.28/V.10	CCITT V.28/V.10	oe	
6	Circuit 107 According to V.28/V.10	CCITT V.28/V.10	oe	
7	Circuit 108/1 According to V.28/V.10	CCITT V.28/V.10	oe	
8	Circuit 109 According to V.28/V.10	CCITT V.28/V.10	oe	
9	Circuit 114 According to V.28	CCITT V.28	oe	
10	Circuit 115 According to V.28	CCITT V.28	me	
11	Circuit 140 According to V.28/V.10	CCITT V.28/V.10	oe	
12	Circuit 141 According to V.28/V.10	CCITT V.28/V.10	oe	
13	Circuit 142 According to V.28/V.10	CCITT V.28/V.10	oe	

Table C.12: Electrical circuit characteristics using interface connector according to ISO 11569

Electrical Pin No	V.10 V11/X.21 > 20 kbit/s	V.28/X.21bis < 20 kbit/s	Reference	Status	Item Implemented V.28	V.10	V.11
1	Shield	Shield	ISO 11569	--			
2	103A	103	ISO 11569	me			
3	104A	104	ISO 11569	me			
4	105A/133A	105	ISO 11569	me			
5	106A	106	ISO 11569	oe			
6	107	107	ISO 11569	oe			
7	102A	102	ISO 11569	me			
8	109A	109	ISO 11569	oe			
9	115B	F	ISO 11569	--			
10	109B	F	ISO 11569	--			
11	113B	F	ISO 11569	oe			
12	114B	F	ISO 11569	me			
13	106B	F	ISO 11569	oe			
14	103B	F	ISO 11569	me			
15	114A	114	ISO 11569	me			
16	104B	F	ISO 11569	me			
17	115A	115	ISO 11569	me			
18	141	141	ISO 11569	oe			
19	105B/133B	F	ISO 11569	me			
20	108	108	ISO 11569	oe			
21	140	140	ISO 11569	oe			
22	125	125	ISO 11569	oe			
23	102B	F	ISO 11569	me			
24	113A	F	ISO 11569	me			
25	142	142	ISO 11569	oe			
26	No Connection	No Connection	ISO 11569	--			

Table C.13: Electrical circuit characteristics using interface connector according to ISO 4902 (37 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED Y(Yes)/N(No)
1	Circuit 103	CCITT V.11	me	
2	Circuit 104	CCITT V.11	me	
3	Circuit 105	CCITT V.11 CCITT V.10	me me	
4	Circuit 106	CCITT V.11 CCITT V.10	oe (NOTE 1) oe (NOTE 1)	
5	Circuit 107	CCITT V.11 CCITT V.10	oe (NOTE 1) oe (NOTE 1)	
6	Circuit 108/1	CCITT V.11 CCITT V.10	oe (NOTE 1/2) oe (NOTE 1/2)	
7	Circuit 109	CCITT V.11 CCITT V.10	oe (NOTE 1) oe (NOTE 1)	
8	Circuit 114	CCITT V.11	me	
9	Circuit 115	CCITT V.11	me	
10	Circuit 140	CCITT V.10	oe (NOTE 2)	
11	Circuit 141	CCITT V.10	oe (NOTE 2)	
12	Circuit 142	CCITT V.10	oe (NOTE 2)	

NOTE 1: One of the options V.10 or V.11 shall be chosen for an implemented circuit.
NOTE 2: Implementation of this circuit is an option.

Table C.14: Electrical circuit characteristics using interface connector according to ISO 2593 (34 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED Y(Yes)/N(No)
1	Circuit 103	CCITT V.35 CCITT V.11	me (NOTE 1) me (NOTE 1)	
2	Circuit 104	CCITT V.35 CCITT V.11	me (NOTE 1) me (NOTE 1)	
3	Circuit 105	CCITT V.28	me	
4	Circuit 106	CCITT V.28	oe	
5	Circuit 107	CCITT V.28	oe	
6	Circuit 108/1	CCITT V.28	oe	
7	Circuit 109	CCITT V.28	oe	
8	Circuit 114	CCITT V.35 CCITT V.11	me (NOTE 1) me (NOTE 1)	
9	Circuit 115	CCITT V.35 CCITT V.11	me (NOTE 1) me (NOTE 1)	
10	Circuit 140	CCITT V.28	oe (NOTE 2)	
11	Circuit 141	CCITT V.28	oe (NOTE 2)	
12	Circuit 142	CCITT V.28	oe (NOTE 2)	

NOTE 1: One of the CCITT Recommendation V.35 or V.11 options shall be implemented.
NOTE 2: Implementation of this circuit is an option.

Table C.15: Electrical circuit characteristics using interface connector according to ISO 4903 (15 pins)

No	Item	Reference	Status	ITEM IMPLEMENTED
1	Transmit	CCITT V.11 CCITT V.10	me me	
2	Receive	CCITT V.11 CCITT V.10	me me	
3	Control	CCITT V.11 CCITT V.10	me me	
4	Indication	CCITT V.11 CCITT V.10	oe oe	
5	Signal Element Timing	CCITT V.11 CCITT V.10	me me	
6	Byte Timing	CCITT V.11 CCITT V.10	oe oe	

C.2.6 Data rates

Table C.16: Data rates

No	Item	Reference	Status	ITEM IMPLEMENTED Y(Yes)/N(No)
1	600 bit/s	CCITT X.1	oe NOTES 1 & 2	
2	2400 bit/s	CCITT X.1	oe NOTES 1 & 2	
3	4800 bit/s	CCITT X.1	oe NOTES 1 & 2	
4	9600 bit/s	CCITT X.1	oe NOTES 1 & 2	
5	19200 bit/s	CCITT X.1	oe NOTES 1 & 2	
6	48000 bit/s	CCITT X.1	oe NOTES 1 & 4	
7	64000 bit/s	CCITT X.1	oe NOTE 1	
8	n x 64kbit/s n = 2 to 30	CCITT X.1	oe NOTE 3	
9	1920 kbit/s	CCITT X.1	oe NOTE 3	
10	other data rate	CCITT X.1	oe	

NOTE 1: One of these data rates shall be implemented.
NOTE 2: Only allowed for CCITT Recommendation X.21 or X.21bis access.
NOTE 3: TSS X.1 (1992), User Class 59, Table 4-1/X.1 allows for 1 920 kbit/s.
NOTE 4: Only allowed for CCITT Recommendation X.21 [7] access using an interface with an electrical characteristic according to CCITT Recommendation X.27 (V.11), or for CCITT Recommendation X.21bis access using the CCITT Recommendation V.35 or V.36 interface.

PIXIT COVER PAGE PROFORMA

PIXIT

(Protocol Implementation eXtra Information for Testing)

FOR TBR 2,PHYSICAL LAYER

PROTOCOL SUPPLIER (IF NOT THE SYSTEM SUPPLIER)

Name : **Contact :**

Street : **Phone No :**

City : **Telex No :**

Country : **Fax No :**

REFERENCE PROTOCOL IDENTIFICATION

NAME:

REFERENCE STANDARDS:

NUMBER/REVISION DATE:

ADDENDA APPLICABLE:

DTE IDENTIFICATION:

NAME:

VERSION No:

DATE:

C.3 Introductory guidance for the PIXIT

To evaluate essential requirements of a particular protocol implementation, information relating to the implementation and its declared environment in addition to that provided by the PICS is essential. Such extra information is called a Protocol Implementation eXtra Information for Testing (PIXIT).

This annex contains a PIXIT proforma for the physical layer implementation of an CCITT Recommendation X.25 [2] DTE conforming to this TBR.

C.3.1 Physical layer PIXIT

C.3.1.1 Characteristics for non-integral interconnection cable

Table C.17: Characteristics of non-integral interconnection cable

Item No	State Characteristics:(Cable specification length, number of leads, twisted?, capacity etc.)

Table C.18: Unused leads of interconnection cable

Item No	Reference to PICs	Interface connector Type	Pin No	Comment

Unproperly terminated connections

Table C.19: Connections terminated other than by an appropriate generator or load at the DTE

Item No	Reference to PICs	Interface connector Type	Pin No	Comment

C.3.1.2 Generators that are held in a steady state

Table C.20: Generators that are held in a steady state

Item No	Reference to PICs	Interface connector Type	Pin No	Comment

Table C.21: Suppliers additional information about interface circuits

Item No	List appended information (e.g. circuit diagrams etc.)

C.3.1.3 Suppliers additional general information

Table C.22: Suppliers additional general information

Item No	Reference to PICs	Justification, statements and clarification etc.

PICS COVER PAGE PROFORMA

PICS

(Protocol Implementation Conformance Statement)

FOR TBR 2,LINK AND PACKET LAYER

PROTOCOL SUPPLIER(IF NOT THE SYSTEM SUPPLIER)

Name : **Contact :**

Street : **Phone No :**

City : **Telex No :**

Country : **Fax No :**

REFERENCE PROTOCOL IDENTIFICATION

NAME:

REFERENCE STANDARDS:

NUMBER/REVISION DATE:

ADDENDA APPLICABLE:

DTE IDENTIFICATION:

NAME:

VERSION No:

DATE:

Table C.23: Link set-up functions

INSTRUCTIONS FOR DECLARER:

Please insert "Y or N" inside [ ] to state whether the FUNCTION IS SUPPORTED in your implementation.

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
	LINK SET UP		
3.1.1	**DTE initiates Link Set-up sending**	**[ ]**	
3.1.2	**DTE initiates Link Set-up sending**	**[ ]**	
3.1.3	**DTE waits for DCE sending unsolicited DM to solicit Link Set-up**	**[ ]**	
3.1.4	**DTE waits for DCE sending SABM to initiate Link Set-up**	**[ ]**	

Table C.24: Packet layer functions

INSTRUCTIONS FOR DECLARER:

Please, insert choice label(s) "Y" or "N" inside [ ] to state the choice(s) implemented.

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
	TYPES OF SERVICE		
4.1.1	**a)Switched Virtual Call (SVC)**		
	- Incoming Call	**[ ]**	
	- Outgoing Call	**[ ]**	
	- Bothway	**[ ]**	
	b)Permanent Virtual Circuit (PVC)	**[ ]**	

Table C.25: Call set-up function

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
4.2.1	CALL ESTABLISHMENT a SEND Call Request Packet and RECEIVE Call Connected Packet	[ ]	
	b RECEIVE Incoming Call Packet and SEND Call Accepted Packet only if there is no collision	[ ]	

Table C.26: Data transfer function

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
4.3.1	DATA TRANSFER Send or Receive Data Packet		

PIXIT COVER PAGE PROFORMA

PIXIT

(Protocol Implementation eXtra Information for Testing)

FOR TBR 2,LINK AND PACKET LAYER

PROTOCOL SUPPLIER (IF NOT THE SYSTEM SUPPLIER)

Name : **Contact :**

Street : **Phone No :**

City : **Telex No :**

Country : **Fax No :**

REFERENCE PROTOCOL IDENTIFICATION

NAME:

REFERENCE STANDARDS:

NUMBER/REVISION DATE:

ADDENDA APPLICABLE:

DTE IDENTIFICATION:

NAME:

VERSION No:

DATE:

Table C.27: PIXIT physical layer requirements

No	Item	Interface	Connector	ITEM IMPLEMENTED Y(Yes)/N(No)
5.1.1	up to 19 200 bit/s	V.24/V.28/V.10	ISO 2110	
5.1.2	up to 19 200 bit/s	V.24/V.28	ISO11569	
5.1.3	up to 1 920kbit/s	V.35/V.28	ISO 2593	
5.1.44	up to 1 920kbit/s	V.11/V.28	ISO 2593	
5.1.5	up to 1 920 kbit/s	V.36	ISO 4902	
5.1.6	up to 1 920 kbit/s	X.21/V.11	ISO 4903	
5.1.7	up to 1 920 kbit/s	V.11	ISO 11569	

C.4 PIXIT for link level

Table C.28: Link setup

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
6.1.1	Is the IUT active i.e. tries to bring up the link continuously [Y/N]?	[ ]	
6.1.2	Can the IUT setup the link without intervention. i.e. after link disconnection the link can be initialised by all the tests of Annex A.6 without operator intervention at the IUT [Y/N]?	[ ]	
6.1.3	Can the IUT send a SABM(E) frame also under operator control and enter the link setup state [Y/N]?	[ ]	

Table C.29: Information transfer

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
6.2.1	Will the IUT send the first I-Frame upon entering data transfer phase		
6.2.2	Specify, in the subsequent fields in hexadecimal format, the content of the first 10 information frames expected by the IUT. I-Frame type 1 I-Frame type 2 I-Frame type 3 I-Frame type 4 I-Frame type 5 I-Frame type 6 I-Frame type 7 I-Frame type 8 I-Frame type 9 I-Frame type 10		
6.2.3	Specify the sequence numbering mechanism supported by the IUT		
	a. Modulo 8	[ ]	
	b. Modulo 128	[ ]	

Table C.30: Link disconnection

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
6.3.1	Can the IUT send DISC frames under operator control and enter Link Disconnected state or Disconnected phase [Y/N]?	[ ]	
6.3.2	Is the Disconnected phase a stable phase for the IUT [Y/N]?	[ ]	

Table C.31: Timers

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
6.4.1	State the time that the tester has to wait before determining that the IUT will not respond to tester stimuli [sec's]?	[ ]	
6.4.2	State the maximum time that operator intervention will be required to initiate Layer 2 frames		

Table C.32: System parameter values

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
6.5.1	Timer T1	[ ]	
6.5.2	Maximum number of attempts to complete a transmission (N2)	[ ]	
6.5.3	Maximum number of bits in an I Frame (N1)	[ ]	
6.5.4	Maximum number of outstanding I-Frames for modulo 8 (k)	[ ]	
6.5.5	Maximum number of outstanding I-Frames for modulo 128 (k)	[ ]	

Table C.33: Speed values

At what line speed is the packet handler declared as supporting ?

Please indicate "Y" or "N" in the " [ ] "

No	Item	Status	Item Implemented Yes (Y) No (N)
6.6.1	2400 bit/s	[ ]	
6.6.2	4800 bit/s	[ ]	
6.6.3	9600 bit/s	[ ]	
6.6.4	19200 bit/s	[ ]	
6.6.5	48000 bit/s	[ ]	
6.6.6	64000 bit/s	[ ]	
6.6.7	n x 64kbit/s n = 2 to 30	[ ]	
6.6.8	1920 kbit/s	[ ]	
6.6.9	other data rate	[ ]	

C.5 PIXIT for packet layer

Table C.34: Logical channel assignments

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
7.1.1	Specify the range of logical channel numbers to be available for test purposes as PVC (the lowest group PVC number has to be 0)	HGPVCn= LPVCn = HPVCn =	
7.1.2	Specify the range of logical channel numbers to be available for test purposes as one way incoming logical channels for Virtual Calls	LIGCn= LICn = HIGCn= HICn =	
7.1.3	Specify the range of logical channel numbers to be available for test purposes as one way outgoing logical channels for Virtual Calls	LOGCn= LOCn HOGCn HOCn	
7.1.4	Specify the range of logical channel numbers to be available for test purposes as two way logical channels for Virtual Calls	LTGCn LTCn HTGCn HTCn	

NOTE: HGPVCn: Highest Group Permanent Virtual Circuit number.

LPVCn: Lowest Permanent Virtual Circuit number.

HPVCn: Highest Permanent Virtual Circuit number.

LIGCn: Lowest Incoming Group Channel number.

LICn : Lowest Incoming Channel number.

HIGCn: Highest Incoming Group Channel number.

HICn : Highest Incoming Channel number.

LOGCn: Lowest Outgoing Group Channel number.

LOCn : Lowest Outgoing Channel number.

HOGCn: Highest Outgoing Group Channel number.

HOCn : Highest Outgoing Channel number.

LTGCn: Lowest Two-way Group Channel number.

LTCn : Lowest Two-way Channel number.

HTGCn: Highest Two-way Group Channel number.

HTCn : Highest Two-way Channel number.

Table C.35: Packet procedural information

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
7.2.1	State if the IUT is able to Send only, data receive only ,data/send + receive only data [S,R,S+R,Non]		
7.2.2	State the non-reaction time which the tester should wait before determining that the IUT will not respond to a tester stimuli [sec]		
7.2.3	State type of initialisation sequence used by the IUT for SVC [A/B] where A= Call setup procedure initiated by the tester B= Call setup procedure initiated by the IUT		
7.2.4	State IUT reaction when the IUT receives D bit set to 1 in Incoming Call Packets: [CA] for Call Accepted Packet [CL] for Clear Request Packet		

(continued)

Table C.35: Packet procedural information (concluded)

7.2.5	**State IUT reaction when IUT receives D bit set to 1 in Call Connected Packets:** **[CL] for Clear Request packet** **[N] for Nothing**		
7.2.6	**State the packet type required from the tester to solicit a Clear Request from the IUT in order clear a call whilst it is in the information transfer state:** **a. Clear Confirm** **b. Call Connect** **c. Incoming Call** **d. Operator Intervention**		
7.2.7	**Does the IUT demand Fast Select or is Fast Select always demanded on Incoming Calls by the IUT**		
7.2.8	**Does the IUT disconnect the Layer 2 after receiving a L3 clear condition?**		

Table C.36: Packet specific requirements

Item No	Item Description	Status	Item Implemented Yes (Y) No (N)
7.3.1	Receive specific Called Address to be used by the Tester in Incoming Call Packet?(If Yes, then BCD string)		
7.3.2	Receive specific Calling Address to be used by the IUT in the Call Request Packet and by the Tester in Call Connected Packet?(If Yes, then BC		
7.3.3	Receive specific Called Address to be used by the IUT in Call Request Packet and by the Tester in Call Connected Packet? (If Yes, then BCD string)		
7.3.4	Receive specific call user data in Incoming Call Packet? (If Yes. specify string Hexadecimal code)		
7.3.5	Receive specific in Incoming Call Packet? (If Yes. specify string Hexadecimal code)		
7.3.6	Specify a Called Address with a LENGTH=15 for Incoming Call Packet to be used in specific test (string of BCD characters)		

Annex D (informative): Explanatory note to this TBR

The justification of the compliance principles in this TBR assumes that the DTE has been designed to operate with CCITT Recommendation X.25 [1], [2] and [3] network interface and in particular will:

- observe the safety requirements under the procedures available through the Low Voltage Directive (73/23/EEC);

- observe the Electro-Magnetic Compatibility requirements under the procedures available through the EMC Directive (89/336/EEC);

- implement one or more of the physical level configurations specified in subclauses 1.1, 1.2 and 1.3 of CCITT Recommendation X.25 [1], [2] and [3] on the basis of a conformance declaration only;

- implement one or more of the electrical level configurations specified in subclauses 1.1, 1.2 and 1.3 of CCITT Recommendation X.25 [1], [2] and [3] on the basis of a conformance declaration and test procedure;

- implement one or more of the Link Access procedures (LAPB or LAPB Extended) as defined in subclauses 2.1, 2.2, 2.3 and 2.4 of CCITT Recommendation X.25 [1], [2] and [3] for those features for which the DTE claims a capability on the basis of a conformance declaration and test procedure;

- implement the packet layer procedures and formats defined in Clauses 3, 4 and 5 of CCITT Recommendation X.25 [1], [2], [3] for those features for which the DTE claims a capability on the basis of a conformance declaration and test procedure, (e.g. out-going calls, incoming calls, etc.);

- at no time will the packet terminal equipment be expected to operate outside its normal mode of operation in order to demonstrate compliance with the essential requirements set out in this TBR.

The TBR has, therefore, been structured on the basis of four principles that consists of:

- requirements that a terminal has to satisfy in order to meet the EC Council Directive 91/263/EEC;

- a justification of which article within the directive, the requirement is based upon, with informative references to other related standards that are outside the scope of ETSI;

- normative test specifications and procedures that are designed to reasonably demonstrate a terminals functionality in order to meet the requirements;

- a conformance statement to declare the terminals behaviour depending upon its designed functionality.

Throughout the TBR there are clear references to mandatory and optional requirements. The mandatory requirements are those, that all terminals shall meet, whereas optional requirements are for those terminal features that are only mandatory when declared within the conformance statement for each terminal type.

The requirements themselves are demonstrated by one of two methods:

- a specific measurement, by use of a test specification and procedure, on a particular feature of a terminal's functionality;

- by a declaration that other functions have been implemented according to the TBR.

As such the conformance statement section forms an integral part of this TBR, in order to allow for the normative test case selection as well as a terminal declaration by type, of those functional features, deemed essential and declared as implemented.

There are informative references in the form of notes; throughout the normative part of the TBR, that are intended for help and guidance purposes only in the drafting of this TBR. These will be removed after the Public Enquiry stage has been completed but before this TBR is submitted TRAC and ACTE for the regulatory framework to be considered.

D.1 CCITT V.28 alternative effective capacitance measurement for a load

Reference Receiver: A hypothetical circuit comprising a resistor of 3 000 ohm in parallel with a capacitor. The worst case complaint receiver will contain a capacitance of 2 500pF.

Degraded Generator: A generator circuit which when connected to a worst case complaint receiver (a reference receiver containing a capacitance of 2 500pF),will cause the waveform to take $0{,}03t_b$ seconds to travel from -3 volts to +3 volts. For simplicity, the degraded generator is modelled by a pulse generator and a resistor.

Effective Capacitance: A value of capacitance associated with a practical receiver. The value of capacitance is that value which when placed in the reference receiver will give the same degradation as the practical receiver.

Degradation: The time taken for the degraded generator waveform to change from -3 volts to +3 volts.

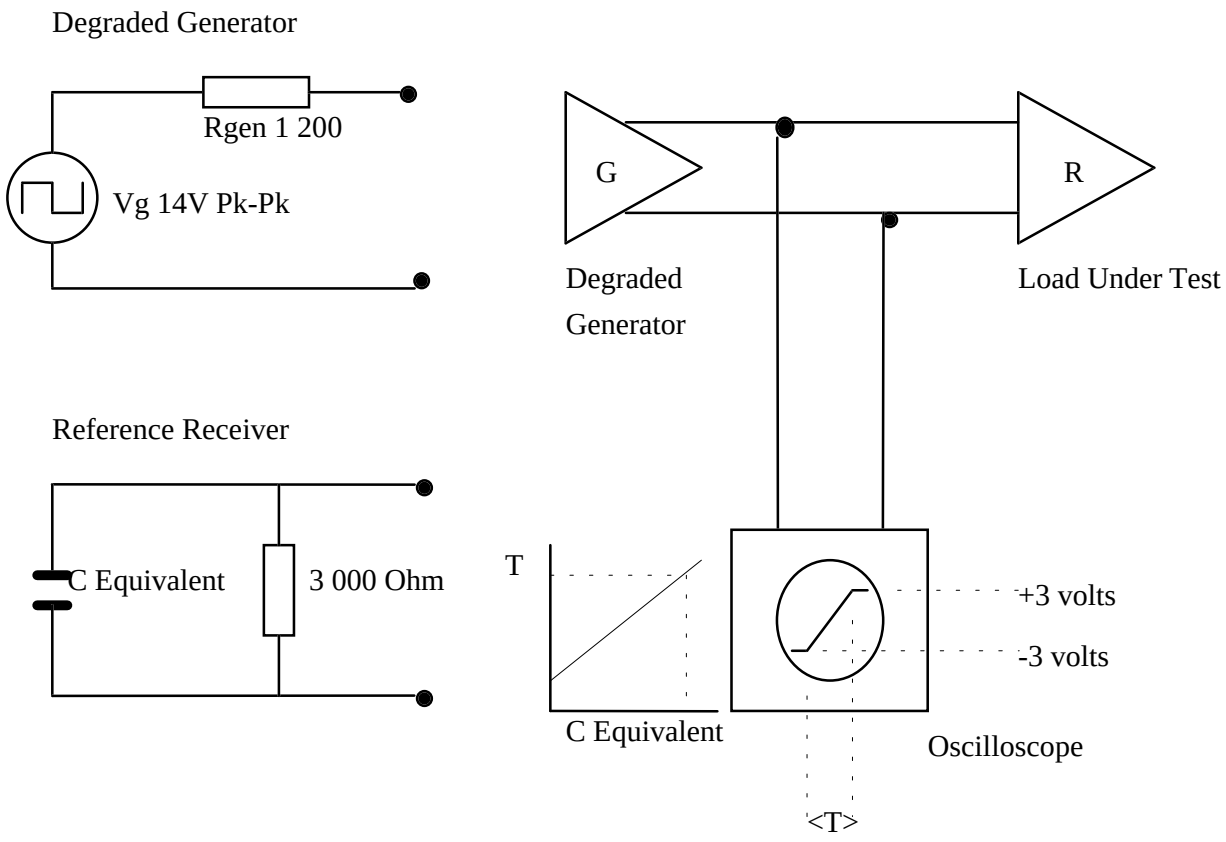


Figure D.1

CCITT Recommendation V.28 recommends that a data circuit generator produces a signal which passes from -3 volts to +3 volts in $0,03t_b$ when connected to a worst case receiver, but limited by a capacitance of 2 500pF. CCITT Recommendation V.28 also recommends that a receiver has a minimum voltage of + or - 5 volts in magnitude for any load resistance between 3 000 ohms and 7 000 ohms, when the open circuit voltage (E_L) is zero.

This requirement has been translated as a worst case receiver of 3 000 ohms in parallel with 2 500pF. Whilst a receiver with 7 000 ohms would produce a larger time constant, it would also have a larger voltage produced across it which would tend to improve the performance in the range - to +3 volts. The degraded generator is defined from the CCITT Recommendation V28 requirement and is relevant to a particular data-rate since the limiting characteristic of $0,03t_b$ is a function of data-rate.

The degraded generator is assumed to be resistive only with no dc bias. It produces a signal at the data-rate under consideration of V_g (peak to peak). The voltage is selected such that the voltage across the reference circuit V_L is 10 volts (peak to peak) which is the limiting situation from CCITT Recommendation V.28. The resistance of the generator Rgen is determined such that the time taken for the waveform to pass from - to +3 volts at the reference receiver with 2 500pF installed is exactly $0,03t_b$.

In order to standardise on a test circuit, a degraded generator shall consists of a voltage in the 10 to 15 volt range. Figure D.2 gives an example of a degraded generator of 14 volts (peak to peak) and a resistance Rgen of 1,2 Kohm for a conversion chart for a simulated data signalling rate of 9 600 bps. The measurement involves the use of 2 reference circuits called a "degraded generator" with a "reference receiver". The test for maximum load shunt capacitance is based upon a worst case generator (that is degraded by a known amount) that will permit the data signal to pass from -3 volts to +3 volts in $0,03\ t_b$ when connected to a reference receiver which includes a capacitance of 2 500pF. The receiver under test is then replaced by a reference receiver in the test configuration and measurements of the same amount of degradation in the data signal are recorded so that the receiver under test can be said to possess an "effective capacitance" of 2 500pF.

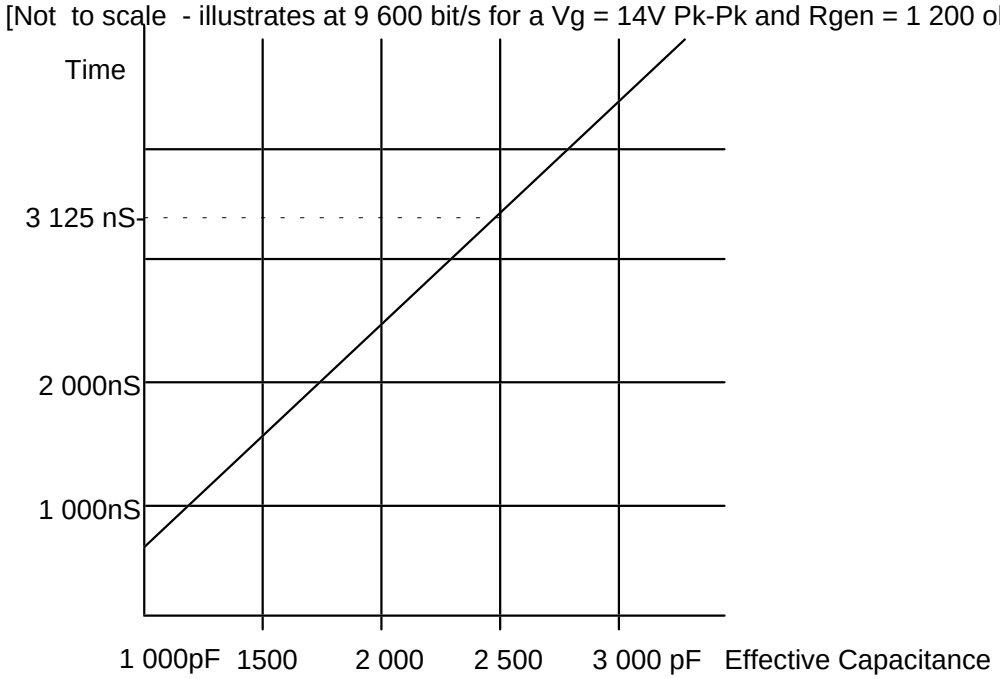
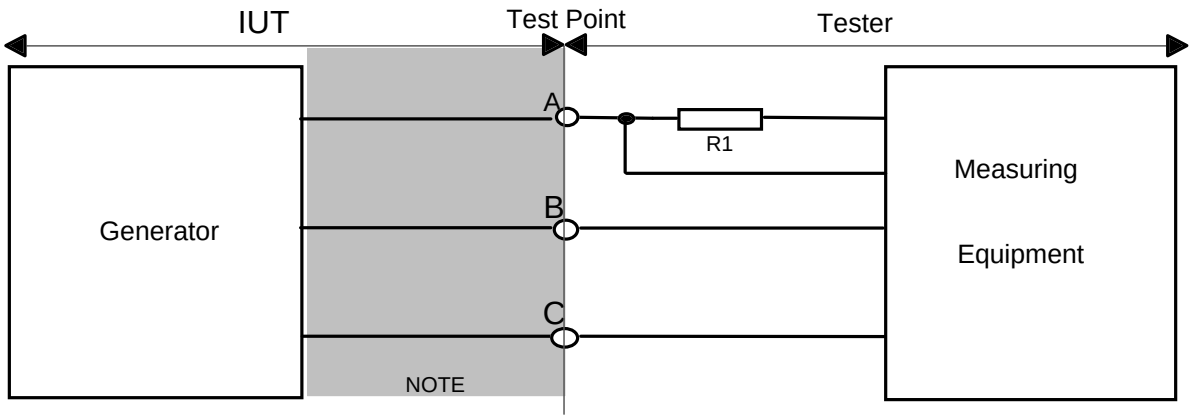


Figure D.2: Degraded generator conversion chart

D.2 CCITT V.35 Alternative Impedance Measurement for a Generator

Test configuration:

A 100 ohm non-reactive impedance (R1) shall be connected in series with a amperemeter, between point A and point C. A device for measuring dc voltage is connected across R1.



NOTE: The shaded area denotes an interconnection means, e.g. interface cable and connector.

Figure D.3

IUT interface state:

The IUT will be powered.

Test stimulus and action:

The dc resistance will be calculated by recording the voltage drop across and the current through the 100 ohm non reactive impedance when the IUT is in the binary 1 state. The IUT is then set to the binary 0 state and the voltage and current recorded. Calculate the source impedance from the formula shown below. The limits of the requirement allow any reactive components to be disregarded from this dc calculation.

$$\frac{\partial V}{\partial I} = R \text{ ohms}$$

Expected results:

The generator source impedance shall be 100 ohms ± 50 ohms.

Annex E (informative): Bibliography

1) Council Directive 73/23/EEC: "European low voltage directive".

2) Council Directive 91/263/EEC: "On the approximation of the laws of the Member States concerning telecommunications terminal equipment including the mutual recognition of their conformity".

3) Council Directive 89/336/EEC: "European EMC directive".

4) CCITT Recommendation V.24 (1984): "List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment".

5) CCITT Recommendation V.28 (1984): "Electrical characteristics for unbalanced double-current interchange circuits".

6) CCITT Recommendation V.10 (1984): "Electrical characteristics for unbalanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications".

7) CCITT Recommendation V.11 (1984): "Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications".

8) Draft ITU-T Recommendation X.21/X.21bis: Interface between data terminal equipment and data circuit-terminating equipment for synchronous operation on public data networks".

9) CCITT Recommendation V.36 (1984): "Modems for synchronous data transmission using 60-108 kHz group band circuits".

10) CCITT Recommendation V.35 (1984): "Data transmission at 48 kbps using 60-108 kHz group band circuits".

11) CCITT Recommendation X.24 (1989): "List of definitions for interchange circuits between data terminal equipment (DTE) and data circuit-terminating equipment (DCE) on public data networks".

12) NET 1 (1988): "Approval requirements for data terminal to connect to circuit switched public data networks and leased circuits using CCITT Recommendation X.21 interface".

13) NET 2 (1988): "Approval requirements for data terminal to connect to packet switched public data networks using CCITT Recommendation X.25 (1984) interface".

History

Document history			
May 1994	Public Enquiry	PE 63:	1994-05-23 to 1994-09-16
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