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Foreword

This draft European Telecommunication Standard (ETS) has been produced by the Radio Equipment and Systems (RES) Technical Committee of the European Telecommunications Standards Institute (ETSI), and is now submitted for the Public Enquiry phase of the ETSI standards approval procedure.

This ETS is a multi-Part standard and will consist of the following parts:

Part 1: "General network design";

Part 2: "Radio Aspects";

Part 3: "Mobile Station to Mobile Station (MS-MS) Air Interface (AI) protocol";

Part 4: "Repeaters ", (DE/RES-06007-4);

Part 5: "Gateways", (DE/RES-06007-5);

Part 6: "Security", (DE/RES-06007-6).

Proposed transposition dates	
Date of latest announcement of this ETS (doa):	3 months after ETSI publication
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	6 months after doa
Date of withdrawal of any conflicting National Standard (dow):	6 months after doa

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1 Scope

This ETS defines the Trans-European Trunked RAdio system (TETRA) Direct Mode Operation (DMO). It specifies the basic air interface, the inter-working between Direct Mode (DM) groups via repeaters, and inter-working with the TETRA Voice plus Data (V+D) system via gateways. It also specifies the security aspects in TETRA DMO, and the intrinsic services that are supported in addition to the basic bearer and teleservices.

This part applies to the TETRA DMO Mobile Station - Mobile Station (MS - MS) air interface and contains the specifications of the physical layer according to the OSI seven layer reference model.

It establishes the TETRA radio aspects (layer 1):

- it defines and specifies the modulation;
- it defines and specifies the radio transmission and reception;
- it defines and specifies the synchronisation;
- it defines and specifies the channel coding;
- it defines and specifies the channel multiplexing;
- it defines and specifies the control over the radio link.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] ETS 300 113: "Radio Equipment and Systems (RES); Land mobile service; Technical characteristics and test conditions for radio equipment intended for the transmission of data (and speech) and having an antenna connector".

[2] prETS 300 396-3: "Radio Equipment and Systems (RES); Trans-European Trunked Radio (TETRA); Technical requirements for Direct Mode Operation (DMO); Part 3: Mobile Station to Mobile Station (MS-MS) Air Interface (AI) protocol".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of this ETS, the following definitions apply:

Bit Error Ratio (BER): The ratio of the bits wrongly received to all bits received in a given logical channel.

broadcast: A unidirectional point to multipoint mode of transmission.

call transaction: All of the functions associated with a complete unidirectional transmission of information during a call. A call can be made up of one or more call transactions. In a simplex call these call transactions are sequential.

Direct Mode (DM): A mode of simplex operation where mobile subscriber radio units may communicate using radio frequencies which may be monitored by but which are outside the control of the TETRA Trunked network. DM is performed without intervention of any base station.

Direct Mode Mobile Station (DM-MS): A physical grouping that contains all of the mobile equipment that is used to obtain TETRA DM services. By definition, a Mobile Station contains at least one

Mobile Radio Stack (MRS). For synchronisation purposes, Direct Mode Mobile Stations can have one of two status levels:

- **Master:** if the DM-MS is either active in a call transaction transmitting traffic or control data, or is reserving the channel by means of channel reservation signalling and hence is **providing** synchronisation information to the channel;

- **Slave:** if the DM-MS is receiving traffic and/or signalling and hence is **deriving** synchronisation information from the channel.

logical channel: A generic term for any distinct data path. Logical channels are considered to operate between logical endpoints.

Message Erasure Rate (MER): The ratio of the messages detected as wrong by the receiver to all messages received in a given logical channel.

Probability Of Undetected Erroneous Message (PUEM): The limit ratio of the erroneous messages detected as right by the receiver to all messages received in a given logical channel.

quarter symbol number: The timing of quarter symbol duration 125/9 µs within a burst.

simplex: A mode of single or dual frequency working in which information can be transferred in both directions but not at the same time.

timebase: A device which determines the timing state of signals transmitted by a Direct Mode Mobile Station.

timeslot number: A counter indicating the timing of timeslots within a DMO frame.

3.2 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

BER	Bit Error Ratio
BN	Bit Number
DLB	Direct Mode Linearisation Burst
DLL	Data Link Layer
DM-MS	Direct Mode Mobile Station
DMO	Direct Mode Operation
DNB	Direct mode Normal Burst
DSB	Direct mode Synchronisation Burst
FN	Frame Number
LCH	Linearisation Channel
MER	Message Erasure Rate.
MN	Multiframe number
mod	modulo (base for counting)
MS	Mobile Station
PACQ	Probability of synchronisation burst acquisition
PUEM	Probability of Undetected Erroneous Message
QN	Quarter Symbol Number
SCH	Signalling Channel
SN	Symbol Number
STCH	Stealing Channel
TCH	Traffic Channel
TDMA	Time Division Multiple Access
TEI	TETRA Equipment Identity
TN	Timeslot Number

4 Radio aspects

4.1 Introduction

This clause is an introduction to the radio aspects of the TETRA DMO standard. It consists of a general description of the organisation of the radio-related functions with reference to the clauses where each part is specified in detail. Furthermore, it introduces the reference configuration that will be used throughout this ETS.

4.2 Set of logical channels

The radio subsystem provides a certain number of logical channels as defined in clause 9. The logical channels represent the interface between the protocol and the radio.

4.3 Reference configuration

For the purpose of elaborating the specification of the radio-related functions, a reference configuration of the transmission chain is used, as shown in figure 1. Only the transmission part is specified, the receiver being specified only via the overall performance requirements. With reference to this configuration, the clauses address the following functional units:

- clause 5: differential encoding and modulation;
- clause 6: characteristics of transmitter and receiver;
- clause 8: coding, reordering and interleaving, and scrambling;
- clause 9: burst building and logical channel multiplexing;
- clause 10: radio link measurements.

This reference configuration also defines a number of points of vocabulary in relation to the names of bits at different levels in the configuration.

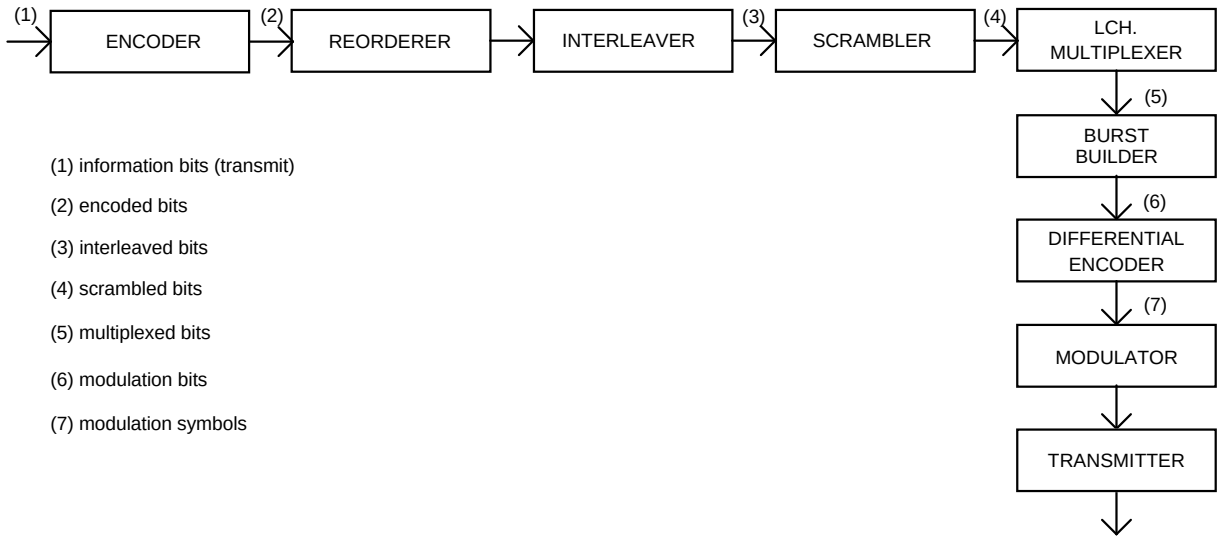

Figure 1: Reference configuration

4.4 Error control schemes

The different error control schemes are described in detail in clause 8.

4.5 Multiple access and timeslot structure

The access scheme is Time Division Multiple Access (TDMA). The carrier separation is 25 kHz.

The basic radio resource is a timeslot lasting 14,167 ms (85/6 ms) and transmitting information at a modulation rate of 36 kbit/s. This means that the timeslot duration, including guard and ramping times, is 510 bit (255 symbol) durations.

The following subclauses briefly introduces the structures of multiframes, frames, timeslots and bursts, as well as the mapping of the logical channels onto the physical channels. The appropriate specifications are found in clause 9.

4.5.1 Framing structure

A diagrammatic representation of the framing structure is shown in figure 2.

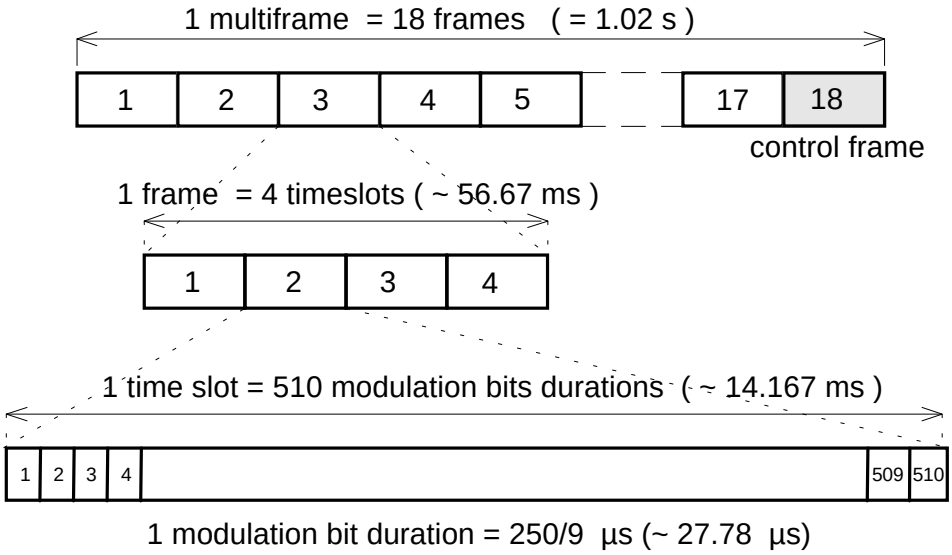

Figure 2: DM framing structure

One multiframe is subdivided into 18 frames, and has a duration of 1,02 s. The eighteenth frame in a multiframe is a control frame.

One frame is subdivided into 4 timeslots, and has a duration of 170/3 ≈ 56,67 ms.

4.5.2 Timeslots and bursts

The timeslot is a time interval of 85/6 ≈ 14,167 ms, which corresponds to 255 symbol durations.

The physical contents of a timeslot is carried by a burst. There are three different types of bursts, as defined in clause 9.

4.5.3 Mapping of logical channels onto physical channels

The mapping of the logical channels onto the physical channels, according to the mode of operation, is defined in clause 9.

4.6 Coding, interleaving and scrambling

The coding, interleaving and scrambling schemes associated with each logical channel are specified in clause 8.

4.7 Modulation

The modulation scheme is $\pi/4$-DQPSK with root-raised cosine modulation filter and a roll-off factor of 0,35. The modulation rate is 36 kbit/s. This scheme is specified in detail in clause 5.

4.8 Transmission and reception

The modulated stream is transmitted on a radio frequency carrier.

The specific RF channels, together with the requirements on the transmitter and the receiver characteristics are specified in clause 6.

DM-MS power classes are defined in clause 6.

4.9 Other radio-related functions

Transmission involves other functions. These functions, which may necessitate the handling of specific protocols, are the radio subsystem synchronisation, and the radio subsystem link control.

The synchronisation incorporates:

- frequency and time acquisition by the receiver;

- adjustment of the timebase in the DM-MS.

The requirements on synchronisation are specified in clause 7.

4.10 Performance

Under typical urban fading conditions the quality threshold for full-rate speech is reached at a C/I_c (co-channel interference) value of 19 dB, and the dynamic reference sensitivity level is - 103 dBm for mobile equipment. Details of performance requirements in various channel conditions are given in clause 6.

5 Modulation

5.1 Introduction

The following specifications apply to the baseband part of the transmitter.

5.2 Modulation type

The modulation used shall be $\pi/4$-shifted Differential Quaternary Phase Shift Keying ($\pi/4$-DQPSK).

5.3 Modulation rate

The modulation rate shall be 36 kbit/s.

5.4 Modulation symbol definition

B(m) denotes the modulation bit of a sequence to be transmitted, where m is the bit number. The sequence of modulation bits shall be mapped onto a sequence of modulation symbols S(k), where k is the corresponding symbol number.

The modulation symbol S(k) shall result from a differential encoding. This means that S(k) shall be obtained by applying a phase transition $D\phi(k)$ to the previous modulation symbol S(k-1), hence, in complex notation:

$$S(k) = S(k-1)\exp\left(jDf(k)\right)$$

$$S(0) = 1 \qquad (1)$$

The above expression for S(k) corresponds to the continuous transmission of modulation symbols carried by an arbitrary number of bursts. The symbol S(0) is the symbol before the first symbol of the first burst and shall be transmitted as a phase reference.

The phase transition Dϕ(k) shall be related to the modulation bits as follows:

Table 1: Phase transitions

B(2k-1)	B(2k)	Dϕ(k)
1	1	-3π/4
0	1	+3π/4
0	0	+π/4
1	0	-π/4

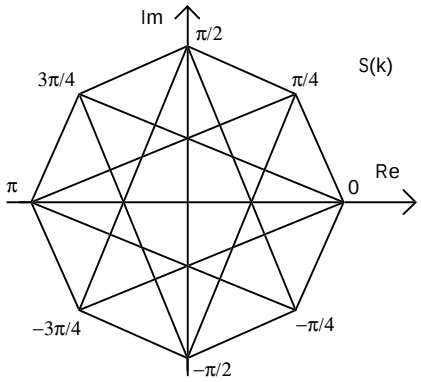

Figure 3: Modulation symbol constellation and possible transitions

The complex modulation symbol S(k) shall take one of the eight values exp(j nπ/4), where n = 2, 4, 6, 8 for even k and n = 1, 3, 5, 7 for odd k. The constellation of the modulation symbols and the possible transitions between them are as shown in figure 3.

5.5 Modulated signal definition

The modulated signal, at carrier frequency f_c, shall be given by:

$$M(t) = \mathrm{Re}\left\{s(t)\exp\left(j\left(2pf_c t + f_0\right)\right)\right\} \quad (2)$$

where:

- ϕ_0 is an arbitrary phase;
- s(t) is the complex envelope of the modulated signal defined as:

$$s(t) = \sum_{k=0}^{K} S(k)\,g\left(t - t_k\right) \quad (3)$$

where:

- K is the maximum number of symbols;
- T is the symbol duration;
- t_k = kT is the symbol time corresponding to modulation symbol S(k);

- g(t) is the ideal symbol waveform, obtained by the inverse Fourier transform of a square root raised cosine spectrum G(f), defined as follows:

$$G(f) = 1 \quad \text{for} \quad |f| \le (1-a)/2T$$

$$G(f) = \sqrt{0.5\left(1 - \sin\left(p\left(2|f|T - 1\right)/2a\right)\right)} \quad \text{for} \quad (1-a)/2T \le |f| \le (1+a)/2T$$

$$G(f) = 0 \quad \text{for} \quad |f| \ge (1+a)/2T \qquad (4)$$

- where α is the roll-off factor, which determines the width of the transmission band at a given symbol rate. The value of α shall be 0,35. For practical implementation, a time limited windowed version of g(t), designed under the constraints given by the specified modulation accuracy and adjacent channel attenuation may be applied.

5.6 Modulation filter definition

The modulation filter shall be a linear phase filter which is defined by the magnitude of its frequency response |H(f)| = G(f).

5.7 Modulation block diagram

A block diagram of the modulation process is shown on figure 4. This diagram is for explanatory purposes and does not prescribe a specific implementation. The modulation filter excited by the complex Dirac impulse function $S(k)\delta(t-t_k)$ ideally has an impulse response g(t).

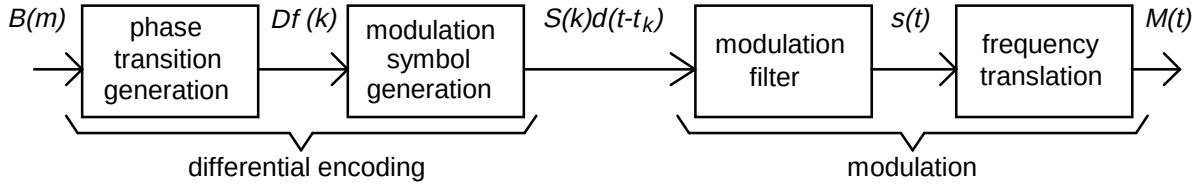

Figure 4: Block diagram of the modulation process

6 Radio transmission and reception

6.1 Introduction

This clause defines the requirements for the MS transceiver of the TETRA DMO system. This clause is applicable to TETRA systems operating at radio frequencies of 380 MHz to 520 MHz.

6.2 Frequency bands and channel arrangement

DM-MSs may only transmit and receive in those channels allocated for TETRA DMO.

Dual Watch Mobile Stations (DW-MSs) and Dual Mode Mobile Stations (DU-MSs) shall also be able to transmit and receive within TETRA Voice plus Data (V+D) channels.

The TETRA DM RF carrier separation shall be 25 kHz.

6.3 Reference test planes

For the purpose of testing, all DM-MSs shall have at least one antenna connector. Measurements shall be carried out at the appropriate antenna connector of the equipment as specified by the manufacturer.

6.4 Transmitter characteristics

6.4.1 Output power

In the following, power is defined as the average power, measured through the square root raised cosine filter defined in clause 5 over the scrambled bits of one transmitted burst as defined in clause 9.

A DM-MS may be switched to operate in more than one power class.

6.4.2 Power classes

The DM-MS nominal power shall be, according to its class, as defined in table 2.

Table 2: Nominal power of MS transmitters

Power class	Nominal power
1	not defined in DM
2 (10W)	40 dBm
3 (3W)	35 dBm
4 (1W)	30 dBm
5 (0,3W)	25 dBm

6.4.3 Unwanted conducted emissions

6.4.3.1 Definitions

Unwanted conducted emissions are defined as conducted emissions at frequencies or time intervals outside the nominal operating channel. The specified limits shall be met under realistic conditions, for instance under varying antenna mismatch.

Unless otherwise stated, unwanted emissions are specified for an equipment in the active transmit state.

A DM-MS is in the active transmit state whenever it transmits bursts or whenever it ramps-up/linearises or ramps-down.

The non-active transmit state is a state occurring during two timeslot durations (approximately 28 ms) before and after any active transmit state.

An equipment is said to be in the non-transmit state whenever it is not in the active or non-active transmit state (refer to figure 5).

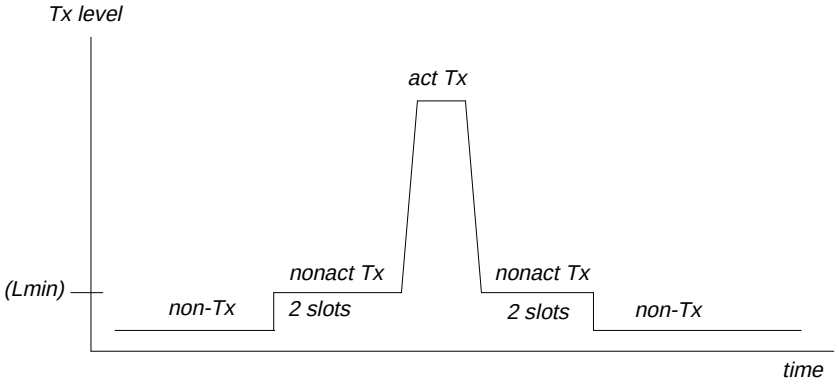

Figure 5: Schematic presentation of transmitter states

6.4.3.2 Unwanted emissions close to the carrier

Unwanted emissions close to the carrier shall be measured through the square root raised cosine filter with a roll-off factor of 0,35, as defined in clause 5 .

Measurements shall be carried out at the actual centre frequency and at frequency offsets specified in the following subclauses. When applicable, relative measurements (dBc) shall refer to the level measured at the actual centre frequency.

6.4.3.2.1 Emissions during the useful part of the burst

The levels given in table 3, at the listed frequency offsets from the actual carrier frequency, shall not be exceeded.

Table 3: Maximum adjacent power levels

Frequency offset	Max. level
25 kHz	- 60 dBc
50 kHz	- 70 dBc
75 kHz	- 70 dBc

In any case, no requirement in excess of - 36 dBm shall apply.

Frequency offset is defined as the difference of the centre measurement frequency from the actual carrier frequency. The measured values shall be averaged over the scrambled bits of the burst (see clause 9). The scrambled bits shall have a pseudo-random distribution from burst to burst.

6.4.3.2.2 Emissions during the switching transients

At the frequency offset from the actual carrier frequency given below, peak power measurements shall be carried out, covering at least the ramp-up period and the ramp-down period (see figure 7, periods t_1 and t_3 and subclause 6.4.5 for definition of t_1 and t_3. The following maximum hold level shall not be exceeded:

- frequency offset: 25 kHz;

- maximum level: - 50 dBc.

In any case no requirement in excess of - 36 dBm shall apply.

6.4.3.3 Unwanted emissions far from the carrier

These unwanted emissions are emissions (discrete, wideband noise, modulated or un-modulated) occurring at offsets equal to, or greater than, 100 kHz from the carrier frequency, measured in the frequency range 9 kHz to 4 GHz.

1) Discrete spurious:

   - the maximum allowed power for each spurious emission shall be less than - 36 dBm measured in 100 kHz bandwidth. The lower part of the spectrum (near to 9 kHz) is subject to specific measurement methods.

2) Wideband noise:

   - the following wideband noise levels, measured through the modulation filter defined in subclause 5.6 should not exceed the limits shown in table 4 for the power classes as stated and at the listed offsets from the actual carrier frequency.

Table 4: DM wideband noise limits

Frequency offset (kHz)	Maximum level (dBc)			
	0,3W (class 5)	1W (class 4)	3W (class 3)	10W (class 2)
100 kHz - 250 kHz	- 75 dBc	- 75 dBc	- 80 dBc	- 82 dBc
250 kHz - 500 kHz	- 80 dBc	- 80 dBc	- 85 dBc	- 87 dBc
>500 kHz	- 85 dBc	- 85 dBc	- 88 dBc	- 92 dBc

All levels are expressed in dBc relevant to the actual transmitted power level.

In the case where a DM-MS transmits on a DM channel frequency which is within the normal V+D MS Tx band, then the limits in table 5 shall apply symmetrically to both sides of the V+D MS Tx band.

Table 5: DM wideband noise limits (continued)

Frequency offset (kHz)	Maximum level all classes (dBc)
> f_{rb}	- 100 dBc

where f_{rb} denotes the frequency offset corresponding to the near edge of the V+D MS receive band with $f_{rb} \geq 5$ MHz.

In other cases, the - 100 dBc requirement shall apply outside of the frequency range f_x which comprises the range of frequencies over which the equipment is able to transmit within the TETRA standard, plus a guard band of 5 MHz on either side as shown in figure 6.

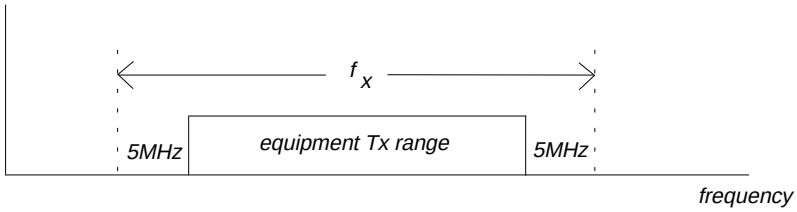

Figure 6: Definition of f_x

In any case no limit tighter than - 70 dBm shall apply.

6.4.3.4 Unwanted emissions during the Linearisation CHannel (LCH)

The peak power emitted at a frequency offset from the carrier of ± 25 kHz during the LCH shall not exceed - 30 dBc for a maximum period of 1ms. At all other times during the LCH period emissions shall not exceed - 45 dBc.

NOTE: 0 dBc refers to the transmit power during normal operation after the LCH.

6.4.3.5 Unwanted emissions in the non-transmit state

The specifications of subclause 6.5.4.2 apply.

6.4.4 Unwanted radiated emissions

Unwanted radiated emissions are emissions (whether modulated or un-modulated) radiated by the cabinet and structure of the equipment. This is also known as cabinet radiation.

The limits given in subclause 6.4.3.3 shall apply.

6.4.5 Radio frequency tolerance

The radio frequency tolerance for DM-MSs is defined in clause 7.

6.4.6 RF output power time mask

The transmit level versus time mask for DM-MS transmissions is shown in figure 7. For the time mask the power level of 0 dBc refers to the output power level of the TETRA station under consideration

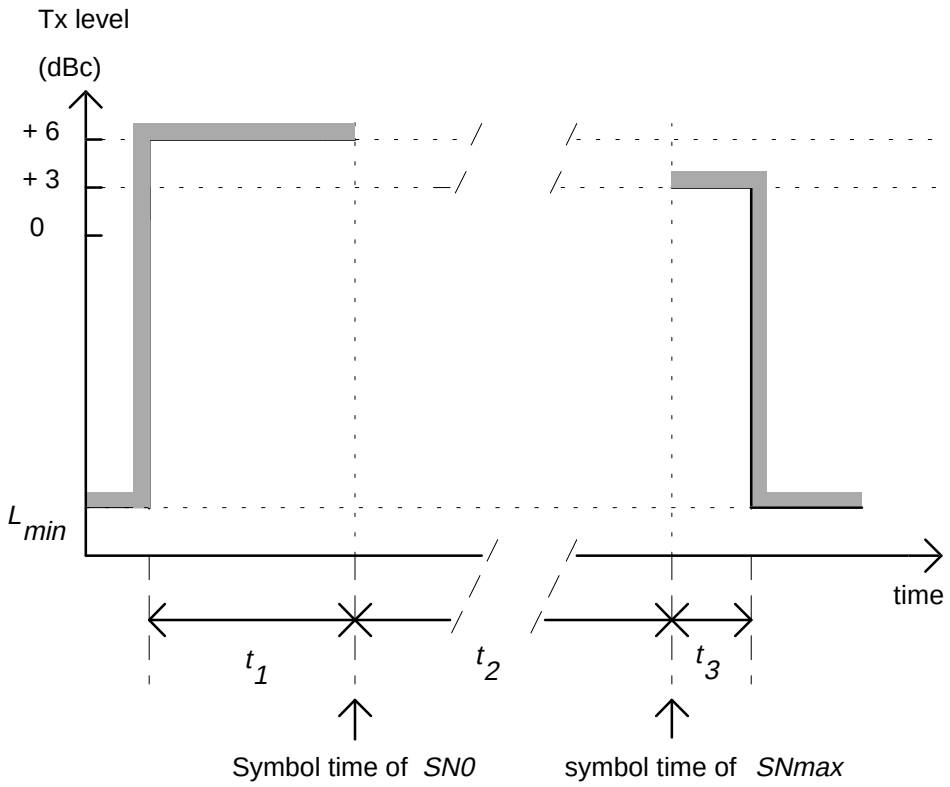

Figure 7: Transmit level versus time mask

Table 6: Transmit level versus time mask symbol durations (refer to figure 7)

Burst Type	t_1	t_2	t_3
Synchronisation	16	235 (note)	15
Linearisation	119	-	15
Normal	16	235	15
NOTE: Applies to single slot transmission only.			

Whenever bursts are consecutively transmitted by the same DM-MS on the same frequency, the transmit level versus time mask applies at the beginning of the transmission of the first burst and at the end of the transmission of the last burst.

The symbol numbers referred to as SN0 and SNmax are defined in clause 9 The timing of the transmitted bursts is specified in clause 7. The time periods t_1, t_2 and t_3, whose durations are stated in table 6, are defined in the following way:

- the time t_1 starts at the beginning of the ramp-up of the first burst, and expires just before the symbol time of SN0;

- the time t_2 starts at the symbol time of SN0 of the first burst and finishes at the symbol time of SNmax of the last burst;

- the time t_3 starts just after the symbol time of SNmax of the last burst and finishes at the end of the ramp-down.

In this subclause, the specifications of subclauses 6.4.1 and 6.6.1 shall apply during the time t_2. The output power shall be measured through the square root raised cosine filter with a roll off factor of 0,35 as defined in clause 5.

During the non-active transmit state the specification L_{min} = - 70 dBc or L_{min} = - 36 dBm, whichever is greater, shall apply.

6.4.7 Transmitter intermodulation

Intermodulation may be caused when a DM-MS transmits in the close vicinity of the antenna of another DM-MS.

6.4.7.1 Definition

Transmitter intermodulation attenuation is the ratio of the power level of the wanted signal to the power level of an intermodulation component. It is a measure of the capability of the transmitter to inhibit the generation of signals in its non-linear elements caused by the presence of the useful carrier and an interfering signal reaching the transmitter via its antenna (see ETS 300 113 [1]).

6.4.7.2 Specification

For a transmitting MS operating at the nominal power defined by its class, the intermodulation attenuation shall be at least 60 dB for any intermodulation component when measured in 30 kHz bandwidth. The interfering signal shall be un-modulated and have a frequency offset of at least 100 kHz from the carrier frequency. The power level of the interfering signal shall be 50 dB below the power level of the modulated output signal from the transmitter under test.

6.5 Receiver characteristics

In this clause, the levels of the test signals are given in terms of power levels (dBm) at the antenna connector of the receiver.

Sources of test signals shall be connected in such a way that the impedance presented to the receiver input is a 50Ω non-reactive impedance.

Static propagation conditions are assumed in all cases, for both wanted and unwanted signals.

6.5.1 Blocking characteristics

6.5.1.1 Definition

Blocking is a measure of the capability of the receiver to receive a modulated wanted input signal in the presence of an unwanted un-modulated input signal on frequencies other than those of the spurious responses or the adjacent channels, without this unwanted input signal causing a degradation of the performance of the receiver beyond a specified limit.

6.5.1.2 Specification

The blocking performance specification shall apply at all frequencies except those at which spurious responses occur (see subclause 6.5.2).

The static reference sensitivity performance as specified in subclause 6.6.2.4 shall be met when the following signals are simultaneously input to the receiver:

- a wanted signal at the nominal receive frequency f_0, 3 dB above the static reference sensitivity level as specified in subclause 6.6.2.4;

- a continuous sine wave signal at a frequency offset from f_0 and level as defined in table 7.

Table 7: Blocking levels of the receiver

Offset from nominal Rx freq.	Level of interfering signal
50 kHz to 100 kHz	- 40 dBm
100 kHz to 200 kHz	- 35 dBm
200 kHz to 500 kHz	- 30 dBm
>500 kHz	- 25 dBm

6.5.2 Spurious response rejection

6.5.2.1 Definition

Spurious response rejection is a measure of the capability of a receiver to receive a wanted modulated signal without exceeding a given degradation due to the presence of an unwanted un-modulated signal at any other frequency at which a response is obtained, i.e. for which the blocking limit is not met.

6.5.2.2 Specification

The static reference sensitivity performance as specified in subclause 6.6.2.4 shall be met when the following signals are simultaneously applied to the receiver:

- a wanted signal at nominal receive frequency f_o, 3 dB above the static reference sensitivity level as specified in subclause 6.6.2.4;

- a continuous sine wave signal at frequency f as defined below at a level of -45 dBm.

The number of spurious responses at any frequency f within a limited frequency range, defined below at which the blocking specification of subclause 6.5.1.2 is not met shall not exceed 0,05 x (number of frequency channels in the limited frequency range).

The limited frequency range is defined as the frequency of the local oscillator signal f_{lo} applied to the first mixer of the receiver plus or minus the sum of the intermediate frequencies (f_{i1},.....f_{in}) and a half of the switching range (sr) of the receiver.

Hence the frequency f_l of the limited frequency range is:

$$f_{lo} - \sum_{j=1}^{n} f_{ij} - sr/2 \le f_l \le f_{lo} + \sum_{j=1}^{n} f_{ij} + sr/2 \qquad (5)$$

Where receiver switching range (sr) is the maximum frequency range over which the receiver can be operated without reprogramming or realignment as declared by the manufacturer.

6.5.3 Intermodulation response rejection

6.5.3.1 Definition

Intermodulation response rejection is a measure of the capability of the receiver to receive a wanted modulated signal without exceeding a given degradation due to the presence of two or more unwanted signals with a specific frequency relationship to the wanted signal frequency as defined in ETS 300 113 [1].

6.5.3.2 Specification

The static reference sensitivity performance as specified in subclause 6.6.2.4 shall be met when the following signals are simultaneously input to the receiver:

- a wanted signal at the nominal receive frequency f_o, 3 dB above the static reference sensitivity level;
- a continuous sine wave signal at frequency f_1 and with a level of - 47 dBm;

- a pseudo-random sequence TETRA modulating a signal at frequency f_2, with a level of - 47 dBm, such that $f_o = 2f_1 - f_2$ and $| f_2-f_1 | = 50$ kHz.

6.5.4 Unwanted conducted emissions

6.5.4.1 Definition

Unwanted emissions from the equipment when in reception are defined as conducted emissions at any frequency, when the equipment is in the non-transmit state.

6.5.4.2 Specification

The power emitted by the equipment shall not exceed - 57 dBm at frequencies between 9 kHz and 1 GHz and - 47 dBm at frequencies from 1 GHz to 4 GHz, as measured in the bandwidth of 30 kHz.

6.5.5 Unwanted radiated emissions

Unwanted radiated emissions are emissions radiated by the cabinet and structure of the equipment (MS or BS) in the non-Tx state. This is also known as cabinet radiation.

The limits given in subclause 6.5.4.2 shall apply

6.6 Transmitter/receiver performance

Subclause 6.6.1 specifies the modulation accuracy requirement, by setting limits on the Root Mean Square (RMS) error between the actual transmitted signal waveform and the ideal signal waveform. Subclause 6.6.2 specifies the receiver performance, assuming that transmit errors do not occur. Subclause 6.6.3 specifies all the propagation models that are defined in this ETS.

6.6.1 Modulation accuracy

The specified requirement is vector error magnitude; this does not only take into account modulation filtering linear distortion (amplitude and phase) or modulator impairments (quadrature offset, phase and linear amplitude errors in the modulation symbol constellation) but is a measure of the whole transmitter quality. It also takes into account local oscillator phase noise, filter distortion, and non-linearity of amplifiers. Vector error magnitude shall be specified at symbol time (see subclause 6.6.1.2) and the vector error magnitude requirement shall be fulfilled by the TETRA equipment with maximum and with minimum power levels (as defined in subclause 6.4.1).

6.6.1.1 Ideal case

The modulation symbol s(t) transmitted by an ideal transmitter having a filter impulse response g(t) is defined in clause 5.

$$g^*(-t)\big|_{t=t_k}$$

Let Z(k) denote the output of an ideal receive filter with impulse response .The ideal transmit and receive filters in cascade form a raised cosine Nyquist filter, having a symbol waveform going through zero at symbol duration intervals, so there is no inter-symbol interference at any instant t = t_k, where t_k is the symbol time corresponding to the k-th symbol (as defined in clause 5).

In this case, the output of an ideal receive filter at any instant t_k, stimulated by an ideal transmitter, will be equal to the k-th modulation symbol S(k):

$$Z(k) = s(t) * g^*(-t)\big|_{t=t_k} = S(k) \qquad (6)$$

In this subclause, the numbering of the modulation symbols used is the one defined in clause 9.

6.6.1.2 Vector error magnitude requirement at symbol time

Let Z(k) be the output produced by observing the real transmitter through the ideal receive filter at symbol time t_k. Z(k) is modelled as:

$$Z(k) = \left\{ C_0 + \left[S(k) + E(k) \right] \right\} C_1 W(k) \qquad (7)$$

where:

- E(k) is the vector error of modulation symbol S(k);

- W(k) = exp(jkΘ) accounts for a frequency offset giving Θ radians per symbol phase rotation due to transmitter frequency inaccuracy (see clause 7). The possible amplitude variations shall be integrated in the vector error;

- C_0 is a complex constant characterising the residual carrier;

- C_1 is a complex constant representing the output amplitude and initial phase of the transmitter.

The magnitude of C_0 shall be less than 5 % of the magnitude of S(k). The task of the test receiver is then to:

- estimate the symbol time for processing the receive part;

- estimate the values of C_0, C_1 and Θ. The resulting estimates shall be denoted by C_0', C_1' and Θ′ respectively;

- perform a normalisation of the modulation symbol Z(k) accordingly. The modulation symbol that results from this normalisation shall be denoted by Z′(k):

$$Z'(k) = \left[Z(k) \exp(-jkQ') \Big/ C_1' \right] - C_0' \tag{8}$$

With the above notations, the Sum Square Vector Error (SSVE) is defined as:

$$SSVE = \sum_{k=1}^{SN\max} \left| Z'(k) - S(k) \right|^2 \tag{9}$$

where SNmax is the number of symbols in the burst.

The RMS vector error is then computed as the square root of the SSVE divided by the number of symbols in the burst:

$$RMSVE = \sqrt{SSVE / SN\max} \tag{10}$$

The RMS vector error in any burst shall be less than 0,1.

The peak vector error magnitude |Z′(k)-S(k)| shall be less than 0,3 for any symbol.

6.6.2 Receiver performance

This subclause specifies the minimum required receiver performance in terms of Bit Error Ratio (BER), Message Erasure Rate (MER) or Probability of Undetected Erroneous Message (PUEM) (whichever is appropriate), taking into account that transmitter errors do not occur, and that the transmitter shall be tested separately (see subclause 6.6.1).

In this clause, the levels of the test signals are given in terms of power levels (dBm) at the antenna connector of the receiver. For the definition of power level refer to subclause 6.4.1.

The receiver performance for the speech channel is not specified in this clause.

6.6.2.1 Nominal error rates

This subclause describes the transmission requirements in terms of error rates in nominal conditions i.e. without interference and with an input level of - 85 dBm. The relevant propagation conditions are given in subclause 6.6.3.

Under the following propagation conditions, the BER of the non-protected bits, equivalent to the TCH/7,2 shall have the limits given in table 8.

Table 8: Nominal error rates

Propagation model	BER
STATIC	0,01 %
DR50	0,40 %
DU50	0,60 %

This performance shall be maintained up to - 40 dBm input level for the static conditions, and multipath conditions. Furthermore, for static conditions, a BER of < 0,1 % shall be maintained up to - 20 dBm.

6.6.2.2 Dynamic reference sensitivity

The minimum required dynamic reference sensitivity is specified according to the logical channel, and the propagation condition at the dynamic reference sensitivity level. The dynamic reference sensitivity level for DM-MSs shall be - 103 dBm.

Table 9 gives the maximum permissible DM-MS receiver MER or BER at the dynamic reference sensitivity level for DU50 and DR50 propagation models.

For Signalling CHannel (SCH)/S, SCH/H and SCH/F, a PUEM < 0,001 % shall be achieved at the dynamic reference sensitivity level.

Table 9: Maximum permissible DM-MS receiver MER or BER at dynamic reference sensitivity level

Logical channel	Criterion	Propagation Model	
		DU50	DR50
SCH/S	MER	5,60 %	8,00 %
SCH/H	MER	6,40 %	8,00 %
SCH/F	MER	5,40 %	8,00 %
TCH/7.2	BER	1,70 %	2,20 %
TCH/4.8 N=1	BER	1,50 %	2,00 %
TCH/4.8 N=4	BER	0,45 %	0,40 %
TCH/4.8 N=8	BER	0,15 %	0,06 %
TCH/2.4 N=1	BER	0,37 %	0,35 %
TCH/2.4 N=4	BER	0,01 %	0,01 %
TCH/2.4 N=8	BER	0,01 %	0,01 %
STCH	MER	6,40 %	8,00 %
NOTE: N gives the interleaving depth in number of blocks (see clause 8).			

6.6.2.3 Reference interference ratios

The minimum required reference interference ratios are specified according to the logical channel and the propagation condition at the reference interference ratio (for co-channel, C/I_c, or adjacent channel, C/I_a). The reference interference ratio shall be:

- for co-channel interference: C/I_c = 19 dB;

- for adjacent channel interference: C/I_a = - 45 dB.

In the case of co-channel interference, these specifications apply for a wanted input signal level of - 85 dBm, and in the case of adjacent channel interference for a wanted input signal level 3 dB above the dynamic reference sensitivity level. In any case the interference shall be a continuous TETRA random modulated signal subjected to an independent realisation of the same propagation condition as the wanted signal.

Table 10 specifies the maximum permissible DM-MS receiver MER or BER at the reference interference level for DU50 and DR50 propagation conditions.

For SCH/S, SCH/H and SCH/F, a PUEM < 0,001 % shall be achieved at the reference interference level.

Table 10: Maximum permissible DM-MS receiver MER or BER at reference interference level

Logical channel	Criterion	Propagation Model	
		DU50	DR50
SCH/S	MER	4,90 %	6,00 %
SCH/H	MER	5,60 %	7,00 %
SCH/F	MER	4,80 %	6,50 %
TCH/7,2	BER	1,70 %	2,00 %
TCH/4,8 N=1	BER	1,60 %	2,00 %
TCH/4,8 N=4	BER	0,47 %	0,40 %
TCH/4,8 N=8	BER	0,18 %	0,06 %
TCH/2,4 N=1	BER	0,45 %	0,35 %
TCH/2,4 N=4	BER	0,01 %	0,01 %
TCH/2,4 N=8	BER	0,01 %	0,01 %
STCH	MER	5,60 %	7,00 %
NOTE: N gives the interleaving depth in number of blocks (see clause 8).			

6.6.2.4 Static reference sensitivity

The minimum required static reference sensitivity is specified according to the logical channel and the receiver class at the static reference sensitivity level. For DM-MSs the static reference sensitivity level shall be - 112 dBm.

Table 11 gives the maximum permissible DM-MS receiver MER or BER at the static reference sensitivity level.

For SCH/S, SCH/H and SCH/F, a PUEM < 0,001 % shall be achieved at the static reference sensitivity level.

Table 11: Maximum permissible DM-MS receiver MER or BER at static reference sensitivity level

Logical channel	Criterion	Propagation model
		STATIC
SCH/S	MER	3,00 %
SCH/H	MER	5,00 %
SCH/F	MER	9,00 %
TCH/7,2	BER	4,00 %
TCH/4,8 N=1	BER	0,30 %
TCH/4,8 N=4	BER	0,20 %
TCH/4,8 N=8	BER	0,15 %
TCH/2,4 N=1	BER	0,01 %
TCH/2,4 N=4	BER	0,01 %
TCH/2,4 N=8	BER	0,01 %
STCH	MER	5,00 %
NOTE: N gives the interleaving depth in number of blocks (see clause 8).		

6.6.2.5 MS receiver performance for acquisition of synchronisation burst

This subclause specifies reference sensitivity performance of a MS receiver for the acquisition of the Direct mode Synchronisation Burst (DSB). The performance is defined in terms of the Probability of synchronisation burst ACQuisition (PACQ) of detecting DSB and correctly decoding SCH information for the condition where the MS is listening on the frequency while DSB is transmitted.

Table 12: MS receiver performance requirement (probability of correct detection and decoding) for synchronisation burst acquisition

Propagation condition	DR50
PACQ	0,8

6.6.3 Propagation conditions

The following contains all necessary information on the propagation models that are referred to in this ETS.

6.6.3.1 Tap-gain process types

This subclause defines the statistical properties of the stationary complex tap-gain processes, to be applied for the propagation models, in terms of a Probability Density Function (PDF) and a Power Density Spectrum (PDS) which models the Doppler spectrum. The complex tap-gain processes, denoted by a(t) and defined hereunder, are normalised to unity power.

CLASS is the tap-gain process having a PDS equal to the classical Doppler spectrum. The real and imaginary parts of a(t) exhibit an identical gaussian PDF, an identical PDS and are mutually statistically independent. Hence |a(t)| is Rayleigh distributed. The PDS of a(t) is defined by:

$$S(f) = S_{CLASS}(f, f_d) = \begin{cases} \dfrac{1}{\pi f_d \sqrt{1-(f/f_d)^2}} & for\ -f_d < f < f_d \\ 0 & elsewhere \end{cases} \quad (11)$$

where the parameter f_d represents the maximum Doppler shift (in Hz), defined as $f_d = v/\lambda$ with the vehicle speed v (in m/s) and the wavelength λ (in m).

STATIC(f_s) is a tap-gain process with a constant magnitude |a(t)|=1. The PDS of a(t) is defined by:

$$S(f) = S_{STATIC}(f, f_s) = \delta(f - f_s) \quad (12)$$

where $\delta(.)$ represents the Dirac delta function and f_s the Doppler shift (in Hz).

RICE is a tap-gain process which is the sum process of the two processes CLASS and STATIC(f_s), with $f_s = 0,7\ f_d$, each contributing half of the total power. Hence |a(t)| is Rician distributed and the PDS is:

$$S(f) = S_{RICE}(f, f_d) = 0,5\, S_{CLASS}(f, f_d) + 0,5\, S_{STATIC}(f, 0,7 f_d) \quad (13)$$

6.6.3.2 DM propagation models

In this subclause, the propagation models that are referred to in this ETS are defined. The vehicle speed x (in km/h), which affects f_d (see above), is attributed to the model designation (e.g. DU50 means Urban Area for 50 km/h).

Table 13: Propagation models

Propagation model	Tap number	Relative delay (µs)	Average relative power (dB)	Tap-gain process
Static	1	0	0	STATIC(0)
Urban Area (DUx)	1	0	0	RICE
Rural Area (DRx)	1	0	0	CLASS

7 Radio sub-system synchronisation

7.1 Introduction

This subclause defines the requirements for synchronisation in TETRA DM Operation, for carrier frequencies of between 380 MHz and 520 MHz.

7.2 Definitions and general requirements for synchronisation of DM-MSs

The DM-MS which provides the synchronisation reference is defined as the "master" DM-MS. A DM-MS which initiates a call becomes the master for the duration of that transaction. Any DM-MS which synchronises on a "master" DM-MS is defined as a "slave" DM-MS.

At the beginning of a call, during a call or during channel reservation, the master DM-MS shall transmit synchronisation bursts to enable any receiving DM-MS on the same channel to synchronise itself in terms of frequency and time, or to maintain synchronisation.

In any case the slave DM-MS shall align its burst transmission to the timeslots and carrier frequency dictated by the transmission of the master DM-MS.

The timebase of a DM-MS shall continuously count quarter symbols, symbols, timeslots, frames and multiframes, independently of whether the DM-MS is transmitting or not (see subclause 7.3). A slave DM-MS is said to be fully time synchronised if all of its timebase counters run synchronously, within a specified tolerance to those of the master DM-MS.

The timing information contained in the SCH/S transmitted by the master DM-MS in the synchronisation burst shall refer to the slot and frame number at which the synchronisation burst is transmitted. Upon reception of an SCH/S, the slave DM-MS shall use this timing information to set its slot and frame counters.

In normal cases (see note) a slave DM-MS which becomes the new master DM-MS after a changeover has been carried out successfully shall adopt the state of the timing counters indicated by the old master DM-MS but not the carrier frequency synchronisation. The DM-MS taking over the master role shall use its own frequency source as the reference to generate the carrier frequency and to increment its timebase counters. The transition point at which changeover occurs shall be at a timeslot boundary.

NOTE: An exception may be in the case of dual watch.

7.3 Timebase counters

7.3.1 Definition of counters

The timing state of the signals transmitted by a DM-MS shall be defined by the following counters:

- Quarter symbol Number (QN) (1 - 4);
- Symbol Number (SN) (1 - 255);
- Timeslot Number (TN) (1 - 4);
- Frame Number (FN) (1 - 18);
- Multiframe Number (MN) (1-60).

7.3.2 Relationship between the counters

The relationship between these counters shall be as follows:

QN increments every 125/9 µs (unless otherwise required by the slave DM-MS timebase adjustment) as follows:

QN: = QN mod (4) + 1; (14)

SN increments whenever QN changes from 4 to 1 as follows:

SN: = SN mod (255) + 1; (15)

TN increments whenever SN changes from 255 to 1 as follows:

TN: = TN mod (4) + 1; (16)

FN increments whenever TN changes from 4 to 1 as follows:

FN: = FN mod (18) + 1; (17)

MN increments whenever FN changes from 18 to 1 as follows:

MN: = MN mod (60) + 1. (18)

The simultaneous change of state of all counters to 1 defines the timebase reference point.

7.4 Requirements for the frequency source of DM mobiles

A DM-MS shall use a single frequency source of accuracy better than ± 2 ppm for both RF frequency generation and clocking the timebase.

7.5 Requirements for the synchronisation of a slave DM mobile

The following requirement for carrier frequency and timebase accuracy shall be met by a slave DM-MS for a transmission period of one multiframe duration following initial synchronisation. This requirement shall be achieved at receive signal levels greater than or equal to 3dB below the reference sensitivity:

- whenever the slave DM-MS transmits its carrier frequency, it shall be accurate to within ± 0,5 ppm and its burst timing shall be accurate to within ½ symbol period compared to signals received from the master DM-MS.

The following requirement for the carrier frequency and timebase shall be met by a slave DM-MS for the time period following one multiframe after initial synchronisation to the end of reception of the masters transmission:

- whenever the slave DM-MS transmits its carrier frequency, it shall be accurate to within ± 0,2 ppm and its burst timing shall be accurate to within ¼ symbol period compared to signals received from the master DM-MS.

The signals received from the master DM-MS shall be averaged over sufficient time so that errors due to noise, interference or Doppler spread are minimised.

8 Channel coding

8.1 Introduction

A reference configuration of the TETRA transmission chain is given in figure 1. This clause defines the error control process which applies to the information bits (packed in DATA LINK LAYER (DLL) blocks, see definition in clause 14), and which provides multiplexed bits (packed in multiplexed blocks) as shown in figure 1.

This clause applies to logical channels that are not related to speech transmission. The definition of logical channels is given in clause 9.

This clause includes the specification of encoding, reordering and interleaving, and scrambling, but does not specify any data processing on the receive part.

A definition of the error control process is provided for each kind of logical channel.

8.2 General

8.2.1 Interfaces in the error control structure

The definition of interfaces within the error control structure is given by figure 8.

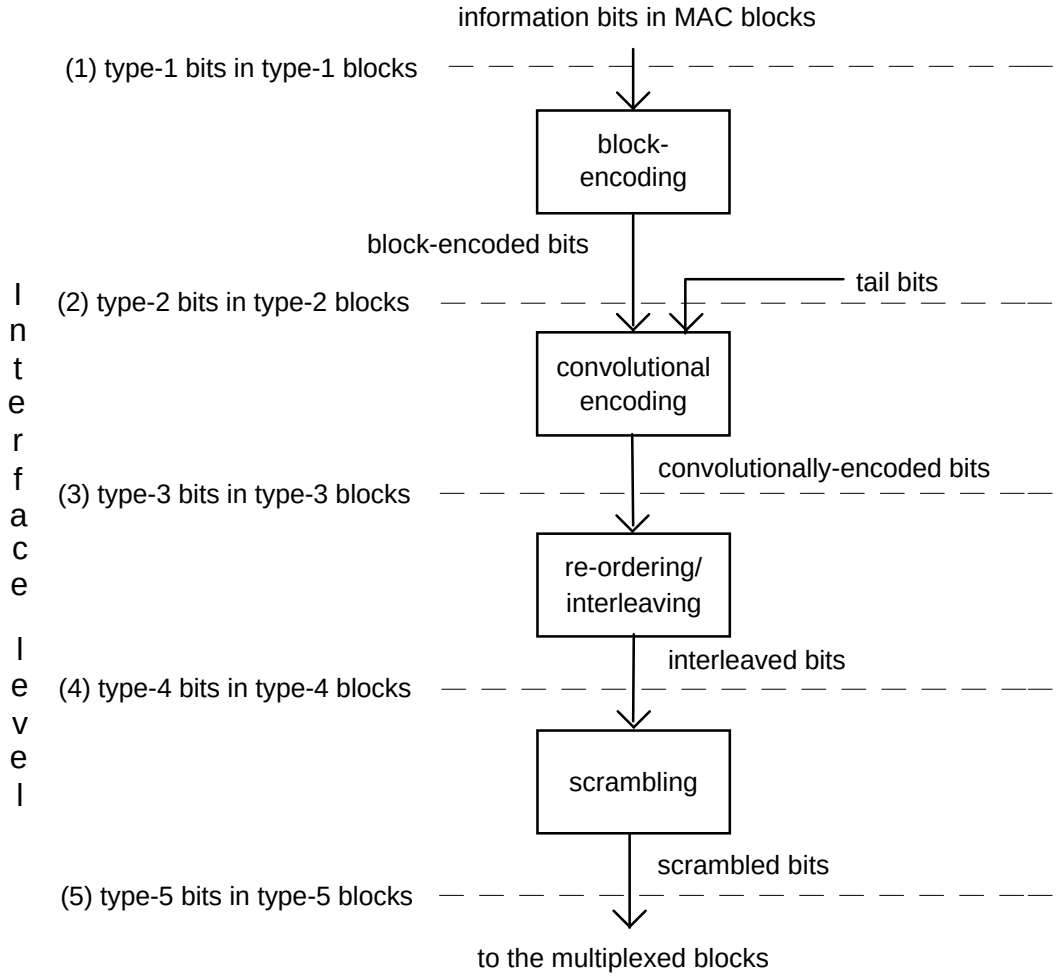

Figure 8: Interfaces in the error control structure

Each logical channel shall have its own error control scheme. For each one, the information bits (eventually including a DLL header) are referred to as type-1 bits. The type-1 bits are packed in DLL blocks (see clause 14), which are referred to as type-1 blocks. This defines interface (1) in figure 8.

The processing in the transmit part shall be as follows:

- the type-1 bits shall be encoded by a block code, providing block-encoded bits. In some cases tail bits shall be appended to these block-encoded bits. The block-encoded bits and the tail bits (if added) are referred to as type-2 bits and shall be packed in a type-2 block. This defines interface (2);

- the type-2 bits shall be encoded by a convolutional code, which provides the convolutionally-encoded bits. The convolutionally-encoded bits are referred to as type-3 bits and shall be packed in a type-3 block. This defines interface (3);

- the type-3 bits shall be reordered and interleaved, into interleaved bits: the interleaved bits are referred to as type-4 bits and shall be packed in encoded blocks (see clause 14). Encoded blocks are referred to as type-4 blocks. This defines interface (4);

- the type-4 bits shall be scrambled, into type-5 bits, which compose type-5 blocks. This defines the interface (5). These bits shall then be mapped into multiplexed blocks. A multiplexed block shall be one of 5 different kinds:

- control block;
- broadcast block;
- synchronisation block;
- block-1 block; or
- block-2 block.

All these operations are made on a per type-1 block basis. The sizes of type-1 blocks and of type-5 blocks and multiplexed blocks depend on the logical channel with which they are associated.

8.2.2 Notation

For ease of understanding, a notation for bits and blocks is given for use throughout this clause:

- x is the interface number, as defined in figure 8: x = 1, 2, 3, 4, 5;
- n is a block number;
- $B_x(n)$ is the type-x block number n;
- K_x is the number of bits that are carried by one type-x block;
- k is a bit number;
- $b_x(n,k)$ is the type-x bit number k in the type-x block number n;
- alternatively $b_x(k)$ is the type-x bit number k in a type-x block (for ease of notation), with k = 1, 2,..., K_x, and n = 1, 2,...

The bits of the multiplexed blocks shall be denoted as, accordingly:

- sb(k) is bit number k in a synchronisation block;
- bkn1(k) is bit number k in a block-1 block;
- bkn2(k) is bit number k in a block-2 block.

8.2.3 Definition of error control codes

8.2.3.1 16-state Rate-Compatible Punctured Convolutional (RCPC) codes

The RCPC codes shall encode K_2 type-2 bits $b_2(1)$, $b_2(2)$,..., $b_2(K_2)$ into K_3 type-3 bits $b_3(1)$, $b_3(2)$,..., $b_3(K_3)$. This encoding shall be performed in two steps:

- encoding by a 16-state mother code of rate 1/4;
- puncturing of the mother code so to obtain a 16-state RCPC code of rate K_2/K_3.

A general description of these two steps is given in subclauses 8.2.3.1.1 and 8.2.3.1.2 respectively. The puncturing coefficients of the 16-state RCPC codes of rates 2/3, 1/3, 292/432 and 148/432 are given in subclauses 8.2.3.1.3, 8.2.3.1.4, 8.2.3.1.5 and 8.2.3.1.6 respectively.

8.2.3.1.1 Encoding by the 16-state mother code of rate 1/4

The input to the mother code of any type-2 bit $b_2(k)$, k = 1, 2,..., K_2, implies the output, by the mother code, of 4 bits, denoted by V(4(k-1)+i), i = 1, 2, 3, 4, which shall be calculated as follows.

- any of the 4 generator polynomials of the mother code , $G_i(D)$, i = 1, 2, 3, 4, can be written as:

$$G_i(D) = \sum_{j=0}^{4} g_{i,j} D^j \quad , \quad \text{for i =1,2,3,4,} \tag{19}$$

where $g_{i,j}$ = 0 or 1, j = 0,1,2,3,4.

This means that the encoded bits are defined by:

$$V(4(k-1)+i) = \sum_{j=0}^{4} b_2(k-j) g_{i,j} \quad , \quad \text{for i=1,2,3,4, and k=1,2,...} K_2 \tag{20}$$

where the sum is meant modulo 2, and where $b_2(k-j) = 0$ for $k \leq j$.

The generator polynomials of the mother code shall be:

$G_1(D) = 1 + D + D^4$ (21)

$G_2(D) = 1 + D^2 + D^3 + D^4$ (22)

$G_3(D) = 1 + D + D^2 + D^4$ (23)

$G_4(D) = 1 + D + D^3 + D^4$ (24)

8.2.3.1.2 Puncturing of the mother code

The puncturing of the mother code into a 16-state RCPC code of rate (K_2/K_3) is achieved by selecting K_3 type-3 bits out of the (4 K_2) bits encoded by the mother code. This selection shall be as follows.

Denoting by P(1), P(2),.., P(t) the t puncturing coefficients (each one being equal to 1, 2, 3, 4, 5, 6, 7, or 8), the type-3 bits are given by:

$b_3(j) = V(k)$, for j=1, 2,..., K_3, (25)

with k = 8 ((i -1) div t) + P(i - t((i -1) div t)),

where i and t are defined in the following puncturing schemes.

8.2.3.1.3 Puncturing scheme of the RCPC code of rate 2/3

The t=3 puncturing coefficients shall be:

P(1) = 1, P(2) = 2, P(3) = 5, and i=j. (26)

8.2.3.1.4 Puncturing scheme of the RCPC code of rate 292/432

The t=3 puncturing coefficients shall be:

P(1)=1, P(2)=2, P(3)=5, and i=j+(j -1) div 65, with j=1, 2,..., 432. (27)

8.2.3.1.5 Puncturing scheme of the RCPC code of rate 148/432

The t=6 puncturing coefficients shall be:

P(1)=1, P(2)=2, P(3)=3, P(4)=5, P(5)=6, P(6)=7, and i=j+(j -1) div 35, with j=1, 2,..., 432. (28)

8.2.3.2 (K_1+16, K_1) block code

The (K_1+16, K_1) code shall encode K_1 type-1 bits $b_1(1)$, $b_1(2)$,..., $b_1(K_1)$ into (K_1+16) type-2 bits $b_2(1)$, $b_2(2)$,..., $b_2(K_1+16)$. The encoding rule shall be as follows:

- the type-1 bits are treated as the coefficients of the polynomial:

$$M(X) = \sum_{k=1}^{K_1} b_1(k) X^{K_1-k} \tag{29}$$

Let F(X) be:

$$F(X) = \left[\left(X^{16} M(X) + X^{K_1} \sum_{i=0}^{15} X^i\right) \bmod G(X)\right] + \sum_{i=0}^{15} X^i \tag{30}$$

where all operations are meant modulo 2, and G(X) is the generator polynomial of the code:

$$G(X) = X^{16} + X^{12} + X^5 + 1 \tag{31}$$

F(X) is of degree 15, with coefficients denoted by f(0), f(1),..., f(15):

$$F(X) = \sum_{i=0}^{15} f(i) X^i \tag{32}$$

The K_2 type-2 bits, with $K_2 = K_1+16$, are then given by:

$b_2(k) = b_1(k)$, for $k = 1, 2, ..., K_1$, and

$b_2(k) = f(K_1+16-k)$, for $k = K_1+1, K_1+2, ..., K_1+16$. (33)

8.2.4 Definition of interleaving schemes

8.2.4.1 Block interleaving

A (K,a) block interleaver shall re-order K_3 type-3 bits $b_3(1)$, $b_3(2)$,..., $b_3(K_3)$ into K_4 type-4 bits $b_4(1)$, $b_4(2)$,..., $b_4(K_4)$, with $K=K_3=K_4$, in the following way:

$b_4(k) = b_3(i)$, $i = 1, 2, ..., K$, (34)

with $k = 1 + ((a * i) \bmod K)$

8.2.4.2 Interleaving over N blocks

Interleaving over N blocks use two steps to interleave a sequence of M type-3 blocks $B_3(1)$, $B_3(2)$,.. $B_3(M)$ of 432 bits each into a sequence of (M+N-1) type-4 blocks $B_4(1)$, $B_4(2)$,...$B_4(M+N-1)$ of 432 bits each, where M is an integer and N has values 1, 4, or 8. This interleaving shall be as follows.

Firstly, a diagonal interleaver interleaves the M blocks $B_3(1)$, $B_3(2)$,..$B_3(M)$ into (M+N-1) blocks $B'_3(1)$, $B'_3(2)$,.. $B'_3(M+N-1)$. Denoting by $b'_3(m,k)$ the k-th bit of block $B'_3(m)$, with k = 1, 2,.., 432 and m = 1, 2,..., M+N-1,

$b'_3(m,k) = b_3(m-j, j+1+(i * N))$, for $1 \le m - j \le M$,

$b'_3(m,k) = 0$, otherwise (35)

with $j = (k-1) \text{ div } (432/N)$, and $i = (k-1) \bmod (432/N)$.

A block interleaver then interleaves each block $B'_3(m)$ into type-4 block $B_4(m)$, m = 1, 2,..M+N-1:

$b_4(m,i) = b'_3(m,k)$, (36)

with k = 1, 2,..., 432, and i = 1+ ((103 * k) mod 432).

8.2.5 Definition of scrambling

8.2.5.1 Scrambling method

Scrambling shall transform K_4 type-4 bits $b_4(1)$, $b_4(2)$,..$b_4(K_4)$ into K_5 type-5 bits $b_5(1)$, $b_5(2)$,..$b_5(K_5)$, with $K_5=K_4$, as follows:

$b_5(k) = b_4(k) + p(k)$, for k = 1, 2,..., K_5 , (37)

where the addition is meant modulo 2, and p(k) is the k-th bit of the scrambling sequence.

8.2.5.2 Scrambling sequence

The scrambling sequence {p(k), k = 1, 2,..., K_5} shall be generated from the 30 bits of the DM colour code e(1), e(2),.., e(30), except for the SCH/S and SCH/H of the DSB, by means of linear feedback registers. For the scrambling of SCH/S and SCH/H of the DSB, all bits e(1), e(2),.., e(30) shall be set equal to zero.

The scrambling sequence generator shall be based upon the following connection polynomial:

$$c(x) = \sum_{i=0}^{32} c_i X^i \quad (38)$$

with c_i = 1 for i = 0, 1, 2, 4, 5, 7, 8, 10, 11, 12, 16, 22, 23, 26 and 32, and c_i = 0 elsewhere and where all operations are meant modulo 2. The resultant polynomial is therefore:

$$c(x) = 1 + X + X^2 + X^4 + X^5 + X^7 + X^8 + X^{10} + X^{11} + X^{12} + X^{16} + X^{22} + X^{23} + X^{26} + X^{32} \quad (39)$$

The k-th bit of the scrambling sequence is given by:

$$p(k) = \sum_{i=1}^{32} c_i p(k-i) \quad (40)$$

with the following initialisation:

p(k) = e(1-k), for k = -29, -28,... 0,

p(k) = 1, for k = -31, -30. (41)

8.3 Error control schemes

In this subclause the error control scheme associated with each logical channel is defined. Figures 9 and 10 give the error control structure.

8.3.1 Signalling channels

8.3.1.1 Synchronisation Signalling CHannel (SCH/S)

One type-1 block shall contain 60 type-1 bits $b_1(1)$, $b_1(2)$,..., $b_1(60)$.

A (76,60) block code shall encode the 60 type-1 bits into 76 block-encoded bits, $b_2(1)$, $b_2(2)$,...$b_2(76)$. This code is the (K_1+16, K_1) block code as defined in subclause 8.2.3.3, with K_1=60.

Four tail bits, $b_2(77)$, $b_2(78)$, $b_2(79)$, $b_2(80)$, all set equal to zero, shall be appended to the 76 block-encoded bits.

The resultant bits $b_2(1)$, $b_2(2)$,..., $b_2(80)$ shall be the type-2 bits.

A 16-state RCPC code with rate 2/3 (see subclause 8.2.3.1), shall encode the 80 type-2 bits into 120 type-3 bits, $b_3(1)$, $b_3(2)$,..., $b_3(120)$.

A (120, 11) block interleaving (see subclause 8.2.4.1) shall re-order the 120 type-3 bits into 120 type-4 bits, $b_4(1)$, $b_4(2)$,..., $b_4(120)$.

The 120 type-4 bits, $b_4(1)$, $b_4(2)$,..., $b_4(120)$ compose the type-4 block for SCH/S. They shall be scrambled into bits $b_5(1)$, $b_5(2)$, ..., $b_5(120)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The multiplexed bits of the synchronisation block shall be defined as:

$sb(k) = b_5(k)$, for k = 1, 2,..., 120. (42)

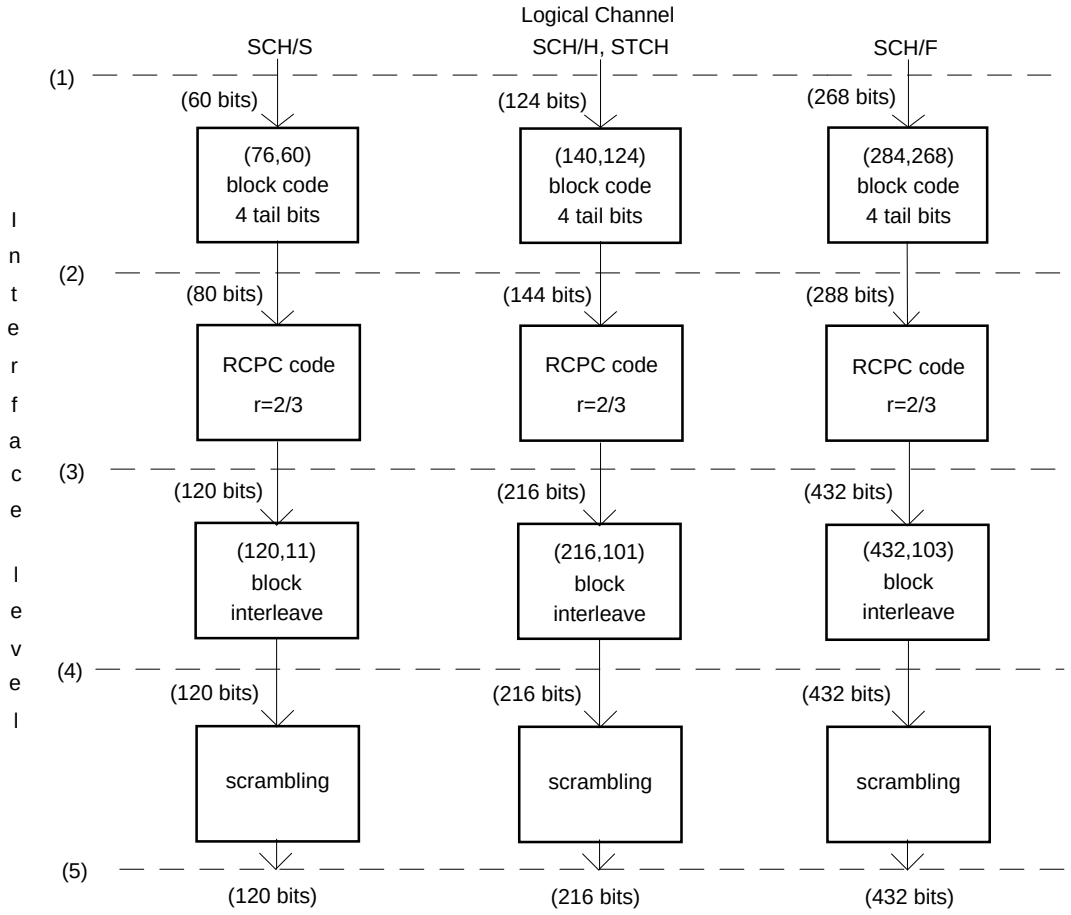

Figure 9: Error control structure for DM logical channels (Part 1)

8.3.1.2 Half-slot Signalling CHannel (SCH/H) and Stealing CHannel (STCH)

One type-1 block shall contain 124 type-1 bits, $b_1(1)$, $b_1(2)$,..., $b_1(124)$.

A (140,124) block code shall encode the 124 type-1 bits into 140 block-encoded bits $b_2(1)$, $b_2(2)$,...$b_2(140)$. This code shall be the (K_1+16, K_1) block code as defined in subclause 8.2.3.3, with $K_1 = 124$.

Four tail bits, $b_2(141)$, $b_2(142)$, $b_2(143)$, $b_2(144)$, all set equal to zero, shall be appended to the 140 block-encoded bits.

The resultant bits $b_2(1)$, $b_2(2)$,..., $b_2(144)$ shall be the type-2 bits.

A 16-state RCPC code with rate 2/3 (see subclause 8.2.3.1) shall encode the 144 type-2 bits into 216 type-3 bits, $b_3(1)$, $b_3(2)$,..., $b_3(216)$.

A (216,101) block interleaver (see subclause 8.2.4.1) shall re-order the 216 type-3 bits into 216 type-4 bits, $b_4(1)$, $b_4(2)$,..., $b_4(216)$.

The 216 type-4 bits $b_4(1)$, $b_4(2)$,..., $b_4(216)$ shall compose the type-4 block for SCH/H and STCH. They shall be scrambled into bits $b_5(1)$, $b_5(2)$, ..., $b_5(216)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The type-5 bits may be multiplexed onto block-1, in which case the multiplexed bits are defined as:

$bkn1(k) = b_5(k)$, for k = 1, 2,..., 216 (43)

or they may be multiplexed into block-2, in which case the multiplexed bits shall be defined as:

$bkn2(k) = b_5(k)$, for k = 1, 2,..., 216. (44)

8.3.1.3 Full-slot Signalling CHannel (SCH/F)

One type-1 block shall contain 268 type-1 bits, $b_1(1)$, $b_1(2)$,..., $b_1(268)$.

A (284,268) block code shall encode the 268 type-1 bits into 284 block-encoded bits $b_2(1)$, $b_2(2)$,...$b_2(284)$. This code shall be the (K_1+16, K_1) block code as defined in subclause 8.2.3.3, with K_1 = 268.

Four tail bits, $b_2(285)$, $b_2(286)$, $b_2(287)$, $b_2(288)$, all set equal to zero, shall be appended to the 284 block-encoded bits.

The resultant bits $b_2(1)$, $b_2(2)$,..., $b_2(288)$ shall be the type-2 bits.

A 16-state RCPC code with rate 2/3 (see subclause 8.2.3.1) encodes the 288 type-2 bits into 432 type-3 bits, $b_3(1)$, $b_3(2)$,..., $b_3(432)$.

A (432,103) block interleaver (see subclause 8.2.4.1) shall re-order the 432 type-3 bits into 432 type-4 bits, $b_4(1)$, $b_4(2)$,..., $b_4(432)$.

The 432 type-4 bits $b_4(1)$, $b_4(2)$,..., $b_4(432)$ shall compose the type-4 block for SCH/F. They shall be scrambled into bits $b_5(1)$, $b_5(2)$, ..., $b_5(432)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The multiplexed bits of block-1 are defined as:

$bkn1(k) = b_5(k)$, for k = 1, 2,..., 216 (45)

and the multiplexed bits of block 2 are defined as:

$bkn2(k) = b_5(k+216)$, for k = 1, 2,..., 216. (46)

8.3.2 Traffic channels in circuit switched mode

In case frame stealing is activated for one of the traffic channels defined below the multiplexed bits either of block-1 or of block-1 and block-2 are replaced by STCH bits. This means that the bits are replaced after coding and interleaving. The construction of STCH bits is defined in subclause 8.3.1.2.

8.3.2.1 Traffic channel, net rate = 7,2 kbit/s (TCH/7,2)

A sequence of M type-1 blocks, $B_1(m)$, m = 1, 2,...M, shall be transmitted, whereby M is not limited.

One type-1 block shall contain 432 type-1 bits, $b_1(1)$, $b_1(2)$,..., $b_1(432)$.

There shall be 432 type-4 bits, which are the same as the type-1 bits:

$b_4(k) = b_1(k)$, for k = 1, 2,..., 432. (47)

The 432 type-4 bit $b_4(1)$, $b_4(2)$,..., $b_4(432)$ shall compose the type-4 block for TCH/7,2. They shall be scrambled into bits $b_5(1)$, $b_5(2)$,..., $b_5(432)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The multiplexed bits of block-1 shall be defined as:

$bkn1(k) = b_5(k)$, for k = 1, 2,..., 216, (48)

and the multiplexed bits of block-2 shall be defined as:

$bkn2(k) = b_5(k+216)$, for k = 1, 2,..., 216. (49)

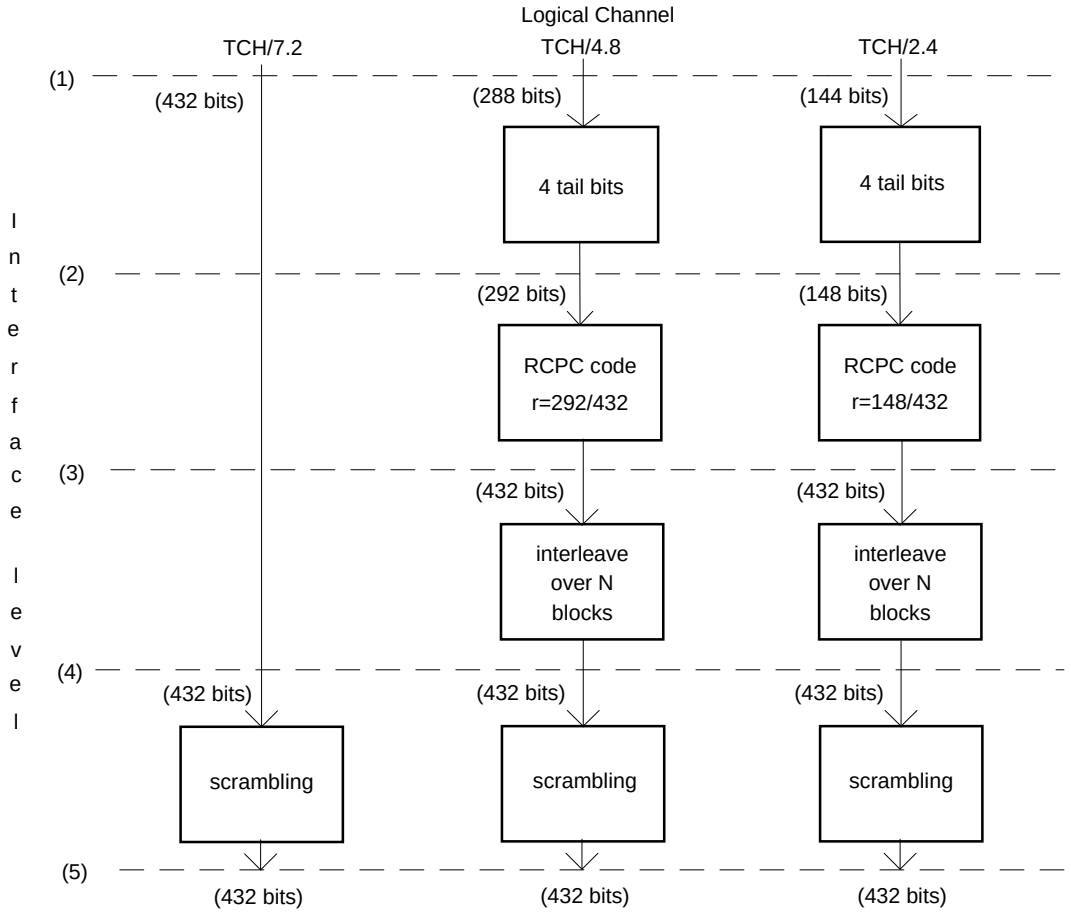

Figure 10: Error control structure for DM logical channels (Part 2)

8.3.2.2 Traffic channel, net rate = 4,8 kbit/s (TCH/4,8)

A sequence of M type-1 blocks, $B_1(m)$, m = 1, 2,...M, shall be transmitted, whereby M is not limited.

One type-1 block shall contain 288 type-1 bits, $b_1(1)$, $b_1(2)$,..., $b_1(288)$.

The K_2 = 292 type-2 bits shall comprise the 288 type-1 bits mapped as follows:

$b_2(j) = b_1(j)$, for j = 1, 2,..., 288. (50)

with the addition of four tail bits, $b_2(289)$, $b_2(290)$, $b_2(291)$, $b_2(292)$, all set equal to zero.

A 16-state RCPC code with rate 292/432 (see subclause 8.2.3.1) shall encode the 292 type-2 bits into 432 type-3 bits, $b_3(1)$, $b_3(2)$,..., $b_3(432)$.

An interleaving over N blocks (see subclause 8.2.4.2) shall interleave bits from M type-3 blocks (of 432 bits each) into (M+N-1) type-4 blocks (of 432 bits each): the bits in one type-4 block shall be denoted by $b_4(1)$, $b_4(2)$,..., $b_4(432)$. The parameter N shall be pre-set at the call set-up, and may take the values 1, 4, or 8.

The 432 type-4 bits $b_4(1)$, $b_4(2)$,..., $b_4(432)$ shall compose the type-4 block for TCH/4,8. They shall be scrambled into bits $b_5(1)$, $b_5(2)$,..., $b_5(432)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The multiplexed bits of block-1 are defined as:

$bkn1(k) = b_5(k)$, for k = 1, 2,..., 216, (51)

and the multiplexed bits of block-2 are defined as:

$bkn2(k) = b_5(k+216)$, for k = 1, 2,..., 216. (52)

8.3.2.3 Traffic channel, net rate = 2,4 kbit/s (TCH/2,4)

A sequence of M type-1 blocks, $B_1(m)$, m = 1, 2,...M, shall be transmitted, whereby M is not limited.

One type-1 block shall contain 144 type-1 bits, $b_1(1)$, $b_1(2)$,..., $b_1(144)$.

The K_2 = 148 type-2 bits shall comprise the 144 type-1 bits mapped as follows:

$b_2(j) = b_1(j)$, for j = 1, 2,..., 144, (53)

with the addition of four tail bits, $b_2(145)$, $b_2(146)$, $b_2(147)$, $b_2(148)$, all set equal to zero.

A 16-state RCPC code with rate 148/432 (see subclause 8.2.3.1) encodes the 148 type-2 bits into 432 type-3 bits, $b_3(1)$, $b_3(2)$,..., $b_3(432)$.

An interleaving over N blocks (see subclause 8.2.4.2) shall interleave bits from M type-3 blocks (of 432 bits each) into (M+N-1) type-4 blocks (of 432 bits each): the bits in one type-4 block shall be denoted by $b_4(1)$, $b_4(2)$,..., $b_4(432)$. The parameter N shall be pre-set at the call set-up, and may take the values 1, 4, or 8.

The 432 type-4 bits $b_4(1)$, $b_4(2)$,..., $b_4(432)$ shall compose the type-4 block for TCH/2,4. They shall be scrambled into bits $b_5(1)$, $b_5(2)$,..., $b_5(432)$, according to subclause 8.2.5.1, with the scrambling sequence as defined in subclause 8.2.5.2.

The multiplexed bits of block-1 are defined as:

$bkn1(k) = b_5(k)$, for k = 1, 2,..., 216, (54)

and the multiplexed bits of block-2 are defined as:

$bkn2(k) = b_5(k+216)$, for k = 1, 2,..., 216. (55)

9 Channel multiplexing for DM

9.1 Introduction

This clause defines the physical channels of the DM radio sub-system required to support the logical channels. It includes a description of the logical channels and the definitions of DM frames, timeslots and bursts.

9.2 Logical channels

A logical channel is defined as a logical communication pathway between two or more parties. The logical channels represent the interface between the protocol and the radio subsystem.

The definition of the logical channels that are supported by the radio subsystem is given below.

9.2.1 Logical channels hierarchy

The logical channels may be separated into two categories: the traffic channels carrying speech or user data and the control channels carrying signalling. The logical channels supported by the DLL are described here, with their hierarchical relationship.

9.2.2 Traffic channels

The traffic channels shall carry user information. Different traffic sub channels are defined for speech or data applications and for different data message speeds:

- speech traffic channel (TCH/S);

- data traffic channels;

    - 7,2 kbit/s net rate (TCH/7,2);
    - 4,8 kbit/s net rate (TCH/4,8);
    - 2,4 kbit/s net rate (TCH/2,4).

Three different depths of interleaving (with N = 1, 4, or 8) may be applied to the traffic channels TCH/4,8 and TCH/2,4 as detailed in subclause 8.2.4.2

9.2.3 Control channels

9.2.3.1 General

There are three categories of control channel defined for DM:

- linearization;

- signalling; and

- stealing channels.

9.2.3.2 DM Linearisation CHannel (LCH)

The LCH shall be used by the mobile stations to linearize their transmitters.

9.2.3.3 DM SCH

The SCH shall be shared by all mobile stations, but may carry messages specific to one or one group of mobile stations. There are three categories of SCH:

- Synchronisation Signalling CHannel (SCH/S) used for synchronisation messages;

- Half slot Signalling CHannel (SCH/H) used for half slot messages;

- Full slot Signalling CHannel (SCH/F) used for Short Data messages.

9.2.3.4 DM STCH

The STCH is a channel associated to a TCH that temporarily "steals" a part of the associated TCH capacity to transmit control messages. It may be used when fast signalling is required.

9.3 The physical resource

9.3.1 General

The physical resource available to the radio sub-system is an allocation of part of the radio spectrum. Each channel is partitioned in time into multiframes, frames and timeslots as shown in figure 10. This

resource shall be partitioned into radio frequency channels. All DM-MSs in a call shall transmit and receive on the same radio frequency selected by the user.

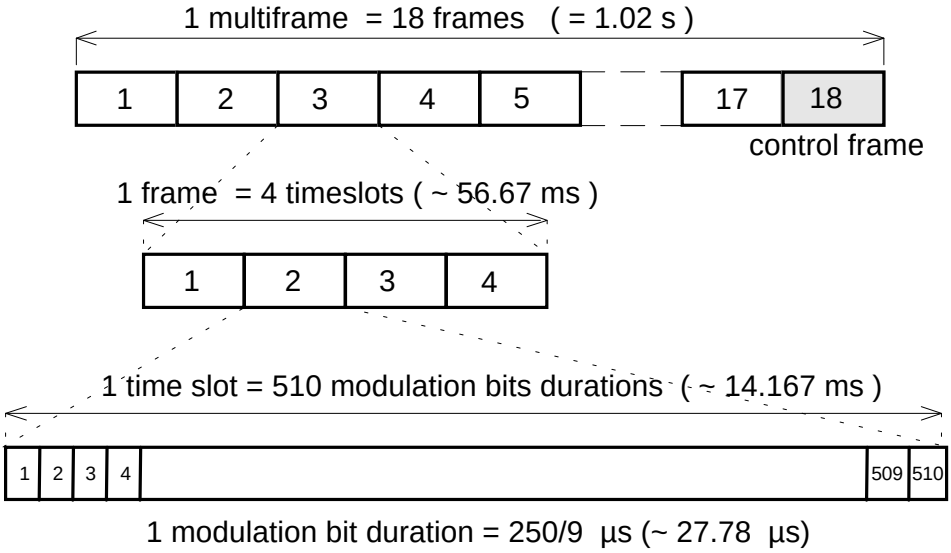

Figure 11: DM frame structure

9.3.2 Timeslots

A timeslot shall have a duration of 85/6 ms (approximately 14,17 ms) which corresponds to 510 modulation bits duration.

The timeslots within a DM frame shall be numbered by timeslot number (TN) 1 to 4.

9.3.3 DM frame

Four timeslots shall form a DM frame. The DM frame has a duration of 170/3 ms (approximately 56,67 ms).

The DM frames shall be numbered by a Frame Number (FN). FN shall be cyclically numbered from 1 to 18. FN shall be incremented at the end of each DM frame.

The frame FN18 shall be exclusively devoted to signalling channels.

9.3.4 Multiframe

Eighteen frames shall form a multiframe. The multiframe shall have a duration of 1,02 s.

The multiframes shall be numbered by a MN. The MN shall be incremented whenever FN returns to 1.

9.4 Physical channels

9.4.1 General

During a call, a DM physical channel is defined as one radio frequency channel and two timeslots per frame.

9.4.2 Bursts

9.4.2.1 General

A burst is a period of RF carrier that is modulated by a data stream. A burst therefore represents the physical content of a timeslot.

9.4.2.2 Modulation symbol numbering

A timeslot shall be divided into 255 modulation symbol durations, each one with a duration of 1/18 ms (approximately 55,56 µs). A particular modulation symbol within a burst shall be referenced by a Symbol Number (SN), with the first modulation symbol numbered SN1 and the last modulation symbol numbered SNmax.

Different types of bursts are defined, having different durations.

At the beginning of the transmission of a single burst or of consecutive bursts, a supplementary symbol SN0 is defined. It does not carry information but shall be used as phase reference for the differential modulation.

9.4.2.3 Modulation bit numbering

In the following subclauses the content of a burst is defined in terms of modulation bits.

A particular modulation bit within a burst shall be referenced by a Bit Number (BN), with the first modulation bit numbered BN1 and the last modulation bit numbered BNmax. At the modulator the modulation bits shall be grouped in pairs of consecutive odd and even numbered bits and each pair shall be converted into one modulation symbol as described in clause 5.

9.4.2.4 Burst timing

The timing of a modulation symbol is determined by its symbol time. The symbol time is defined as the instant at which the transmitted symbol waveform is at a maximum for the symbol of interest.

The bits BN(2n-1) and BN(2n) shall determine the symbol SN(n) and the symbol time of the modulation symbol SN(n) shall be delayed by (n+d) modulation symbol durations with respect to the start of the slot, with:

- n: integer (1 ... (SNmax));

- d: is defined as the burst delay. The burst delay represents the delay between the start of the timeslot and the symbol time of the symbol SN1. The burst delay shall be expressed in modulation symbol duration and varies with the type of burst. The values of the burst delays are given in table 14.

The symbol time of the symbol SN0 occurs one modulation symbol duration before the symbol time of the symbol SN1 of the first burst of a transmission.

9.4.3 Type of bursts

9.4.3.1 General

A DM-MS may transmit three types of bursts. The bursts shall conform to the specification in table 14. Figure 12 summarises the description of the bursts and their timing with respect to the timeslot.

Table 14: Burst types for DM

Burst type	SNmax	d burst delay (in symbol duration)	Bit allocation
DMO Linearisation burst	N/A	120	subclause 9.4.3.2.2
DMO Normal burst	235	17	subclause 9.4.3.2.1
DMO Synchronisation burst	235	17	subclause 9.4.3.2.3

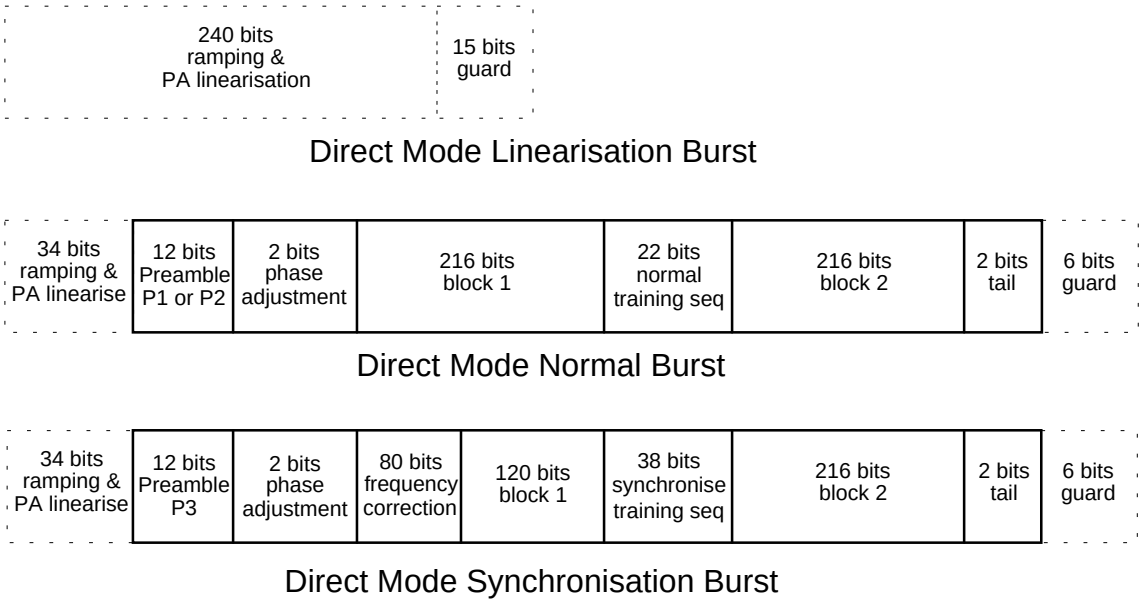

Figure 12: Types of DMO burst

9.4.3.2 Modulation bits allocation

The bursts are divided into burst fields containing contiguous modulation bits of the same type. The burst fields are described in subclause 9.4.3.3.

The DM normal and synchronisation bursts contains two independent blocks, called Block 1 (BKN1) and Block 2 (BKN2). A separate logical channel may be mapped on each block. Block 1 and block 2 shall be made of one field and shall contain 216 scrambled bits each in a DM normal burst and 120 and 216 scrambled bits respectively in a DM synchronisation burst.

9.4.3.2.1 DM Normal Burst (DNB)

The allocation of the modulation bits in the DNB shall be in accordance with table 15. The DNB shall be used by MSs once synchronisation has been achieved to transmit control or traffic messages to other MSs.

Table 15: DNB

Bit Number (BN)	Field length (bits)	Field content	Field bits number	Definition clause or subclause
1 to 12	12	preamble	j1 to j12 or k1 to k12	9.4.3.3.3
13 to 14	2	phase adjustment bits	hk1 to hk2	9.4.3.3.5
15 to 230	216	scrambled block 1 bits	bkn1(1) to bkn1(216)	clause 8
231 to 252	22	normal training sequence	n1 to n22 or p1 to p22	9.4.3.3.3
253 to 468	216	scrambled block 2 bits	bkn2(1) to bkn2(216)	clause 8
469 to 470	2	tail bits	t1 to t2	9.4.3.3.6

9.4.3.2.2 DM Linearisation Burst (DLB)

The DLB may be used by MSs to linearise their transmitters. The linearisation burst contains no useful bits and its timing shall only be determined by the time mask (see clause 6).

9.4.3.2.3 DM Synchronisation Burst (DSB)

The allocation of the modulation bits in the DSB shall be in accordance with table 16. DSB shall be for synchronisation of MSs participating in a DM communication.

Table 16: DSB

Bit Number (BN)	Field length (bits)	Field content	Field bits number	Definition clause or subclause
1 to 12	12	preamble	l1-l12	9.4.3.3.4
13 to 14	2	phase adjustment bits	hl1 to hl2	9.4.3.3.5
15 to 94	80	frequency correction	f1 to f80	9.4.3.3.1
95 to 214	120	scrambled synchronisation block 1 bits	sb(1) to sb(120)	clause 8
215 to 252	38	synchronisation training sequence	y1 to y38	9.4.3.3.4
253 to 468	216	scrambled block 2 bits	bkn2(1) to bkn2(216)	clause 8
469 to 470	2	tail bits	t1 to t2	9.4.3.3.6

9.4.3.3 Burst fields

9.4.3.3.1 Frequency correction field

The frequency correction field shall contain 80 bits:

(f1, f2, ..., f8) = (1, 1, ..., 1) (56)

(f9, f10, ..., f72) = (0, 0, ..., 0) (57)

(f73, f74, ..., f80) = (1, 1, ..., 1) (58)

When transmitted, this frequency correction field generates an un-modulated carrier at 2,25 kHz above the nominal carrier frequency, preceded and followed by a short period (4 symbol durations) of un-modulated carrier at 6,75 kHz below the nominal carrier frequency.

9.4.3.3.2 Inter-slot frequency correction field

The DM-MS inter-slot frequency correction bits are defined as:

(g1, g2, ..., g6) = (0, 0, ..., 0) (59)

(g7, g8, ..., g32) = (1, 1, ..., 1) (60)

(g33, g34, ..., g40) = (0, 0, ..., 0) (61)

When transmitted, this frequency correction field generates an un-modulated carrier at 6,75 kHz below the nominal carrier frequency, preceded and followed by short periods of un-modulated carrier at 2,25 kHz above the nominal carrier frequency.

9.4.3.3.3 Normal training sequence and preamble

Two 22 bit normal training sequences and two 12 bit preambles are defined.

The normal training sequences and preambles shall be used on the DNB. The type of training sequence and preamble shall be used as a flag indicating the presence of one or two logical channels on the blocks 1 and 2 of the burst, according to table 17:

Table 17: Preambles and Training sequences

Preamble	Normal training sequence	Logical channel
P1	T1	TCH, SCH/F
P2	T2	STCH + TCH, STCH + STCH, SCH/H + SCH/H

The preamble P1 shall be:

(j1,j2...,j12) = (0,0 , 1,1 , 0,0 , 1,0 , 0,0 , 1,1) (62)

The preamble P2 shall be:

(k1,k2...,k12) = (1,0 , 0,1 , 1,0 , 1,0 , 1,0 , 0,1) (63)

The normal training sequence T1 shall be:

(n1, n2,..., n22) = (1,1 , 0,1 , 0,0 , 0,0 , 1,1 , 1,0 , 1,0 , 0,1 , 1,1 , 0,1 , 0,0) (64)

The normal training sequence T2 shall be:

(p1, p2,..., p22) = (0,1 , 1,1 , 1,0 , 1,0 , 0,1 , 0,0 , 0,0 , 1,1 , 0,1 , 1,1 , 1,0) (65)

9.4.3.3.4 Synchronisation training sequence

The synchronisation training sequence and 12 bit preamble shall be used on the DSB.

The synchronisation preamble P3 shall be:

(l1, l2...,l12) = (0,0 , 0,1 , 0,1 , 0,0 , 0,1 , 1,1) (66)

The synchronisation training sequence shall be a 38 bit synchronisation word used for the synchronisation burst.

The synchronisation training sequence shall be:

(y1, y2,..., y38) = (1,1 , 0,0 , 0,0 , 0,1 , 1,0 , 0,1 , 1,1 , 0,0 , 1,1 , 1,0 ,
1,0 , 0,1 , 1,1 , 0,0 , 0,0 , 0,1 ,1,0 , 0,1 , 1,1) (67)

9.4.3.3.5 Phase adjustment bits

The phase adjustment bits shall be used on both the normal and synchronisation bursts to provide a known phase relationship between the different preamble sequences and different training sequences of the burst, whatever the content of the blocks is.

The value of the pair of phase adjustment bits shall be set so that the phase shift $D\phi$ they generate (see clause 5) is equal to:

$$D\phi = -\sum_{n=n1}^{n2} D\phi(n) \quad (68)$$

where:

$D\phi(n)$ is the phase transition generated by the bits (BN(2n-1), BN(2n)), n1 and n2 are given by table 18 with respect to the bit numbering of subclause 9.4.4.2.

Table 18: Phase adjustment bits

phase adjustment bits	n1	n2
(hk1, hk2)	8	126
(hl1, hl2)	8	126

9.4.3.3.6 Tail bits

The tail bit field shall contain 2 bits.

The contents of the tail bit field shall be:

(t1,t2) = (0,0) (69)

9.4.4 DM-MS multiple slot transmission

The DM-MS transmitting on more than 1 slot need not ramp down and up between adjacent DM synch bursts. In the case where the DM-MS does not perform the ramping, the burst shall be followed by 6 bits (corresponding to the guard period) defined in table 19 and the subsequent burst shall be preceded by 34 bits (corresponding to the ramp up and linearization period), according to table 20.

Table 19: Bits following the present burst

Bit number	Field length (bits)	Field content	Field bits number	Definition
1 to 6	6	inter-slot frequency correction bits	g1 to g6	9.4.3.3.2

Table 20: Bits preceding the subsequent burst

Bit number	Field length (bits)	Field content	Field bits number	Definition
1 to 26	26	inter-slot frequency correction bits	g7 to g32	9.4.3.3.2
27 to 34	8	inter-slot frequency correction bits	g33 to g40	9.4.3.3.2

9.4.5 General mapping of logical channels

Table 21 defines the mapping of logical channels into physical channel types.

Table 21: Mapping of logical channel into physical channels

Logical channel	Burst type	Block	FN	TN
LCH	DLB	-	3	3
SCH/F	DNB	BKN1+BKN2	1...17	1
SCH/S	DSB	BKN1	1...18	1...4
SCH/H	DSB	BKN2	1...18	1...4
SCH/H	DNB	BKN1, BKN2	1...17	1
TCH	DNB	BKN1+BKN2, BKN2	1...17	1
STCH	DNB	BKN1, BKN2	1...17	1

Table 22 defines the mapping of logical channels into slots and frames.

Table 22 DM Frame mapping

Frame#	Slot Number / Block Number							
	1		2		3		4	
Block#	BKN1	BKN2	BKN1	BKN2	BKN1	BKN2	BKN1	BKN2
3	TCH		------	------	LCH	------	------	------
	SCH/F		------	------	LCH	------	------	------
	STCH	TCH	------	------	LCH	------	------	------
	STCH	STCH	------	------	LCH	------	------	------
	SCH/H	SCH/H	------	------	LCH	------	------	------
	SCH/S	SCH/H	***	***	SCH/S[1]	SCH/H[1]	***	***
1,4, 7,9,10, 13,15, 16	TCH		------	------	------	------	------	------
	SCH/F		------	------	------	------	------	------
	STCH	TCH	------	------	------	------	------	------
	STCH	STCH	------	------	------	------	------	------
	SCH/H	SCH/H	------	------	------	------	------	------
	SCH/S	SCH/H	***	***	SCH/S[1]	SCH/H[1]	***	***
2,5,8, 11,14, 17	TCH		------	------	SCH/S[2]	SCH/H[2]	------	------
	SCH/F		------	------	SCH/S[2]	SCH/H[2]	------	------
	STCH	TCH	------	------	SCH/S[2]	SCH/H[2]	------	------
	STCH	STCH	------	------	SCH/S[2]	SCH/H[2]	------	------
	SCH/H	SCH/H	------	------	SCH/S[2]	SCH/H[2]	------	------
	SCH/S	SCH/H	***	***	SCH/S[1]	SCH/H[1]	***	***
6,12	TCH		------	------	SCH/S[4]	SCH/H[4]	------	------
	SCH/F		------	------	SCH/S[4]	SCH/H[4]	------	------
	STCH	TCH	------	------	SCH/S[4]	SCH/H[4]	------	------
	STCH	STCH	------	------	SCH/S[4]	SCH/H[4]	------	------
	SCH/H	SCH/H	------	------	SCH/S[4]	SCH/H[4]	------	------
	SCH/S	SCH/H	------	------	SCH/S[3]	SCH/H[3]	------	------
	SCH/S	SCH/H	***	***	SCH/S[1]	SCH/H[1]	***	***
18	SCH/S	SCH/H	------	------	SCH/S[3]	SCH/H[3]	------	------
	SCH/S	SCH/H	------	------	SCH/S[4]	SCH/H[4]	------	------
	SCH/S	SCH/H	***	***	SCH/S[1]	SCH/H[1]	***	***

NOTE 1: Mapping of SCH/S+SCH/H used during call set-up signalling.
NOTE 2 Mapping of SCH/S+SCH/H used for pre-emption signalling.
NOTE 3 Mapping of SCH/S+SCH/H used for signalling during channel reservation period and in frame 18.
NOTE 4 Mapping of SCH/S+SCH/H used during channel occupation
------ indicates that nothing is transmitted during this period
*** indicates option of including additional SCH/S+SCH/H in the case of new call set-up signalling only

10 Radio subsystem link control

10.1 Introduction

This clause specifies the radio subsystem link control implementation for TETRA DM. The following aspects of radio subsystem link control are addressed:

- RF power control;

- the basis for signal strength measurement.

10.2 RF power control

Adaptive RF power control is not required for direct DM-MS - DM-MS operation.

Adaptive RF power control may be required in Repeater and Gateway operation.

10.3 Radio link measurements

The radio link measurements include signal strength and signal quality.

10.3.1 Signal strength

The RMS received signal level shall be measured over the full range from reference sensitivity to - 48 dBm, with an absolute accuracy of ± 4 dB from reference sensitivity to - 70 dBm under normal conditions and ± 6 dB over the full range under both normal and extreme conditions.

The relative accuracy between two measurements on the same carrier or on different carriers shall be ± 3 dB.

The parameters relative to signal strength shall be coded as in table 23.

Table 23: Signal strength parameter definition

Parameter value	Signal strength measured at the antenna connector (dBm)	
	from	to
0		- 110
1	- 110	- 109
2	- 109	- 108
...	...	...
62	- 49	- 48
63	- 48	

10.3.1.1 Sample duration for signal strength measurement

In order to enable correct measurement of the received signal strength, the Sample Duration (SD) shall be one of the following defined values:

- SD1 = 1 ms sample duration or;

- SD2 = 4 ms sample duration.

10.3.2 Signal quality

The quality of the radio link shall be estimated from the success rate of decoding the SCH/S (see ETS 300 396-3 [2]).

History

Document history			
July 1996	Public Enquiry	PE 109:	1996-07-08 to 1996-11-01