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**Satellite Earth Stations and Systems (SES);
Modulation and channel coding of
34,368 Mbit/s and 44,736 Mbit/s
digital television contribution links via satellite**

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Foreword

This ETSI Technical Report (ETR) has been prepared by the Satellite Earth Stations and Systems (SES) Technical Committee of the European Telecommunications Standards Institute (ETSI).

ETRs are informative documents resulting from ETSI studies which are not appropriate for European Telecommunication Standard (ETS) or Interim European Telecommunication Standard (I-ETS) status.

An ETR may be used to publish material which is either of an informative nature, relating to the use or application of ETSs or I-ETSs, or which is immature and not yet suitable for formal adoption as an ETS or I-ETS.

Introduction

In June 1993 ETSI TC SES approved a work programme to produce an ETS on digital TV contribution links via satellite. Contribution links are meant high quality transmissions to studios which allow post processing to be performed.

In the discussion on candidate bit rates it was decided to limit the scope of the document to the modulation and channel coding necessary for transmitting a 34/45 Mbit/s bit stream which is produced in conformance with ETS 300 174 [1], on the digital coding of component television signals for contribution quality applications.

A multitude of modulation and channel coding schemes are possible for transmission via satellite e.g. Quadrature Phase Shift Keying (QPSK) or 8 phase Phase Shift Keying (PSK), rate 1/2, rate 3/4 Forward Error Correction (FEC) with VITERBI or sequential detection. However, it was decided to use the modulation and channel coding scheme as given in the INTELSAT Intermediate Data Rate (IDR) specification.

A draft ETS was presented to TC SES in February 1994 where divergent views were expressed about the real need for such an ETS. On the one hand it was stated that the INTELSAT Intermediate Data Rate (IDR) document IESS 308 [2] was virtually a de-facto standard in this area, rendering it unnecessary to have an ETSI standard. On the other hand it was stated that the IDR standard covered many bit rates, was primarily oriented towards telephony and contained many elements such as transmission parameters, which are specific to INTELSAT satellites, thus rendering the document unsuitable to function as the "carriage" for satellite transmissions using the ETSI codec, ETS 300 174.

As a compromise between the opposing views on the need for such an ETS, TC SES decided in June 1994 to make the draft ETS into an annex to this ETR. The advantage of this approach is that the results of the work performed are available for reference to assist those who would like to use the ETSI codec, ETS 300 174 for transmissions via satellite.

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1 Scope

This ETR describes modulation and channel coding equipment used for transmitting via satellite digital signals with the characteristics specified in ETS 300 174 [1]. The purpose of the ETR is to enable harmonization of equipment.

2 References

For the purposes of this ETR the following references apply:

- [1] ETS 300 174: "Network Aspects (NA); Digital coding of component television signals for contribution quality applications in the range 34 to 45 Mbit/s".
- [2] IESS 308: "Performance characteristics for Intermediate Data Rate (IDR) digital carriers (Standard A, B, C, E and F earth stations)".

3 Overview

Annex A gives the draft ETS on digital TV contribution links via satellite using modems operating at 34/45 Mbit/s, which was produced by STC SES 4 in February 1994. The two bit rates given correspond to those of ETS 300 174 [1], on the digital coding of component television signals for contribution quality applications. The bit rate of 34 Mbit/s is relevant to Europe.

Annex A is an extract of the IDR specification, document IESS 308 Rev. 6 [2] and gives those elements relevant to the bit rates of 34,368 Mbit/s and 44,736 Mbit/s. It gives the modulation, channel coding, framing and alarm scheme as well as the method of energy dispersal and a recommendation on buffering. The document is sufficiently detailed to allow equipment purchased from different manufacturers to interwork without special adjustment.

Coherent QPSK modulation is employed together with rate 3/4 convolutional encoding with soft decision VITERBI (maximum likelihood) decoding. The rate 3/4 code is a "punctured" type of convolutional code and is constructed from a rate 1/2 encoder by periodically deleting specific bits from the rate 1/2 output bit sequence. In the IDR document [2] either rate 3/4 or rate 1/2 FEC is used, depending on the satellite being used. In annex A only the rate 3/4 FEC has been retained.

Energy dispersal is performed to ensure that uniform spectral spreading of the transmitted carrier is achieved at all times by using a self-synchronizing scrambler.

Overhead framing is defined by synchronously adding 96 kbit/s of overhead to the transmitted data stream. This enables the transmission of alarms and Engineering Service Circuits (ESC).

In the IDR document [2] the elements on the buffering and clock concept are oriented towards an interconnection with the terrestrial network at either 2 Mbit/s or 1.5 Mbit/s, which is not relevant to annex A. Consequently subclauses 5.8 and 5.10 of annex A are specifically for interconnection with a terrestrial network. The annex has been derived from IESS 308 Rev. 6 [2]. Subsequently IESS 308 has been further revised and certain IDR specifications have been amended.

In TC SES there were different views expressed about the needs for buffer capacity. One view was that no buffering is required for this type of transmission. However, in subclause 5.10 a buffer capacity of 32 ms has been specified, which is an optional feature. A buffer of this capacity costs very little compared to the overall costs of the modem.

It was decided to incorporate the external Reed-Solomon codec as an optional feature, even though this external coding is not necessary with ETS 300 174, which has this feature incorporated internally. The reasoning behind this was that certain users may like to employ this modem for other applications, where very low bit error ratios are necessary.

Annex A (informative): Draft ETS for the modulation and channel coding of 34,368 Mbit/s and 44,736 Mbit/s digital television contribution links via satellite

1 Scope

This annex constitutes a draft common standard for the modulation and channel coding for the transmission via satellite of digital coded component television signals for contribution quality applications with the characteristics specified in ETS 300 174 [1]. The draft standard embraces the modulation, demodulation, channel coding algorithm, channel decoding algorithm and the interface with the terrestrial part of the transmission network. The purpose of the draft standard is to enable harmonization of equipment.

2 Normative references

This ETS incorporates by dated and undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

- [1] ETS 300 174: "Digital coding of component television signals for contribution quality applications in the range 34 - 45 Mbit/s".
- [2] ITU-R Recommendation 601: "Encoding parameters for digital television for studios".
- [3] ITU-T Recommendation G.803: "Maintenance of digital networks".
- [4] ITU-T G.752 Recommendation (1988): "Characteristics of digital multiplex equipments based on a second order bit rate of 6312 kbit/s and using positive justification".
- [5] ITU-T G.823 Recommendation (1988): "The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy".
- [6] ITU-T G.824 Recommendation (1988): "The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy".
- [7] ITU-T G.703 Recommendation (1988): "Physical/electrical characteristics of hierarchical digital Interfaces".

3 Abbreviations

For the purposes of this ETS, the following abbreviations apply:

AIS	Alarm Indication Signal
BER	Bit Error Rate
ESC	Engineering Service Circuits
ETS	European Telecommunication Standard
FEC	Forward Error Correction
GF	Galois Field
IF	Intermediate Frequency
ITU-T	International Telecommunications Union - Telecommunications
NRZ	Non-Return to Zero
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RS	Reed-Solomon
UW	Unique Word

4 General

ETS 300 174 [1] constitutes a common standard for the coding of component television signals for contribution quality applications in the range 34 - 45 Mbit/s in the format specified in ITU-R Recommendation 601 [2]. A Reed-Solomon (RS) code (255, 239) is specified within ETS 300 174 for the protection of the video component. This annex specifies the modulation, channel coding, demodulation and channel decoding algorithms, which shall be employed when transmitting via satellite with the bit rate of either 34,368 Mbit/s (the third level of the European digital hierarchy) or 44,736 Mbit/s (the third level of the international interworking hierarchy). It is not necessary for the channel unit to operate at both bit rates.

Figure 1 illustrates the transmit and receive side channel unit. The 34,368 Mbit/s or 44,736 Mbit/s bit stream at the output of the TV codec, ETS 300 174 [1], is delivered at the input to the transmit channel unit where firstly an overhead of 96 kbit/s is added. The overhead adds its own frame alignment signal and thus passes the information data stream transparently. Then the bit stream is scrambled to provide energy dispersal. Forward Error Correction (FEC) is employed before coherent Quadrature Phase Shift Keying (QPSK) modulation is applied ¹⁾. The frequency at the output of the transmit channel unit is referred to as the Intermediate Frequency (IF). The signal is then upconverted to the Radio Frequency (RF), and amplified for transmission to the satellite.

The receive-side channel unit receives the IF signal from the output of the down-converter. In accordance with figure 1 the signal is demodulated, decoded in the FEC decoder, de-scrambled and, after removal of the overhead, a bit stream of 34,368 Mbit/s or 44,736 Mbit/s is delivered at the output.

5 Channel unit characteristics (requirements)

The channel unit consists of the following:

- 1) modulator/demodulator;
- 2) FEC encoder/decoder;
- 3) scrambler/descrambler;
- 4) overhead framing unit;
- 5) optional Reed-Solomon outer encoder/decoder.

The channel unit shall utilize coherent QPSK modulation along with rate 3/4 FEC. The FEC shall be convolutional encoding with Viterbi decoding. The nominal data rate at the input to the FEC encoder shall be either 34,464 Mbit/s or 44,736 Mbit/s.

An overhead framing structure has also been defined to facilitate the provision of Engineering Service Circuits (ESC) and maintenance alarms. The overhead data rate is 96 kbit/s.

5.1 Modulator

For reference purposes, it is assumed that the modulator accepts two parallel data streams from the FEC encoder, designated the P channel and the Q channel.

¹⁾ The transmission rate (R) is defined as the bit rate entering the QPSK modulator at the earth station (i.e. after the addition of any overhead or FEC coding) and is equal to twice the symbol rate at the output of the QPSK modulator. Figure 1 is a block diagram of the channel unit and illustrates the definitions of information rate, transmission rate and symbol rate.

5.1.1 Output characteristics

The relationship between the bits to be transmitted and the carrier phase of the modulator output is given in table 1 below:

Table 1

Transmitted Bits		Resultant Phase	
P Channel	Q Channel		
1	1	0°	
0	1	+ 90°	
0	0	+ 180°	
1	0	+ 270°	(-90°)

The phase accuracy at the modulator output shall be $\pm 2^\circ$. The amplitude accuracy at the modulator output shall be ± 0.2 dB.

The above specification has been written in terms of absolute phase encoding rather than differential encoding because carrier phase ambiguities are resolved by means of the FEC coding, as discussed in subclause 5.3.

5.1.2 Modulator spectrum output

The transmitted IF spectrum within the frequency range $\pm 0,35 R$ Hz from the nominal centre frequency shall be equivalent to a spectrum present at the output of a filter following an ideal modulator, under the following conditions:

- a) The input to the QPSK ideal modulator is a R bit/s non-return-to-zero (NRZ) random sequence (with equal probability of 0 or 1);
- b) The filter has amplitude characteristics given in figure 2(a);
- c) The filter has group delay characteristics given in figure 3 or a phase response with less than ± 4 degrees departure from a linear phase shift over the frequency range $\pm 0,25 R$ about the nominal centre frequency.

Within the bandwidth 0,35 R to 0,75 R Hz away from the nominal centre frequency the envelope of the transmitted IF spectrum shall not exceed that obtained at the output of a filter following an ideal modulator, under the conditions given in a), b), and c) above. Outside the bandwidth $\pm 0,75 R$ Hz from the nominal centre frequency the transmitted IF spectral density shall be at least 40 dB below the peak spectral density, measured in a 4 kHz bandwidth.

Over the frequency range $\pm 0,35 R$ Hz from the nominal centre frequency b) and c) above are met by a filter consisting of the cascade of a group delay equalized six-pole Butterworth filter ($BT_S = 1.0$) and sinc^{-1} compensation (the overall BT_S of cascaded elements is equal to 1,5),

where:

$$\text{sinc}^{-1} = pDfT_S / \sin(pDfT_S);$$

- and: B = 3 dB double sided bandwidth of filte;
- T_S = Symbol period = 2/R baud;
- Df = Displacement from centre frequency;
- R = Transmission rate in bits per second.

It should be noted that the transmitted IF spectrum requirement is mandatory, not the modulator filter response.

A mask of the power spectral density which will result from a modulator meeting the amplitude characteristics outlined above, is shown in figure 4.

5.2 Demodulator

A coherent QPSK demodulator shall be used. Bit timing shall be recovered and presented to the FEC decoder. The demodulator shall provide an output which is compatible with the soft decision decoder (see subclause 5.3).

5.2.1 Operating conditions

The channel unit shall meet the performance requirements of subclause 5.5 in the presence of adjacent channel interferers and when both the desired carrier and interfering carriers are subject to a common carrier frequency drift of ± 25 kHz. For the purpose of demonstrating compliance with this requirement, the adjacent channel interferers may be assumed to operate at the same transmission rate as the desired carrier, at nominal centre frequencies of $\pm 0,7 R$ Hz about the desired carrier, and at a level + 7 dB higher than the desired carrier.

If the Automatic Frequency Control function is performed in the down converter, then the down converter is considered to be part of the channel unit for the purpose of meeting this performance requirement.

5.2.2 Demodulator filter characteristics

For the development of Bit Error Rate (BER) requirements the amplitude characteristics for the demodulator receive filter have been assumed as given in figure 2b). The group delay characteristics have been assumed as given in figure 3.

The demodulator receive filter characteristics are nominally equivalent to a group delay equalized six-pole Butterworth filter ($BT_s = 1,0$).

5.3 Forward error correction

Rate 3/4 convolutional encoding with Viterbi decoding shall be employed. The function of the data codecs is threefold:

- a) to generate appropriate coding bits and to interface with the modulator;
- b) to accept the demodulated signal and to recover correct code synchronization and correct carrier phase;
- c) in conjunction with the demodulator to make use of the code for reliable decisions about the transmitted sequence of data bits.

There is a need to use three encoders and decoders in parallel. The method for paralleling encoders and decoders is presented in figure 5. To avoid an increase in the number of ambiguities the serial to parallel (S/P) conversions are performed separately on the P and Q Channels, on the satellite side of the encoders and decoders. The serial to parallel (S/P) converters of the encoders and decoders do not need to be synchronized. The signal format at the output of the encoders is shown in figure 6.

5.3.1 Coder

The rate 3/4 convolutional encoder as shown in the functional diagram of figure 7 shall be employed. This is a "punctured" type of convolutional code and is constructed from a rate 1/2 encoder by periodically deleting specific bits from the rate 1/2 output bit sequence. The code has a memory of six which together with the incoming data bit forms a constraint length of seven.

The encoder consists of a binary differential encoder followed by a seven-stage shift register with the outputs of selected stages being added modulo-2 to form the rate 1/2 encoded data. The code generator polynomials of the rate 1/2 code are 133 and 171 in octal notation. Since the code is transparent to 180° carrier phase ambiguities, the incoming data stream is differentially encoded before encoding by the rate 1/2 convolutional encoder.

The rate 3/4 code is constructed by periodically deleting two specified bits from among six bits contained in three consecutive blocks of the original rate 1/2 code. The bit deletion is performed in the following manner:

- a) in the first block, both coded bits are transmitted;
- b) in the second block, the bit generated by generator polynomial 133 is transmitted and the bit generated by generator polynomial 171 is deleted;
- c) in the third block, the bit generated by generator polynomial 133 is deleted, and the bit generated by generator polynomial 171 is transmitted.

Three encoders shall be used in parallel as shown in figure 5.

5.3.2 Decoder

The decoding is performed by first re-constructing the Rate 1/2 coded data by inserting "erasure" bits into the received data stream at the positions in which the original Rate 1/2 coded bits were deleted on the transmitting side. The re-constructed Rate 1/2 coded data is then decoded by a soft-decision Viterbi (maximum likelihood) decoder.

The decoder shall have the following characteristics:

- the coding gain shall be compatible with the required E_b/N_0 . For this type of decoder 3 bit (8 level) quantization may be required as an input, and hence the demodulator would provide such an interface;
- internal resolution for 90° carrier phase ambiguity and code synchronization shall be provided;
- binary differential decoding of the serial output data stream shall be provided;
- it is recommended that an indication of the rate of error correction be provided for monitoring the performance of the carrier;
- the decoder shall be able to operate with the signal format shown in figure 6. This implies that it will be necessary to operate the decoders in parallel as shown in figure 5.

5.3.3 Reed-Solomon outer coding (optional)

The channel unit may include the optional RS outer coding specified in clause 6. In this case it shall be possible to disable the use of the RS coder/decoder by switching the RS coder/decoder out of the channel unit.

5.4 Energy dispersal (scrambling)

Scrambling shall be provided to ensure that uniform spectral spreading is applied to the transmitted carrier at all times.

The scrambler ²⁾ shall have a logic diagram equivalent to that shown in figure 8, and the descrambler shall have the impulse response shown in figure 9. It should be noted that this is a self-synchronizing scrambler and that a single error in the received data stream can produce 3 errors over an interval of 20 bits. For this reason the FEC encoder shall follow the scrambler at the transmit channel unit. At the receive channel unit, the descrambler shall follow the decoder.

²⁾ In the case of use of the optional RS outer coding a different scrambler is used, see subclause 6.4.

5.5 BER performance characteristics

The channel unit shall meet the performance requirements given in this subclause in an IF back-to-back mode. These values apply with the scrambler enabled and with FEC coding, and under the conditions outlined in subclause 5.2.1.

Table 2

BER better than:	Composite Data Rate E_b/N_0 (dB)
10^{-3}	5.3
10^{-4}	6.2
10^{-6}	7.6
10^{-7}	8.3
10^{-8}	8.8
10^{-10}	10.3

The E_b/N_0 is referred to the modulated carrier power and to the composite data rate (information rate plus overhead) entering the FEC coder.

5.6 Overhead framing for ESC and alarms

An overhead framing structure has been defined to facilitate the provision of ESC and maintenance alarms. The information data stream is passed transparently by the overhead unit; as such, no knowledge of the framing imbedded within the information stream is assumed or required.

The overhead framing structure described in subclause 5.6.1 shall be employed.

5.6.1 Overhead frame structure

The frame structure is derived by synchronously adding 96 kbit/s of overhead to the transmitted data stream.

In order to preserve the proper clock accuracy over the satellite channel, the timing of the transmitted composite stream (information plus overhead) shall be derived from the incoming information data stream. In the event of a failure of the clock from the incoming information stream a back-up clock with a long-term stability of at least 1 part in 10^5 per month shall be used to generate the timing needed to keep the overhead unit operational. The overhead unit shall be designed such that it will continue to operate in the absence of either (or both) the incoming transmit data or clock.

On the receive side the overhead unit shall derive its timing from a clock recovered from the received data.

The frame structure is derived by adding 12 bits every 125 microseconds resulting in a 96 kbit/s overhead rate. The overhead bits are allocated as follows:

- a) 4 bits for frame and multiframe alignment, backward alarm, and digital ESC data for a total rate of 32 kbit/s; the rates applicable to each are:
 - 20 kbit/s for frame and multiframe alignment;
 - 4 kbit/s for backward alarm to up to four destinations (1 kbit/s to each destination);
 - 8 kbit/s for digital ESC data;
- b) 8 bits for two 32 kbit/s ESC voice channels for a total rate of 64 kbit/s.

An 8-frame multiframe is defined, in order to increase the uniqueness of the alignment signal, and to allocate the backward alarm to four destinations.

The details of the overhead structure shall be as shown in figure 10.

The overhead unit, on the transmit side, shall take as input the incoming information stream, add the framing, alarm, and ESC bits as described above, and pass the composite stream to the scrambler. No knowledge of the framing imbedded within the information stream is assumed or required. On the receive side, the reverse process shall occur. The unit shall have the capability to provide, as ESC input/output, two 32 kbit/s channels for digitized voice or voiceband data, and one 8 kbit/s data channel. The 8 kbit/s data channel bits shall be set to one when not in use. Separate receive and transmit clocks shall be available for use by the ESC equipment at the 32, 8 and 1 kHz rates. The 1 kHz clock shall be synchronized to the multiframe rate. The other outputs shall be synchronized to this 1 kHz clock. The unit shall also detect the fault conditions and take the consequent actions described in subclause 5.6.2 for maintenance purposes. It shall also have the capability to provide four separate backward alarm input/outputs.

5.6.1.1 Frame and multiframe alignment

Frame and multiframe alignment shall be carried out simultaneously using the alignment signal, comprising the eight bit code inserted in the first bit of every frame and the three bit code inserted in the second, third, and fourth bits of every other frame, as depicted in figure 10.

Frame and multiframe alignment shall be assumed to be lost when four consecutive alignment signals have each been received with one or more errors.

Frame and multiframe alignment shall be assumed to have been recovered when, for the first time, the presence of the correct alignment signal is detected.

In the event of loss of alignment, a continuous alignment signal search shall be initiated. On correct receipt of an alignment signal the recovery sequence given in the previous subclause shall be initiated.

5.6.2 Maintenance alarm concept for the channel unit

The basis for this maintenance alarm concept is ITU-T Recommendation G.803 [3]. The maintenance entity is defined as the digital equipment between interfaces A and D (for the transmit channel unit) and interfaces E and H (for the receive channel unit) of figure 1 and as illustrated in figure 11.

The fact that the signal is subject to FEC and scrambling is not to be considered with respect to the maintenance alarm concept, i.e. AIS (Alarm Indication Signal) applied across interface D as an all ones condition is still scrambled and encoded prior to transmission to the satellite.

5.6.2.1 Fault conditions and consequent actions

Table 4 shows the actions to be taken after detection of specific fault conditions for each carrier. It is anticipated that these functions will be performed by the overhead framing unit. The faults shown in table 4 are defined as follows:

From the terrestrial side across interface A

FA1 loss of incoming signal (data or clock).

From the satellite across interface E

FE1 loss of incoming signal.

FE2 loss of overhead frame and multiframe alignment.

FE3 BER of 1 in 10^3 exceeded. Measured on the overhead alignment signal over any 1 minute period.

The actions shown in table 4 are defined as follows:

Channel unit alarm output

AS1 prompt maintenance alarm generated, as defined in ITU-T Recommendation G.803 [3].

To the terrestrial link (across interface H)

AH1 AIS applied across interface H on the information stream to indicate that a fault has been detected, and to be used as a service alarm by the terrestrial link.

To the satellite (across interface D)

AD1 AIS applied across interface D to indicate that a fault has been detected and to be used as a service alarm at the distant end. The AIS is sent in the information bit stream (not including the overhead bits).

5.6.2.2 Definition of AIS

AIS is transmitted as an "all ones condition" for the 34,368 Mbit/s information rate. For the 44,736 Mbit/s information rate, the equivalent binary content of AIS is a signal with a valid frame alignment signal, parity and justification control bits as defined in table 2 of ITU-T Recommendation G.752 [4], with the tributary bits being set to a 1010... sequence, starting with a binary 1 after each frame alignment, multiframe alignment and justification control bit and with all justification control bits being set to a binary 0.

5.7 Timing jitter

The transmit channel unit shall be able to accept input timing jitter up to the limits specified in ITU-T Recommendations G.823 [5] and G.824 [6] appropriate for the information rate input to the channel unit. This jitter is in addition to any jitter generated by the channel unit itself.

Under these conditions, the channel unit shall still meet the BER performance requirements given in subclause 5.5.

5.8 Terrestrial link interfaces

The transmit and receive channel unit interfaces with the terrestrial link are interfaces A and H illustrated in figure 1.

5.8.1 Physical/electrical characteristics

The transmit channel unit shall accept from the terrestrial side across interface A a signal with a nominal bit rate of 34 368 kbit/s or 44 736 kbit/s with the physical/electrical characteristics defined in ITU-T Recommendation G.703 [7].

The receive channel unit shall provide to the terrestrial network across interface H a signal with a nominal bit rate of 34 368 kbit/s/44 736 kbit/s with the physical/electrical characteristics defined in ITU-T Recommendation G.703 [7].

5.8.2 Timing interfaces

The timing interface from the terrestrial side across interface A shall be a codirectional interface. The definition of codirectional interface is given in subclause 1.1.4.1 of ITU-T Recommendation G.703 [7].

The timing interface to the terrestrial side across interface H shall be selectable between a codirectional interface, an external clock interface, and for transmit/receive channel units a contradirectional interface. The definition of centralized clock interface is given in subclause 1.1.4.2 of ITU-T Recommendation G.703 [7] and the definition of contradirectional interface is given in subclause 1.1.4.3 of ITU-T Recommendation G.703 [7].

5.9 IF frequency

The nominal centre of the IF signal frequency across interface D and across interface E shall be either 70 MHz or 140 MHz. The centre IF signal frequency may be adjustable, in which case the frequency step shall be 125 kHz or a submultiple of 125 kHz.

5.9.1 IF frequency stability

The long-term IF signal frequency stability from the transmit channel unit across interface D shall be at least 10^{-5} , long-term being assumed to be at least one month.

5.10 Buffering and slip control

In order to compensate for the effect of satellite movement and, in certain cases, for disparity between clocks at originating and receiving ends, buffering may be required at the receiving end.

In general, buffering to compensate for the satellite transmission delay variation is not required if in the terrestrial network between the receive channel unit and the video decoder the timing interfaces are codirectional. However, buffering will be required to connect the receive channel unit to a synchronous digital terrestrial network.

The receive channel unit shall provide buffering of the data signal. The buffering equipment write the data into the buffer using the recovered receive clock and shall read from the data buffer using a clock derived from the receive timing interface (see subclause 5.8.2).

5.10.1 Buffer capacity

The buffer capacity shall be adjustable between 0 and 32 ms in steps not exceeding 2 ms.

5.10.2 Slip control

Buffers shall be reset whenever the channel suffers loss of service and when they reach saturation or become empty. It shall also be possible to reset the buffers manually. To avoid loss of synchronization of the multiplex equipment it is preferable that slips consist of integer multiples of either a frame (1 536 bit) for the case of 34 368 kbit/s or a multiframe (4 760 bit) for the case of 44 736 kbit/s.

5.11 Local clock

As an emergency backup, a local clock (with a long term stability of at least 1 part in 10^5 per month shall be available in order to keep the circuit operating in the event that the primary clock source fails (see subclause 5.8.2). The emergency clock shall be slaved to the primary clock unless there is a failure of the primary clock.

6 Channel unit characteristics (optional requirements)

RS codes are a class of block codes which can be concatenated with the rate 3/4 FEC (convolutional encoding/Viterbi decoding) specified in subclause 5.3. The RS code constitutes the outer code while the convolutional code is designated as the inner code.

This clause specifies the outer RS code, the method of interleaving used between the inner and outer codes and the synchronization method used for the descrambler, de-interleaver and RS decoder.

The provision of the RS outer coding within the channel unit is optional.

6.1 RS outer code

6.1.1 Polynomials

6.1.1.1 Field generating polynomial

The binary primitive polynomial for generating the extended field of 256 elements, Galois Field (GF) (2^8), is:

$$p(x) = x^8 + x^7 + x^2 + x + 1$$

6.1.1.2 Code generator polynomials

The generator polynomials of the selected RS code is given by:

$$\prod_{i=120}^{119+2t} (x - \alpha)^i$$

where:

a is a root of $p(x)$, i.e., $p(\alpha) = 0$ over the extended field.

t is the maximum number of symbol errors per RS codeword that can be corrected (error-correction capability). For the selected RS code, $t = 8$ (see subclause 6.1.2.4).

Since each RS symbol is an element of the extended field, $GF(2^8)$, it can be represented by a binary octet (8-bit tuple). For the selected RS code, the octet:

$$(d_7, d_6, \dots, d_1, d_0)$$

with:

$$d_j = 0 \text{ or } 1; \quad 0 \leq j \leq 7$$

is identified with the element:

$$d_7\alpha^7 + d_6\alpha^6 + \dots + d_1\alpha + d_0$$

in $GF(2^8)$.

6.1.2 Code parameters

The RS code selected is derived by block length shortening of RS codes over the finite extended field, $GF(2^8)$, using the following parameters:

- n 255 RS symbols per codeword (block length);
- m 8, the number of bits per RS symbol;
- t the maximum number of symbol errors per RS codeword that can be corrected (error-correction capability);
- k $n - 2t$, the number of RS symbols in a RS codeword representing information (encoder input data). This block of k RS symbols is referred to as the information block;
- $n - k$ $2t$, the number of RS symbols representing error check symbols.

The selected RS code is a systematic code, i.e., each RS codeword (block length of n RS symbols), consists of an information block (k RS symbols), which is unaffected by the RS encoding process, to which a block of $(n - k)$ RS check symbols is appended (see figure 12)

6.1.3 Shortened codes

The block length of the RS code described in subclause 6.1.1 is shortened using the following procedure (see figure 12):

- a) For RS encoding and decoding the leading (in the order of transmission) q complete symbols within the information block of each RS codeword of length $n = 255$ are all preset to logical "0";
- b) The leading q all-zero symbols are not transmitted;

- c) The resulting transmitted codeword consists of $n' = (n - q)$ RS symbols and the transmitted information block has length $k' = (k - q)$. The number of RS check symbols $(n - k) = (n' - k')$ and the error-correction capability, t , is not affected by the described method of shortening the block length.

To preclude the possibility of misinterpretation, all subsequent references in the remainder of clause 6 to the RS code parameters n , k and t shall refer exclusively to the shortened RS code with $n = 208$, $k = 192$ and $t = 8$.

6.1.4 Type of RS code

The shortened systematic RS code which shall be used has $n = 208$, $k = 192$ and $t = 8$. The RS code selected can accommodate modem clock designs that are based on integer multiples of 8 kHz.

6.1.5 Interleaving

Since errors from the Viterbi decoder tend to occur in bursts, block interleaving shall be employed in conjunction with the RS outer code to reduce the correlation among erroneous symbols in a RS codeword. This minimizes the occurrences of error bursts at the output of the Viterbi decoder which might exceed the error-correcting capability of the RS decoder.

The inner FEC encoder/decoders comprises three parallel encoders/decoders. To ensure proper operation of the RS decoder, RS symbol integrity and the full interleaving depth (i.e. 4) shall be maintained at the input to the FEC encoder and at the input of the RS decoder. The signal formats at the interface between the output of the interleaver and the three inputs (1, 2 and 3) to the parallel FEC encoders are shown in figure 6.

6.2 Implementation of the RS outer coder/decoder

From a functional point of view, on the transmit channel unit the synchronous scrambler followed by the RS encoder/interleaver shall be inserted between the overhead framing unit and the FEC encoder and on the receive channel unit the RS decoder/de-interleaver followed by the synchronous descrambler shall be inserted between the FEC decoder and the overhead framing unit.

6.2.1 Switchability of the RS coder/decoder

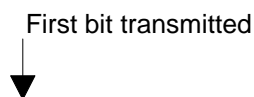
It shall be possible to enable or disable the use of RS outer coding by switching the RS coder/decoder in or out of the channel unit. It is expected that this function can be performed from the front-panel control of the channel unit.

6.3 Synchronization

To ensure that complete RS codewords reach the RS decoder and in the proper sequence, it is necessary to synchronize the descrambler, the de-interleaver, the RS decoder and the interface demultiplexer function. Synchronization of all four functions is accomplished by detecting a Unique Word (UW) which is inserted in certain RS codewords by the transmit channel unit, as specified below.

6.3.1 UW Definition

The UW which shall be used for the synchronization of the descrambler, RS de-interleaver and RS decoder and the interface demultiplexer function is the following 32-bit binary word:



Binary: 01011010 00001111 10111110 01100110

or,

Hexadecimal: 5A 0F BE 66

Note that the serial-to-parallel interpretation of the information bit stream given here is preserved during the byte-oriented RS processing. That is, the left-most bit, which is the most-significant bit of each RS symbol, is the bit that is transmitted first.

6.3.2 Insertion of UW

The 32-bit (4-byte) UW shall be inserted, after RS encoding has been performed, into the last two RS symbols (in the order of transmission) of the last two consecutive codeword outputs from the block interleaver by overwriting these RS error check symbols.

The RS error check symbols overwritten by the UW shall be declared and treated as erasures by the RS codec and shall be recovered by the RS decoder using erasure decoding.

Insertion of the unique word shall occur periodically once every 24 RS codewords. Insertion of the unique word shall be done so that the last byte of the unique word is the last byte of a three byte bit-multiplexer group. That is, the last unique word byte shall be serially shifted out of switch position number 1 as seen in the block diagram of figure 13.

6.3.3 Synchronization acquisition

6.3.3.1 Initial acquisition and UW detection

Detection of the 32-bit unique word shall be based on the total Hamming distance, d , being less than or equal to a detection threshold, E .

The detection of the unique word is expected to occur within a window which can be either fully open or have a width of 32 bits.

During initial acquisition, the window shall be fully open. Following the first detection of a UW, the window shall be narrowed to a width of 32 bits and centred about the expected arrival of the UW of 24 RS codewords later.

Valid detection of a UW ("sync acquired") shall be declared if d is less than or equal to $E = 1$ and if, 24 RS codewords before, d was also less than or equal to $E = 1$. The first valid UW detected in the window shall be the only one employed. If valid detection of the UW is not declared in the window, the UW shall be considered "missed".

6.3.3.2 Steady state and loss of synchronization

To ensure synchronization is maintained after initial acquisition, the occurrence of the UW every 24 RS codewords shall be monitored continuously. Loss of synchronisation ("sync loss") shall be declared if d is greater than or equal to $E = 6$ for four consecutive detections of the UW.

Following the loss of synchronization, the initial acquisition sequence described in subclause 6.3.3.1 shall be initiated.

6.4 Synchronous scrambler

The self-synchronizing scrambler specified in subclause 5.4 shall be disabled. A synchronous scrambler with the configuration depicted in figure 14 shall be employed instead in the RS encoder.

The polynomial of figure 14 is $1 + X^{-14} + X^{-15}$. Loading of the initial sequence 001001001001001 shall be performed at each insertion of the UW, i.e. every 24 RS codewords to aid the descrambling synchronization process. The right-most bit in the sequence (i.e., the "1") shall be located in shift register stage number 15 as indicated in figure 14. Loading of the initial sequence shall occur at the start of the first RS codeword following the last codeword in which UW substitution has been performed .

Whenever the RS outer codec is not being used the self-synchronizing scrambler shall be on (active). This is to ensure that scrambling is always applied to the information data stream.

6.5 Modulator/Demodulator filter response guidelines

6.5.1 Analogue filters

For channel units equipped with analogue filters, the modulator/demodulator filter masks when employing the optional RS outer coding may be determined, as indicated in figures 2(a) and 2(b), with respect to R, where R is the transmission rate without RS outer coding.

6.5.2 Digital filters

For channel units equipped with digital filters, the modulator/demodulator filter masks when employing the optional RS outer coding may be determined, as indicated in figures 2(a) and 2(b), but the value of R is multiplied by (n/k).

6.6 Power spectral density requirement

The power spectral density mask at the output of the transmit channel unit, interface D of figure 1, when employing the optional RS outer coding shall be determined, as specified in subclause 5.1.2 and in figure 4, as follows:

- Points B, D, F, H, K and M shall be determined with respect to the transmission rate without RS outer coding (R);
- Points A, C, E, G, I, J, L, P, Q, N and S shall be determined with respect to R multiplied by (n/k).

6.7 BER performance characteristics for the concatenated RS plus inner FEC coding

For the RS outer code concatenated with the inner rate 3/4 FEC code, the channel unit shall meet the performance requirements given in this subclause in an IF back-to-back mode. These values apply with the self-synchronizing scrambler disabled, the synchronous scrambler enabled, the use of RS outer coding and inner convolutional encoding/Viterbi decoding, and under the conditions outlined in subclause 5.2.1.

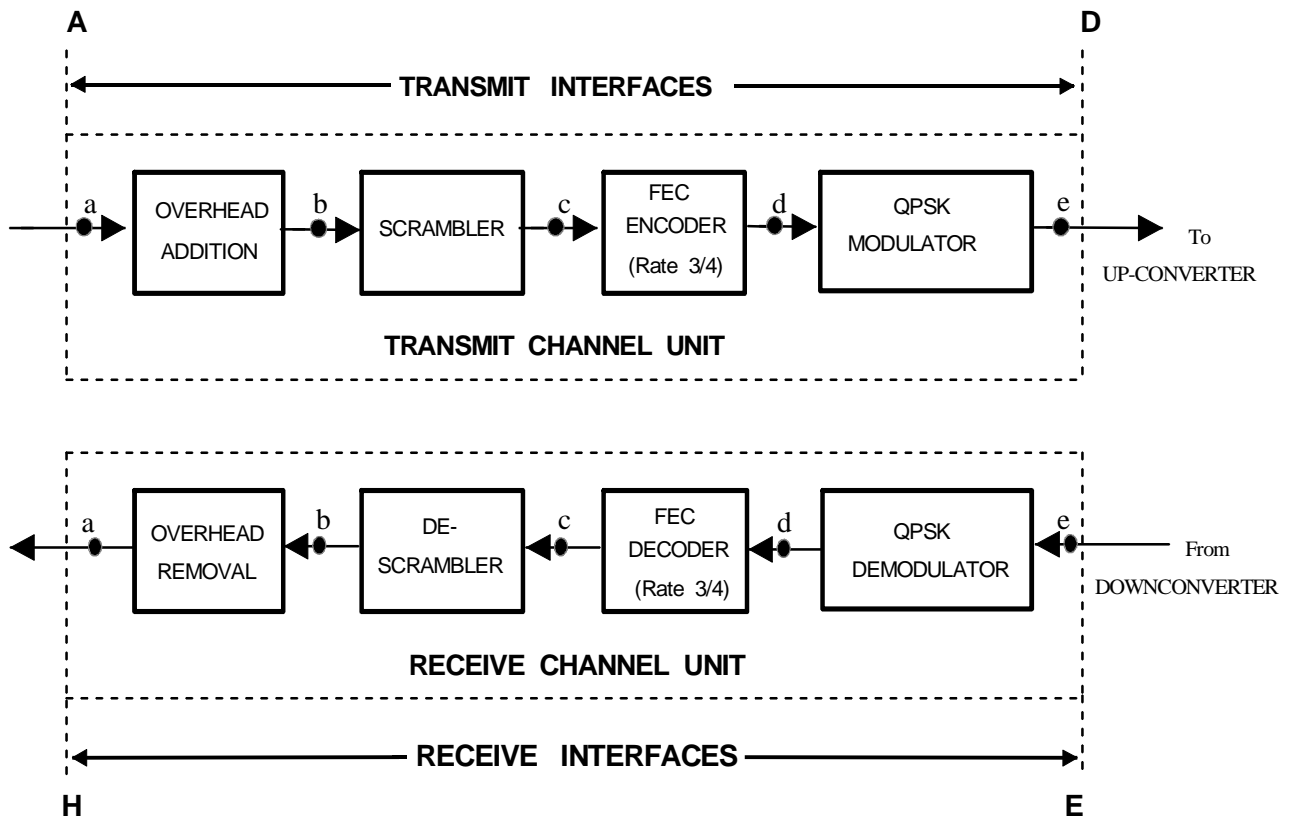
Table 3

BER better than:	Composite Data Rate E_b/N_0 (dB)
10^{-6}	5.6
10^{-7}	5.8
10^{-8}	6.0
10^{-10}	6.3

The E_b/N_0 is referred to the modulated carrier power and to the composite data rate (information rate plus overhead) entering the RS encoder. These E_b/N_0 values include a 0.3 dB allowance for increased intersymbol interference caused by allowing the use of analogue modem filters whose designs are based on the transmission rate without the use of RS outer coding.

Table 4: Fault conditions and consequent actions

Fault (F) detected	Action (A) to be taken			
	Condition	Channel Unit Alarm Output	To terrestrial link (across interface H)	To satellite (across interface D)
From terrestrial link (across interface a)	FA1	AS1	-	AD1
From satellite (across interface E)	FE1	AS1	AH1	-
	FE2	AS1	AH1	-
	FE3	AS1	-	-

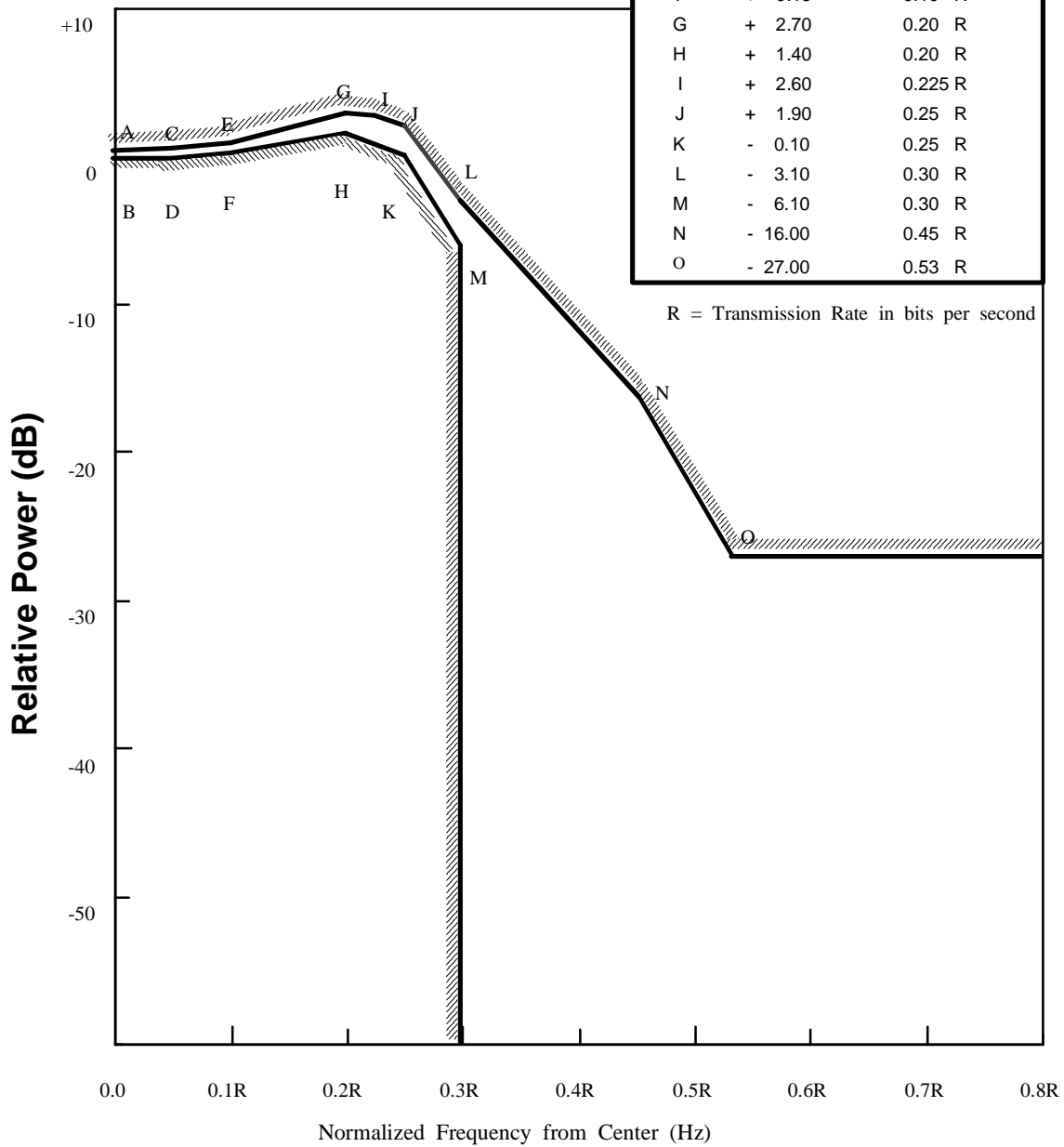


- a Information Rate, IR
- b, c Composite Rate, $CR = IR \text{ plus OVERHEAD}$
- d Transmission Rate, $R = CR/C$ ($C = \text{Code Rate} = 3/4$)
- e Symbol Rate, $SR = R/2$

Figure 1: Illustration of channel unit

COORDINATES OF POINTS

POINT	AMP. (dB)	NORM. FREQ. (Hz)
A	+ 0.25	0.0
B	- 0.25	0.0
C	+ 0.40	0.05 R
D	- 0.25	0.05 R
E	+ 0.80	0.10 R
F	+ 0.15	0.10 R
G	+ 2.70	0.20 R
H	+ 1.40	0.20 R
I	+ 2.60	0.225 R
J	+ 1.90	0.25 R
K	- 0.10	0.25 R
L	- 3.10	0.30 R
M	- 6.10	0.30 R
N	- 16.00	0.45 R
O	- 27.00	0.53 R



NOTE: The filter response is not a mandatory requirement. It is used to specify the transmit spectrum, which is a mandatory requirement.

Figure 2 (a): Modulator filter amplitude response

COORDINATES OF POINTS

POINT	AMP. (dB)	NORM. FREQ. (Hz)
A	+ 0.25	0.0
B	- 0.25	0.0
C	+ 0.25	0.15 R
D	- 0.25	0.15 R
E	+ 0.25	0.20 R
F	- 1.00	0.20 R
G	- 0.50	0.225 R
H	- 2.00	0.25 R
I	- 4.00	0.25 R
J	- 9.00	0.30 R
K	- 12.00	0.30 R
L	- 35.00	0.50 R
M	- 40.00	0.55 R

R = Transmission Rate in bits per second

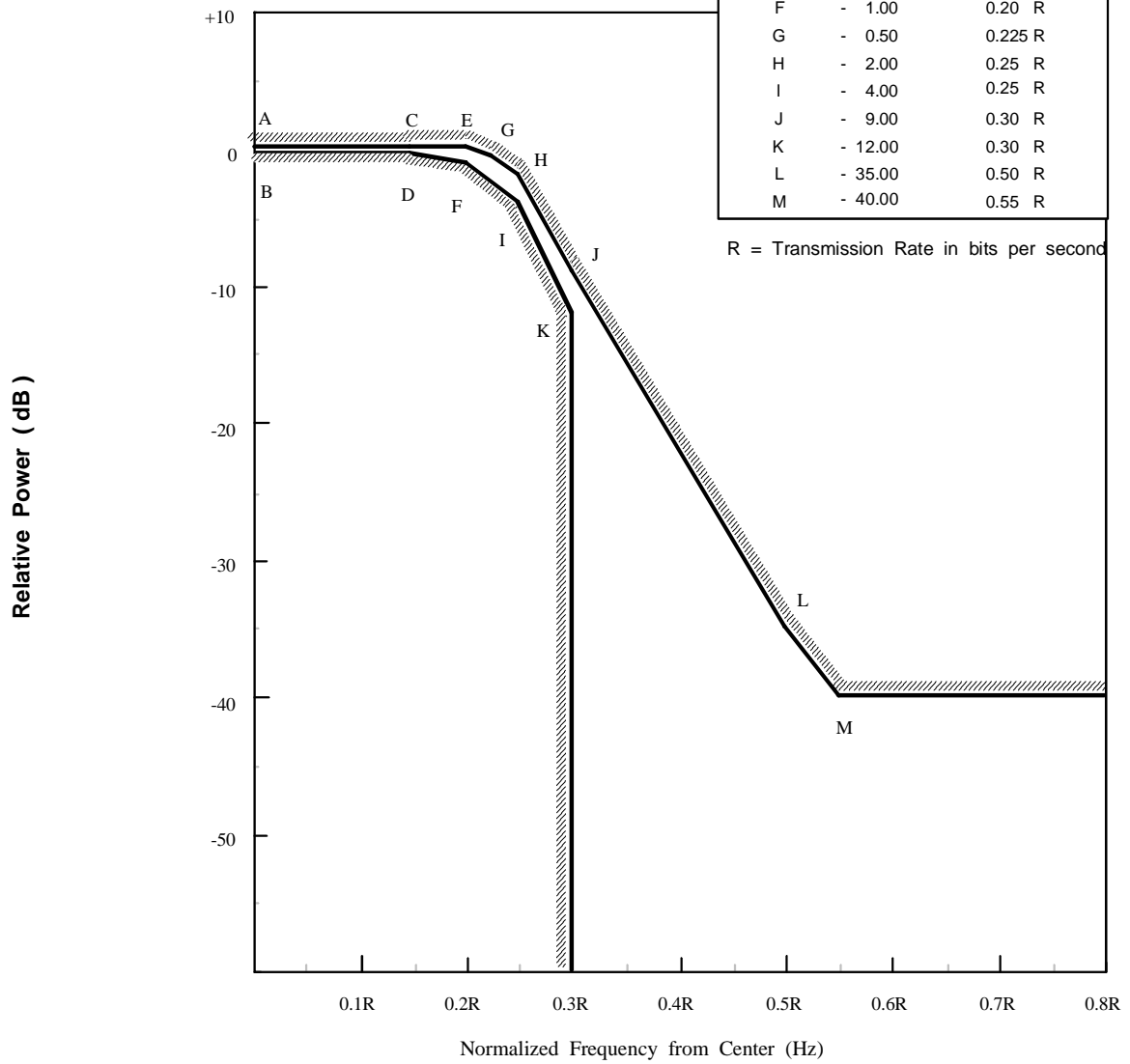
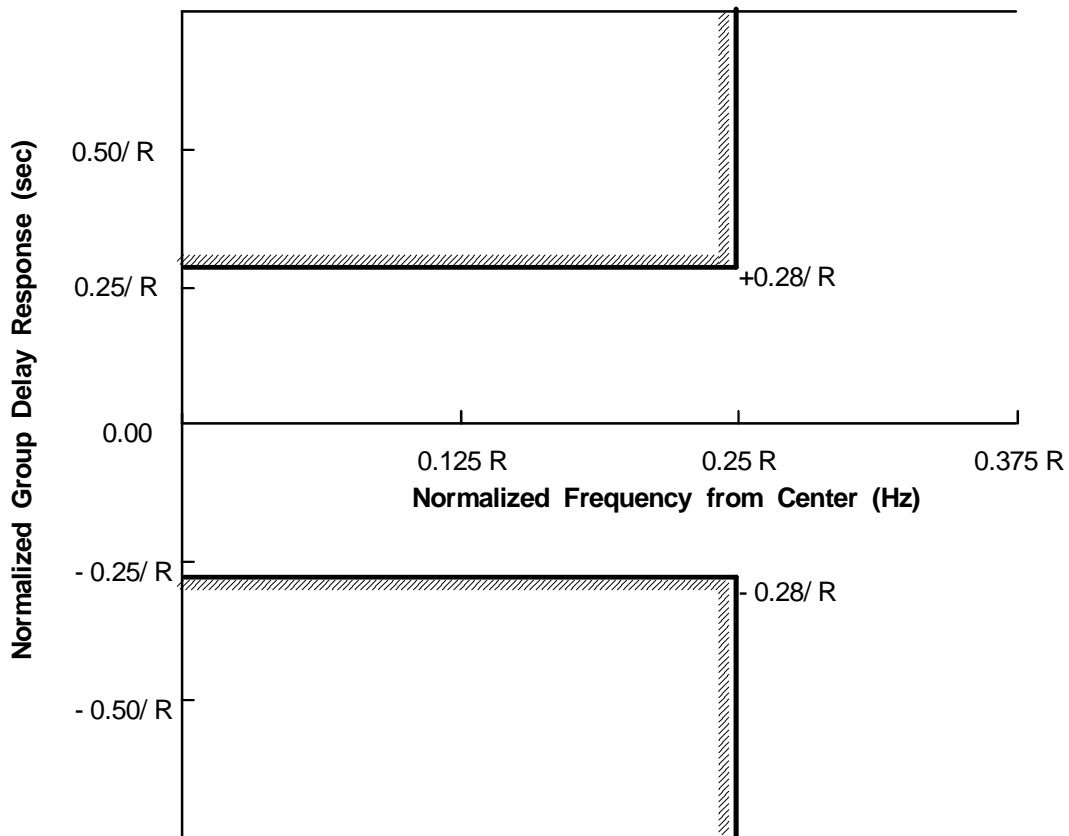


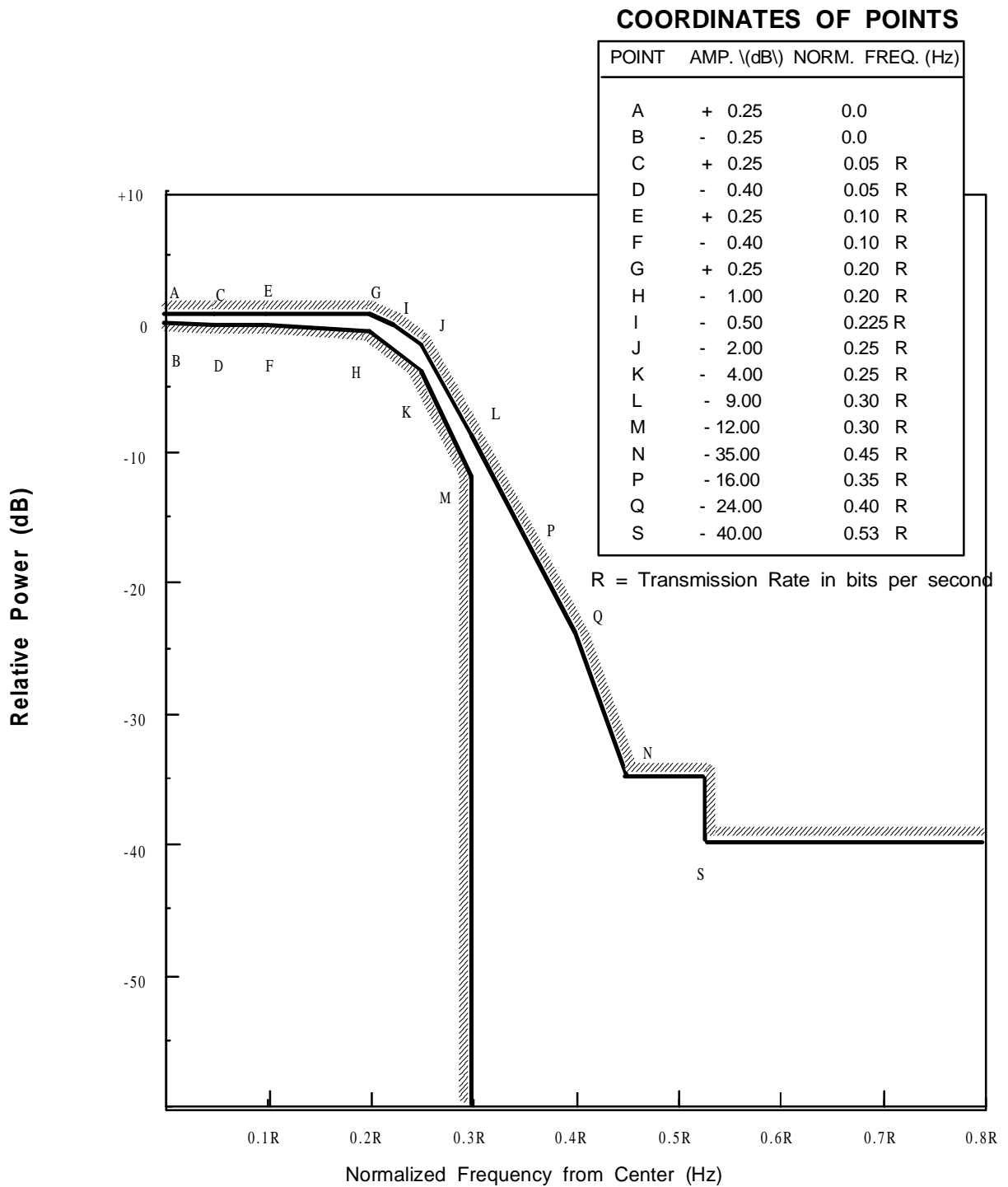
Figure 2 (b): Demodulator filter amplitude response



R = Transmission Rate in bits per second

- NOTE 1: The filter response is not a mandatory requirement. It is used to specify the transmitted carrier spectrum, which is a mandatory requirement.
- NOTE 2: Either the above group delay response or a phase response with less than ± 4 degrees departure from a linear phase shift (over the frequency range $\pm 0.25 R$ Hz above the center frequency) may be used.

Figure 3: Modulator and demodulator filter group delay response



NOTE 1: Points A through N correspond to points A through N in figure 2 (a) Modular filter amplitude response.

NOTE 2: 0 dB relative power corresponds to $-10 \log (R/2)$ dB/Hz relative to the unmodulated carrier power.

Figure 4: Power spectral density mask at modulator output

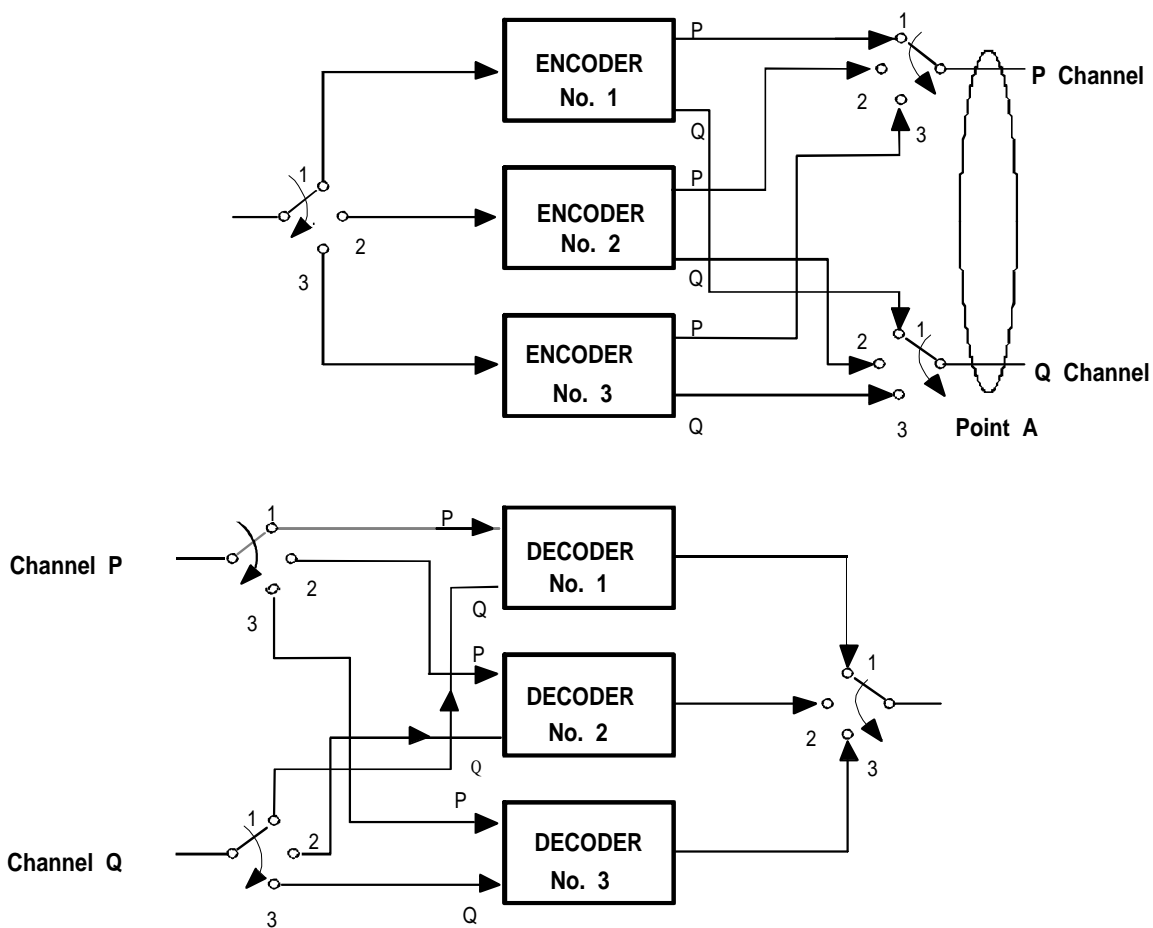


Figure 5: Configuration of encoder and decoder

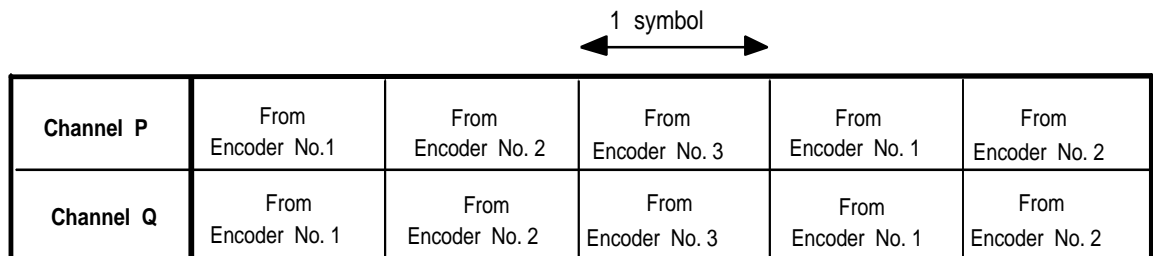
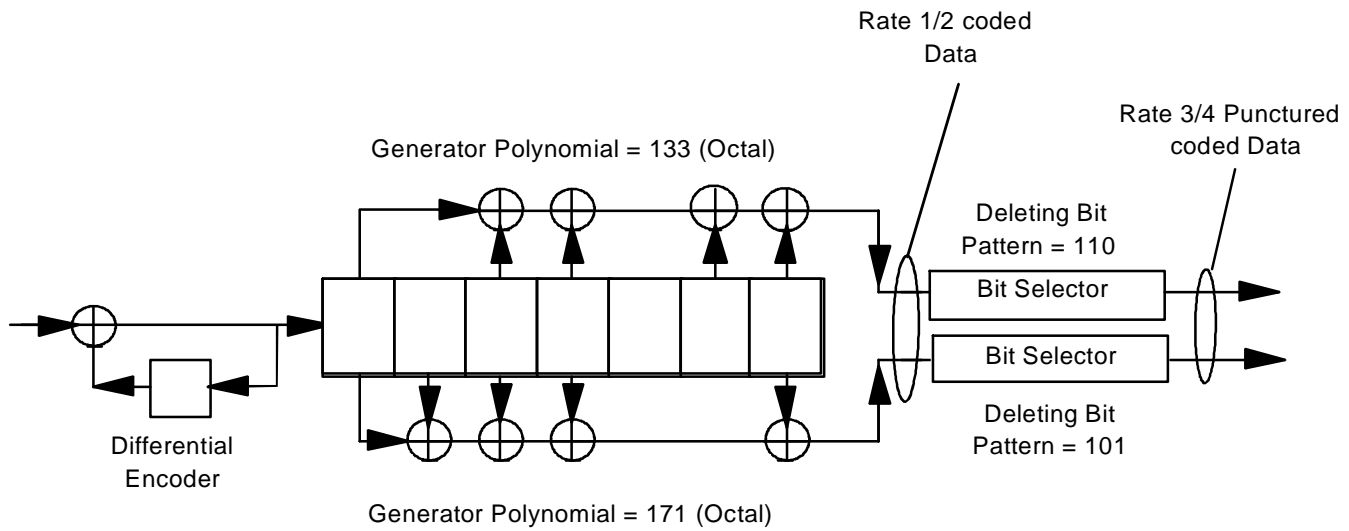


Figure 6: Signal format at point A in figure 5



NOTE 1: The symbol \oplus denotes a modulo-2 adder.

NOTE 2: In the deleting bit pattern, 1 denotes transmitting and 0 denotes deleting.

NOTE 3: The far right-most shift register stage corresponds to the least significant bit in the General Polynomial.

Figure 7: Convolution encoding process block diagram (for use with VITERBI decoding)

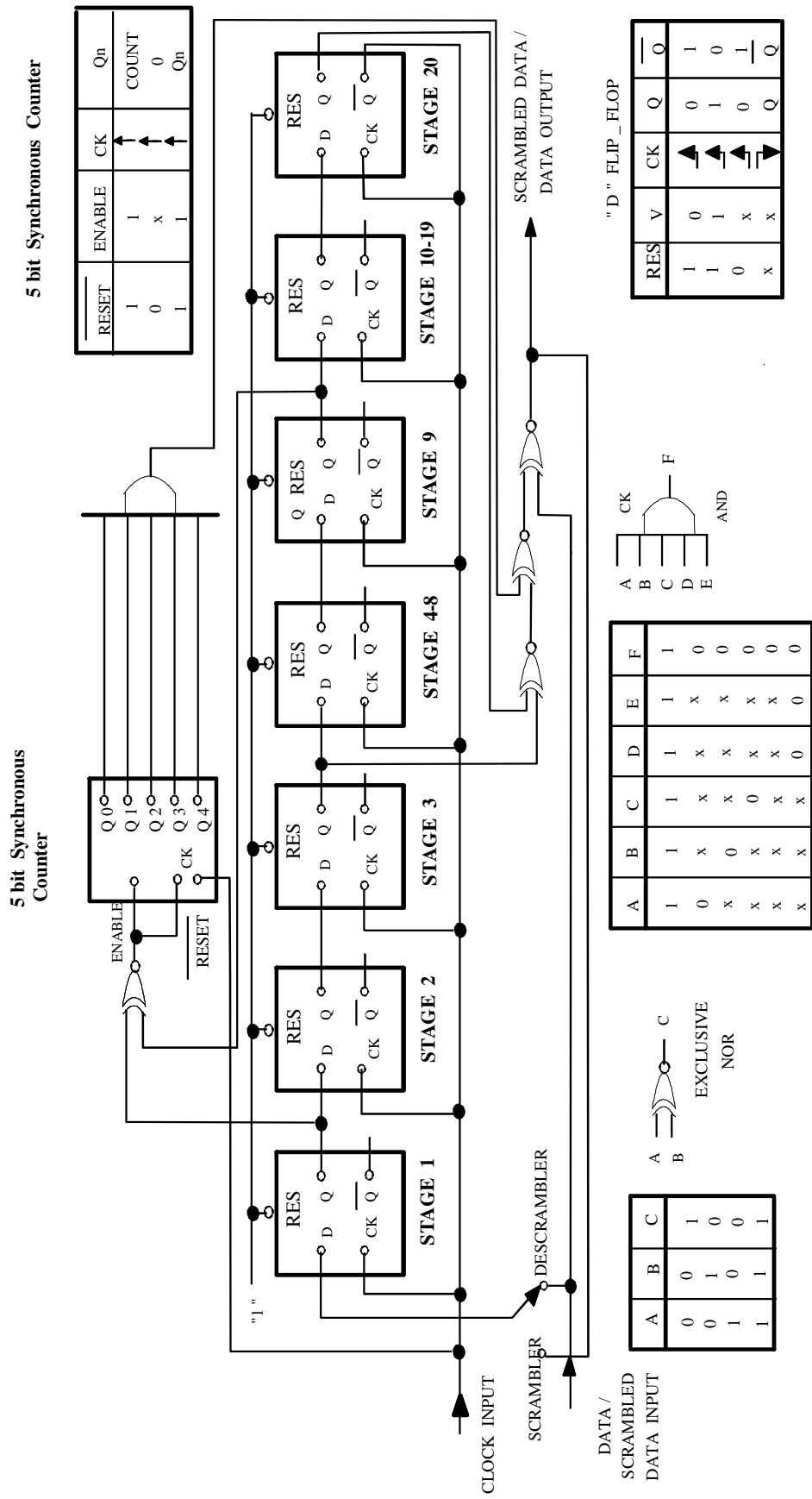
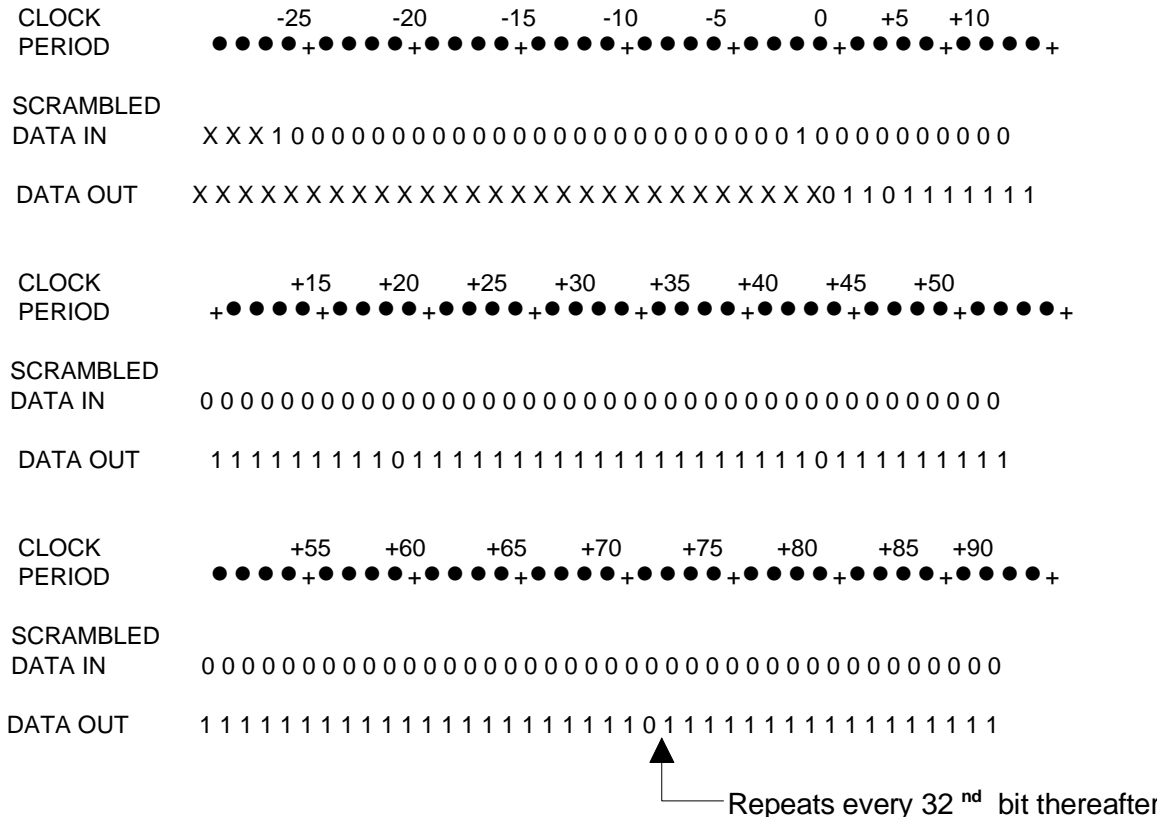


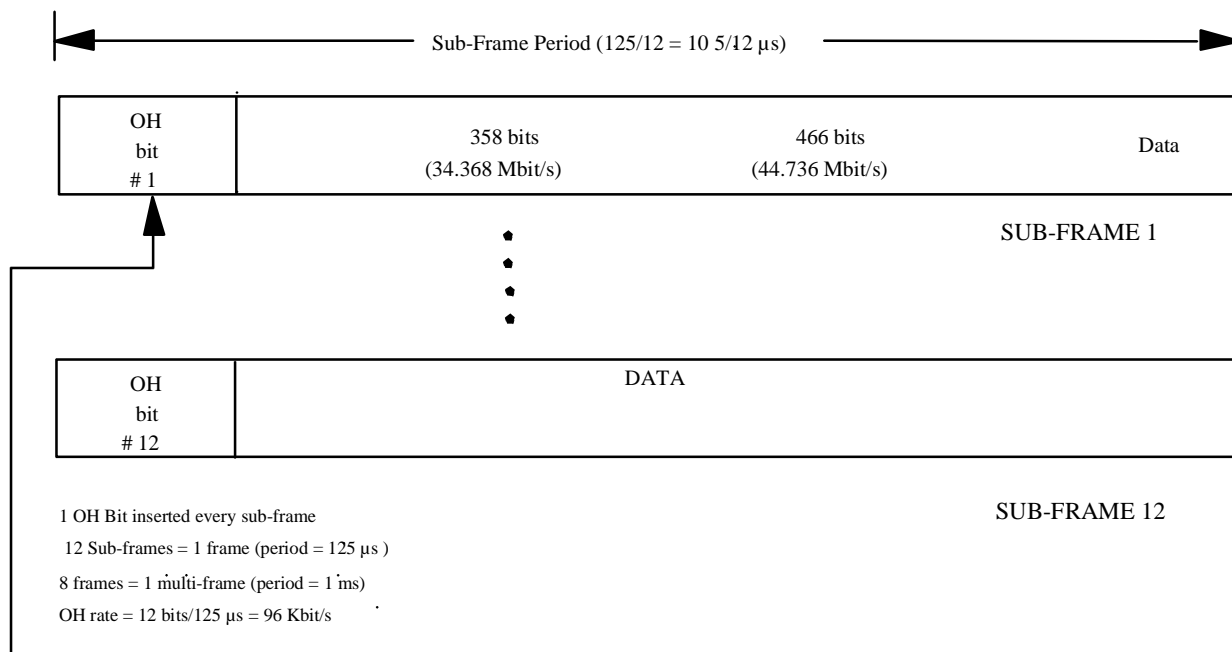
Figure 8: Scrambler/Descrambler logic diagram



NOTE 1: x = Either 1 or 0 (don't care)

NOTE 2: The purpose of the digital "one" followed by 25 "zeroes" beginning at clock period -26 is to reset the 5-bit counter and "flush-out" the 20-stage shift register.

Figure 9: Scrambler impulse response



first bit transmitted

ALLOCATION OF OH BITS

FRAME #	OH bit # (SUB-FRAME #)											
	1	2	3	4	5*	6	7	8	9*	10	11	12
1	0	1	0	0		P ₁					P ₂	
2	1	A ₁	d ₁ **	d ₂		P ₁					P ₂	
3	0	1	0	0		P ₁					P ₂	
4	0	A ₂	d ₃	d ₄		P ₁					P ₂	
5	0	1	0	0		P ₁					P ₂	
6	1	A ₃	d ₅	d ₆		P ₁					P ₂	
7	1	1	0	0		P ₁					P ₂	
8	1	A ₄	d ₇	d ₈		P ₁					P ₂	

P_i = ESC Voice Channel i Bits (i = 1 or 2); (Set to 1 if not used)
 A_i = Backward Alarm to Destination i (i = 1 to 4); no alarm = 0; alarm = 1
 d_i = ESC Digital Data (i = 1 to 8); (Set to 1 if not used)
 8 Frames = 1 Multiframe (Period = 1 ms)
 OH Rate = 12 bit/125 μs = 96 Kbits/s
 * Bits 5 and 9 in the overhead frame correspond to the first bits transmitted in the ESC voice channels.
 **d₁ corresponds to the first bit transmitted in the ESC data channel

Figure 10: Overhead structure

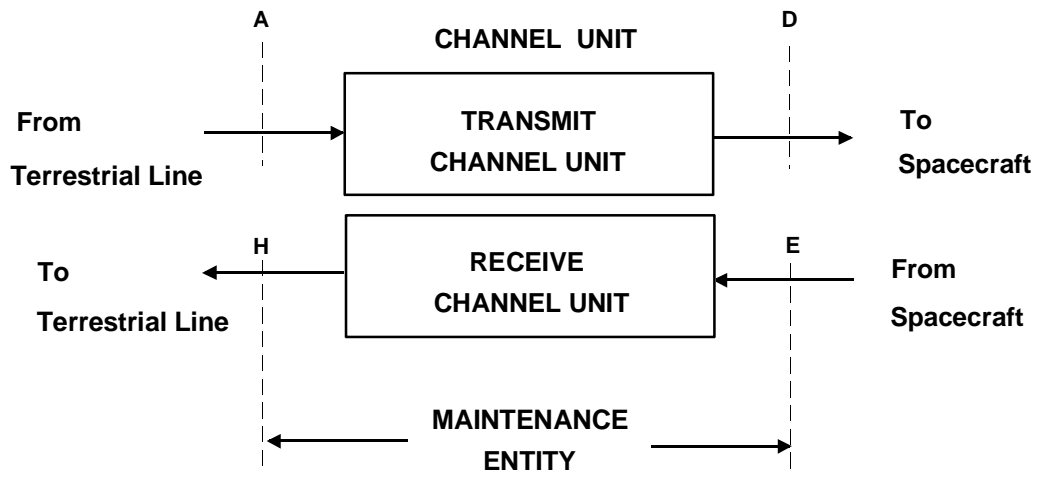


Figure 11: Channel unit alarm concept

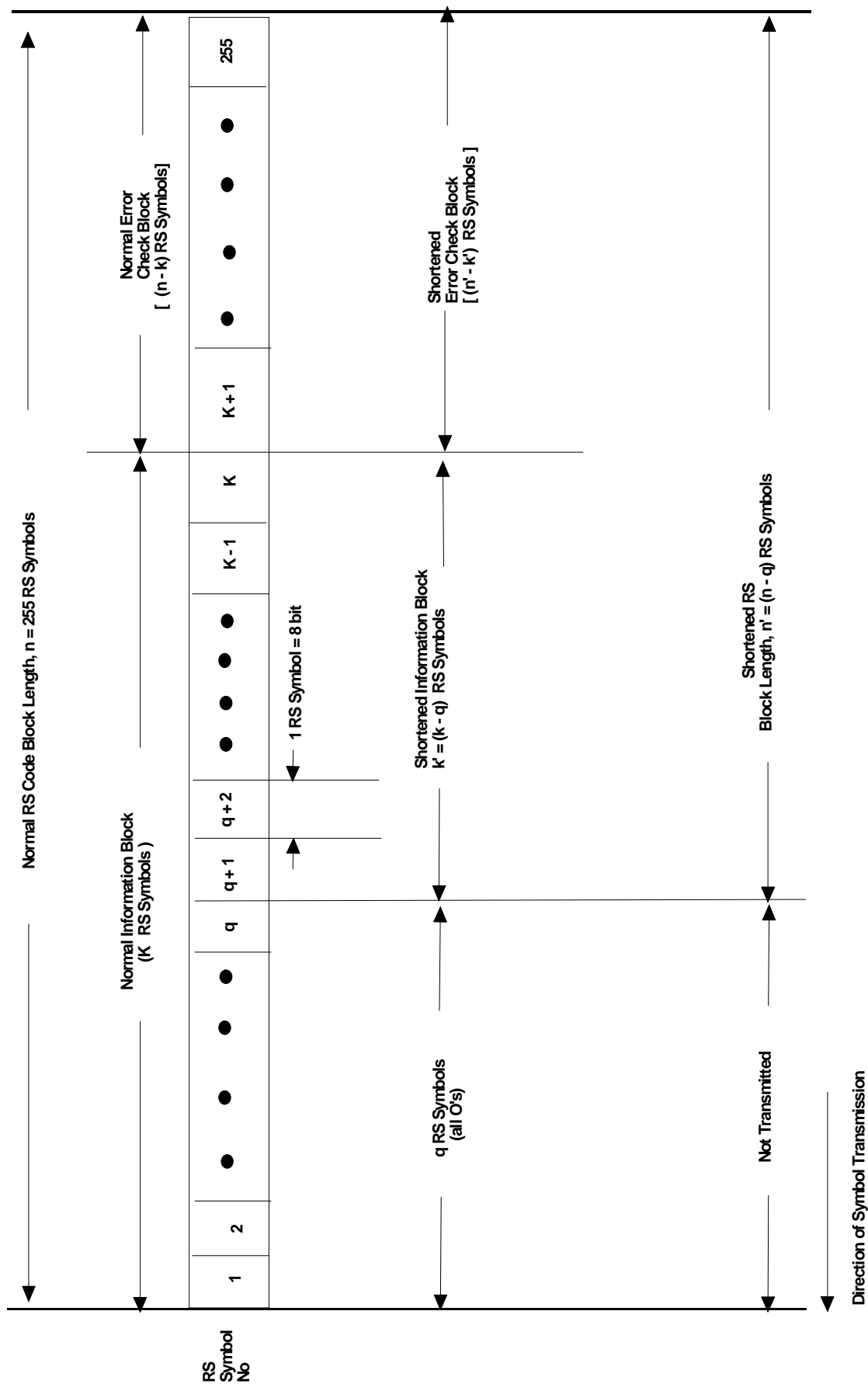


Figure 12: Systematic reed-solomon codeword configuration

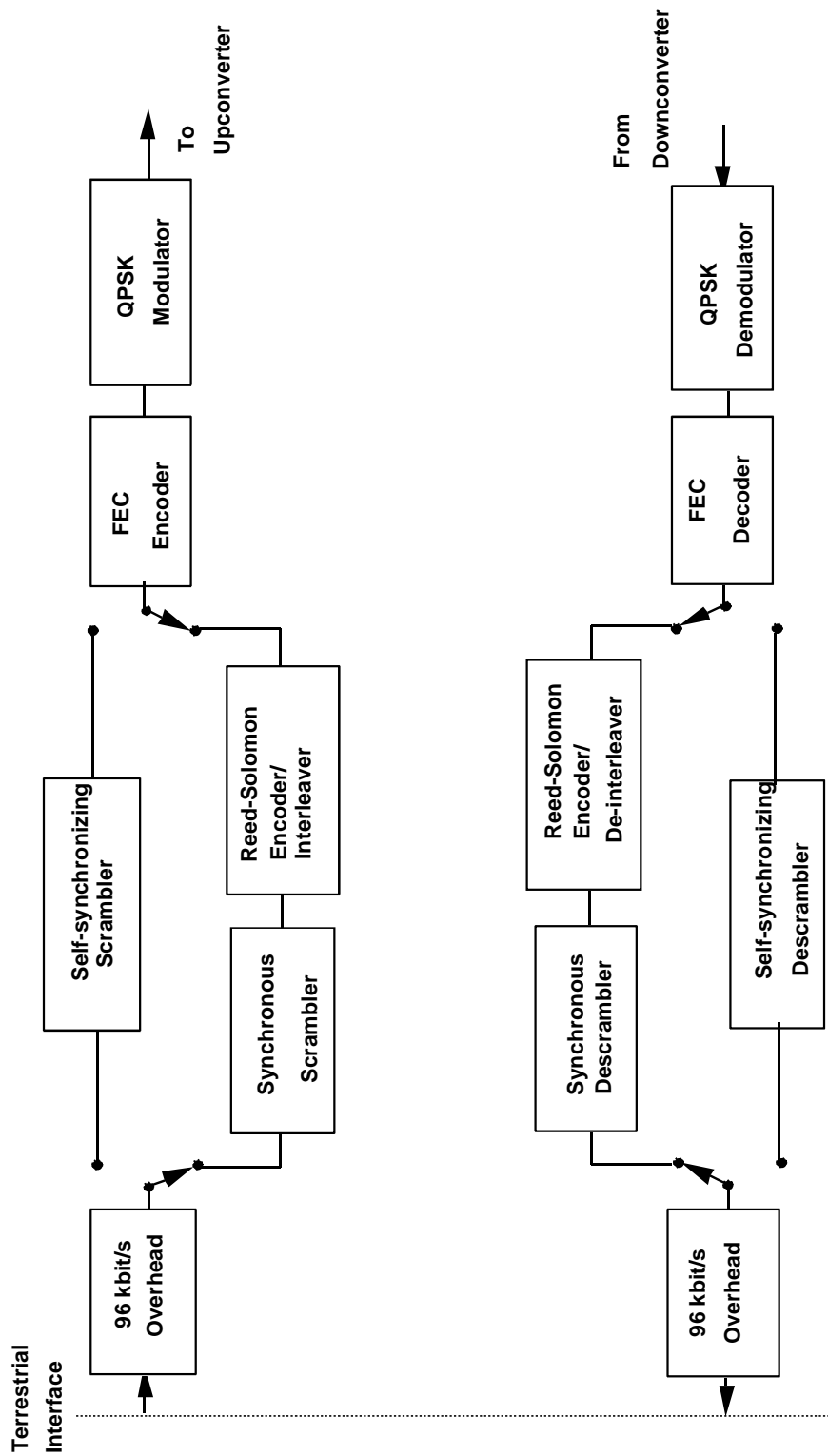
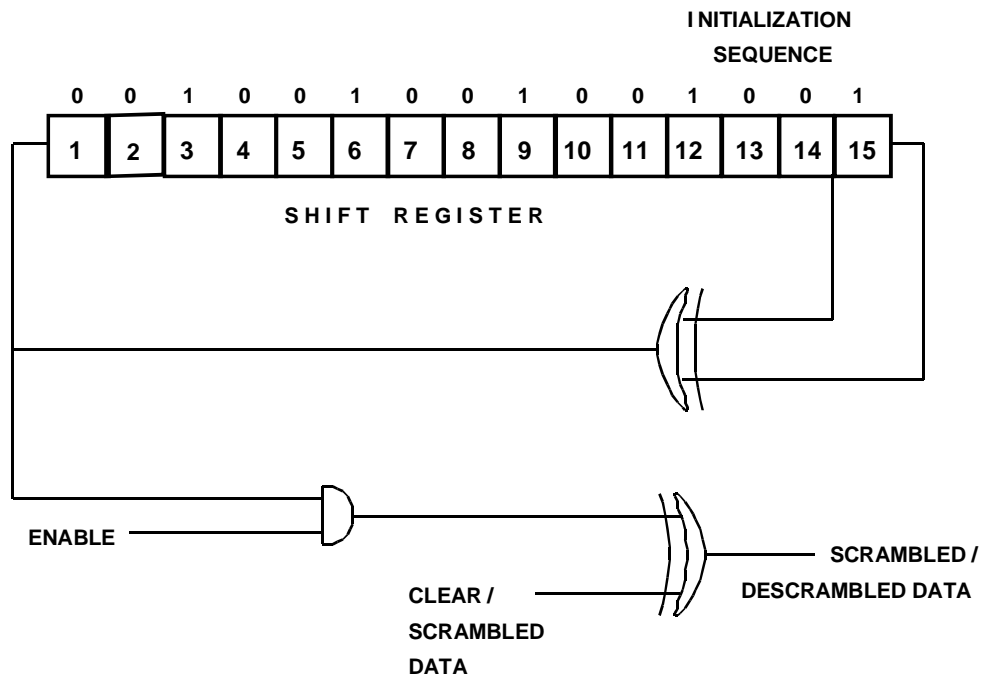


Figure 13: Functional block diagram of channel unit with reed-solomon outer coding



SYMBOL	FUNCTION	LOGIC TABLE		
		A	B	C
	EXCLUSIVE OR	0	0	0
		0	1	1
		1	0	1
		1	1	0
	AND	0	0	0
		0	1	0
		1	0	0
		1	1	1

Figure 14: Synchronous scrambler and descrambler schematic

History

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