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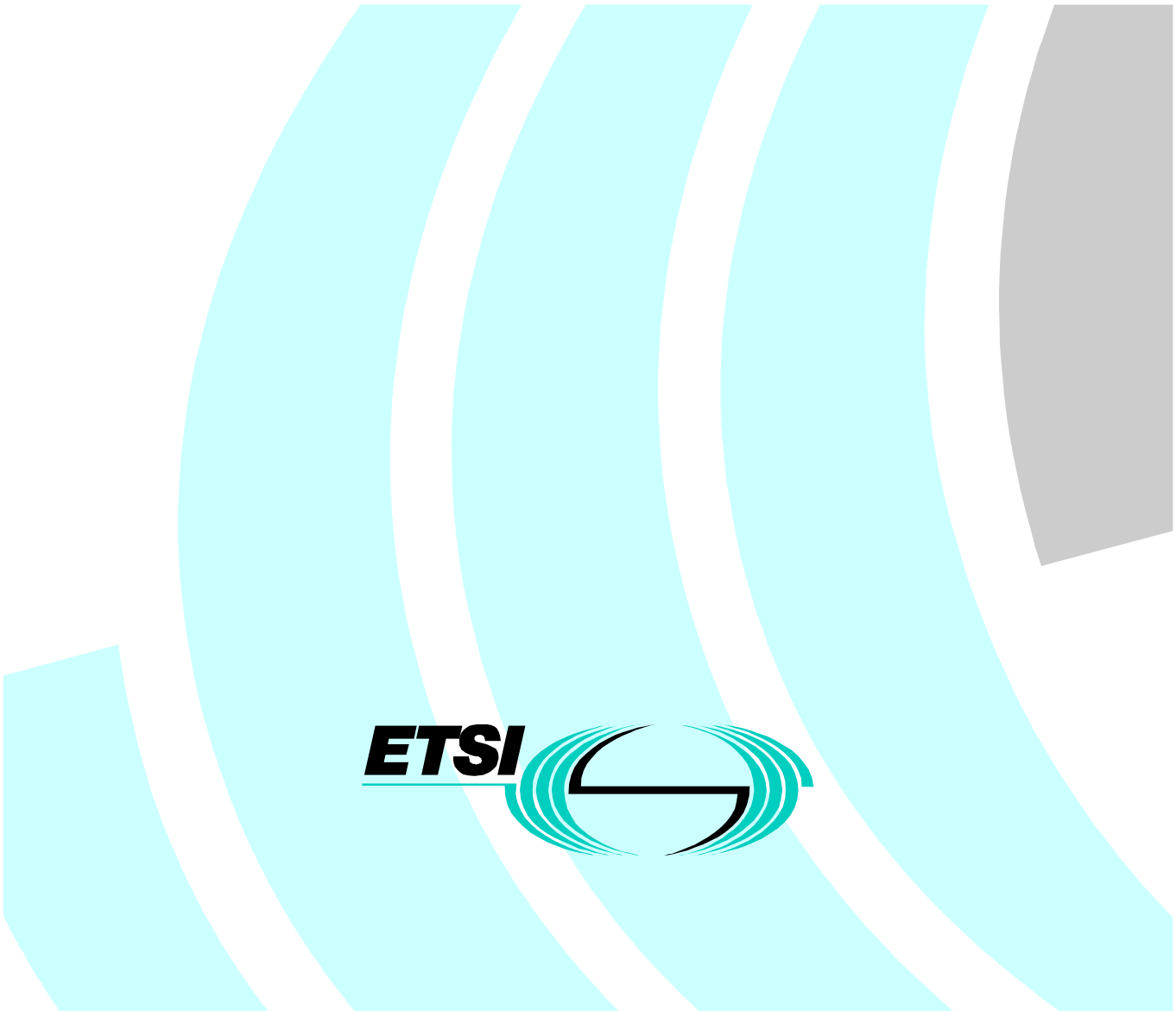
European Standard (Telecommunications series)

Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2-1: Synchronization network architecture



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Contents

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Foreword

This European Standard (Telecommunications series) has been produced by the Transmission and Multiplexing (TM) Technical Committee.

The present document has been produced to provide requirements for synchronization networks that are compatible with the performance requirements of digital networks. It is one of a family of documents covering various aspects of synchronization networks:

Part 1-1:	"Definitions and terminology for synchronization networks";
Part 2-1:	**"Synchronization network architecture";**
Part 3-1:	"The control of jitter and wander within synchronization networks";
Part 4-1:	"Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment";
Part 4-2:	"Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment Implementation Conformance (ICS) Statement";
Part 5-1:	"Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment";
Part 6-1:	"Timing characteristics of primary reference clocks";
Part 6-2:	"Timing characteristics of primary reference clocks Implementation Conformance (ICS) Statement";
Part 7-1:	"Timing characteristics of slave clocks suitable for synchronization supply to equipment in local node applications".

Parts 1-1, 2-1, 3-1 and 5-1 have previously been published as ETS 300 462 Parts 1, 2, 3 and 5, respectively.

Additionally, parts 4-1 and 6-1 completed the Voting phase of the Two Step Approval procedure as ETS 300 462 Parts 4 and 6, respectively.

It was decided to prepare ICS proformas for several of the parts and this necessitated a re-numbering of the individual document parts. It was also decided to create a new part 7-1.

This in turn led to a need to re-publish new versions of all six parts of the original ETS. At the same time, the opportunity was taken to convert the document type to EN.

This has involved no technical change to any of the documents. However part 5-1 has been modified, due to editorial errors which appeared in ETS 300 462-5.

Transposition dates	
Date of adoption of this ETS:	16 August 1996
Date of latest announcement of this ETS (doa):	31 December 1996
Date of latest publication of new National Standard or endorsement of this ETS (dop/e):	30 June 1997
Date of withdrawal of any conflicting National Standard (dow):	30 June 1997

NOTE: The above transposition table is the original table from ETS 300 462-2 (September 1996, see History).

1 Scope

This European Standard (Telecommunications series) specifies the architectural principles that should be applied for the design of synchronization networks that are suitable for the synchronization of Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) networks. It supports the construction of synchronization networks that support both the short term stability requirements of SDH networks and the long term stability requirements of PDH networks. It applies to the design of new synchronization networks. It does not characterize existing PDH synchronization networks.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, subsequent revisions do apply.
- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1] EN 300 462-1-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1-1: Definitions and terminology for synchronization networks".

[2] EN 300 462-3-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks".

[3] ETS 300 147 (1995): "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH) Multiplexing structure".

[4] EN 300 462-5-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[5] EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[6] ITU-T Recommendation G.783 (1994): "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks".

[7] EN 300 462-4-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4-1: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the definitions given in EN 300 462-1-1 [1] apply:

3.2 Abbreviations

For the purposes of the present document, the abbreviations given in EN 300 462-1-1 [1], together with the following, apply:

AIS	Alarm Indication Signal
NE	Network Element
PDH	Plesiochronous Digital Hierarchy
ppm	parts per million
PRC	Primary Reference Clock
PSTN	Public Switched Telephone Network
SASE	Stand-Alone Synchronization Equipment
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SETS	SDH Equipment Timing Source
SSU	Synchronization Supply Unit
STM-N	Synchronous Transport Module N
TU	Tributary Unit

4 Synchronization methods

There are two fundamental methods of synchronizing nodal clocks. These are identified in EN 300 462-1-1 [1]:

- master-slave synchronization;
- mutual synchronization.

4.1 Master-slave synchronization

Master-slave synchronization is appropriate for synchronizing SDH networks and the following material offers guidance on using this method.

Master-slave synchronization uses a hierarchy of clocks in which each level of the hierarchy is synchronized with reference to a higher level. There are four qualities of clock in the synchronization hierarchy shown below:

- Primary Reference Clock (PRC): see EN 300 462-6-1 [5];
- slave clock (transit node): see EN 300 462-4-1 [7];
- slave clock (local node): see EN 300 462-4-1 [7];
- SDH Equipment Clock (SEC): see EN 300 462-5-1 [4].

The PRC is the highest quality hierarchical clock and the SEC is the lowest quality clock. Higher quality clocks must not be synchronised by lower quality clocks in holdover mode, but clocks in holdover mode can be used to synchronise clocks of the same quality. There are limits on the number of clocks which can be connected in a synchronization distribution trail (see clause 8). Clock reference signals are distributed between levels of the hierarchy via a distribution network which may use the facilities of the transport network. The transport network may contain SECs. The distribution of timing between hierarchical node clocks shall be performed using a method which avoids intermediate pointer processing. Two possible methods are as follows:

a) recover timing from a received Synchronous Transport Module N (STM-N) signal (this avoids the unpredictable effect of a pointer adjustment on the downstream slave clock);

b) derive timing from a synchronization trail that is not supported by a SDH network.

The master-slave method uses a single-ended synchronization technique with the slave clock determining the synchronization trail to be used as its reference and changing to an alternative if the original trail fails. This is a unilateral control scheme.

4.2 Mutual synchronization

The feasibility of employing mutual synchronization is left for further study. The remainder of the present document refers only to the hierarchical master-slave approach.

5 Functional description of clock types

5.1 Primary Reference Clock (PRC)

A PRC is a stand-alone clock and a logical function which:

- is either an autonomous clock; or
- it accepts synchronization from a radio or satellite signal and performs filtering.

The PRC shall conform to EN 300 462-5-1 [4].

5.2 Synchronization Supply Unit (SSU)

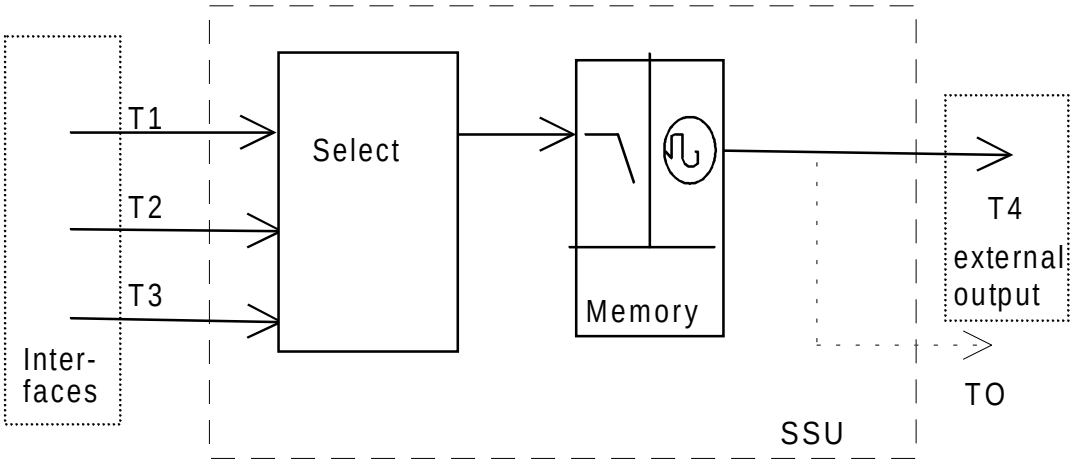
A SSU is a logical function which:

- accepts synchronization inputs from a number of sources;
- selects one of these inputs;
- filters this source's clock; and
- distributes the resultant clock to other elements within a node.

A functional diagram of the SSU is shown in figure 1.

In the event of failure or degradation of all synchronization reference inputs, the SSU will use an internal timing source (under study).

The physical implementation of this function may be integrated within a SDH network element, integrated within Public Switched Telephone Network (PSTN) switch, or as a stand-alone unit (a Stand-Alone Synchronization Equipment (SASE)).



Key:

T0: Internal network element timing reference signal.

T1: Timing signal derived from STM-N input.

T2: Timing signal derived from 2 Mbit/s input.

T3: Timing signal derived from 2 MHz synchronization input.

T4: External timing output.

NOTE 1: Where the SSU is integrated within a SDH Network Element (NE), T0 should be provided.
NOTE 2: It may be possible to force the SSU into a free running condition.

Figure 1: The SSU clock function

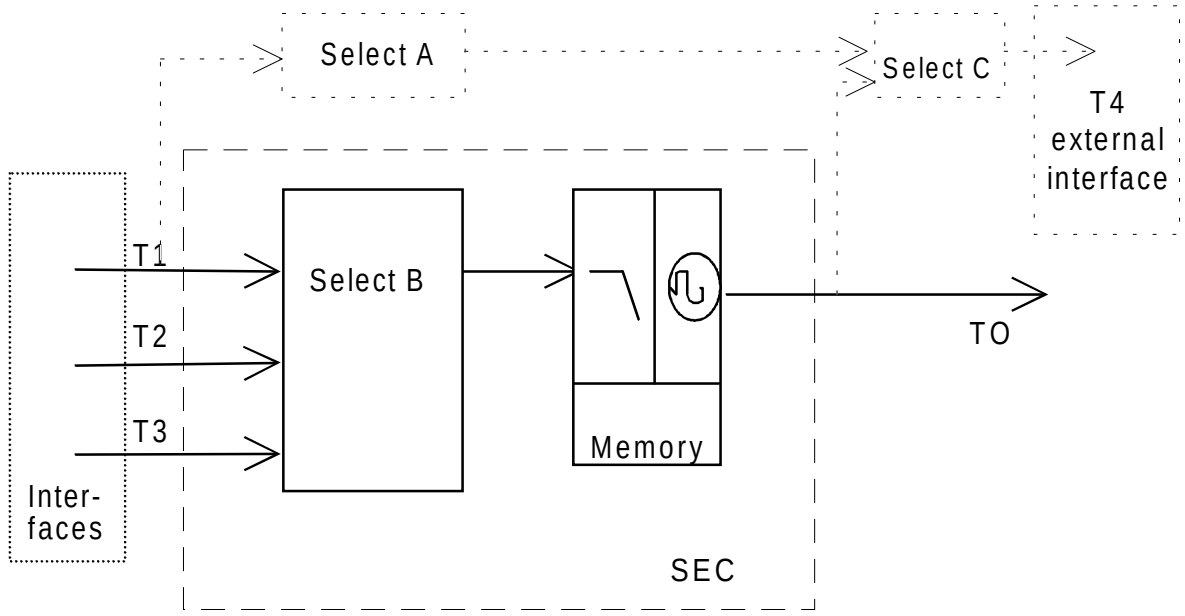
5.3 SDH Equipment Clock (SEC)

An SEC is the internal clock of an SDH network element and a logical function which;

- accepts synchronization inputs from a number of sources within that element;
- selects one of these inputs;
- filters this source´s clock according to EN 300 462-5-1 [4].

The SDH clock is used to time the outgoing SDH STM-N interfaces of the network element. A functional diagram of the SEC is shown in figure 2.

In the event of failure of all synchronization reference inputs the SEC shall use its own internal clock which shall conform to EN 300 462-5-1 [4].



Key:

T0: Internal timing reference signal.
T1: Timing signal derived from STM-N input.
T2: Timing signal derived from 2 Mbit/s input.
T3: Timing signal derived from 2 MHz synchronization input.
T4: External timing references.

NOTE 1: This is a functional subset of the SETS as defined in ITU-T Recommendation G.783 [6].
NOTE 2: It may be possible to force the SEC into a free running condition.

Figure 2: The SEC clock function

6 Synchronization network architecture

The architecture employed in SDH requires the timing of all network element clocks to be traceable to a PRC. This clause details the target architecture for SDH network synchronization. Evolutionary aspects are discussed in clause 10.

The distribution of synchronization can be categorized into intra-node within nodes containing a SSU and inter-node as follows:

a) intra-node distribution within nodes containing a SSU conforms to a logical star topology. All lower level network element clocks within a node boundary derive timing from the highest hierarchical clock level in the node. An exception may be made for the network element clock that carries the synchronization trail to the SSU. An example illustrating this exception is given in the following:

   Assume that network timing has to be distributed along a ring structure where each node, in addition to the ring ADM, contains an SSU. By considering the ring ADM's to belong to a synchronization trail rather than to the nodes where they are located, excessive cascading of SSU's can be prevented. All other outputs from each node may be timed from the local SSU.

   Apart from these network elements, only the clock of the highest hierarchical level in the node will recover timing from synchronization links from other nodes. Timing is distributed from network elements within the boundary to network elements beyond the boundary via the SDH transmission medium. The relationship between clocks within a node is shown in figure 3.

NOTE: Any interface used for synchronization of SDH NE should comply with the requirements given in EN 300 462-3-1 [2].

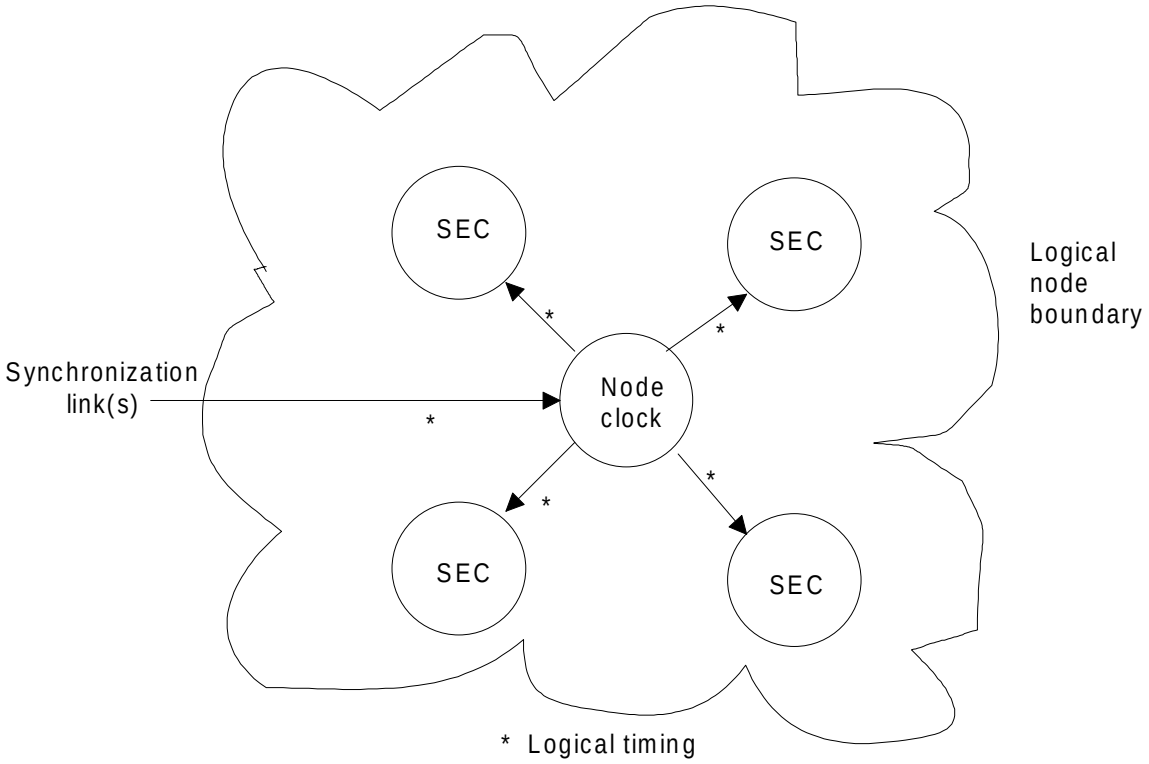


Figure 3: Synchronization network architecture for intra-node distribution

b) inter-node distribution conforms to a tree-like topology and enables all the nodes in the SDH network to be synchronized. The hierarchical relationship between clocks is shown in figure 4. With this architecture, it is important for the correct operation of the synchronization network that clocks of lower hierarchical level only accept timing from clocks of the same or higher hierarchical level and that timing loops are avoided. To ensure that this relationship is preserved, the distribution network shall be designed such that, even under fault conditions, only valid higher level references are presented to hierarchical clocks.

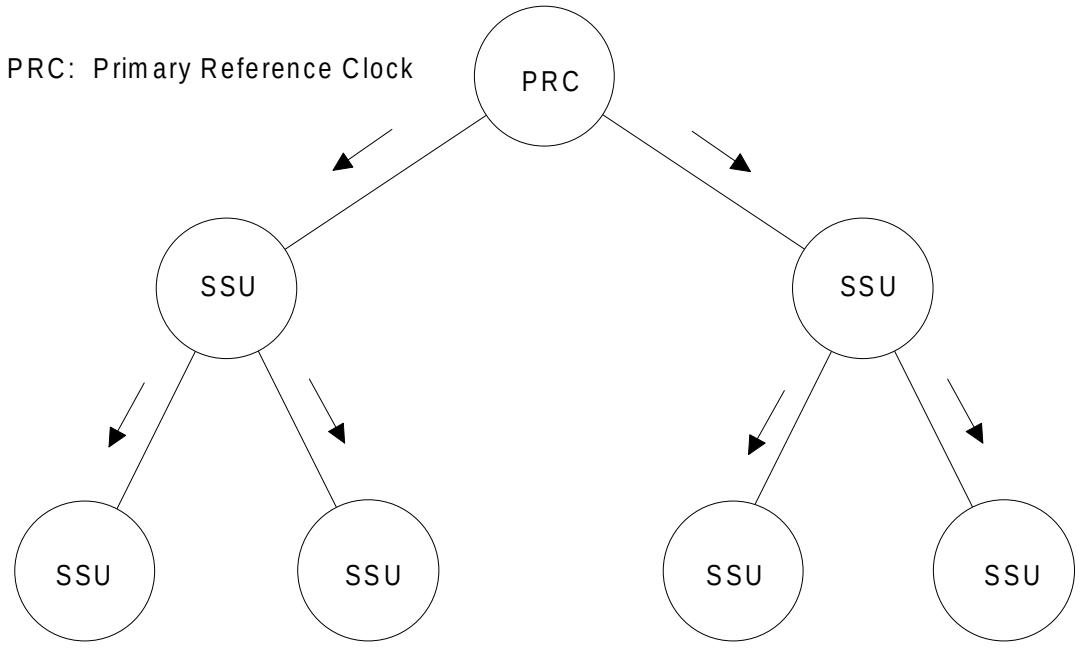


Figure 4: Synchronization network architecture for inter-node distribution

Clocks of a lower hierarchical level shall have a pull-in range which ensures that they can automatically acquire and lock to the timing signal generated by the same or higher level clock that they are using as a reference.

Phase reference information is transferred between synchronization nodes by means of a synchronization trail. When a trail becomes disabled then the node clock shall select another reference from a set of valid alternatives. When none exist, the node clock shall enter holdover mode.

The synchronization trail is provided by one or more synchronization link connections each supported by a synchronized primary or secondary rate PDH trail or a SDH multiplex section trail. When the distribution network is based on SDH, one or more link connections each supported by a multiplex section trail is recommended to conform to the requirement given in clause 4. The sub-network connections (switches) in the synchronization trail need to be set to maintain only valid hierarchical relationships between clocks. The algorithms for achieving this in SDH reference distribution networks are under study.

A synchronization link that distributes timing from the public network across a User Network Interface (UNI) should be timed from the SDH network element clock. The performance characteristics of this method and other techniques, such as deriving timing from the Tributary Unit - 12 (TU-12) within which the data signal is carried, are under study.

7 Synchronization modes

Four synchronization modes can be identified. These are:

- synchronous;
- pseudo-synchronous;
- plesiochronous;
- asynchronous.

In synchronous mode, all clocks in the network will be traceable to a single PRC. Pointer adjustments will only occur randomly. This is the normal mode of operation within a single operator's domain.

In pseudo-synchronous mode (see note), not all clocks in the network will have timing traceable to the same PRC. However, each PRC will comply with EN 300 462-6-1 [5] and, therefore, pointer adjustments will be generated in the network elements at the boundary between equipments synchronized to different PRC. This is the normal mode of operation for the international and inter-operator network.

NOTE: In a large single operator domain where more than one PRC is used, this mode of operation may be employed.

In plesiochronous mode, the synchronization trail and the fallback alternatives to one or more clocks in the network will have been disabled. The clock will enter holdover or free-run mode. If synchronization is lost to a gateway SDH network element performing asynchronous mapping, the frequency offset and drift of the clock will cause pointer adjustments persisting through the whole SDH network connection. If synchronization is lost to the last network element in the SDH network connection (or the penultimate network element in the case where the last one is slaved, e.g. consists of a loop-timed multiplexer), there will also be pointer adjustments to cater for at the SDH network output. However, if the synchronization failure occurs at an intermediate network element, this will not result in a net pointer movement at the final output gateway network element provided the input gateway network element remains synchronized to the same PRC. Pointer movement at the intermediate network element will be corrected by the next network element in the connection which is still synchronized.

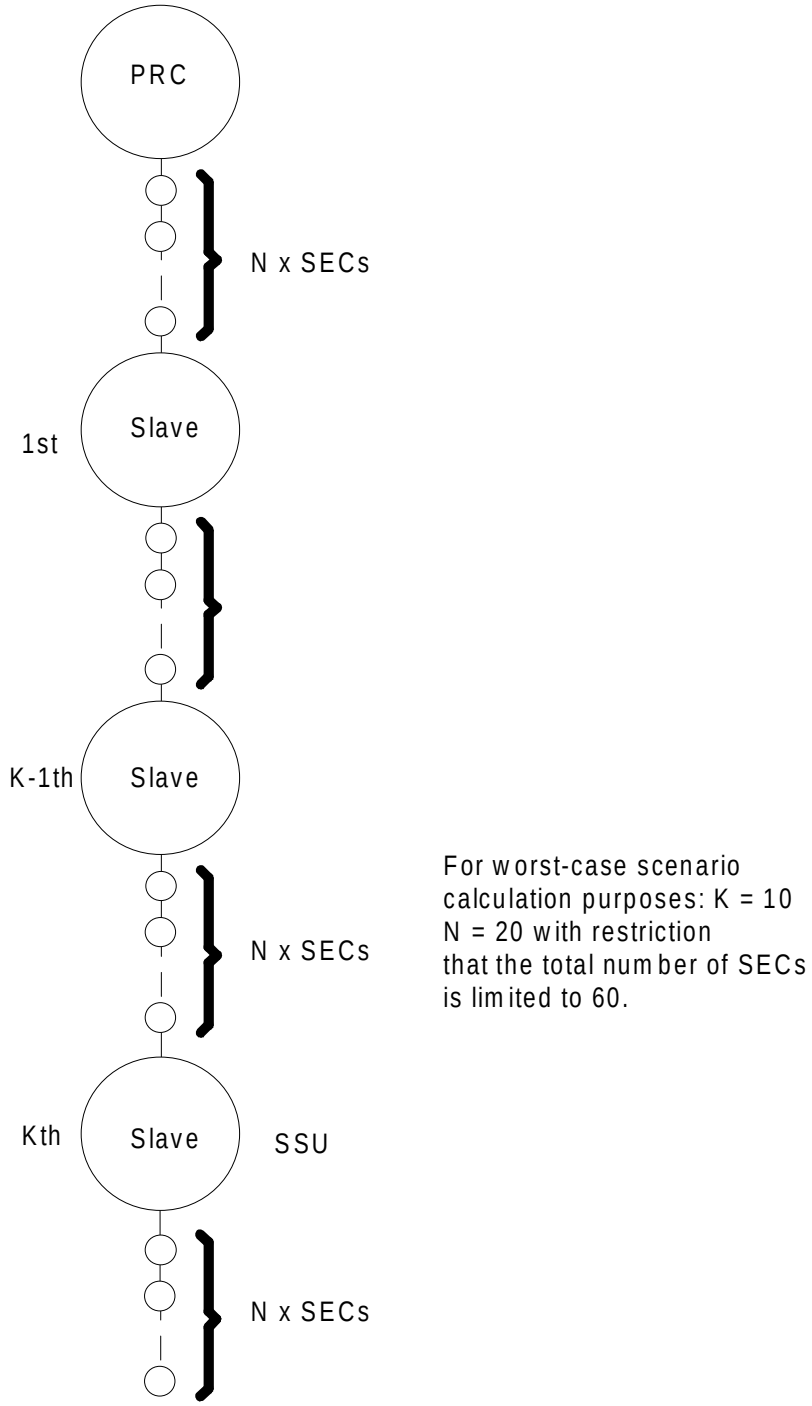
Asynchronous mode corresponds to the situation where large frequency offsets occur. The SDH network is not required to maintain traffic when the clock accuracy is less than that of a SEC. A clock accuracy of ±20 ppm is required to send an Alarm Indication Signal (AIS) (applicable for regenerators and any other SDH equipment where loss of all synchronization inputs implies loss of all traffic).

8 Synchronization network reference chain

The synchronization network reference chain is shown in figure 5 Timing is distributed via master-slave synchronization from the PRC to all clocks in the chain. The longest chain should not exceed K SSUs with up to N SECs interconnecting any two SSUs.

In general, the quality of timing will deteriorate as the number of synchronized clocks in tandem increases and hence for practical synchronization network design, the number of network elements in tandem should be minimized. However to determine synchronization clock requirements, the values for the worst case synchronization reference chain are K = 10, N = 20 with the total number of SECs limited to 60. The value of N is limited by the quality of timing required by the last network element in the chain and ensures the short term stability mask of EN 300 462-3-1 [2] is met.

The values of K and N have been derived from theoretical calculations and practical measurements are required for their verification.



NOTE: It is possible for the PRC to be conected directly to an SSU without an intervening SEC.

Figure 5: Synchronization network reference chain

9 Synchronization strategy

The synchronization strategy is to integrate SDH network synchronization with the existing PDH network synchronization architecture with the minimum of disruption and reconfiguration. Present node clocks are either separate units or integrated in the exchanges. With the introduction of SDH there is also the possibility to integrate the node clock in certain types of SDH equipment, typically in large SDH cross-connects. In that case the SDH network element has a SSU and not a SEC.

10 Synchronization network evolution

The SDH is designed to operate in pseudo-synchronous mode. The network elements can be integrated into existing synchronization hierarchies.

During the evolution of the network to SDH, the network synchronization plan will have to be altered to accommodate the SDH network elements. This requires careful planning to ensure that network synchronization is not jeopardized.

When SDH equipment is initially introduced, the gateway network element shall be timed from either the PRC or an existing SSU. This may require a new interface on the SSU. Timing within the SDH network should follow the master-slave approach.

Evolutionary scenarios with multiple SDH islands supporting the transport of a PDH payload are for further study.

If the SDH network introduction results in PDH islands, steps shall be taken so that synchronization links supported by primary rate PDH trails do not transit the SDH network. This requires a reconfiguration of the synchronization architecture since all synchronization links transiting the SDH network shall be supported on SDH multiplex section trails. This may require new interfaces on the SSUs and on the PRC.

Where a network is completely SDH based, the synchronization distribution will be determined solely by the synchronization network reference chain.

11 Synchronization network robustness

It is preferable if all SSUs and SECs are able to recover timing from at least two synchronization trails. The slave clock shall reconfigure to recover timing from an alternative trail if the original trail fails. Where possible synchronization trails should be provided over diversely routed paths.

In the event of a failure of synchronization distribution, all network elements will seek to recover timing from the highest hierarchical level clock source available. To effect this, both SSUs and SECs may have to reconfigure and recover timing from one of their alternate synchronization trails. This will ensure that a SEC rarely enters holdover or free-run mode. However, it may have to recover timing from a SSU which is itself in holdover if this is the highest hierarchical level source available to it. In order to indicate faults in the synchronization distribution network across non-SDH interfaces, the use of a squelching function may be required.

Within SDH sub-networks, timing is distributed between network nodes via a number of network elements with clocks of lower hierarchical level. A timing quality marking scheme is provided to allow selection and confirmation of the highest quality synchronization trail (including under synchronization failure conditions).

The quality marking scheme provides an indication of the quality of the timing using a status messaging approach. The status message is conveyed in the section overhead as described in ETS 300 147 [3]. For outputs used for timing distribution using status messaging, the status message shall reflect the selected reference.

Where timing quality markers are used in a meshed network, potential problems have been identified. It shall therefore be possible to restrict the links used for synchronization. Network synchronization planners are reminded that careful consideration is needed when using timing quality markers.

To provide an example of a reconfiguration, if the first network element from the PRC loses its synchronization trail from the PRC, it should reconfigure and accept timing from the SSU. This is shown in figure 6.

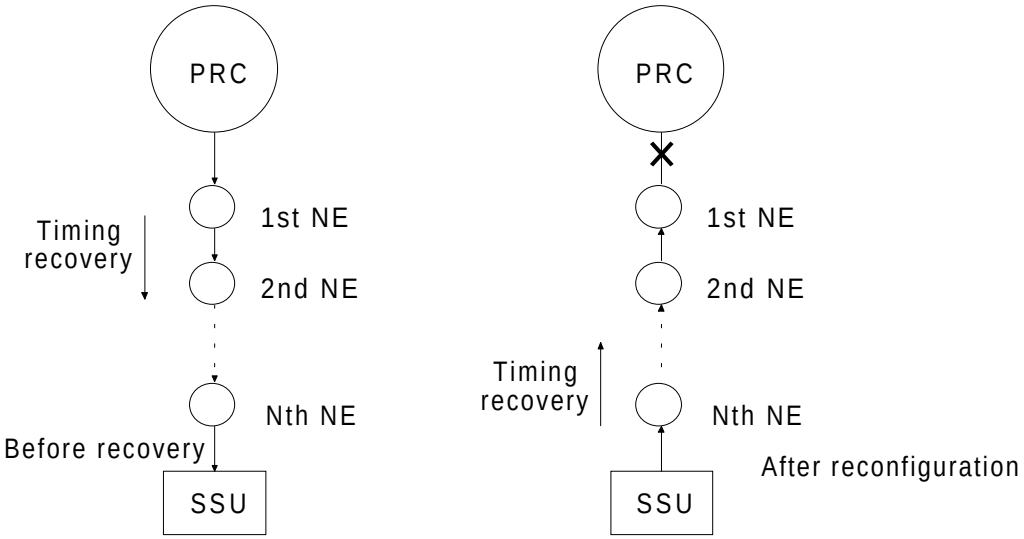


Figure 6: Reconfiguration example

History

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