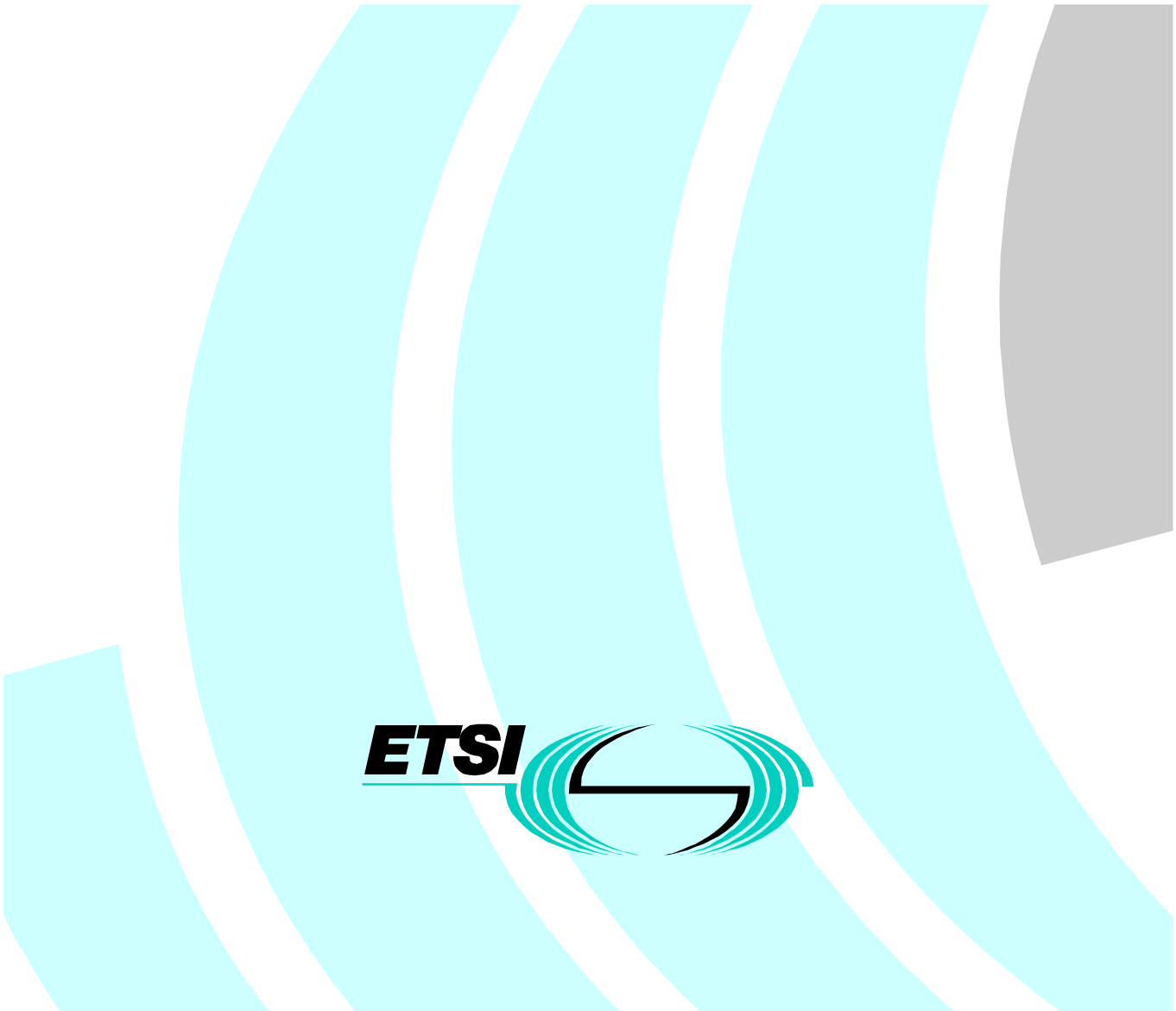
ETSI EN 300 420 V1.2.1 (2001-07)

European Standard (Telecommunications series)

Access and Terminals (AT);
2 048 kbit/s digital structured leased lines (D2048S);
Terminal equipment interface



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Contents

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Foreword

This European Standard (Telecommunications series) has been produced by ETSI Technical Committee Access and Terminals (AT).

The present document results from a mandate from the Commission of the European Community (CEC) to provide standards for the support of the Directive on Open Network Provision (ONP) of leased lines (92/44/EEC).

There are two other standards directly related to the present document:

- EN 300 418: "Access and Terminals (AT); 2 048 kbit/s digital unstructured and structured leased lines (D2048U and D2048S); Network interface presentation";
- EN 300 419: "Access and Terminals (AT); 2 048 kbit/s digital structured leased lines (D2048S); Connection characteristics".

The present document is based on information from ITU-T Recommendations and ETSI publications and the relevant documents are quoted where appropriate.

National transposition dates	
Date of adoption of this EN:	29 June 2001
Date of latest announcement of this EN (doa):	30 September 2001
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Date of withdrawal of any conflicting National Standard (dow):	31 March 2002

Introduction

The Council Directive on the application of ONP to leased lines (92/44/EEC) concerns the harmonization of conditions for open and efficient access to, and use of, the leased lines provided over public telecommunications networks, and the availability throughout the European Union (EU) of a minimum set of leased lines with harmonized technical characteristics.

The consequence of the Directive is that telecommunications organizations within the EU shall make available a set of leased lines between points in these countries with specified connection characteristics and specified interfaces.

Two categories (voluntary and regulatory) of standard were used for the interfaces of terminal equipment designed for connection to the ONP leased lines. Technical Basis for Regulations (TBRs) gave the earlier essential requirements under the Directive 91/263/EEC, later replaced by 98/13/EC, for attachment to the leased lines, whereas other voluntary standards (ETSs or ENs) gave the full technical specifications for these interfaces. This document, which is based on an earlier ETS, belongs to the second category.

The requirements of TBR 13 are a subset of the present document.

The present version of the present document has been produced to introduce some necessary changes.

ETS 300 166 and ITU-T Recommendations G.703 [1], G.704 [2] and G.706 were used as the basis for the terminal interface aspects of the present document.

1 Scope

The present document specifies the physical and electrical characteristics (except safety, over voltage and EMC aspects), the necessary functional characteristics and the corresponding test principles for a terminal equipment interface for connection to the Network Termination Points (NTPs) of Open Network Provision (ONP) 2 048 kbit/s digital structured leased lines using 120 Ω interfaces with an information transfer rate of 1 984 kbit/s without restriction on binary content.

The present document is to ensure that the interface of the terminal equipment is compatible with the ONP 2 048 kbit/s digital structured leased line. A terminal equipment interface that conforms to the present document will also be compatible with an ONP 2 048 kbit/s unstructured leased line. The present document is applicable to all interfaces designed for connection to the leased line, however in the cases of apparatus that carries a particular service, of complex apparatus and of apparatus in private networks, other requirements may apply in addition to the present document.

Customer premises wiring and installation between the terminal equipment and the NTP are outside the scope of the present document.

2 References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication and/or edition number or version number) or non-specific.
- For a specific reference, subsequent revisions do not apply.
- For a non-specific reference, the latest version applies.

[1] ITU-T Recommendation G.703 (1998): "Physical/electrical characteristics of hierarchical digital interfaces".

[2] ITU-T Recommendation G.704 (1998): "Synchronous frame structures used at 1 544, 6 312, 2 048, 8 448 and 44 736 kbit/s hierarchical levels".

[3] ITU-T Recommendation O.151 (1992): "Error performance measuring equipment operating at the primary rate and above".

[4] ITU-T Recommendation O.171 (1997): "Timing jitter and wander measuring equipment for digital systems which are based on the plesiochronous digital hierarchy (PDH)".

[5] ETSI EN 300 418: " Access and Terminals (AT); 2 048 kbit/s digital unstructured and structured leased lines (D2048U and D2048S); Network interface presentation".

[6] ETSI EN 300 419: "Access and Terminals (AT); 2 048 kbit/s digital structured leased lines (D2048S); Connection characteristics".

3 Definitions and abbreviations

3.1 Definitions

For the purposes of the present document, the following terms and definitions apply:

errored Sub-MultiFrame: Sub-MultiFrame (SMF) where the calculated Cyclic Redundancy Check-4 bit (CRC-4) does not correspond with the CRC-4 contained within the next SMF (see clause C.2.2)

frame: sequence of 256 bits of which the first 8 bits define the frame structure (see annex C)

leased lines: telecommunications facilities provided by a public telecommunications network that provide defined transmission characteristics between NTPs and that do not include switching functions that the user can control, (e.g. on-demand switching)

multiframe: sequence of two SMFs containing the multiframe alignment word (see annex C)

Network Termination Point (NTP): physical connections and their technical access specifications which form part of the public telecommunications network and are necessary for access to and efficient communication through that public network

PRBS(2^{15}-1): Pseudo Random Bit Sequence (PRBS) (as defined in clause 2.1 of ITU-T Recommendation O.151 [3])

S_a bits: bits 4 to 8 (bits S_{a4} to S_{a8}) in frames not containing the frame alignment signal (see annex C)

Sub-Multiframe (SMF): sequence of 8 frames, each of 256 bits, over which the CRC-4 is calculated (see annex C)

terminal equipment: equipment intended to be connected to the public telecommunications network, i.e.:

- to be connected directly to the termination of a public telecommunication network; or
- to interwork with a public telecommunications network being connected directly or indirectly to the termination of a public telecommunications network,

in order to send, process, or receive information.

3.2 Abbreviations

For the purposes of the present document, the following abbreviations apply:

AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
CRC-4	Cyclic Redundancy Check-4 bit
D2048S	2 048 kbit/s digital structured leased line
dc	direct current
EMC	ElectroMagnetic Compatibility
HDB3	High Density Bipolar code of order 3 (see annex B)
ISDN	Integrated Services Digital Network
NTP	Network Termination Point
ONP	Open Network Provision
ppm	parts per million
PRBS	Pseudo Random Bit Sequence
RAI	Remote Alarm Indication
rms	root mean square
RT	Requirements Table
RX	RX is a signal input (at either the terminal equipment interface or the test equipment, see figure 1)
SDH	Synchronous Digital Hierarchy
SMF	Sub-MultiFrame
TX	TX is a signal output (at either the terminal equipment interface or the test equipment, see figure 1)
UI	Unit Interval

4 Requirements

The terminal equipment interface is for use with 2 048 kbit/s structured leased lines that provide bi-directional, point-to-point digital connections with an information transfer rate of 1 984 kbit/s without restriction on binary content. Any structuring of the data within the transparent 1 984 kbit/s part of the frame is the responsibility of the user.

4.1 Physical characteristics

Currently no standardized connector is readily available. Consequently, the only method of connection that can be specified in the present document is the use of solid conductors of 0,4 mm to 0,6 mm. The present document requires the terminal equipment to be capable of presenting either a point for the attachment of unterminated solid conductors, or solid conductors themselves (see clause 4.1.1). It is a requirement that such a connection method be available to be provided for use with the terminal equipment if necessary.

In order to allow connection to be made using other methods (e.g. connectors), the terminal equipment is permitted to be supplied with a connection method suitable for use with those methods (see clause 4.1.2).

NOTE 1: The following are examples of arrangements that comply with the requirements. The list below should not be regarded as an exhaustive list of all permitted arrangements:

a) a cord, permanently connected to the terminal equipment at one end and unterminated at the other end, with wires that are solid conductors with diameters in the range 0,4 mm to 0,6 mm;

b) a cord, connected via a plug and socket to the terminal equipment at one end and unterminated at the other end, with wires that are solid conductors with diameters in the range 0,4 mm to 0,6 mm;

c) an insulation displacement connector, designed to accept wires with solid conductors with diameters in the range 0,4 mm to 0,6 mm, but with no cord;

d) a screw connector, designed to accept wires with solid conductors with diameters in the range 0,4 mm to 0,6 mm, but with no cord;

e) the arrangement in b) plus one or more additional alternative cords with the same plug or socket arrangement at the terminal end and any plug or socket at the other end;

f) the arrangement in c) or d) plus one or more cords suitable for connection to the terminal equipment at one end and any plug or socket at the other end.

The transmit pair is the output from the terminal equipment interface. The receive pair is the input to the terminal equipment interface, as shown in figure 1. Where the terms "output" and "input" are used without qualification in the present document, they refer to the terminal equipment interface.

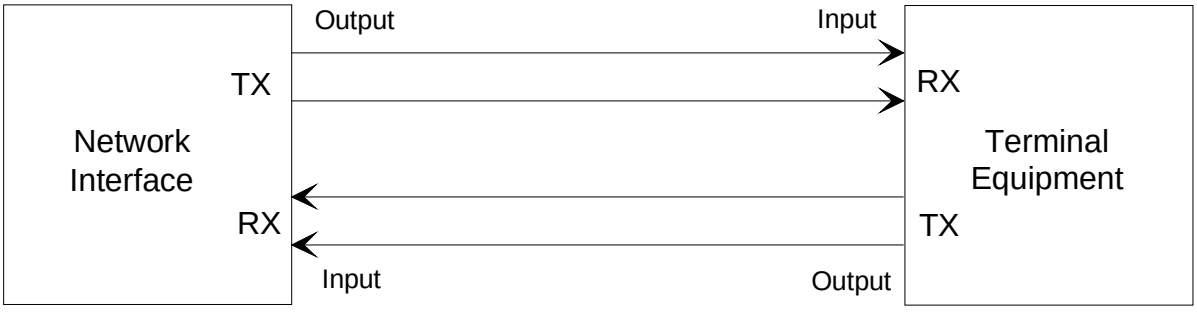


Figure 1

NOTE 2: The use of a shielded cord or cable may be necessary to meet radiation and immunity requirements defined in ElectroMagnetic Compatibility (EMC) standards.

4.1.1 Hardwired connection

Requirement: the terminal equipment shall provide:

a) a set of connection contacts (e.g. an insulation displacement connector or a screw terminal block) to which solid wire conductors with diameters in the range 0,4 mm to 0,6 mm may be connected; or

b) a wiring arrangement connected by any means to the terminal equipment, with unterminated solid wire conductors with diameters in the range 0,4 mm to 0,6 mm at the end distant from the terminal equipment.

Test: there is no test. All subsequent tests are carried out via the specified connection method.

4.1.2 Alternative means of connection

Any alternative means of connection may be provided in addition to the connection arrangements under clause 4.1.1.

4.2 Electrical characteristics

4.2.1 Output port

4.2.1.1 Signal coding

Requirement: the signal transmitted at the output port shall comply with the High Density Bipolar code of order 3 (HDB3) encoding rules (see annex B).

Test: the test shall be conducted according to clause A.2.1.

4.2.1.2 Waveform shape

Requirement: the pulse at the output port shall comply with the requirements given in table 1 and figure 2, based on ITU-T Recommendation G.703 [1].

Table 1: Waveform shape at output port

Pulse shape (nominally rectangular)	All marks of a valid signal shall conform to the mask (see figure 2) irrespective of the polarity. The value V corresponds to the nominal peak voltage of a mark.
Test load impedance	120 Ω non-reactive
Nominal peak voltage V of a mark	3 V
Peak voltage of a space	0 ± 0,3 V
Nominal pulse width	244 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0,95 to 1,05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0,95 to 1,05

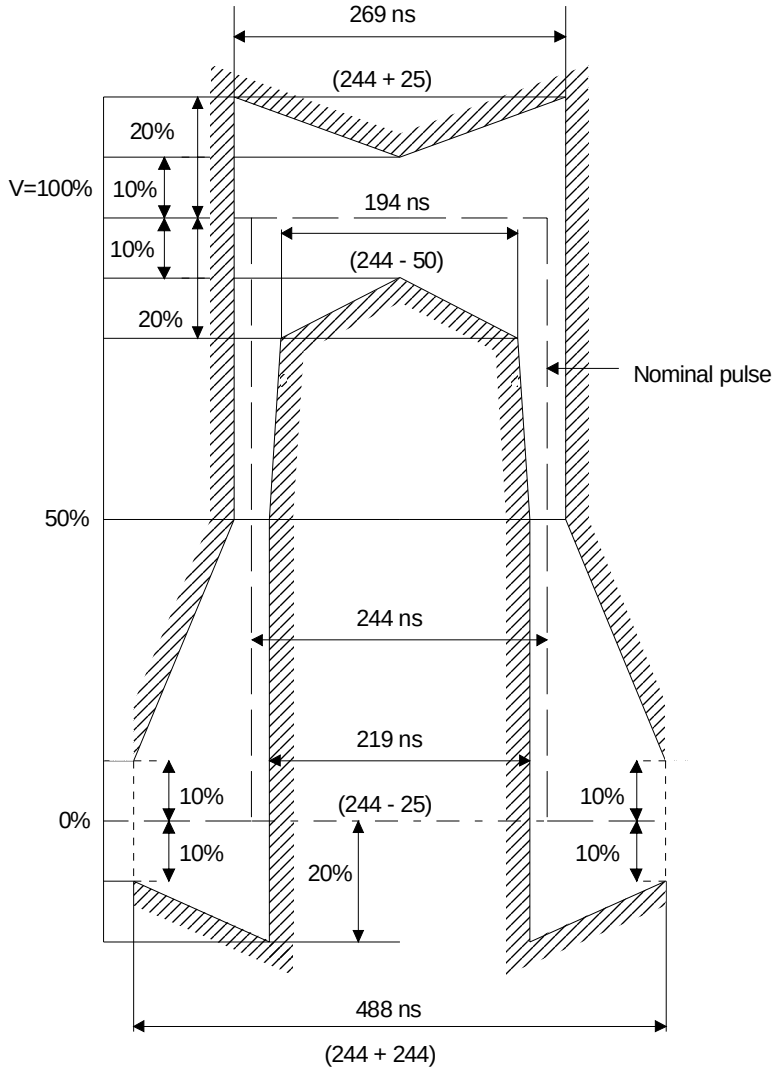


Figure 2: Pulse mask for 2 048 kbit/s pulse

Test: the test shall be conducted according to clause A.2.2.

4.2.1.3 Output timing

This requirement is such that the terminal equipment is capable of operating when connected to leased lines capable of carrying user timing within the range 2 048 kbit/s ±50 parts per million (ppm) and when connected to leased lines that provide timing that is synchronous to the network timing. For further information see annex E.

Requirement: the terminal equipment shall have:

a) an internal clock which shall provide a bit rate at the output port within the limits of 2 048 kbit/s ±50 ppm; and

b) the capability to provide a clock loop such that the signal timing at the output port is derived from the timing at the input port.

The terminal equipment may also have:

c) an external reference signal input from which the output timing may be derived.

Test: for case a) the test shall be conducted according to clause A.2.3. The capability to provide a clock loop, case b), and the derivation of a clock signal from an external reference signal input, case c), are covered by the test of clause A.2.8.

4.2.1.4 Impedance towards ground

Requirement: where the terminal equipment has a ground, the impedance towards ground of the output port shall be greater than 1 000 Ω for frequencies in the range 10 Hz to 1 MHz when measured with a sinusoidal test voltage of 2 V root mean square (rms). For the purpose of this requirement, ground shall be the terminal equipment common reference point or test reference point.

NOTE: This requirement is included to allow transformerless implementations.

Test: the test shall be conducted according to clause A.2.7.

4.2.1.5 Output jitter

Requirement: the peak-to-peak output jitter shall not exceed the limits of table 2 when measured with a band pass filter with linear cut-off with the defined cut-off frequencies. At frequencies below the lower 3 dB point, the attenuation of the high pass filter shall rise with a value equal to 20 dB per decade. At frequencies above the upper 3 dB point, the attenuation of the low pass filtration shall rise with a value greater than, or equal to, 60 dB per decade.

For the purpose of testing, any signal input from which the output timing is derived shall be provided with the maximum tolerable input jitter, and with the maximum tolerable input frequency deviation, as specified by the manufacturer.

Where the output timing of the terminal equipment is taken from the leased line, the input to the terminal equipment shall be provided with components of sinusoidal jitter at points on the curve of figure 3 and table 4.

NOTE: A separate requirement for output jitter at frequencies below 40 Hz is not required because the measurement filter with a first order lower cut-off will allow the jitter to have a spectrum whose amplitude rises at 20 dB/decade as the frequency reduces below 40 Hz. Where timing is taken from the leased line, the test uses input jitter frequencies from 20 Hz upwards.

Table 2: Maximum output jitter

Measurement filter bandwidth		Output jitter
Lower cut-off (high pass)	Upper cut-off (low pass)	Unit Interval (UI) peak-to-peak (maximum)
40 Hz	100 kHz	0,11 UI

Test: the test shall be conducted according to clause A.2.8.

4.2.1.6 Output return loss

There are no requirements for output return loss under the present document.

NOTE: A requirement for output return loss may be added to the present document when appropriate specifications become available.

4.2.1.7 Output signal balance

There are no requirements for output signal balance under the present document.

NOTE: The effects of the output signal imbalance are covered under the EMC Directive (89/336/EEC).

4.2.1.8 Output structure

Requirement: the bit stream transmitted at the output of the terminal equipment shall be structured as defined in clause C.1.

Test: the test shall be conducted according to clause A.2.9.1.

4.2.1.8.1 CRC-4

Requirement: the CRC-4 bits transmitted at the output of the terminal equipment shall be as defined in tables C.1 and C.2 and clause C.2.1 of annex C and shall correspond to the data transmitted at the output of the terminal equipment.

Test: the test shall be conducted according to clause A.2.9.1.

4.2.1.8.2 Use of the E-bits

The terminal equipment shall comply either with clause 4.2.1.8.2.1 or clause 4.2.1.8.2.2.

4.2.1.8.2.1 Terminals not using the E-bits

This clause is applicable to those terminal equipments which do not use the E-bits to indicate errored SMFs.

Requirement: both E-bits transmitted at the output of the terminal equipment shall be set to binary ONE in all instances.

Test: the test shall be conducted according to clause A.2.9.2.

4.2.1.8.2.2 Terminals using the E-bits to indicate errored SMFs

This clause is applicable to those terminal equipments which use the E-bits to indicate errored SMFs.

Requirement: the E-bits transmitted at the output of the terminal equipment shall indicate errored SMFs in the input bit stream. One E-bit in a multiframe shall be set to binary ZERO for each errored SMF received in the input bit stream. The E-bits corresponding to non-errored SMFs shall be set to binary ONE. Any delay between the detection of an errored SMF and the setting of the E-bit that indicates the errored SMF shall be less than 1 second.

Test: the test shall be conducted according to clause A.2.9.3.

4.2.1.8.3 Use of the A-bit

The terminal equipment shall comply either with clause 4.2.1.8.3.1 or clause 4.2.1.8.3.2.

4.2.1.8.3.1 Terminals not using the A-bit

Requirement: the A-bit transmitted at the output of the terminal equipment shall be set to binary ZERO in all instances.

Test: the test shall be conducted according to clause A.2.9.4.

4.2.1.8.3.2 Terminals using the A-bit

Requirement: the A-bit transmitted at the output of the terminal equipment shall be set to binary ZERO in normal operation but may be changed from binary ZERO to binary ONE within 30 ms of any of the following conditions occurring in the input bit stream:

a) three consecutive incorrect frame alignment signals, (the correct frame alignment signal is defined in table C.1);

b) there being = 915 errored SMFs out of 1 000 SMFs.

The terminal may also change the A-bit from binary ZERO to binary ONE within 30 ms of:

c) bit 2 in frames not containing the frame alignment signal being in error (i.e. bit 2 is a binary ZERO) on three consecutive occasions.

For a terminal equipment recovering from loss of frame alignment (i.e. the A-bit set to binary ONE) the A-bit transmitted at the output of the terminal equipment shall be set from binary ONE to binary ZERO within 30 ms of any of the following conditions occurring in the input bit stream:

d) for the first time, the presence of the correct frame alignment signal (as defined in table C.1); and

e) the absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a binary ONE; and

f) for the second time, the presence of the correct frame alignment signal in the next frame.

Test: the test shall be conducted according to clause A.2.9.4.

4.2.1.8.4 Use of the S_a bits

There is no requirement on the value or setting of the S_a bits at the output of the terminal equipment.

4.2.2 Input port

4.2.2.1 Signal coding

Requirement: the input port shall decode without error HDB3 encoded signals in accordance with HDB3 encoding rules (see annex B).

Test: the test shall be conducted according to clause A.2.6.

4.2.2.2 Input return loss

Requirement: the input return loss with respect to 120 Ω at the interface shall be greater than or equal to the values given in table 3, which is taken from clause 9.3 of ITU-T Recommendation G.703 [1].

Table 3: Input port minimum return loss

Frequency range	Return loss
51 kHz to 102 kHz	12 dB
102 kHz to 2 048 kHz	18 dB
2 048 kHz to 3 072 kHz	14 dB

Test: the test shall be conducted according to clause A.2.4.

4.2.2.3 Input loss tolerance

Requirement: the input port shall decode without errors a 2 048 kbit/s signal as defined in clauses 4.2.1.1 and 4.2.1.2 above but modified by a cable or artificial cable with the following characteristics:

a) attenuation that follows a $\sqrt{f}$ law with values throughout the range 0 to 6 dB at 1 024 kHz; and

b) characteristic impedance of 120 Ω with a tolerance of ±20 % in the frequency range from 200 kHz up to, but not including, 1 MHz, and ±10 % at 1 MHz.

Test: the test shall be according to clause A.2.5.

4.2.2.4 Immunity against reflections

Requirement: when a signal comprising a combination of a normal signal and an interfering signal is applied to the input port, via an artificial cable with a loss in the range 0 dB to 6 dB at 1 MHz, no errors shall result due to the interfering signal.

The normal signal shall be a signal encoded according to HDB3, shaped according to the mask of figure 2, with a binary content in accordance with a PRBS(2^{15}-1).

The interfering signal shall be the same as the normal signal except that the level is attenuated by 18 dB, the bit rate is within 2 048 kbit/s ±50 ppm and the timing shall not be synchronized to the normal signal.

Test: the test shall be conducted according to clause A.2.5.

4.2.2.5 Tolerable longitudinal voltages

Requirement: the receiver shall operate without errors with any input signal in the presence of a longitudinal voltage of magnitude 2 V rms over the frequency range 10 Hz to 30 MHz.

NOTE: This requirement is included to allow transformerless implementations.

Test: the test shall be conducted according to clause A.2.6.

4.2.2.6 Impedance towards ground

Requirement: where the terminal equipment has a ground, the impedance towards ground of the input port shall be greater than 1 000 Ω for frequencies in the range 10 Hz to 1 MHz when measured with a sinusoidal test voltage of 2 V rms. For the purpose of this requirement, ground shall be the terminal equipment common reference point or test reference point.

NOTE: This requirement is included to allow transformerless implementations.

Test: the test shall be conducted according to clause A.2.7.

4.2.2.7 Input jitter tolerance

Requirement: the terminal equipment shall tolerate at its input port the maximum input jitter as shown in table 4 and figure 3.

NOTE: Terminal equipment with more than one input will normally need to be designed with a wander buffer of at least 18 µs, however, to accommodate the wander that may be produced by Synchronous Digital Hierarchy (SDH) networks, up to 40 µs may be needed.

Table 4: Input jitter tolerance

Peak-to-peak amplitude (UI)		Frequency (Hz)			
A1	A2	f1	f2	f3	f4
1,5	0,2	20	2 400	18 000	100 000

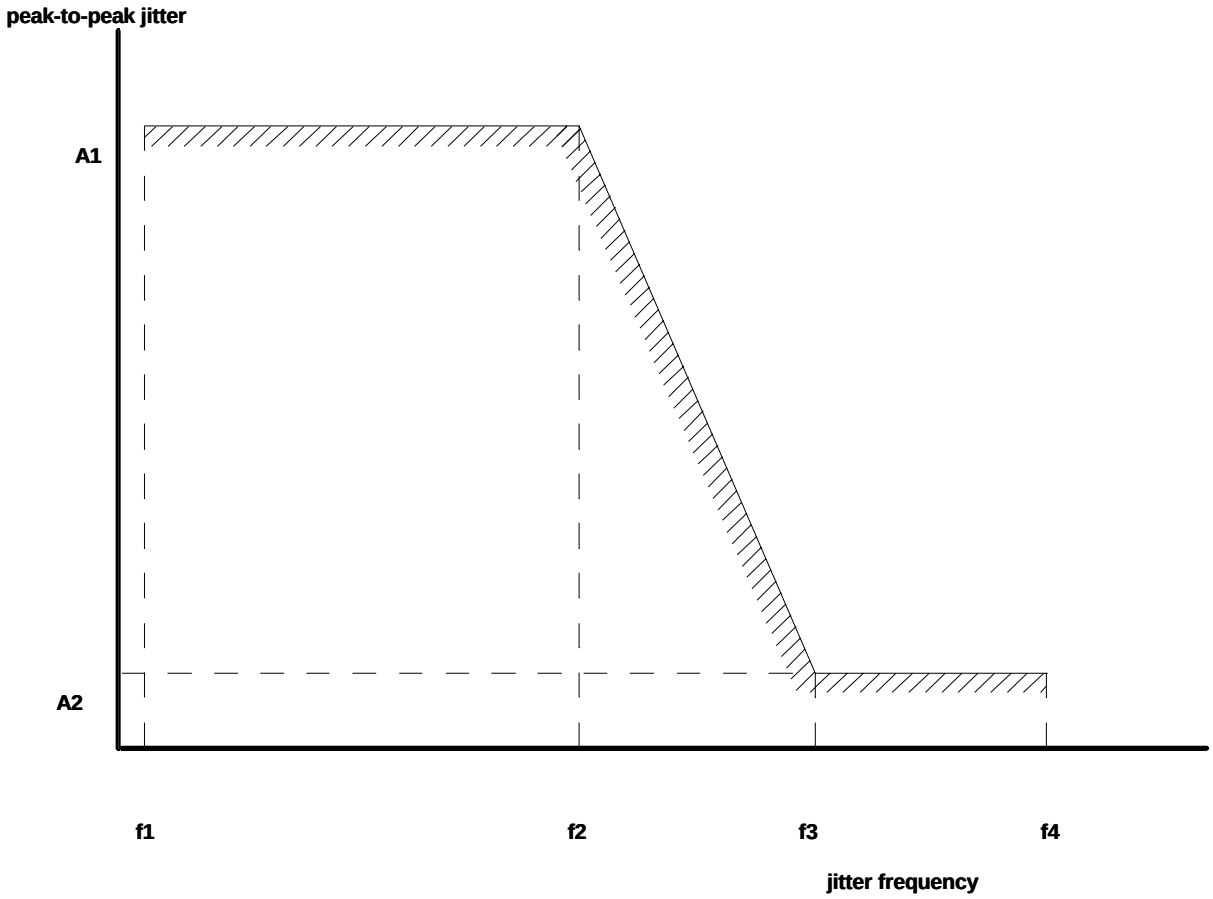


Figure 3: Input jitter tolerance

Test: the test shall be conducted according to clause A.2.8.

4.2.2.8 Input clock tolerance

Requirement: the terminal equipment shall decode without error HDB3 encoded signals over the frequency range 2 048 kbit/s ±50 ppm.

Test: the test shall be conducted in accordance with clause A.2.8.

4.2.2.9 Input frame structure

4.2.2.9.1 Frame alignment

Requirement: the input port shall accept an input bit stream with a frame and multiframe structure as defined in annex C. The terminal equipment shall be capable of achieving frame alignment in order to separate the user data from the frame information.

Frame alignment shall be achieved following:

a) for the first time, the presence of the correct frame alignment signal; and

b) the absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a binary ONE; and

c) for the second time, the presence of the correct frame alignment signal in the next frame, provided that the data does not contain any simulated frame alignment words.

The terminal equipment shall continue to maintain frame alignment in the event of receiving one or two consecutive incorrect frame alignment signals. On receipt of three consecutive incorrect frame alignment signals the terminal equipment shall consider frame alignment to have been lost and initiate a search for frame alignment.

Frame alignment may also be considered to have been lost following:

d) the occurrence of = 915 errored SMFs out of 1 000 SMFs; or

e) bit 2 in frames not containing the frame alignment signal being in error on three consecutive occasions; or

f) the inability to achieve multiframe alignment within 8 ms (see clause 4.2.2.9.2).

Test: the test shall be conducted in accordance with clause A.2.10.1.

4.2.2.9.2 Multiframe alignment

This requirement is optional and applies only to those terminal equipments needing to obtain multiframe alignment in order to extract CRC-4 information in order to comply with clause 4.2.1.8.2.2.

Requirement: CRC-4 multiframe alignment shall be achieved if at least two valid CRC-4 multiframe alignment signals can be located within 8 ms (the time separating two CRC-4 multiframe alignment signals being 2 ms or a multiple of 2 ms). If multiframe alignment cannot be achieved within 8 ms it shall be assumed that frame alignment is due to a spurious frame alignment signal and a research for frame alignment shall be initiated.

NOTE: The research for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Test: the test shall be conducted in accordance with clause A.2.10.2.

4.3 Safety

Requirements for safety are outside the scope of the present document.

Safety standards are published by CENELEC.

NOTE 1: An example of such a CENELEC product safety standard is EN 60950 (see annex F).

NOTE 2: For safety categories of interfaces, see EG 201 212. This document is also available from CENELEC as ROBT-002.

NOTE 3: Designers should take into account the minimum impedance towards ground specified in the present document.

4.4 Over voltage

Over voltage aspects are outside of the scope of the present document.

4.5 ElectroMagnetic Compatibility (EMC)

EMC requirements are outside the scope of the present document.

Annex A (normative): Test methods

A.1 General

This annex describes the test principles to determine the compliance of a terminal equipment against the requirements of the present document.

It is outside the scope of the present document to identify the specific details of the implementation of the tests.

A terminal equipment may be designed for through-connecting and may fulfil the electrical requirements only if through-connected. In these cases the requirements of the present document are valid and the tests shall be carried out with the through-connection terminated as specified by the manufacturer.

Details of test equipment accuracy and the specification tolerance of the test devices are not included in all cases. Where such details are provided they shall be complied with, but the way they are expressed shall not constrain the method of implementing the test.

NOTE: Attention is drawn to the issue of measurement uncertainty which may be addressed in future documents. Not all the required test results make allowance for spurious events during testing (e.g. errors due to EMC effects), which may make it necessary to repeat a test.

The test configurations given do not imply a specific realization of test equipment or test arrangement, or the use of specific test devices for conformance testing. However, any test configuration used shall provide those test conditions specified under "interface state", "stimulus" and "monitor" for each individual test.

The test equipment shall be a device, or a group of devices, that is capable of generating a stimulus signal conforming to the present document and capable of monitoring the signal received from the interface.

A.1.1 Additional information to support the test

The following facilities shall be provided by the terminal equipment interface under test:

a) an ability to configure the terminal equipment such that it provides a transparent loopback of the input to the output; and

b) an ability to transmit a given bit pattern, e.g. PRBS(2^{15}-1), within the 1 984 kbit/s user channel.

Where a) or b) cannot be provided, the terminal equipment supplier shall provide an alternative means of performing the test.

NOTE: Where terminals equipments use the E-bits to indicate errored SMFs, this may be used as an alternative to a transparent loopback in order to determine if data at the input has been correctly received.

A.1.2 Equipment connection

The tests in the present document shall be carried out using the connection method suitable for use with unterminated solid conductors as defined in clause 4.1.1. However, in the case of the tests specified in clauses A.2.2, A.2.4 and A.2.7, an alternative method of connection may be provided by the terminal equipment supplier for test purposes. In this case, this method of connection shall be used for these tests because the requirement considers any wiring to be part of the installation cabling.

NOTE: This alternative method of connection is for test purposes only and has been introduced because the characteristics tested in clauses A.2.2, A.2.4 and A.2.7 are based on ITU-T Recommendation G.703 [1] which makes no allowance for additional wiring. This alternative method may not be the same as the alternative method of connection referred to in clause 4.1 which is for operational use.

A.2 Test methods

One test may cover more than one requirement. The scope of each test is defined under the heading "purpose".

A.2.1 Signal coding at the output port

Purpose: to verify that the signal coding at the terminal equipment output port complies with the HDB3 coding rules as required by clause 4.2.1.1.

Test configuration (see figure A.1):

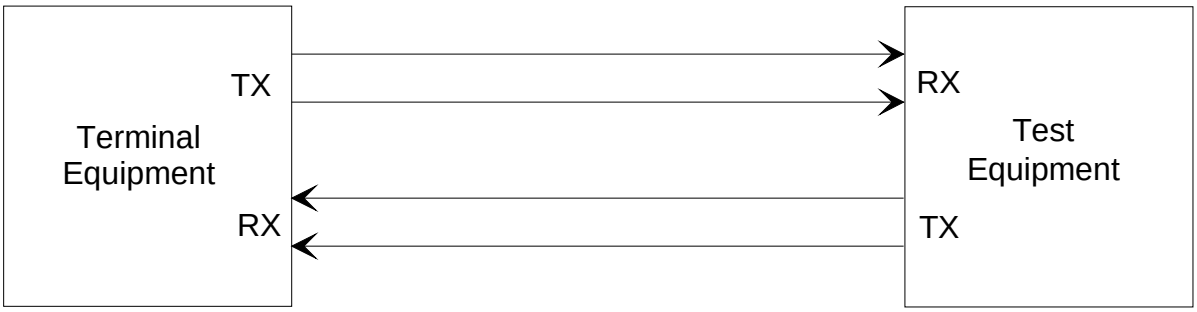


Figure A.1: Signal coding

Interface state: powered.

Stimulus: the terminal equipment shall transmit a HDB3 bit stream according to the frame structure of annex C. The binary content of the data contained in bits 9 to 256 of the frame shall be a bit stream including the sequences <0000><even number of binary ONEs><0000> and <0000><odd number of binary ONEs><0000>, where 0 = space and 1 = mark input to the HDB3 encoder, (see note).

Monitor: the output bit stream for a test period of sufficient time to allow transmission of 100 occurrences of the above patterns plus the latency period of the error detection mechanism.

Results: there shall be no errors in the decoded bit stream.

NOTE: A pseudo random bit stream, e.g. PRBS(2^{15}-1), will be acceptable if the bit patterns of the above clause are included in the bit stream.

A.2.2 Waveform shape at output port

Purpose: to verify conformance of the output waveform shape with the requirements of clause 4.2.1.2.

Test configuration (see figure A.2):

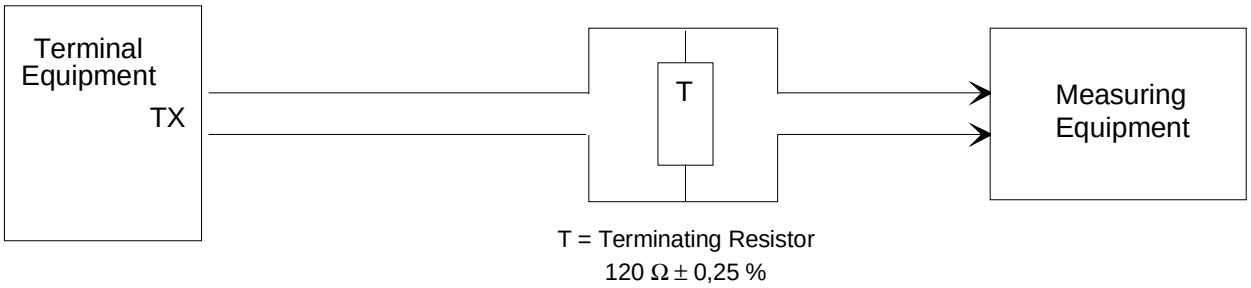


Figure A.2: Waveform shape at output port

Interface state: powered.

Stimulus: undefined.

Monitor:

- marks and spaces transmitted by the terminal equipment, measuring the amplitude and shape of positive and negative pulses (measured at the centre of the pulse interval) and the time duration of positive and negative pulses (measured at the nominal half of the pulse amplitude, i.e. 1,5 V);
- the overall measurement accuracy shall be better than 90 mV. All the measurements shall be performed using measuring equipment capable of recording direct current (dc). A bandwidth of 200 MHz or greater shall be used to ensure the capture of over or undershoot of the pulse.

Results:

- both positive and negative pulses shall be within the mask of figure 2, where V = 100 % shall be 3 V;
- the bit interval corresponding to a space shall not present voltages higher than ±0,3 V;
- the ratio between the amplitude of positive and negative pulses shall be contained in the range from 0,95 to 1,05;
- the ratio between the pulse widths of positive and negative pulses shall be in the range from 0,95 to 1,05.

A.2.3 Output timing

Purpose: to verify the bit rate is within the limits of 2 048 kbit/s ±50 ppm when the terminal equipment is generating timing from an internal clock, clause 4.2.1.3.

Test configuration (see figure A.3):

- the terminal equipment shall be configured to provide output timing from the internal clock source. The terminal equipment output shall be any HDB3 encoded bit stream.

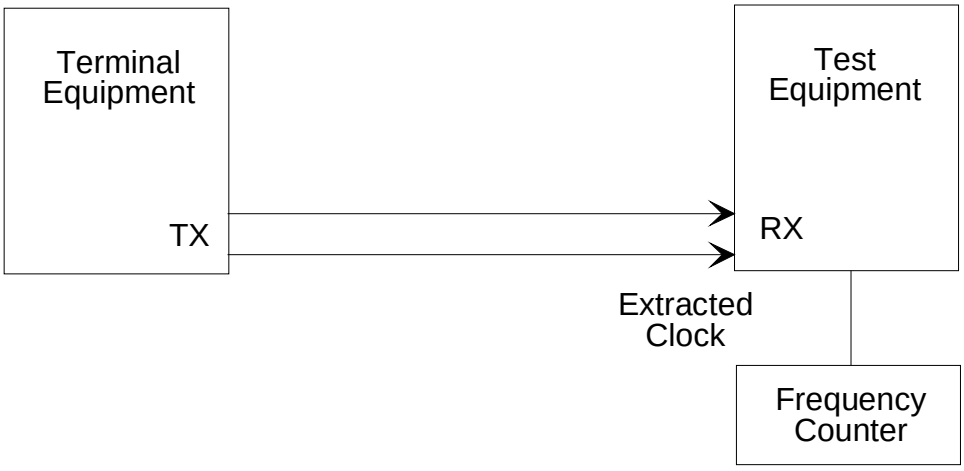


Figure A.3: Output timing

Interface State: powered.

Stimulus: undefined.

Monitor: the bit rate from the terminal equipment output port.

Results: the bit rate shall be within the limits of 2 048 kbit/s ±50 ppm.

A.2.4 Return loss at input port

Purpose: to verify that the return loss of the receive pair of the terminal equipment interface complies with the requirements of clause 4.2.2.2.

Test configuration (see figure A.4):

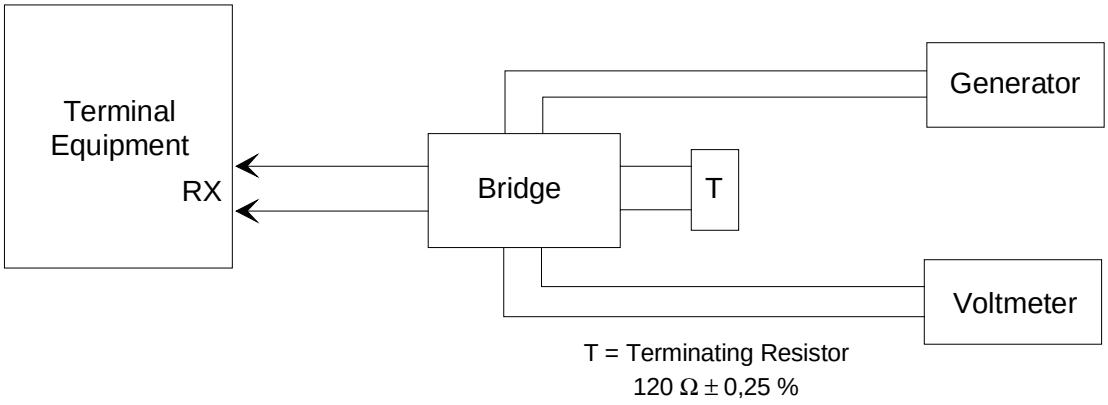


Figure A.4: Return loss at input port

Interface state: powered.

Stimulus: sinusoidal signal of 3 V peak at the input to the terminal equipment with a frequency variable between 51 kHz and 3 072 kHz.

Monitor: voltage measured across the bridge, representing a terminating resistor of 120 Ω, using a selective voltmeter with a bandwidth of less than 1 kHz.

Results: the measured return loss shall be greater than or equal to the values in table 3 of clause 4.2.2.2.

NOTE: The characteristics of the generator and of the voltmeter may be different depending on the implementation of the bridge, however, the total error of the test set-up should be less than 0,5 dB in the range between 10 dB and 20 dB. When connected to a 120 Ω ±0,25 % resistor the measured return loss of the bridge should be 20 dB higher than the limits specified for the interface.

A.2.5 Input loss tolerance and immunity against reflections

Purpose: to check the input port immunity against an interfering signal combined with the input signal, as specified in clause 4.2.2.4, both without cable (i.e. 0 dB attenuation loss) and with a cable attenuation of 6 dB, as specified in clause 4.2.2.3.

Test configuration (see figure A.5):

- the interfering signal shall be combined with the main signal in a combining network of impedance 120 Ω, with zero dB loss in the main path and an attenuation in the interference path of 18 dB;
- the cable simulator shall have an attenuation of 6 dB measured at 1 024 kHz and an attenuation characteristic that follows a ^1f law over the frequency range 100 kHz to 10 MHz;
- the conformance of the interface shall be verified in the following test conditions:
    a) without cable simulator and without interfering signal; and
    b) with cable simulator and without interfering signal; and
    c) without cable simulator and with interfering signal; and
    d) with cable simulator and with interfering signal.
- the test shall be repeated with the wires at the terminal equipment interface input (RX) reversed.

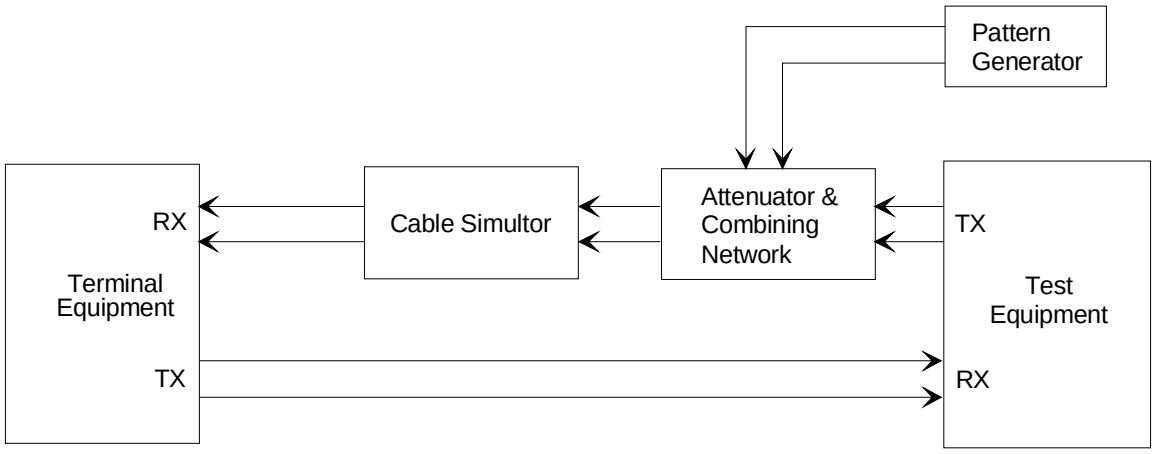


Figure A.5: Immunity against reflections

Interface state: powered, with received data looped back to the output port.

Stimulus:

- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document. The bit stream shall be structured into frames, with the CRC-4, according to ITU-T Recommendation G.704 [2]. Within the frames not containing the frame alignment signal, bit 3 (Remote Alarm Indication (RAI)) shall be set to 0 and bits 4 to 8 (S_{a4} to S_{a8}) shall be set to 1. The binary content of the data contained in bits 9 to 256 of the frame shall be a PRBS(2^{15}-1). The bit rate shall be within the limits 2 048 kbit/s ±50 ppm;
- the interfering signal from the pattern generator shall:

  a) be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document; and

  b) have a binary content with a PRBS(2^{15}-1); and

  c) have a bit rate within the limits 2 048 kbit/s ±50 ppm, not synchronized to the output signal of the test equipment.

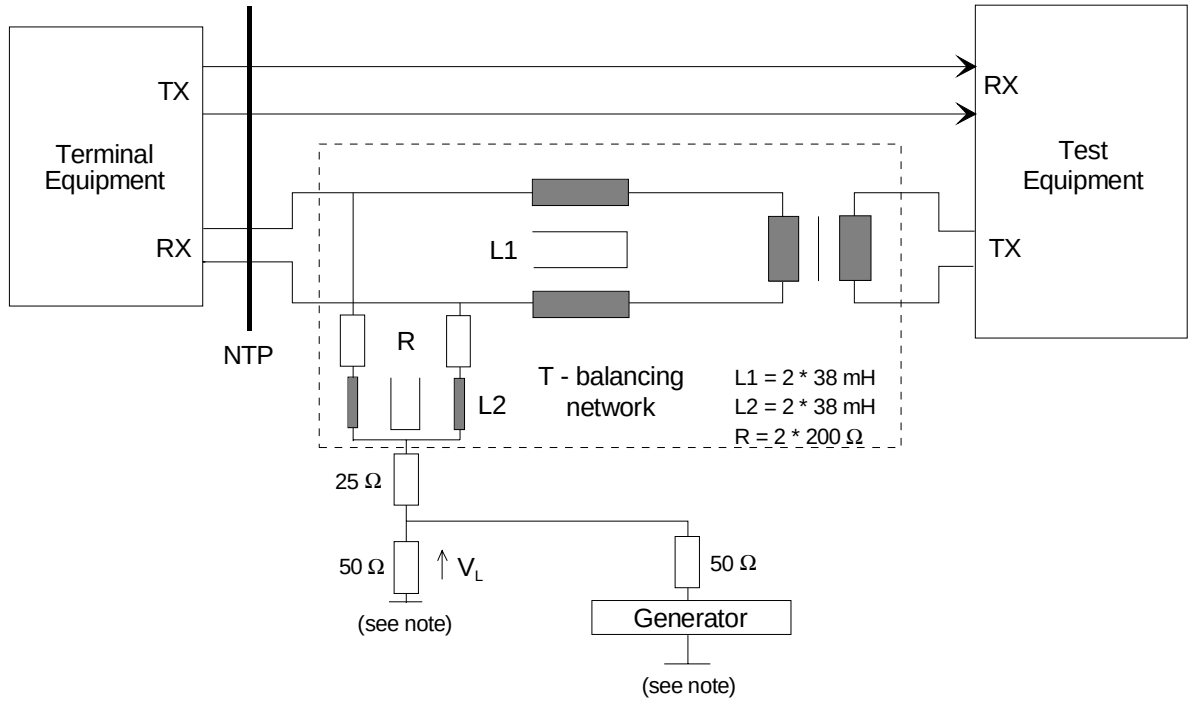
Monitor: data at output port of the terminal equipment.

Results: verify that the data received from the equipment under test is identical with the generated sequence for a period of at least one minute.

A.2.6 Tolerable longitudinal voltage, HDB3 input coding

Purpose: to check minimum tolerance to longitudinal voltages at the input of the terminal equipment, as specified in clause 4.2.2.5, and correct recognition of HDB3 code, as specified in clause 4.2.2.1.

Test configuration (see figure A.6):



NOTE: This point shall be connected to the terminal equipment common reference point or to the equipment test reference point.

Figure A.6: Tolerable longitudinal voltage and HDB3 input coding

Interface state: powered, with received data looped back to the output port of the terminal equipment.

Stimulus:

- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document. The bit stream shall be structured into frames, with the CRC-4, according to ITU-T Recommendation G.704 [2]. Within the frames not containing the frame alignment signal, bit 3 (RAI) shall be set to 0 and bits 4 to 8 (S_{a4} to S_{a8}) shall be set to 1. The binary content of the data contained in bits 9 to 256 of the frame shall be a PRBS(2^{15}-1);
- a longitudinal voltage V_L of 2 V rms, ±20 mV with a frequency variable between 10 Hz and 30 MHz shall be applied for a minimum of 2 seconds.

Monitor: data at output port of the terminal equipment.

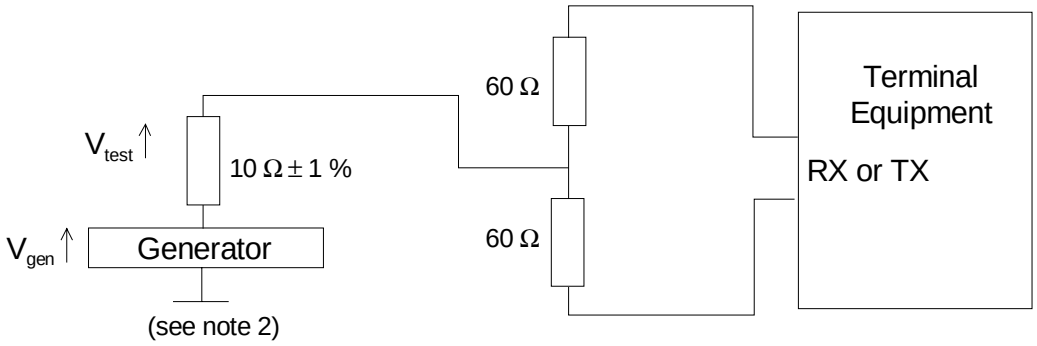
Results: verify that the data received from the equipment under test is identical with the generated sequence.

NOTE: The inherent longitudinal conversion loss of the T-balancing network should be greater than 30 dB.

A.2.7 Impedance towards ground

Purpose: to check terminal equipment input and output ports impedance towards ground, as specified in clauses 4.2.1.4 and 4.2.2.6.

Test configuration (see figure A.7):



NOTE 1: The 60 Ω resistors should be within 1 % and matched to better than 0,1 %.
NOTE 2: This point shall be connected to the terminal equipment common reference point or to the equipment test reference point.

Figure A.7: Impedance towards ground

Interface state: powered.

Stimulus: sinusoidal test signal (V_{gen}) of 2 V rms, ±20 mV applied over the frequency range 10 Hz to 1 MHz.

Monitor: voltage of V_{test}.

Results: voltage V_{test} shall be less than 19,2 mV rms.

A.2.8 Input and output jitter

Purpose: this test is used to measure tolerance to input jitter (clause 4.2.2.7), maximum output jitter (clause 4.2.1.5) and operation over the specified timing input range (clause 4.2.2.8).

NOTE: Further information on the measurement of jitter can be found in ITU-T Supplement number 3.8, Fascicle IV.4 (1988).

Test Configuration (see figure A.8):

- the terminal equipment shall be tested in each of the following configurations (where these modes of operation are supported):

  a) output timing referenced to the internal clock; and

  b) output timing referenced to any external clock source from which timing can be derived (including derivation from the input signal).

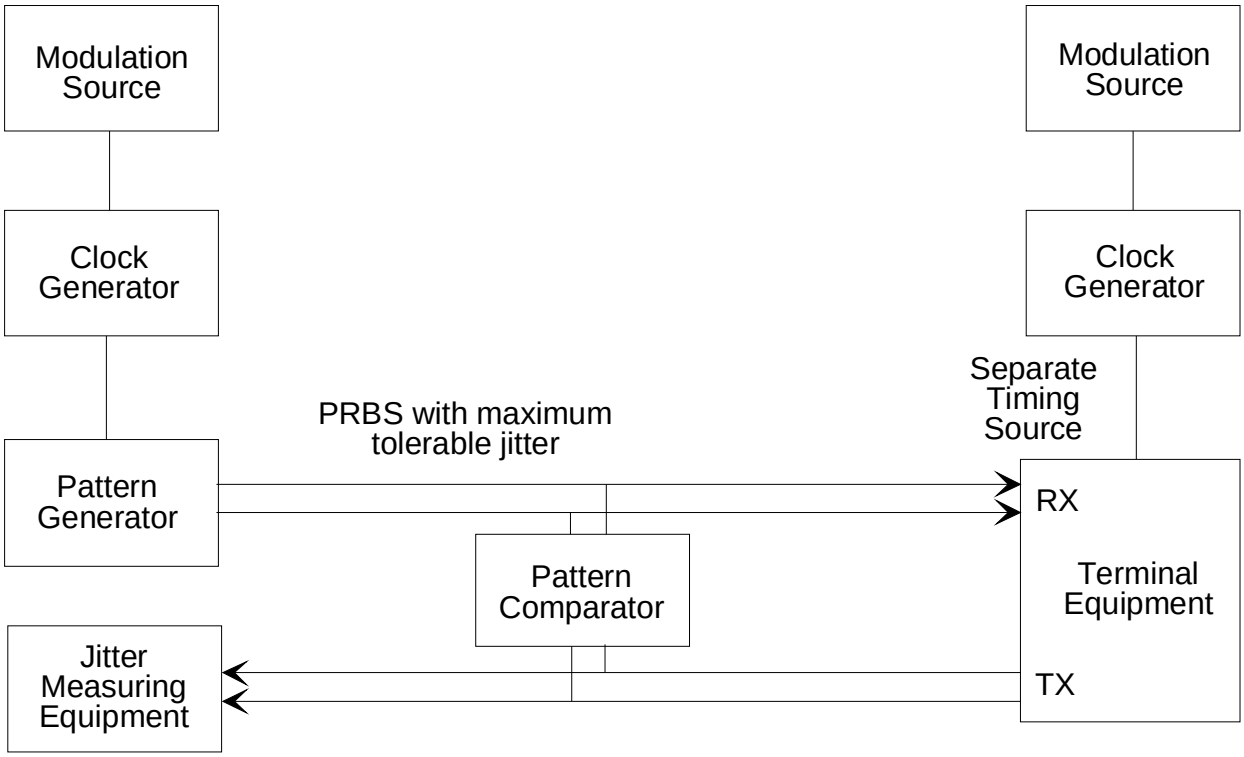


Figure A.8: Jitter measurement

Interface state: powered, with received data looped back to the output port.

Stimulus:

- the output signal of the pattern generator shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document. The bit stream shall be structured into frames, with the CRC-4, according to ITU-T Recommendation G.704 [2]. Within the frames not containing the frame alignment signal, bit 3 (RAI) shall be set to 0 and bits 4 to 8 (S_{a4} to S_{a8}) shall be set
  to 1. The binary content of the data contained in bits 9 to 256 of the frame shall be a PRBS(2^{15}-1);

- measurements shall be made with both the input signals at the digital rate limits and between these limits, sufficient to verify jitter compliance over the specified frequency range. As a minimum the test shall be performed at the upper and lower limits and at the nominal rate;

- the modulation source for the terminal equipment input bit stream shall generate individual components of sinusoidal jitter at points on the curve of figure 3 and table 4;

- the modulation source for the external timing (if needed) shall be independent from that for the input signal and shall generate the maximum tolerable jitter, and maximum frequency deviation, as specified by the manufacturer of the terminal equipment;

- it may be necessary to synchronize the two clock generators to avoid a high occurrence of slips.

Monitor:

a) the signal transmitted by the terminal equipment; and

b) the jitter extracted from this signal, using equipment complying with ITU-T Recommendation O.171 [4], with defined cut-off frequencies as shown in table 2 of the present document.

Results:

a) there shall be no bit errors reported by the test equipment within the period of the test; and

b) the peak-to-peak jitter shall comply with table 2 when measured with linear filters with the defined cut-off frequencies.

NOTE: The modulation source may be included in the clock generator and/or the pattern generator, or it may be provided separately.

A.2.9 Frame structure

A.2.9.1 Output structure and CRC-4 generation

Purpose: to test the correct output structure (clause 4.2.1.8) and CRC-4 generation (clause 4.2.1.8.1) at the terminal equipment output port.

Test configuration (see figure A.9):

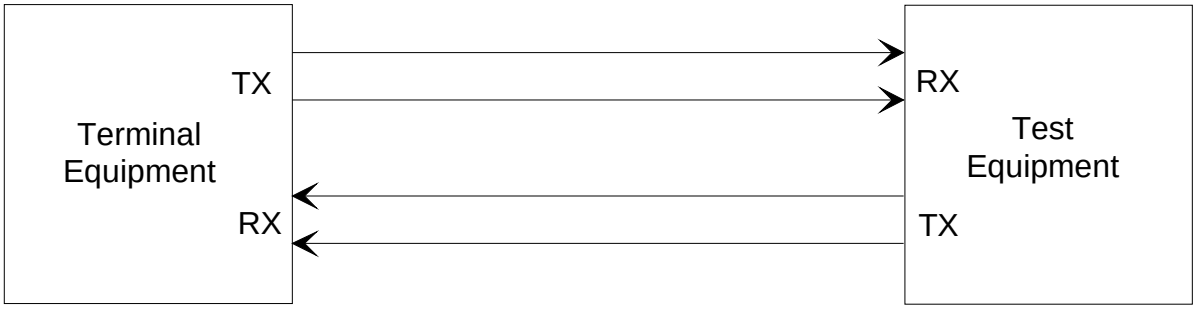


Figure A.9: Frame structure

Interface state: powered.

Stimulus:

- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2];

- the terminal equipment shall transmit a HDB3 bit stream with a binary content that has a frame structure according to annex C of the present document. The binary content of the data contained in bits 9 to 256 of the frame shall be a pseudo random bit stream, e.g. PRBS(2^{15}-1).

Monitor: the frame alignment signal and CRC-4 in the output bit stream from the terminal equipment.

Results:

- the frame alignment signal and bit 2 of the frame not containing the frame alignment signal shall be as defined in table C.1;

- the CRC-4 shall correspond with the data in the previous SMF, as defined in clause C.2 and clause C.2.1.

A.2.9.2 Terminals not using the E-bits

Purpose: to verify that for terminal equipments not using the E-bit to indicate SMF errors, the E-bits are set to binary ONE, as specified in clause 4.2.1.8.2.1.

Test configuration (see figure A.9):

Interface state: powered.

Stimulus:

- the terminal equipment shall transmit a HDB3 bit stream according to the frame structure of annex C. The binary content of the data contained in bits 9 to 256 of the frame shall be a pseudo random bit stream, e.g. PRBS(2^{15}-1);
- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2]. The test equipment shall generate the stimuli as defined in column 1 of table A.1.

Table A.1: Terminals not supporting the E-bit

Stimulus from test equipment	Result
Continuous SMFs with correct CRC-4	E = 1
Continuous SMFs with incorrect CRC-4	E = 1
Signal causing loss of frame alignment (e.g. Alarm Indication Signal (AIS))	E = 1

Monitor: the E-bit in the output bit stream from the terminal equipment.

Results: the E-bit shall be as defined in column 2 of table A.1.

A.2.9.3 Terminals using the E-bits to indicate errored SMFs

Purpose: to verify that for terminal equipments using the E-bit to indicate SMF errors, the E-bits are set correctly to indicate errored SMFs, as specified in clause 4.2.1.8.2.2.

Test configuration (see figure A.9):

Interface state: powered.

Stimulus:

- the terminal equipment shall transmit a HDB3 bit stream according to the frame structure of annex C. The binary content of the data contained in bits 9 to 256 of the frame shall be a pseudo random bit stream, e.g. PRBS(2^{15}-1);
- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2]. The test equipment shall generate the stimuli as defined in column 1 of table A.2.

Table A.2: Terminals using the E-bits to indicate errored SMFs

Stimulus from test equipment	Result
One SMF with an incorrect CRC-4 within a stream of SMFs with correct CRC-4s	One E-bit of E = 0, sent within 1 second of the errored SMF, the other E-bits being E = 1.
Two consecutive SMFs with incorrect CRC-4s within a stream of SMFs with correct CRC-4s	Two consecutive E-bits of E = 0, sent within 1 second of the errored SMF, the other E-bits being E = 1.
NOTE: Two consecutive E-bits may be in consecutive multiframes.	

Monitor: the E-bit in the output bit stream from the terminal equipment.

Results: the E-bit shall be as defined in column 2 of table A.2.

A.2.9.4 Use of the A-bit

Purpose: to verify that the A-bit is set correctly to indicate conditions at the terminal equipment input port as specified in clause 4.2.1.8.3.1 or clause 4.2.1.8.3.2.

Test configuration (see figure A.9):

Interface state: powered.

Stimulus:

- the terminal equipment shall transmit a HDB3 bit stream according to the frame structure of annex C. The binary content of the data contained in bits 9 to 256 of the frame shall be a pseudo random bit stream, e.g. PRBS(2^{15}-1);
- the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2]. The binary content of the data contained in bits 9 to 256 of the frame shall be a fixed pattern that does not contain a simulated frame alignment signal. The test equipment shall generate the stimuli as defined in column 1 of table A.3.

Table A.3: Terminals using the A-bit

	Stimulus from test equipment (see notes 1 and 2)	Result (see note 3)
1	Continuous frame sequence containing one incorrect frame alignment signal. (..2 F 2 F 2 /F 2 F 2 F..)	A = 0
2	Continuous frame sequence containing two consecutive incorrect frame alignment signals. (..2 F 2 F 2 /F 2 /F 2 F 2 F..)	A = 0
3	Continuous frame sequence containing three consecutive incorrect frame alignment signals. (..2 F 2 F 2 /F 2 /F 2 /F 2 F 2 F..)	A = 1 within 30 ms of the last incorrect frame alignment signal, returning to A = 0 within 30 ms of two correct frame alignment signals.
4	Continuous frames with three consecutive incorrect frame alignment signals, then N x frame sequences alternating correct and incorrect frame alignment signals, a correct frame then M x frame sequences with the correct frame alignment signal but with the frames not containing the frame alignment signal with bit 2 = 0, followed by continuous correct frames. (..2 F 2 F 2 /F 2 /F 2 /F Nx(2 F 2 /F) 2 F Mx(/2 F) 2 F 2 F..)	A = 1 within 30 ms of the third incorrect frame alignment signal, staying at A = 1 until A = 0 within 30 ms of two consecutive correct frame alignment signals. It is recommended that M and N be between 40 and 100.
5	Continuous frames with two consecutive frames not h containing the frame alignment signal having bit 2 = 0. (..2 F 2 F /2 F /2 F 2 F 2 F..)	A = 0
6	Continuous frames with three consecutive frames not containing the frame alignment signal having bit 2 = 0. (..2 F 2 F /2 F /2 F /2 F 2 F 2 F..)	A = 1 shall be set within 30 ms of the third frame with bit 2 = 0, returning to A = 0 within 30 ms of two correct frame alignment signals.
7	Continuous frames with 914 consecutive errored SMFs. followed by 86 consecutive non-errored SMFs, followed by 914 consecutive errored SMFs, followed by continuous non-errored SMFs. (..SMF SMF 914x/SMF 86xSMF 914x/SMF SMF..)	A = 0

	Stimulus from test equipment (see notes 1 and 2)	Result (see note 3)
8	Continuous frames with 915 consecutive errored SMFs, followed by 85 consecutive non-errored SMFs, followed by 915 consecutive errored SMFs, followed by continuous non-errored SMFs. (..SMF SMF 915x/SMF 85xSMF 915x/SMF SMF..)	During this time the A-bit shall change at least once from A = 0 to A = 1 and back to A = 0.
NOTE 1: Each test defined within the table shall be preceded by sufficient correct frames to ensure frame and multiframe alignment. NOTE 2: F is a frame with a correct frame alignment signal; /F is a frame with an incorrect frame alignment signal; 2 is the frame not containing the frame alignment signal having bit 2 set to 1; /2 is the frame not containing the frame alignment signal having bit 2 set to 0; SMF is a Sub-MultiFrame having correct frame alignment and correct CRC-4 bits; /SMF is a Sub-MultiFrame having correct frame alignment and incorrect CRC-4 bits. NOTE 3: Result for terminals complying with clause 4.2.1.8.3.2.		

Monitor: the A-bit in the output bit stream from the terminal equipment.

Results:

- for terminal equipments complying with clause 4.2.1.8.3.1 (i.e. those not using the A-bit), the A-bit shall be set to binary ZERO for all stimuli in column 2 of table A.3;

- for terminal equipments complying with clause 4.2.1.8.3.2 (i.e. those using the A-bit), the A-bit shall be as defined in table A.3. Requirements tested by test 6 of table A.3 is an optional requirements, it shall only be performed if this implementation is declared by the manufacturer.

A.2.10 Input frame structure

A.2.10.1 Frame alignment

Purpose: to verify that the terminal equipment input port can achieve frame alignment as specified in clause 4.2.2.9.1. Terminal equipments using the A-bit according to clause 4.2.1.8.3.2 and conforming to the tests in clause A.2.9.4 do not need to be tested as defined in this clause since conformance is demonstrated by compliance with clause A.2.9.4.

Test configuration (see figure A.10):

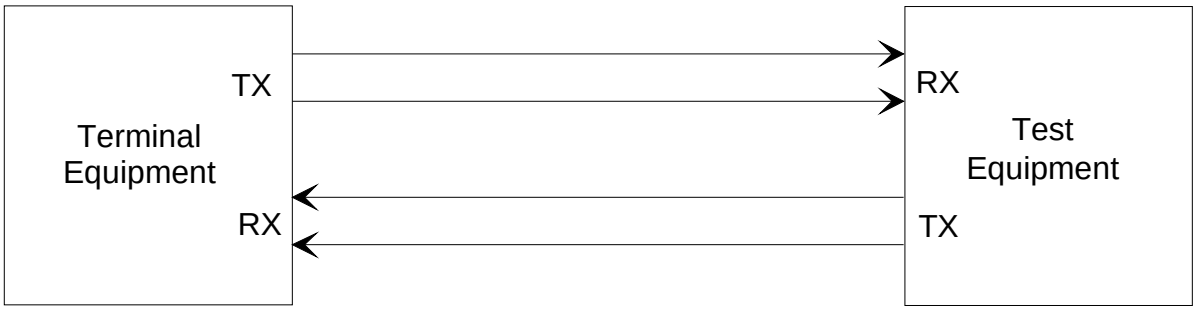


Figure A.10: Frame alignment

Interface state: powered, with received data from bits 9 to 256 of the input frame looped back to the output port.

Stimulus: the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2]. The binary content of the data contained in bits 9 to 256 of the frame shall be a fixed pattern that does not contain any simulated frame alignment signal. The test equipment shall generate the stimuli as defined in column 1 of table A.4.

Table A.4: Frame alignment

	Stimulus from test equipment (see notes 1 and 2)	Result
1	Continuous frame sequence containing one incorrect frame alignment signal. (..2 F 2 F 2 /F 2 F 2 F..)	No breaks in the data. No errors in the received data.
2	Continuous frame sequence containing two consecutive incorrect frame alignment signals. (..2 F 2 F 2 /F 2 /F 2 F 2 F..)	No breaks in the data. No errors in the received data.
3	Continuous frame sequence containing three consecutive incorrect frame alignment signals. (..2 F 2 F 2 /F 2 /F 2 /F 2 F 2 F..)	Any break in the data shall be less than 20,5 ms.
4	Continuous frames with three consecutive incorrect frame alignment signals, then N x frame sequences alternating correct and incorrect frame alignment signals, a correct frame then M x frame sequences with the correct frame alignment signal but with the frames not containing the frame alignment signal with bit 2 = 0, followed by continuous correct frames. (..2 F 2 F 2 /F 2 /F 2 /F Nx(2 F 2 /F) 2 F Mx (/2 F) 2 F 2 F..)	Any break in data transmission shall be less than 20,75 + 0,5 x (N + M/2) ms. It is recommended that M and N be between 40 and 100.
5	Continuous frames with two consecutive frames not containing the frame alignment signal having bit 2 = 0. (..2 F 2 F /2 F /2 F 2 F 2 F..)	No breaks in the data. No errors in the received data.
6	Continuous frames with three consecutive frames not containing the frame alignment signal having bit 2 = 0. (..2 F 2 F /2 F /2 F /2 F 2 F 2 F..)	A break in the data may occur in some implementations. Any break shall be less than 20,5 ms.
7	Continuous frames with 914 consecutive errored SMFs, followed by 86 consecutive non-errored SMFs, followed by 914 consecutive errored SMFs, followed by continuous non-errored SMFs. (..SMF SMF 914x/SMF 86xSMF 914x/SMF SMF..)	No breaks in the data. No errors in the received data.
8	Continuous frames with 915 consecutive errored SMFs, followed by 85 consecutive non-errored SMFs, followed by 915 consecutive errored SMFs, followed by continuous non-errored SMFs. (..SMF SMF 915x/SMF 85xSMF 915x/SMF SMF..)	A break in the data may occur in some implementations. Any break shall be less than 20,5 ms.
NOTE 1: Each test defined within the table shall be preceded by sufficient correct frames to ensure frame and multiframe alignment. NOTE 2: F is a frame with a correct frame alignment signal; /F is a frame with an incorrect frame alignment signal; 2 is the frame not containing the frame alignment signal having bit 2 set to 1; /2 is the frame not containing the frame alignment signal having bit 2 set to 0; SMF is a Sub-MultiFrame having correct frame alignment and correct CRC-4 bits; /SMF is a Sub-MultiFrame having correct frame alignment and incorrect CRC-4 bits.		

Monitor: monitor the data received in bits 9 to 256 of the frames from the terminal equipments and compare this the data transmitted from the test equipment. Monitor any breaks in the data.

Results: any break in the data shall be as defined in column 2 of table A.4.

A.2.10.2 Multiframe alignment

Purpose: to verify that the terminal equipment input port can achieve multiframe alignment as specified in clause 4.2.2.9.2.

Test configuration (see figure A.10):

Interface state: powered.

Stimulus: the output signal of the test equipment shall be HDB3 encoded and conform to a pulse shape as defined in figure 15 of ITU-T Recommendation G.703 [1], which is reproduced in figure 2 of the present document, and a framing structure as defined in ITU-T Recommendation G.704 [2]. The binary content of the data contained in bits 9 to 256 of the frame shall be a fixed pattern that does not contain any simulated frame alignment signal. The test equipment shall generate the stimuli as defined in column 1 of table A.5.

Table A.5: Multiframe alignment

	Stimulus from test equipment (see notes 1 and 2)	Result
1	Continuous correct multiframes. (..MF MF MF MF..)	Multiframe alignment.
2	A sequence of correct multiframes, followed by three incorrect frame alignment signals, followed by one incorrect multiframe, one correct multiframe, two incorrect multiframes, two correct multiframes, two incorrect multiframes, continuous correct multiframes. (..MF /F 2 /F 2 /F 2 /MF MF /MF /MF MF MF /MF /MF MF..)	Multiframe alignment shall be achieved after the first correct multiframe following the two incorrect multiframes.
NOTE 1: Each test defined within the table shall be preceded by sufficient correct frames to ensure frame and multiframe alignment. NOTE 2: F is a frame with a correct frame alignment signal; /F is a frame with an incorrect frame alignment signal; 2 is the frame not containing the frame alignment signal having bit 2 set to 1; MF is a multiframe having correct frame alignment signal, bit 2 = 1, correct multiframe alignment signal and correct CRC-4 bits; /MF is a multiframe having correct frame alignment signal, bit 2 = 1, incorrect multiframe alignment signal and correct CRC-4 bits.		

Monitor: monitor for multiframe alignment; the supplier of the terminal equipment shall declare how this shall be done. Those terminal equipments using the E-bits to indicate errored SMFs may indicate multiframe alignment by the correct recognition of errored SMFs inserted into the stimulus signal from the test equipment (i.e. MF /F 2 /F 2 /F 2 /MF MF /MF /MF MF MF /MF /MF /SMF /SMF MF).

Results: multiframe alignment shall be achieved as defined in column 2 of table A.5.

Annex B (normative): Definition of HDB3 code

B.1 General

This annex specifies the modified Alternate Mark Inversion (AMI) code HDB3. The contents of this annex are based on annex A of ITU-T Recommendation G.703 [1].

In this code, binary 1 bits are represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

In the definition below, B represents an inserted pulse corresponding to the AMI rule, and V represents an AMI violation.

B.2 Definition

Each block of 4 successive zeros is replaced by 000V or B00V. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no dc component is introduced.

Annex C (normative): Definition of frame structure

C.1 Frame structure

The bit stream shall be structured into a frame of length 256 bits, numbered 1 to 256. The frame repetition rate shall be nominally 8 000 Hz. The allocation of bits 1 to 8 within the frame shall be as shown in table C.1.

Table C.1: Allocation of bits 1 to 8

Bit no	Frame containing the frame alignment signal	Frame not containing the frame alignment signal
1	CRC-4 (see clause B.2)	CRC-4 (see clause B.2)
2	0	1
3	0	A (see note 1)
4	1	S_{a4} (see note 2)
5	1	S_{a5} (see note 2)
6	0	S_{a6} (see note 2)
7	1	S_{a7} (see note 2)
8	1	S_{a8} (see note 2)

NOTE 1: Bit A: RAI (see clause 4.1.3.4).
NOTE 2: Bits S_{a4} to S_{a8} are for the use of the leased line operator. Their value at the output port of a leased line is undefined.

C.2 CRC-4

The allocation of the CRC-4 bits shall be as given in table C.2 for a complete CRC-4 multiframe. Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, shall be divided into two 8-frame SMFs, designated SMF I and SMF II which shall signify their respective order within the CRC-4 multiframe structure. The SMF is the block (size 2 048 bits) for the CRC-4.

In those frames containing the frame alignment signal, bit 1 shall be used to transmit the CRC-4 bits. These shall be the 4 bits designated C_1, C_2 C_3 and C_4 in each SMF. In those frames not containing the frame alignment signal, bit 1 shall be used to transmit the six bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E-bits). The CRC-4 multiframe alignment signal shall have the form 001011.

Table C.2: Allocation of CRC-4 bits with a multiframe

	SMF	Frame	Bit 1
Multiframe	SMF I	0	C1
		1	0
		2	C2
		3	0
		4	C3
		5	1
		6	C4
		7	0
	SMF II	8	C1
		9	1
		10	C2
		11	1
		12	C3
		13	E
		14	C4
		15	E

C.2.1 CRC-4 generation

A particular CRC-4 word, located in SMF N shall be the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of SMF (N-1). When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0 bit 1 or frame 8 bit 1, shall be taken as the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

The CRC-4 encoding process is described below:

a) the CRC-4 bits in the SMF are replaced by binary ZEROs;

b) the SMF is then acted upon by the multiplication/division process defined above;

c) the remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

NOTE: The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in a) above, the CRC-4 bit positions in a SMF are initially set to binary ZERO during the multiplication/division process.

C.2.2 CRC-4 monitoring

The CRC-4 monitoring process used to detect errored SMFs shall be as described below:

a) a received SMF is acted upon by the multiplication/division process defined in clause C.2.1 after having its CRC-4 bits extracted and replaced by ZEROs;

b) the remainder resulting from the multiplication/division process is stored and subsequently compared on a bit by bit basis with the CRC-4 bits received in the next SMF;

c) if the remainder calculated in the decoder does not exactly correspond to the CRC-4 bits received in the next SMF, the SMF is defined as being an errored SMF.

Annex D (normative): Requirements Table (RT)

Table D.1: RT for the present document

Reference		the present document		
No	**Reference to the clause**	**Requirement**	**Status (see note 1)**	**Support (see note 2)**
1	4.1.1	Hardwired connection	M	
2	4.1.2	Additional means of connection	O	
3	4.2.1.1	Signal coding	M	
4	4.2.1.2	Waveform shape	M	
5	4.2.1.3 (a)	Output timing (internal clock)	M	
6	4.2.1.3 (b)	Output timing (clock loop)	M	
7	4.2.1.3 (c)	Output timing (external reference)	O	
8	4.2.1.4	Impedance towards ground	M	
9	4.2.1.5	Output jitter	M	
10	4.2.1.6	Output return loss	N	
11	4.2.1.7	Output signal balance	N	
12	4.2.1.8	Output structure	M	
13	4.2.1.8.1	CRC-4 procedure	M	
14	4.2.1.8.2.1	Terminals not using the E-bits	O.1	
15	4.2.1.8.2.2	Terminals using the E-bits to indicate errored SMFs	O.1	
16	4.2.1.8.3.1	Terminals not using the A-bit	O.2	
17	4.2.1.8.3.2 a b d e f	Terminals using the A-bit	O.2	
18	4.2.1.8.3.2 c		If 17 then O else N	
19	4.2.1.8.4	Use of the S_a bits	N	
20	4.2.2.1	Signal coding	M	
21	4.2.2.2	Input return loss	M	
22	4.2.2.3	Input loss tolerance	M	
23	4.2.2.4	Immunity against reflections	M	
24	4.2.2.5	Tolerable longitudinal voltages	M	
25	4.2.2.6	Impedance towards ground	M	
26	4.2.2.7	Input jitter tolerance	M	
27	4.2.2.8	Input clock tolerance	M	
28	4.2.2.9.1	Frame alignment	M	
29	4.2.2.9.2	Multiframe alignment	If 15 then M else N	
30	4.3.1	Safety – general requirements	M	
31	4.3.2	Touch current	M	
32	4.4.1	Surge simulation, common mode	M	
33	4.4.2	Surge simulation, transverse mode between transmit and receive pairs	M	
34	4.4.3	Mains simulation, common mode	C1	
35	4.4.4	Mains simulation, transverse mode	C1	
36	4.4.5	Impulse transfer from mains, common mode	C1	
37	4.4.6	Impulse transfer from mains, transverse mode	C1	

Reference		the present document		
No	**Reference to the clause**	**Requirement**	**Status (see note 1)**	**Support (see note 2)**
38	4.4.7	Conversion of common mode to transverse mode	M	
39	4.4.8	Impulse transfer from auxiliary port	N	
40	4.5	ElectroMagnetic Compatibility (EMC)	N	

O.1 It is mandatory to support one of these options.
O.2 It is mandatory to support one of these options.
C1 If the terminal is mains powered then M else N.
NOTE 1: Status is "Mandatory (M)", "Not a requirement (N)", "Optional (O)" or "Conditional (Cn)". O.n indicates that one or more of the numbered options shall be provided from the set n and Cn indicates reference shall be made to boolean expression Cn.
NOTE 2: Support is "Y" (equipment conforms to the standard), "X" (equipment does not conform to the present document), "N" (equipment does not claim to conform to the present document).

Annex E (informative): Timing synchronization

E.1 General

The 2 048 kbit/s digital structured leased line (D2048S) connection provided by the leased line operator will comply with one of three timing requirements. The leased line will either:

- carry user timing over the range 2 048 kbit/s ±50 ppm (referred to as user timing); or
- provide timing that is synchronous to the network timing (referred to as network timing); this is timing that is derived from the source or sources of timing that are used for the network and will be similar to that provided by other digital services;
- take user timing within the range 2 048 kbit/s ±50 ppm from one input and provide this timing at both outputs of the leased line.

In these three cases, the terminal equipments at either end of the leased line may need to be configured differently in order to establish synchronous data transfer and, if required, synchronous operation. The requirements on terminal equipment output timing imposed within the present document are sufficient for each terminal to be connected to, and operate with, each of the three types of leased line.

E.1.1 User timing

Where the leased line is capable of carrying user timing and if synchronous operation of the two directions of transmission is required, one terminal equipment (referred to as the master) will generally be responsible for originating the timing signal. The other terminal equipment (referred to as the slave) will generally extract the timing from the leased line and transmit data back in the opposite direction of transmission in synchronism with this signal. This is referred to as "looping back" the timing and results in synchronous data transfer in both directions. The master terminal equipment may take its timing from an internal source or from an external source such as another leased line or an Integrated Services Digital Network (ISDN) interface from the public network, if synchronous operation of the leased line connection with those services is required.

Other configurations are also possible. It is possible to use independent clock sources in each direction with both terminals acting as masters. Any divergence between these clock sources would result in the occurrence of slips in the terminal equipment; this may not be satisfactory if synchronous data transfer is required. However, if both terminals extract their timing from high accuracy sources, such as the public network, the overall synchronization would be satisfactory and the number of slips would be acceptable for most applications.

A configuration where both terminal equipments attempted to "loop back" the timing would not be practical with this type of leased line and may lead to an unstable operating condition.

E.1.2 Network timing

Where the leased line provides network timing, both terminal equipments would generally provide looping back of the clock ("clock loops"), ensuring synchronous data transfer in each direction and between terminals and the leased line connection.

Other configurations are also available. A terminal equipment could use timing derived from another source, however this could generate slips between the terminal equipment and the network; the number of slips would depend on the accuracy of the timing sources. Timing derived from a source of equivalent accuracy, e.g. the public ISDN network, is likely to result in an acceptable number of slips, but not when an internal timing source within the limits of 2 048 kbit/s ±50 ppm is used.

E.2 Further information

Further information on synchronization can be found in ISO/IEC DIS 11573.

Annex F (informative): Bibliography

- Council Directive 89/336/EEC of 3 May 1989 on the approximation of the laws of the Member States relating to electromagnetic compatibility.
- Council Directive 91/263/EEC of 29 April 1991 on the approximation of the laws of Member States concerning telecommunications terminal equipment, including the mutual recognition of their conformity.
- Council Directive 92/44/EEC of 5 June 1992 on the application of Open Network Provision to leased lines.
- Directive 98/13/EC of the European Parliament and of the Council of 12 February 1998 relating to telecommunications terminal equipment and satellite earth station equipment, including the mutual recognition of their conformity.
- ITU-T Recommendation G.706 (1991): "Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704".
- ITU-T Recommendation G.823 (2000): "The control of jitter and wander within digital networks which are based on the 2 048 kbit/s hierarchy".
- ETSI ETS 300 166 (1993): "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2 048 kbit/s-based plesiochronous or synchronous digital hierarchies".
- ETSI TBR 13: "Business TeleCommunications (BTC); 2 048 kbit/s digital structured leased line (D2048S); Attachment requirements for terminal equipment interface".
- ISO/IEC 11573 (1994): "Information technology - Telecommunications and information exchange between systems - Synchronization methods and technical requirements for Private Integrated Services Networks".
- ETSI EG 201 212: "Electrical safety; Classification of interfaces for equipment to be connected to telecommunication networks".
- CENELEC EN 60950: "Safety of information technology equipment".

History

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