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European Standard (Telecommunications series)

Transmission and Multiplexing (TM);
Generic requirements of transport functionality of equipment;
Part 6-1: Synchronization layer functions

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Contents

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Foreword

This European Standard (Telecommunications series) has been produced by ETSI Technical Committee Transmission and Multiplexing (TM).

The present document is one of a family of documents that has been produced in order to provide inter-vendor and inter-operator compatibility of Synchronous Digital Hierarchy (SDH) equipment.

The present document is part 6-1 of a multi-part EN covering the Generic requirements of transport functionality of equipment, as identified below:

Part 1-1:   "Generic processes and performance".

Part 1-2:   "General information about Implementation Conformance Statement (ICS) proforma".

Part 1-3   "Generic processes and performance; Abstract Test Suite (ATS)".

Part 2-1:   "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions".

Part 2-2:   "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 2-3:   "Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions; Abstract Test Suite (ATS)".

Part 3-1:   "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".

Part 3-2:   "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 3-3:   "Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions; Abstract Test Suite (ATS)".

Part 4-1:   "Synchronous Digital Hierarchy (SDH) path layer functions".

Part 4-2:   "Synchronous Digital Hierarchy (SDH) path layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 4-3:   "Synchronous Digital Hierarchy (SDH) path layer functions; Abstract Test Suite (ATS)".

Part 5-1:   "Plesiochronous Digital Hierarchy (PDH) path layer functions".

Part 5-2:   "Plesiochronous Digital Hierarchy (PDH) path layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 5-3:   "Plesiochronous Digital Hierarchy (PDH) path layer functions; Abstract Test Suite (ATS)".

Part 6-1:   "Synchronization layer functions".

Part 6-2:   "Synchronization layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 6-3:   "Synchronization layer functions; Abstract Test Suite (ATS)".

Part 7-1:   "Auxiliary layer functions".

Part 7-2:   "Auxiliary layer functions; Implementation Conformance Statement (ICS) proforma specification".

Part 7-3:   "Auxiliary layer functions; Abstract Test Suite (ATS)".

Parts 2 to 7 specify the layers and their atomic functions.

NOTE 1:   The present document does not currently address configuration management.

NOTE 2:   The SDH radio equipment functional blocks are addressed by ETSI WG TM4.

Various of the above parts have previously been published as parts of ETS 300 417.

They have been converted to parts of EN 300 417 without technical changes, but some editorial changes have been necessary (e.g. references). In particular:

-   Parts 2-1 and 3-2 have been modified to take account of editorial errors present in edition 1.

-   Part 1-1 has had its title change of to align with other parts published at a later date.

Also note that in the meantime parts 8-1, 8-2 and 8-3 have been stopped.

Transposition dates	
Date of adoption of this EN:	24 July 1998
Date of latest announcement of this EN (doa):	30 November 1998
Date of latest publication of new National Standard or endorsement of this EN (dop/e):	31 May 1999
Date of withdrawal of any conflicting National Standard (dow):	31 May 1999

# 1	Scope

The present document specifies a library of basic Synchronization Distribution (SD) building blocks, referred to as "atomic functions" and a set of rules by which they are combined in order to describe a digital transmission equipment. The library defined in the present document forms part of the set of libraries defined in EN 300 417 series. The library comprises the functional building blocks needed to completely specify the generic functional structure of the European digital transmission hierarchy. Equipment that is compliant with the present document should be describable as an interconnection of a subset of these functional blocks contained within the present document. The interconnection of these blocks should obey the combination rules given in EN 300 417. The generic functionality is described in EN 300 417-1-1 [6].

The present document assumes that there are only two types of Synchronization Supply Units (SSUs), transit and local, as currently defined in CCITT Recommendation G.812 [17]. However, STC TM3 has approved in September 1996 a new SSU with enhanced characteristics. The inclusion of such an SSU in the present document is for further study.

The present document does not specify the atomic functions that are specific to SSU and Primary Reference Clock (PRC); the Synchronization Status Message (SSM) selection algorithm specified in the present document applies only to SEC's.

# 2	References

The following documents contain provisions which, through reference in this text, constitute provisions of the present document.

- References are either specific (identified by date of publication, edition number, version number, etc.) or non-specific.

- For a specific reference, subsequent revisions do not apply.

- For a non-specific reference, the latest version applies.

- A non-specific reference to an ETS shall also be taken to refer to later versions published as an EN with the same number.

[1]	ETS 300 147: "Transmission and Multiplexing (TM); Synchronous Digital Hierarchy (SDH); Multiplexing structure".

[2]	ETS 300 166 (1993): "Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2 048 kbit/s - based plesiochronous or synchronous digital hierarchies".

[3]	ETS 300 167: "Transmission and Multiplexing (TM); Functional characteristics of 2 048 kbit/s interfaces".

[4]	ETS 300 337 (1996): "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[5]	ETS 300 337 (1995): "Transmission and Multiplexing (TM); Generic frame structures for the transport of various signals (including Asynchronous Transfer Mode (ATM) cells and Synchronous Digital Hierarchy (SDH) elements) at the ITU-T Recommendation G.702 hierarchical rates of 2 048 kbit/s, 34 368 kbit/s and 139 264 kbit/s".

[6]	EN 300 417-1-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 1-1: Generic processes and performance".

[7]	EN 300 417-2-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 2-1: Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) physical section layer functions".

[8]   EN 300 462-1-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 1-1: Definitions and terminology for synchronization networks".

[9]   EN 300 462-2-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 2-1: Synchronization network architecture".

[10]   EN 300 462-4-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 4-1: Timing characteristics of slave clocks suitable for synchronization supply to Synchronous Digital Hierarchy (SDH) and Plesiochronous Digital Hierarchy (PDH) equipment".

[11]   EN 300 462-5-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave clocks suitable for operation in Synchronous Digital Hierarchy (SDH) equipment".

[12]   EN 300 462-6-1: "Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 6-1: Timing characteristics of primary reference clocks".

[13]   ITU-T Recommendation G.704 (1995): "Synchronous frame structures used at 1 544, 6 312, 2 048, 8 488 and 44 736 kbit/s hierarchical levels".

[14]   ITU-T Recommendation G.707 (1996): "Network node interface for the synchronous digital hierarchy (SDH)".

[15]   ITU-T Recommendation G.783: "Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks".

[16]   CCITT Recommendation G.811 (1988): "Timing requirements at the outputs of primary reference clocks suitable for plesiochronous operation of international digital links".

[17]   CCITT Recommendation G.812 (1988.): "Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links".

[18]   ITU-T Recommendation G.813 (1996): "Timing characteristics of SDH equipment slave clocks (SEC)".

3   Definitions, abbreviations and symbols

3.1   Definitions

For the purposes of the present document, the following definition applies:

Timing loop: This is a network condition where a slave clock providing synchronization becomes locked to its own timing signal. It is generally created when the slave clock Timing Information (TI) is looped back to its own input, either directly or via other network equipments. Timing loops should be prevented in networks by careful network design.

QL minimum: QL_minimum is a configurable parameter used in the squelching of clock output signals. If the Quality Level (QL) of the signal used to derive the output falls below QL_Minimum then the output will be squelched (cut-off or set to Alarm Indication Signal (AIS)).

Clock-Source Quality-Level: The clock-source quality-level of a SDH Equipment Clock (SEC) or Stand Alone Synchronization Equipment (SASE) is defined as the grade of clock to which it is ultimately traceable; i.e. the grade-of-clock to which it is synchronized directly or indirectly via a chain of SEC's, and SASE's however long this chain of clocks is. For example, the clock-source quality-level may be a PRC complying with EN 300 462-6-1 [12], or it may be a Slave Clock in holdover-mode, complying with EN 300 462-4-1 [10], or a EN 300 462-5-1 [11] Clock in holdover or free-run.

The clock-source quality-level is essentially, therefore, an indication only of the long-term accuracy of the Network Element (NE) Clock.

Station Clock: This is a node clock as defined in EN 300 462-1-1 [8].

The functional definitions are given in EN 300 417-1-1 [6].

3.2   Abbreviations

For the purposes of the present document, the following abbreviations apply:

AI	Adaptation Information
AIS	Alarm Indication Signal
AP	Access Point
CI	Characteristic Information
CK	timing information - Clock signal
CLR	Clear
CP	Connection Point
CS	timing information - Clock Source
CSid	Clock Source identifier
DNU	Do Not Use
ES1	STM-1 Electrical Section layer
EXTCMD	External Command
FS	timing information - Frame Start
FSw	Forced Switch
HO	Hold Over mode
HO	Hold Off time
ID	IDentifier
INVx	INValid x
LC	Layer Clock
LO	Lock Out
LO	Locked mode
LOS	Loss Of Signal
LSB	Least Significant Bit
LTI	Loss of Timing Information
MA	Maintenance and Adaptation
MI	Management Information
MON	MONitored
MFP	MultiFrame Present
MFS	MultiFrame Start
MS	Multiplex Section
MSB	Most Significant Bit
MSw	Manual Switch
MTIE	Maximum Time Interval Error
NE	Network Element
NS	Network Synchronization
NSUPP	Not supported
OSn	STM-N Optical Section layer
P12s	2 048 kbit/s PDH path layer with synchronous 125 µs frame structure according to ETS 300 167 [3]
P31s	34 368 kbit/s PDH path layer with synchronous 125 µs frame structure according to ETS 300 337 [4]
P4s	139 264 kbit/s PDH path layer with synchronous 125 µs frame structure according to ETS 300 337 [4]
PDH	Plesiochronous Digital Hierarchy
PRC	Primary Reference Clock
QL	Quality Level
RI	Remote Information
RSn	STM-N Regenerator Section layer
SASE	Stand Alone Synchronization Equipment
SD	Synchronization Distribution
SDH	Synchronous Digital Hierarchy
SDL	Specification and Description Language
SEC	SDH Equipment Clock

SF	Signal Fail
SQLCH	Squelch
SSF	Server Signal Fail
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
SSUL	Local SSU
SSUT	Transit SSU
STM-N	Synchronous Transport Module, level N
Sk	Sink
So	Source
TCP	Termination Connection Point
TDEV	Time DEViation
TI	Timing Information
TL	Transport Layer
TM	Timing Marker
TT	Trail Termination
TSF	Trail Signal Fail
UNC	UNConnected
VC-n	Virtual Container, level n
WTR	Wait to Restore

3.3   Symbols and diagrammatic conventions

For the purposes of the present document, the symbols and diagrammatic conventions given in EN 300 417-1-1 [6] apply.

3.4   Introduction

This subclause defines the atomic functions that are part of the 2 synchronization layers, the SD layer and the Network Synchronization (NS) layer. It also defines some atomic functions, part of the Transport Layer (TL), which are related with synchronization.

These functions describe the synchronization of SDH NEs and how SDH NEs are involved in NS.

4   Synchronization principles

4.1   Network synchronization

Synchronization network architecture is specified in EN 300 462-2-1 [9].

Synchronization information is transmitted through the network via synchronization network connections. These synchronization network connections can transport different synchronization levels. Each synchronization network connection is provided by one or more synchronization link connections, each supported by a synchronized primary or secondary rate Plesiochronous Digital Hierarchy (PDH) trail or SDH multiplex section trail (see clause 5 of EN 300 462-2-1 [9]).

Some of these synchronized primary or secondary rate PDH trail or SDH multiplex section trail signals contain a communication channel, the SSM or the Timing Marker (TM) transporting a quality Identifier (ID). This QL ID can be used to select the highest synchronization level incoming reference signal from a set of nominated synchronization references available at the NE.

Synchronization network connections are uni-directional and generally point to multipoint. EN 300 462-2-1 [9] specifies a master-slave synchronization technique for synchronizing SDH networks (see subclause 4.1 of EN 300 462-2-1 [9]). Figures 1 to 4 illustrate the synchronization network connection model.

PRC level

SSU level

SEC level
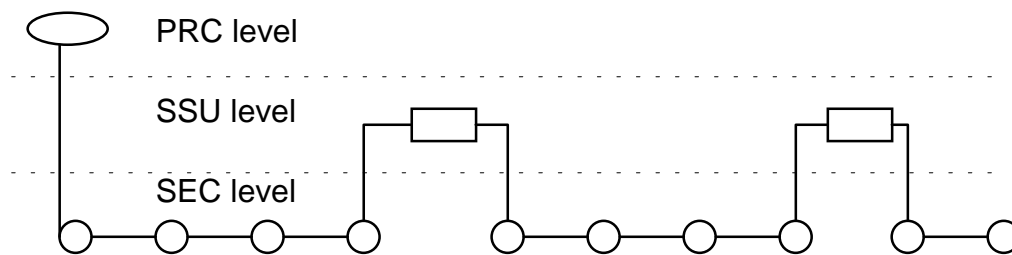
Figure 1: General representation of a synchronization network

·········· PRC synchronization network connection
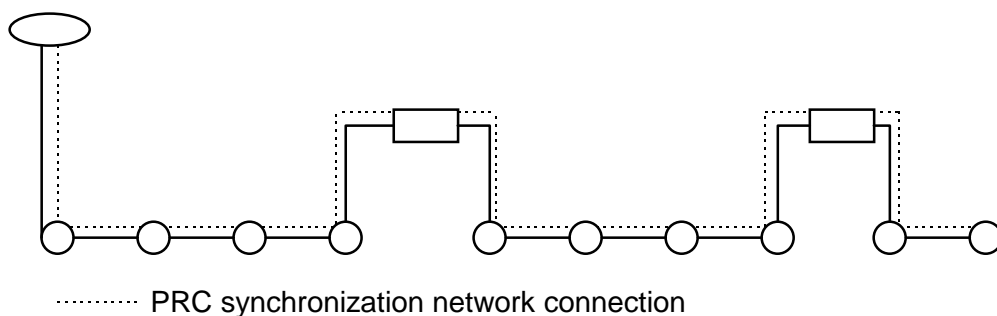
Figure 2: Representation of the PRC network connection

fault

· · · · · PRC synchronization network connection

— — — SSU synchronization network connection

— · · — SEC synchronization network connection
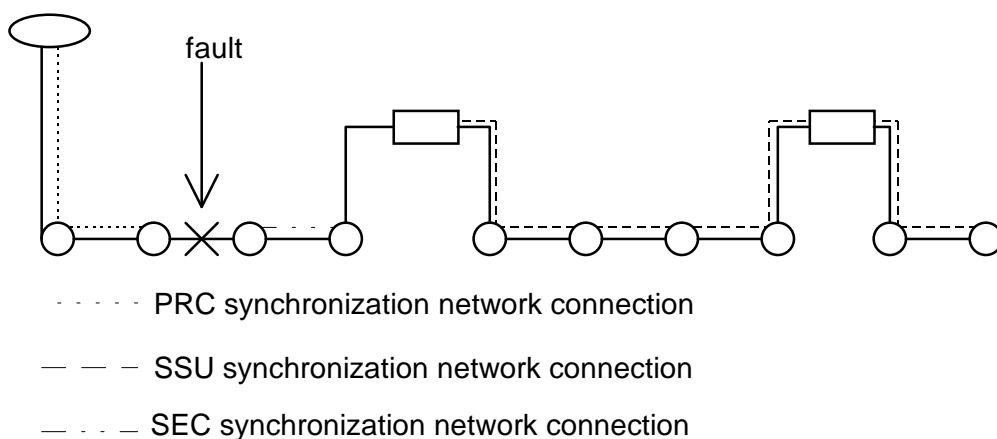
Figure 3: Representation of the synchronization network connection in case of failure

fault

·········· PRC synchronization network connection
— — — SSU synchronization network connection
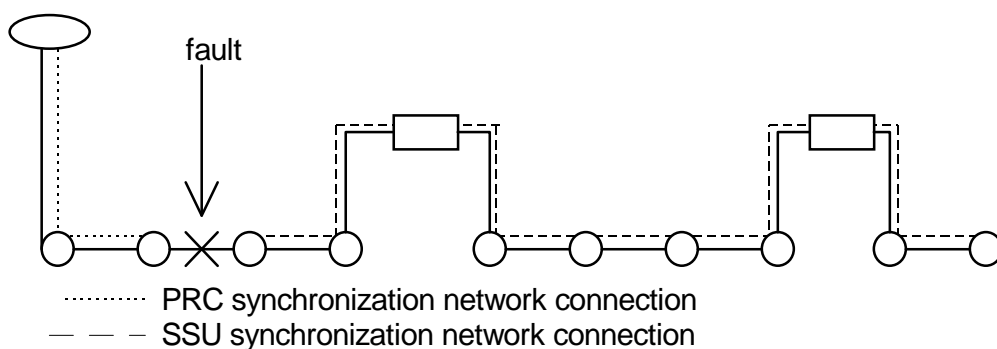
Figure 4: Example of restoration of the synchronization (see figure 7 of EN 300 462-2-1 [9])

4.2   Synchronization distribution trails

SD trails transport timing between two adjacent equipments.

From a synchronization view point, adjacent NEs are those NEs that are interconnected via section signals. Between two such adjacent NEs a uni-directional SD trail exists.

A **SD trail** starts at the input of the SD_TT_So function and ends at the output of the SD_TT_Sk function.

A **SD link connection** transports synchronization TI between two adjacent Connection Points (CP) of the NS_C function.

A **NS network connection** transports synchronization TI over a series of synchronization link connection.
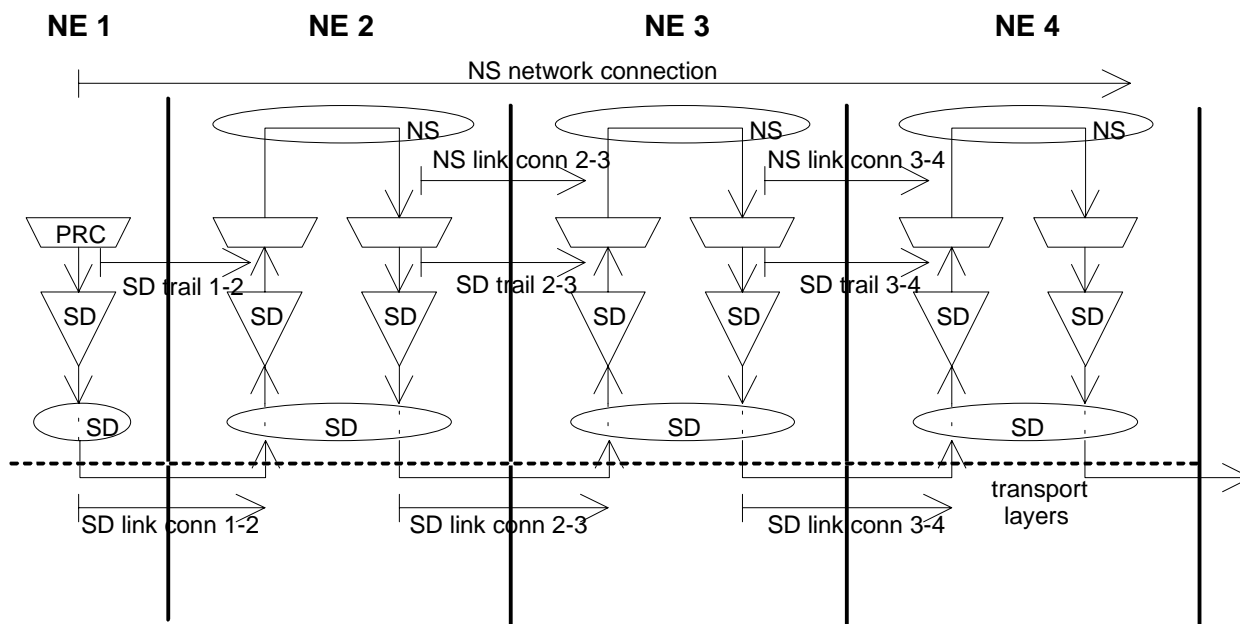
Figure 5: Example of series of SD network connection transporting PRC quality timing reference information

4.3   Synchronization interfaces

Synchronization trails can be carried through the network by a number of interfaces. Currently, the following signals are defined for such transport (refer also to figures B.1 to B.4):

- without traffic:

    - 2 048 kHz (T12);

    - 2 048 kbit/s (E12+P12s);

- with traffic:

    - 2 488 320 kbit/s (OS16+RS16+MS16);

    - 622 080 kbit/s (OS4+RS4+MS4);

    - 155 520 kbit/s (OS1 (or ES1)+RS1+MS1);

    - 139 264 kbit/s (E4+P4s);

    - 34 368 kbit/s (E31+P31s);

    - 2 048 kbit/s (E12+P12s).

4.3.1   Synchronous Transport Module, level N (STM-N)

The STM-N transport signals carry (in addition to the payload) reference TI and an indication of the QL of the source generating this TI, via the SSM as defined in EN 300 147 [1].

NOTE: Old equipment may not be able to support SSM via their STM-N interfaces.

4.3.2   2 Mbit/s

The 2 Mbit/s transport signals may carry (in addition to the payload) reference TI.

The 2 Mbit/s timing reference signals (without payload) carry reference TI to specific synchronization ports.

Both signals can carry an indication of the QL of the source generating the TI via the SSM as specified in ITU-T Recommendation G.704 [13].

NOTE: Old equipment may not be able to support SSM on their 2 Mbit/s interfaces.

4.3.3   2 MHz

Synchronization can be carried through 2 MHz signals to specific synchronization ports (so called station clock ports). This signal does not carry an indication of the QL of the source generating the TI.

4.3.4   34 Mbit/s and 140 Mbit/s with 125 µs frame structure

34 Mbit/s and 140 Mbit/s signals with 125 µs frame structure as defined in ETS 300 337 [4] carry a full 4 bit SSM code.

NOTE: For interworking with equipments compliant with the initial edition of ETS 300 337 [4], new equipments should be able to be configured to recognize and generate the TM which is located in bit 8 of the Maintenance and Adaptation (MA) byte: the TM is set to "0" to indicate that the timing source is traceable to a PRC, and is otherwise set to "1".

4.4   Clock-Source Quality-Level

4.4.1   Clock-Source Quality- Level Definitions

The following Clock Source (CS) QLs are defined in the synchronization process of SDH network corresponding to 4 levels of synchronization quality (EN 300 462-2-1 [9]).

QL-PRC: This synchronization trail transports a timing quality generated by a PRC that is defined in EN 300 462-6-1 [12].

QL-SSU T: This synchronization trail transports a timing quality generated by either a transit slave clock that is defined in CCITT Recommendation G.812 [17] or a SSU that is defined in EN 300 462-4-1 [10].

QL-SSU L: This synchronization trail transports a timing quality generated by a local slave clock that is defined in CCITT Recommendation G.812 [17].

QL-SEC: This synchronization trail transports a timing quality generated by a SEC that is defined in EN 300 462-5-1 [11].

QL-DNU: This signal should not be used for synchronization.

NOTE: The QL-unknown QL was defined to characterize the quality of existing network. This QL is no longer supported by the SSM algorithm.

4.4.2   Hierarchy of Clock-Sources Quality Level or (CS_QL)

The following table defines the QL hierarchy.

Table 1: Hierarchy of quality levels

Quality Level (QL)	Order
QL-PRC	highest
QL-SSU T	
QL-SSU L	
QL-SEC	
QL-DNU	
QL-INVx, -FAILED, -UNC, -NSUPP	lowest

The QLs QL-INVx, QL-FAILED, QL- UNC and QL-NSUPP are internal QLs inside the NE and are never generated at an output port.

QL-INVx is generated by the XX/SD_A_Sk function if an unallocated SSM value is received, where x represents the binary value of this SSM.

QL-NSUPP is generated by the XX/SD_A_Sk function when the function is not supporting the SSM TM processing.

QL-FAILED is generated by the SD_TT_Sk function when the terminated SD trail is in the Signal Fail (SF) state.

QL-UNC is generated by the SD_C or NS_C function when the output signal is not connected to an input, but instead to the internal unconnected signal generator.

4.4.3   Forcing of Clock-Source Quality-Levels

For synchronization source signals/interfaces not supporting SSM transport/processing, it is possible to force the QL to a fixed provisioned value. This allows to use these signals/interfaces as synchronization sources in an automatic reference selection process operating in QL-enabled mode.

Forcing of QLs is used for new equipment operating in QL-enabled mode in order to:

-    interwork with old equipment not supporting SSM/TM generation;

-    interwork with new equipment operating in QL-disabled mode;

-    select interfaces not supporting SSM/TM processing;

-    select signals for which SSM/TM is not defined in (2 MHz).

4.5   SSM and TM channels

The following signals have a four bit SSM channel defined:

-    STM-N (N = 1, 4, 16): bits 5 to 8 of the byte S1 (called SSMB, SSM Byte) of the multiplex section overhead as defined in ITU-T Recommendation G.707 [14].

-    2 Mbit/s octet structured according to ITU-T Recommendation G.704 [13]: bits S_{ax1} to S_{ax4} (x = 4, 5, 6, 7, or 8) of TS0.

-    34 Mbit/s as defined in ETS 300 337 [4]: bit 8 of MA byte with a 4 frame multiframe.

-    140 Mbit/s as defined in ETS 300 337 [4]: bit 8 of MA byte with a 4 frame multiframe.

The following signals may have a one bit TM channel:

-    34 Mbit/s with a 125 µs frame structure as defined in ETS 300 337 [5]: bit 8 of byte MA.

-    140 Mbit/s with a 125 µs frame structure as defined in ETS 300 337 [5]: bit 8 of byte MA.

4.5.1   SSM and TM message sets

Five SSM codes are defined to represent CS QL as listed below:

-    code 0010 (Quality PRC) means that the source of the trail is a PRC clock (EN 300 462-6-1 [12],
     CCITT Recommendation G.811 [16]);

-    code 0100 (Quality SSU-T), means that the source of the trail is a transit SSU clock
     (CCITT Recommendation G.812-T [17]) or a SSU that is defined in EN 300 462-4-1 [10];

-    code 1000 (Quality SSU-L), means that the source of the trail is a SSU clock
     (CCITT Recommendation G.812-L [17]);

-    code 1011 (Quality SEC), means that the source of the trail is a SEC clock (EN 300 462-5-1 [11], option 1 of
     ITU-T Recommendation G.813 [18]);

-    code 1111 (quality DNU), means that the signal carrying this SSM shall not be used for synchronization because
     a timing loop situation could result if it is used.

Two TM codes were defined in ETS 300 337 [4] and [5]:

-    code 0 (Quality PRC), means that the source of the trail is a PRC clock (EN 300 462-6-1 [12],
     CCITT Recommendation G.811 [16]);

-    code 1 (Quality less_than_PRC), means that the source of the trail is not a PRC clock.

4.5.2   SSM and TM code word generation

The SSM can be viewed as an application specific data communication channel with a limited message set. The message
that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function.
The following table presents the relation between the existing set of QLs and SSM codes.

Table 2: Quality level set and coding in SSM

Quality Level (QL)	SSM usage	SSM coding [MSB..LSB]
QL-PRC	enabled	0010
QL-SSUT	enabled	0100
QL-SSUL	enabled	1000
QL-SEC	enabled	1011
QL-DNU	enabled	1111
-	disabled	1111

The TM can be viewed as an application specific data communication channel with a limited message set. The message
that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function.
The following table presents the relation between the existing set of QLs and TM codes.

Table 3: Quality level set and coding in TM

Quality Level (QL)	TM usage	TM coding
QL-PRC	enabled	0
QL-SSUT	enabled	1
QL-SSUL	enabled	1
QL-SEC	enabled	1
QL-DNU	enabled	1
-	disabled	1

At network boundaries, it should be possible to prevent synchronization information passing the interface. This can be achieved by disabling the SSM (TM) usage.

4.5.3   SSM and TM code word interpretation

At the receive side, the received SSM bits are to be validated by a persistency check and then interpreted to determine the QL.

Table 4: Interpretation of SSM codes

SSM code [MSB..LSB]	QL interpretation
0000	QL-INV0
0001	QL-INV1
0010	QL-PRC
0011	QL-INV3
0100	QL-SSUT
0101	QL-INV5
0110	QL-INV6
0111	QL-INV7
1000	QL-SSUL
1001	QL-INV9
1010	QL-INV10
1011	QL-SEC
1100	QL-INV12
1101	QL-INV13
1110	QL-INV14
1111	QL-DNU

Table 5: Interpretation of TM codes

TM code	QL interpretation
0	QL-PRC
1	QL-DNU

4.6   Selection process

The process of selecting a synchronization source from the set of physical ports is performed in three steps.
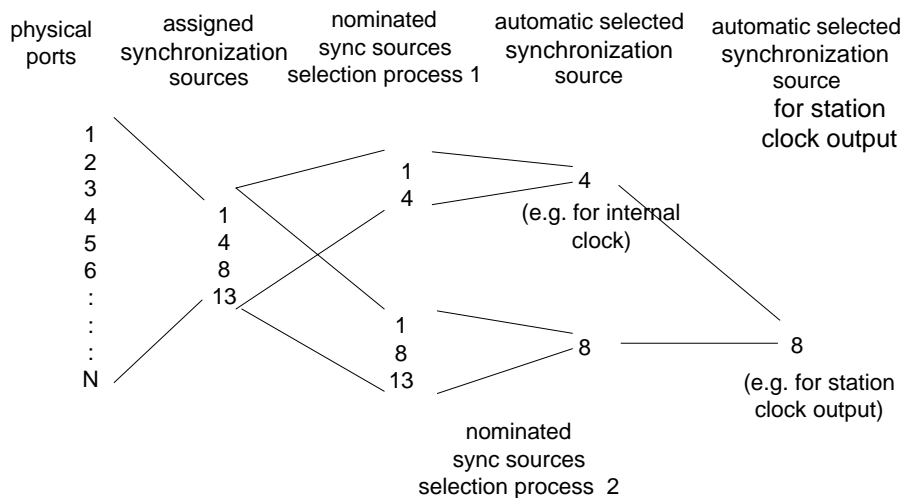
Figure 6: Visualization of the synchronization source selection process(es)

1) *Assignment of a physical port to be a synchronization source*: Select a (limited) set of interface signals (from the total set of interfaces) to act as synchronization sources.

   This is performed in the SD_C function by means of adding matrix connections between a group of inputs (connected to the server layer) and outputs (connected to the SD_TT_Sk functions).

2) *Nomination of a synchronization source for an automatic selection process*: Select a (sub)set of the synchronization sources to contribute to a selection process.

   This is performed in the NS_C function by means of assigning a priority to the synchronization source (see subclause 4.10).

3) *Automatic Selection Process*. Selects the "best" synchronization source of the set from nominated sources according to the selection algorithm (see subclause 4.12).

NOTE: The specifications in the present document allow a selection to be made between any set of synchronization interface signals input to a NE, independent of the actual synchronization network architecture deployed in the network. It is the network operator's responsibility to ensure that timing loops are not created.

4.7   Signal fail

SF for a synchronization source is activated in case of defects detected in the server layers. In addition an unconnected synchronization signal has also SF active in order to allow correct processing in the QL disabled mode. Inclusion of specific synchronization failures (e.g. exceeded frequency deviation, exceeded wander limits) as SF criteria for SSU are for further study.

In order to avoid reactions on short pulses or intermittent SF information, the SF information is passed through a hold-off and Wait to Restore (WTR) processes before it is considered by the selection process.

NOTE 1:   The delay of the SF information is only performed for the information passed to the selection process. The SF information for the main data path to the output of the NS_C function is not delayed.

In QL enabled mode the QL of a synchronization source with active SF is set to QL-FAILED. The selection process will react to this QL value instead of the SF signal in this mode.

NOTE 2:   Due to different persistence times for defect detection and the SSM acceptance process, a defect leading to SF could also result in a change of the QL value shortly before SF is activated. The implementation has to ensure that the selection process does not select a new synchronization source based on this intermediate QL value.

4.8   Hold-off time

The hold-off time ensures that short activation of SF are not passed to the selection process.

In QL-disabled mode SF shall be active for the hold-off time before it is passed to the selection process.

In QL-enabled mode a QL value of QL-FAILED shall exist for the hold-off time before it is passed to the selection process. In the mean time the previous QL value is passed to the selection process.

NOTE: Other QL values than QL-FAILED will be passed to the selection process immediately.

Separate hold-off timers are used for each input to a selection process (nominated source).

The hold-off time is fixed in the range of 300 ms to 1 800 ms.

4.9   WTR time

The WTR time ensures that a previous failed synchronization source is only again considered as available by the selection process if it is fault free for a certain time.

In QL-disabled mode after deactivation of SF, it shall be false for the WTR time before SF false is passed to the selection process. In the mean time SF true is passed to the selection process.

In QL-enabled mode after a change of the QL from QL-FAILED to any other value, the quality value shall be different from QL-FAILED for the WTR time before the new QL value is passed to the selection process. In the mean time the QL QL-FAILED is passed to the selection process.

Separate WTR timers are used for each input to a selection process (nominated source).

The WTR time is configurable in the range of 0 to 12 minutes in steps of 1 minute for all inputs of a selection process in common. The default value is 5 minutes.

Each WTR timer can be cleared with a separate Clear (CLR) command. If a WTR timer is cleared the new QL value (in QL-enabled mode) or SF value (in QL-disabled mode) is immediately passed to the selection process.

4.10   Synchronization source priorities

In order to define a preferred NS flow, priority values are allocated to assigned synchronization sources within a NE.

Different priorities reflect a preference of one synchronization source over the other. Equal synchronization source priorities reflect that no preference exists between the synchronization sources. Within the group of synchronization sources with equal priorities the selection process has a non-revertive behaviour.

A priority of "dis" (disabled) identifies that this assigned synchronization source is not nominated for the selection process.

Table 6: Priority order

Priority value	Order
1	highest
2		
3		
:		
K		
dis, undef	lowest

NOTE 1:   The priority value is not numerical ordered.
            The following relation is present: "1" > "2" > "3" > .. > "K" > "undef", "dis".

The priority value "undef" is associated with the unconnected signal of the NS_C function and is not configurable from the outside.

NOTE 2:   The assigning of equal priorities to synchronization sources in order to allow for non-revertive operation does not allow for a pre-defined initialization state of known synchronization configuration following failure of a higher priority source.

4.11   External commands (EXTCMD)

Several EXTCMDs are available to the user, (e.g. for maintenance purposes). These commands are independent and have different impact on the selection processes.

4.11.1   EXTCMDs per nominated synchronization source

It is possible to temporary remove a timing source as available synchronization source for the selection process.

This is controlled by the lockout commands. Lockout commands are accepted for nominated synchronization sources (synchronization sources that are not disabled) of each selection process.

The lockout status of a disabled synchronization source is "off".

NOTE: A locked out source is still nominated to the selection process and retains its synchronization source priority.

4.11.1.1   Set_Lockout#p command

The Set_Lockout#p command sets the lockout state of input p to "on". This causes this input to be no longer considered available by the selection process.

4.11.1.2   Clear_Lockout#p command

The Clear_Lockout#p command sets the lockout state of input p to "off". This causes this input to be considered available again by the selection process.

4.11.2   EXTCMDs per selection process

The activation and deactivation of EXTCMDs associated with the synchronization selection process are defined below. Furthermore only one of these EXTCMSs are active at a time as per the selection process.

4.11.2.1   CLR command

A CLR command clears the Forced Switch (FSw) and Manual Switch (MSw) commands.

4.11.2.2 Forced switch #p command

A FSw to #p command can be used to override the currently selected synchronization source, assuming the synchronization source #p is enabled and not locked out.

The FSw overrides the MSw and a subsequent FSw pre-empts the previous FSw.

If the source selected by the FSw command (#p) is disabled or locked out, the FSw command is automatically rejected.

The FSw command can be cleared by the CLR command.

> NOTE: A FSw command to a synchronization source #p which is in the SF state or has a QL of DNU in QL enabled mode, will result in the NE entering holdover.

4.11.2.3 Manual switch #p command

A MSw to #p command selects the synchronization source #p, assuming it is enabled, not locked out, not in SF condition, and has a QL better than DNU in QL enabled mode. Furthermore in the QL enabled mode, a MSw can be performed only to a source which has the highest available QL. As such, these conditions have the effect that manual switching can only be used to override the assigned synchronization source priorities.

A MSw request overrides a previous MSw request.

If the source selected by the MSw command (#p) is disabled, locked out, in SF, or has a QL of DNU or lower than one of the other source signals, the MSw command is automatically rejected.

The MSw command can be cleared by the CLR command.

4.12 Automatic reference selection process

One or more reference selection processes are operating independently to select the reference signal for the internal clock and, where present, the station clock output(s). However the SD connection function delivering SD_CI to the station clock output atomic functions (see figure 15) is only operated by operator command and not by an automatic process.

The selection process(es) can work in two distinct modes: QL-enabled, QL-disabled. If multiple selection processes are present in a NE, all processes work in the same mode.

The following is a brief description of the automatic reference selection process. The specific details (Specification and Description Language (SDL) diagrams) are defined in annex A.

4.12.1 QL-enabled mode

In QL-enabled mode the following parameters contribute to the selection process:

- QL;

- SF via QL-failed;

- priority;

- EXTCMDs.

If no overriding EXTCMDs are active, the algorithm selects the reference with the highest QL, which is not experiencing a SF condition. If multiple inputs have the same highest QL, the input with the highest priority is selected. For the case that multiple inputs have the same highest priority and QL, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

4.12.2   QL-disabled mode

In QL-disabled mode the following parameters contribute to the selection process:

- SF;

- priority;

- EXTCMDs.

If no overriding EXTCMDs are active, the algorithm selects the reference with the highest priority which is not experiencing a SF condition. For the case that multiple inputs have the same highest priority, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

4.13   Timing loop prevention

4.13.1   Station clock input used as a source for station clock output

This specification allows the use of the station clock input as a source for the station clock output, either directly or via the SEC. When this functionality is present in a NE, the operator should be aware that this functionality is intended for timing quality monitoring purposes and that its use for other purposes could result in timing loops being created. If a timing loop could be created, the operator should prevent that by a reconfiguration of the synchronization architecture.

4.13.2   Between NEs with SEC type clocks

The master-slave synchronization over several NEs with multiple possible synchronization inputs for protection of synchronization as defined in EN 300 462-2-1 [9] could lead to timing loops between NEs. To avoid timing loops a NE should insert a SSM/TM value of DNU in direction of the NE which is used as actual synchronization source for the NE clock (SEC).
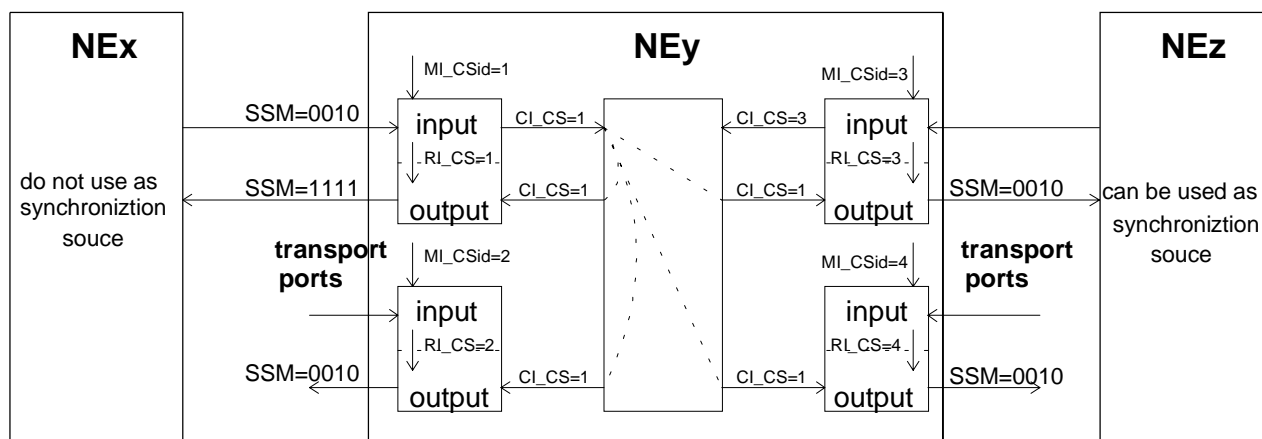

Figure 7: Automatic DNU generation in a NE with SEC timing

The Clock Source identifier (CSid) has been introduced to support the above feature as shown in figure 7. To each transport and station clock input port a unique CSid is assigned (MI_CSid). This ID is processed in the synchronization layers together with the clock and QL of the port. The CSid of the selected source for the SEC is distributed to all output ports. If a transport output port receives the same CSid as its associated input port (signalled via RI_CS) via the SD layer (SD_CI_CS) the outgoing SSM/TM is set to DNU.

> NOTE: The above principle may be extended to generate DNUs on groups, "bundle", of ports, which are known to have the same timing source. A provisional agreement is that processing of DNU generation on all the ports of the "bundle" when any one of them has been selected as the reference source does not require additional information between the atomic functions. Use of identical CS within the "bundle" has been considered but this is left for further study.

4.13.3   Between NEs with a SEC clock and a NE or SASE with a SSU clock and only one link

> NOTE: As indicated in the scope of the present document, the SSM algorithm is not specified for SSU.

A NE can be interconnected with a SASE via its (2 MHz and/or 2 Mbit/s) station clock input and output ports. If the SASE is used as the actual synchronization source for the NE clock the mechanism defined in subclause 4.13.2 above has to be extended to support automatic DNU insertion also for this case.

It is not possible to detect that the SASE has selected the station clock output port of the NE as actual CS, but several conditions exist that indicate that the station clock output port is not used as CS by the SASE.

If a NE is connected to a SASE, Remote Information (RI) is exchanged between the normally uni-directional station clock input and output ports connected to the same SASE. The RI transfers the CSid (CI_CS RI_CS) and in addition in case of QL enabled mode the QL (CI_QL RI_QL) of the Clock signal (CK) selected for the station clock output to the station clock input. The user has to enable this feature by activating the remote indication connection between the station clock ports.

4.13.3.1   QL/SSM processing supported between SASE and NE

If QL/SSM processing is supported by the SASE and all other involved components (NE, station clock ports) different SSM values at the output and input station clock ports indicate that the output port is not used as CS by the SASE. As long as the transmitted QL at the station clock output and the received QL at the station clock input of the NE are identical, it is assumed that the SASE selects the station clock output of the NE as reference clock. The station clock input port uses in this case the remote CSid (from the station clock output) as CSid for the CK to the selection process (RI_CS CI_CS) instead of its own CSid (MI_CSid). This will result in DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock (see figure 8). If the transmitted and received QL are no longer identical, the remote CSid is replaced by the own CSid (MI_CSid) and the automatic DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock is removed (see figure 9). Their are still conditions in which the SASE does not select the station clock output of the NE as synchronization source, but the automatic DNU insertion is still performed, e.g. if the SASE selects another source with the same QL as the station clock output of the NE (see figure 10).

Figure 8: Automatic DNU generation in a NE with SASE timing (SSM/QL supported)
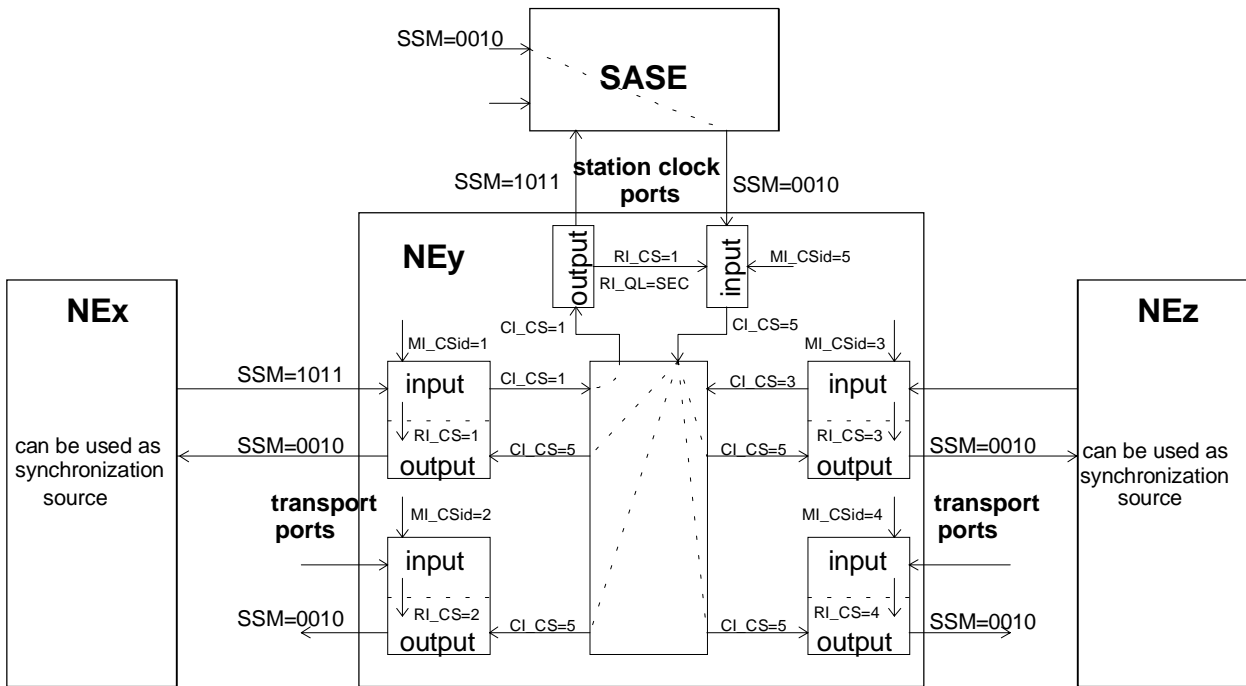
Figure 9: Removal of automatic DNU generation in a NE with SASE timing (SSM/QL supported)
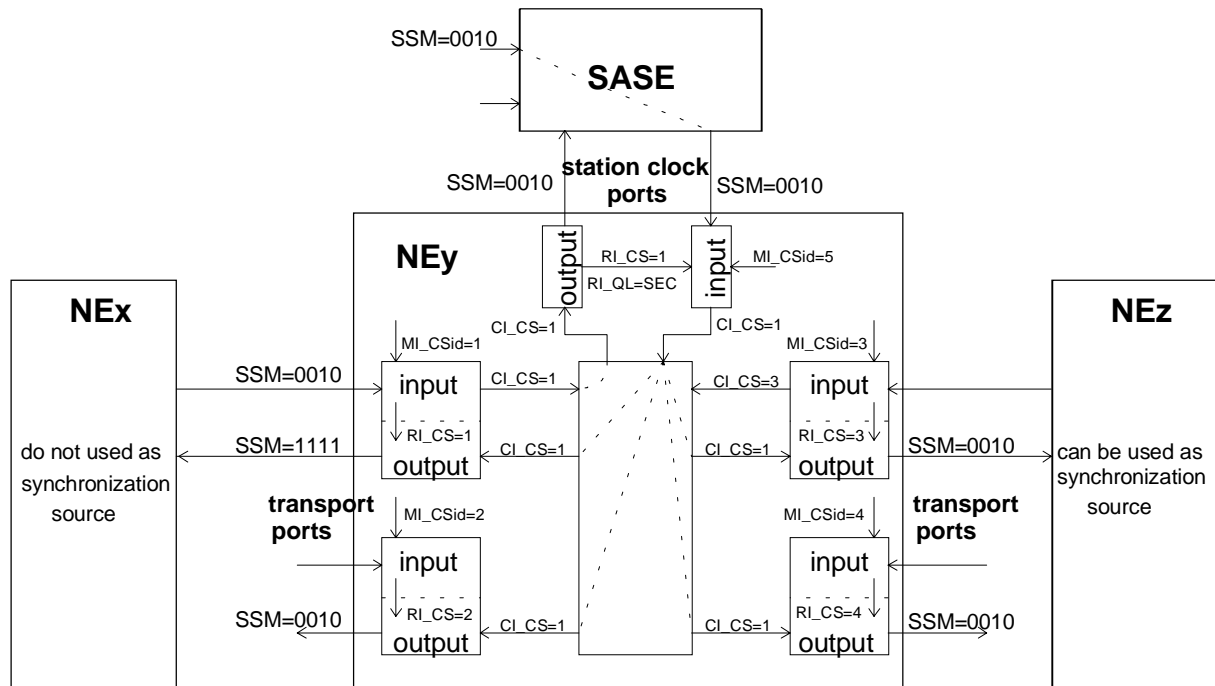
Figure 10: Limitation of automatic DNU generation in a NE with SASE timing (SSM/QL supported)

4.13.3.2   QL/SSM processing not supported between SASE and NE

If QL/SSM processing is not supported by the SASE, station clock ports or NE, a squelched/AIS station clock output port is the only criteria that indicates that the output port is not used as CS by the SASE. As long as the station clock output is not squelched (for 2 MHz station clock ports) or set to AIS (for 2 Mbit/s station clock ports), it is assumed that the SASE selects the station clock output of the NE as reference clock. The station clock input port uses in this case the remote CSid (from the station clock output) as CSid for the CK to the selection process (RI_CS CI_CS) instead of its own CSid (MI_CSid). This will result in DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock (see figure 11). If the station clock output is squelched or set to AIS, the remote CSid is replaced by the own CSid (MI_CSid) and the automatic DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock is removed (see figure 12). Their are still conditions in which the SASE does not select the station clock output of the NE as synchronization source, but the automatic DNU insertion is still performed, e.g. if the SASE selects another source if the station clock output is still transmitting valid TI (see figure 13).
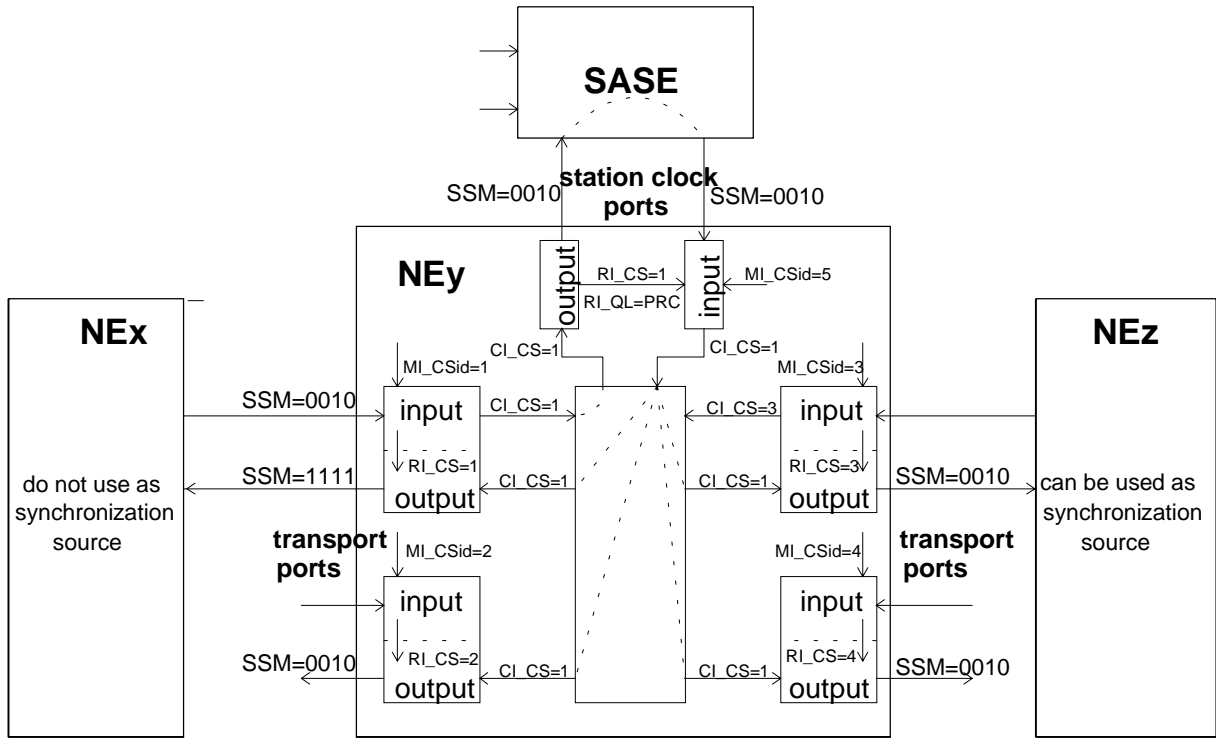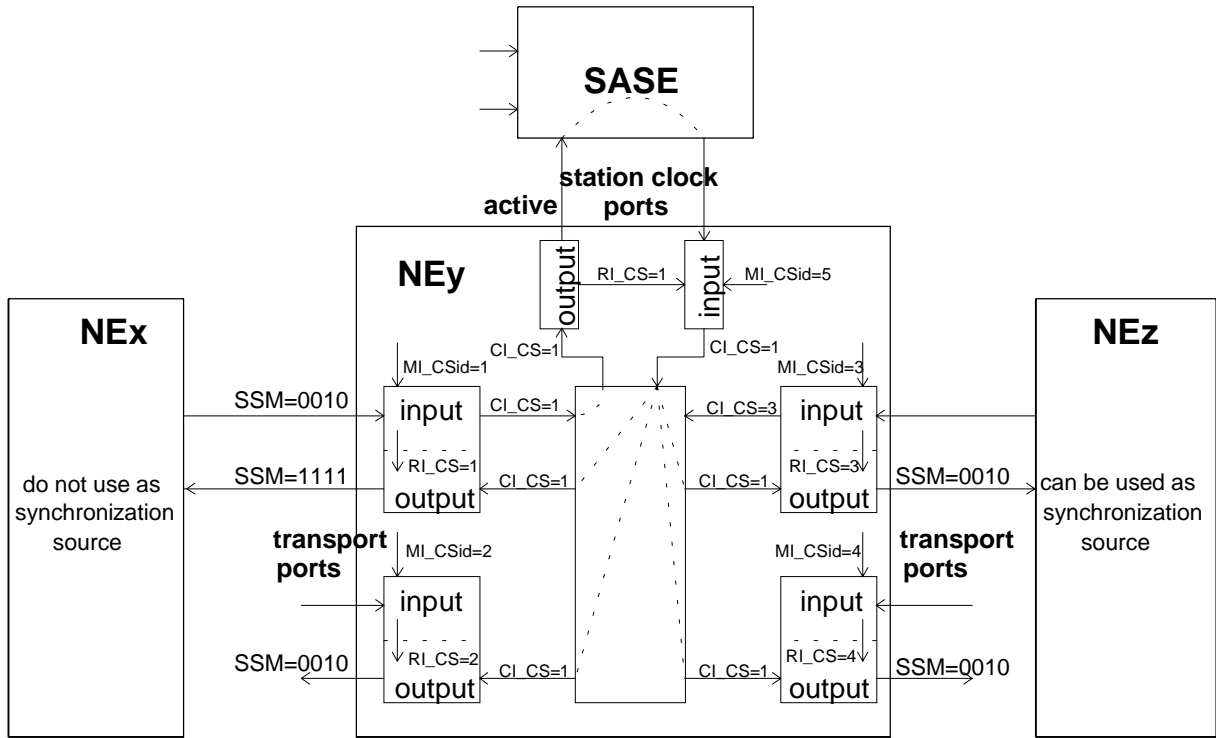
Figure 11: Automatic DNU generation in a NE with SASE timing (SSM/QL not supported)
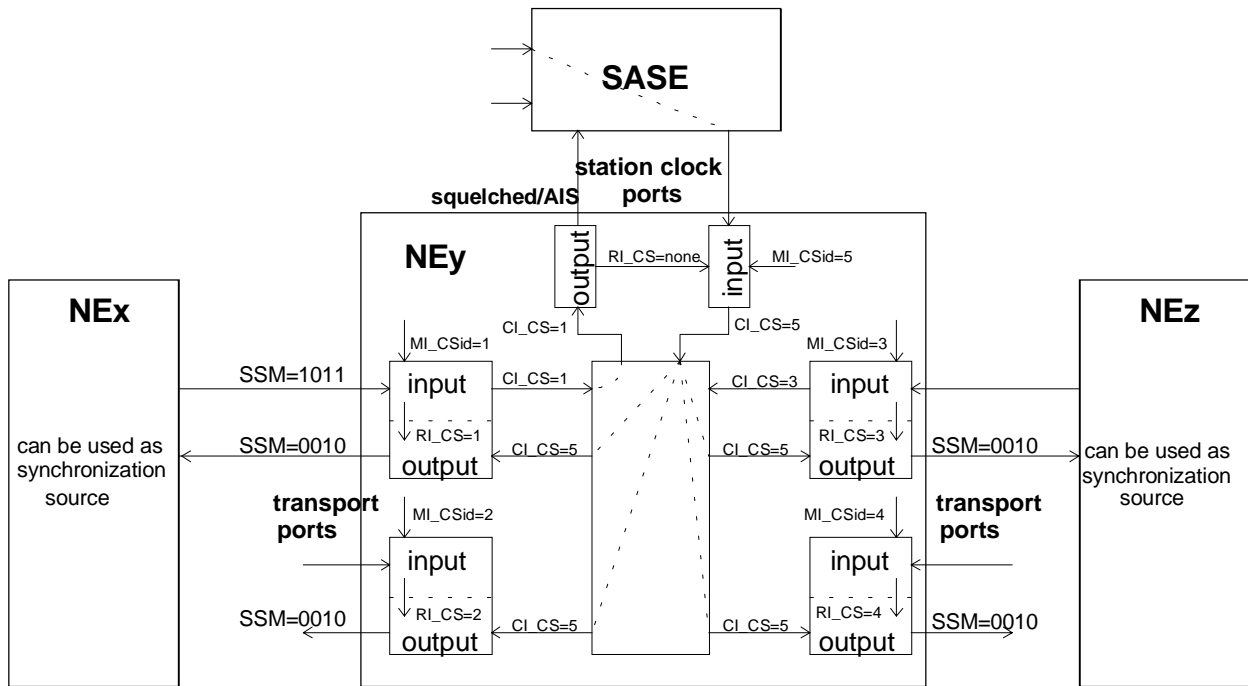
Figure 12: Removal of automatic DNU generation in a NE with SASE timing (SSM/QL not supported)
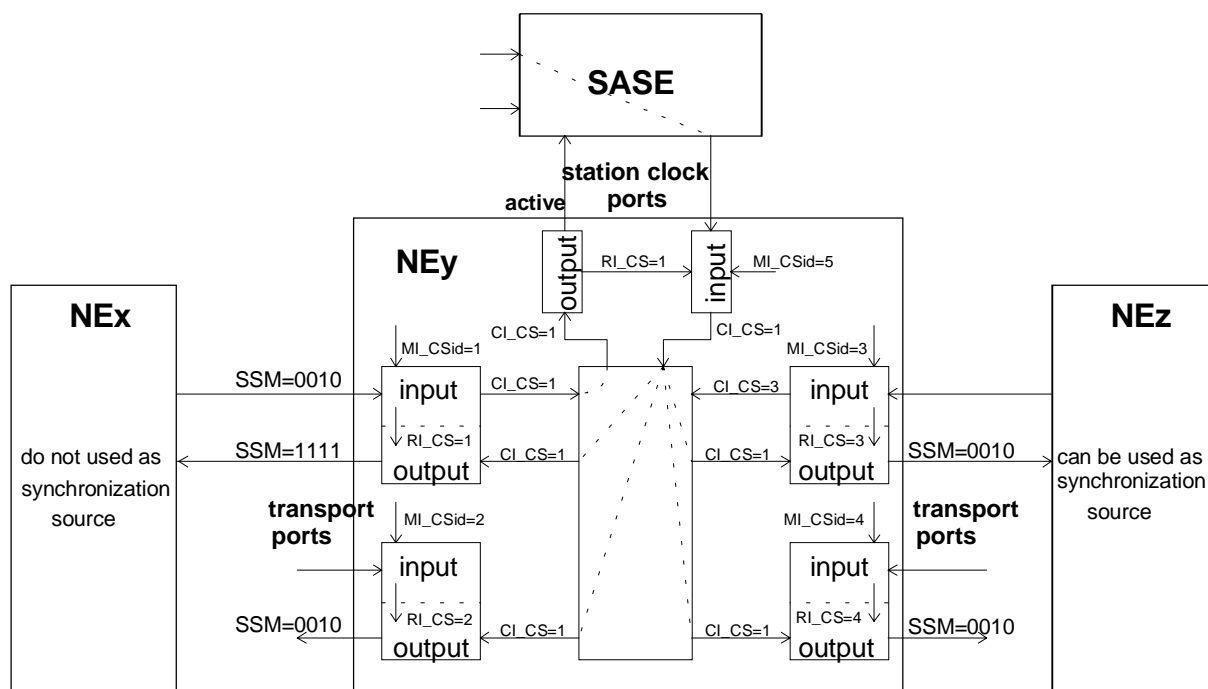
Figure 13: Limitation of automatic DNU generation in a NE with SASE timing (SSM/QL not supported)

4.13.4   Between NEs with a SEC clock and a NE or SASE with a SSU clock and several links

A generalization of the mechanism described in subclause 4.13.3, applicable when SEC and SSU are interconnected by several links, is for further study.

4.14   Delay times for NEs with SEC

The following delay times are caused by the atomic functions which perform the selection of the input synchronization reference. Three delays are defined:

-    Holdover message delay T_{HM}.

This delay applies when the SEC shall enter holdover because of Loss Of Signal (LOS) of the input reference and lack of any other available reference. When this event occurs the SEC goes immediately into holdover but changes the output SSM to the holdover code after a delay which has been defined to be between 500 ms and 2 000 ms.

-    Non switching message delay T_{NSM}.

This delay applies when the QL of the selected synchronization source changes but no switchover to another source is performed. The outgoing SSM/TM follows this change at the input within a time defined to be less than 200 ms.

-    Switching message delay T_{SM}.

This delay applies when a new synchronization source is selected. The output SSM change, if any, is done after a delay that has been defined to be between 180 ms and 500 ms.

A full description of these times is in annex D.

Change of the synchronization direction within a chain of 20 SECs

The above delay times allow the reversal of the synchronization flow in a chain of 20 NEs with SEC timing within 15,6 s. The change of the synchronization direction through 20 SECs requires 39 steps, as shown in figure 14.

Ref1   Ref 2

```
      ┌────┐   ┌────┐   ┌────┐   ┌────┐   ┌────┐
      │ NE │───│ NE │───│ NE │───│ NE │───│ NE │
      └────┘   └────┘   └────┘   └────┘   └────┘
        1                  n                 20
```
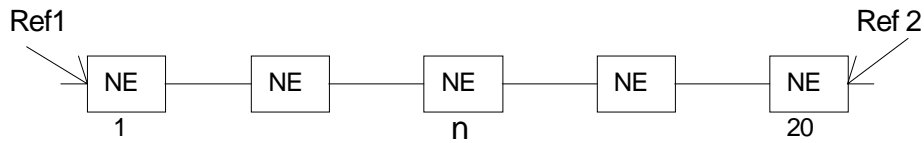
Figure 14: Linear chain of SECs

Step	Action
1	Ref 1 disappears from the first NE of the chain, NE 1 goes into holdover mode and transmits a new SSM. (T_{HM} 2 s maximum)
2 to 19	NE n (n = 2,3,..,19) transmits the new SSM without switch of reference to NE n. (T_{NSM} 200 ms maximum)
20	NE 20 switches to Ref 2. (T_{SM} 500 ms maximum)
21 to 39	NE n (n = 19,18,..,1) change to sync received from NE n+1. (T_{SM} 500 ms maximum)

This leads to a maximum restoration time of 15,6 s (T_{HM} +18 T_{NSM} +20 T_{SM}).

4.15   Delay times for NEs with SSU or for SASE

For further study.

4.16   Synchronization layer functions

The atomic functions which are involved in the transport of synchronization within the NE are shown in the following figure.

This figure shows two synchronization layers plus the TL:

a) The SD layer: This layer terminates and adapts the synchronization trails to the NS layer and performs a pre-selection of candidate input ports.

b) The NS layer: This layer performs the selection of a timing reference.

c) The TL providing the synchronization related SD_CI information.
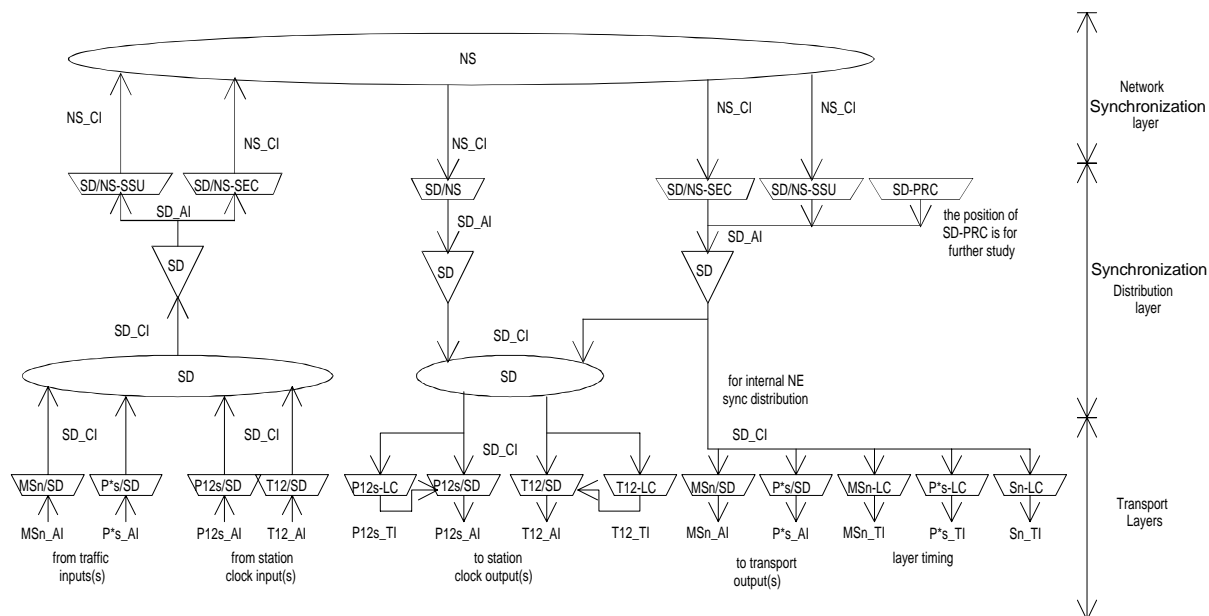
Figure 15: SD and NS layer atomic functions

The relation between the current naming of synchronization signals in ITU-T Recommendation G.783 [15] and in EN 300 417-1-1 [6] is shown on the following table.

Table 7: Naming of synchronization signals

ITU-T Recommendation G.783 [15] naming	EN 300 417-1-1 [6] naming
T0	SD_CI signal for internal NE sync distribution
T1	SD_CI signal derived from an STM-N (OSn/RSn/MSn) signal
T2	SD_CI signal derived from a 2 Mbit/s (E12/P12s) traffic carrying signal
T3	SD_CI signal derived from a 2 MHz station clock (T12) input signal
T4	SD_CI signal towards a 2 MHz station clock (T12) output signal
no name	SD_CI signal derived from a 34 Mbit/s synchronous (E31/P31s) signal
no name	SD_CI signal derived from a 140 Mbit/s synchronous (E4/P4s) signal
no name	SD_CI signal towards a 2 Mbit/s station clock (E12/P12s) output signal
no name	SD_CI signal derived from a 2 Mbit/s station clock (E12/P12s) signal

4.17   Overview of the processes performed within the atomic functions

A list of the synchronization atomic functions and a short description of their functionality is given in table 8. For a more detailed description see clauses 5 to 8.

Table 8: Functional overview of atomic functions

Atomic function	Functionality
XX-LC_A_So	Generation of the layer timing.
XX/SD_A_Sk	Access to reference clock. SSM(TM) acceptance and extraction of QL. Generate QL-NotSupported if signal does not support SSM. Generation of CS.
XX/SD_A_So	Insertion of QL into SSM(TM). Generate QL-DNU or Squelch to prevent timing loops.
SD_C	Pre-selection of transport interfaces as possible synchronization sources. Selection of sources for the station clock outputs.
SD_TT_Sk	Report of QL to management. Manual insertion of a fixed QL value.
SD_TT_So	None.
SD/NS-SEC_A_Sk	None.
SD/NS-SSU_A_Sk	For further study.
SD/NS_A_So	Generation of the clock, for the station clock outputs from the selected synchronization reference.
SD/NS-SEC_A_So	Generation of holdover, locked and free running modes timings. Generation of the NE clock (SEC type), locked to the selected synchronization reference.
SD/NS-SSU_A_So	Generation of the NE clock (SSU type), locked to the selected synchronization reference. The functionality and the position is for further study.
SD/NS-PRC_A_So	Generation of the NE clock (PRC) type. The functionality and the position is for further study.
NS_C	Selection of synchronization reference sources.

5   Synchronization distribution layer atomic functions
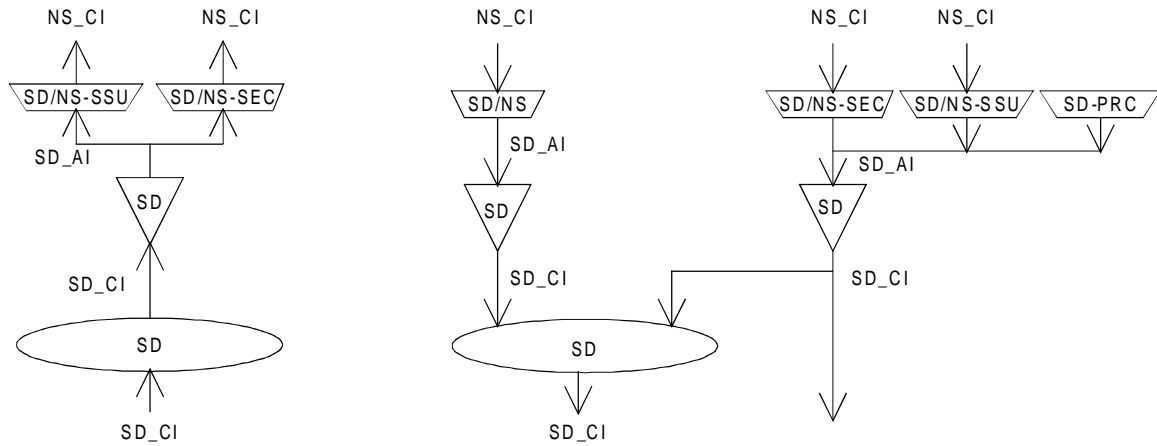
Figure 16: SD layer atomic functions

SD Layer CP

The CI at this point is a CK with associated server SF, QL and CSid.

SD Layer Access Point (AP)

The Adaptation Information (AI) at this point is a CK with associated trail SF, QL and CSid.

5.1 SD Connection function (SD_C)

Symbol:

SD_CI

SD_C_MI → SD
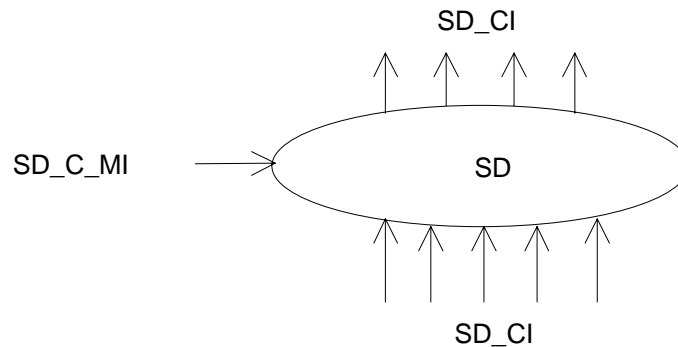
SD_CI

Figure 17: SD_C symbol

Interfaces:

Table 9: SD_C input and output signals

Input(s)	Output(s)
per SD_CI, n x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS per input output CP SD_C_MI_ConnectionPortIds	per SD_CI, m x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS

Processes:

In the SD_C function SD Layer CI is routed between input Termination Connection Points (TCPs) and output TCPs by means of matrix connections.

> NOTE 1: Neither the number of input/output signals to the connection function, nor the connectivity is specified in the present document. That is a property of individual NEs.

Routing: The function shall be able to connect a specific input with a specific output by means of establishing a matrix connection between the specified input and output. It shall be able to remove an established matrix connection.

> NOTE 2: Broadcast connections are handled as separate connections to the same input CP.

Unconnected SD signal generation: The function shall generate an unconnected SD signal, specified as: SSF true, CS value None, QL value QL-UNC and undefined clock.

> NOTE 3: The unconnected signal is a logical signal defined for the purpose of this formal specification; it is not observable at any of the NEs transport interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected SD signal to the output.

Defect correlations: None.

Performance monitoring: None.

5.2   SD Trail Termination (TT) functions

5.2.1   SD TT source function (SD_TT_So)

Symbol:
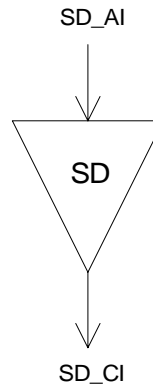
Figure 18: SD_TT_So symbol

Interfaces:

Table 10: SD_TT_So input and output signals

Input(s)	Output(s)
SD_AI_CK	SD_CI_CK
SD_AI_QL	SD_CI_QL
SD_AI_CS	SD_CI_CS
SD_AI_TSF	SD_CI_SSF

Processes:

Output SD_CI_CK is derived from and locked to SD_AI_CK.

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF

Defect correlations: None.

Performance monitoring: None.

5.2.2 SD TT sink function (SD_TT_Sk)

Symbol:
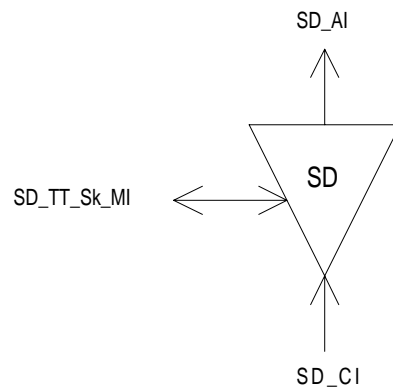
Figure 19: SD_TT_Sk symbol

Interfaces:

Table 11: SD_TT_Sk input and output signals

Input(s)	Output(s)
SD_CI_CK	SD_AI_CK
SD_CI_QL	SD_AI_QL
SD_CI_SSF	SD_AI_TSF
SD_CI_CS	SD_AI_CS
SD_TT_Sk_MI_QLoverwrite	SD_TT_Sk_MI_cSSF
SD_TT_Sk_MI_QLfixedValue	SD_TT_Sk_MI_QL
SD_TT_Sk_MI_QLmode	
SD_TT_Sk_MI_Tpmode	
SD_TT_Sk_MI_SSF_Reported	

Processes:

This function terminates a synchronization trail transmitted via one of the synchronization information's TLs, processes and reports the incoming quality. It can operate in QL-enabled mode and QL-disabled mode.

QL-disabled mode:

In QL disabled mode the function shall report the status of the trail (MI_cSSF).

QL-enabled mode:

In QL-enabled mode the function shall report the status of the trail (MI_cSSF) and the incoming QL value (CI_QL) via MI_QL.

In QL-enabled mode AI_CS=CI_CS, in pass-through and overwrite operations.

The function shall support the ability to pass through or overwrite the incoming QL information.

Pass through:

The QL output (AI_QL) shall be related to the QL input (CI_QL) signal as specified in clause 4.

Overwrite:

The QL output (AI_QL) is a fixed value provisioned via MI_QLfixedValue.

The selection between pass through and overwrite mode shall be controlled via MI_QLoverwrite. The default value of MI_QLoverwrite shall be FALSE. The default for MI_QLfixedValue shall be QL-DNU.

Table 12: Conversion of quality levels

CI_QL	MI_QLoverwrite	CI_SSF	AI_QL
QL-INV0	false	false	QL-INV
QL-INV1	false	false	QL-INV
QL-PRC	false	false	QL-PRC
QL-INV3	false	false	QL-INV
QL-SSUT	false	false	QL-SSUT
QL-INV5	false	false	QL-INV
QL-INV6	false	false	QL-INV
QL-INV7	false	false	QL-INV
QL-SSUL	false	false	QL-SSUL
QL-INV9	false	false	QL-INV
QL-INV10	false	false	QL-INV
QL-SEC	false	false	QL-SEC
QL-INV12	false	false	QL-INV
QL-INV13	false	false	QL-INV
QL-INV14	false	false	QL-INV
QL-DNU	false	false	QL-DNU
QL-NSUPP	false	false	QL-NSUPP
QL-UNC	false	true	QL-FAILED
all	true	false	MI_QLfixedValue
all	x	true	QL-FAILED

Defects: None.

Consequent actions:

   aTSF   ←   CI_SSF

Defect correlations:

   cSSF   ←   MON and CI_SSF and SSF_Reported

Performance monitoring: None.

5.3   SD adaptation functions

5.3.1   SD layer to NS layer SEC quality adaptation source function (SD/NS-SEC-A_So)

Symbol:

NS_CI

SD/NS-SEC_A_So_MI ⟷ SD/NS-SEC
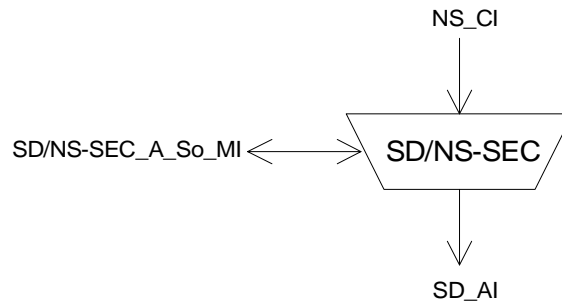
SD_AI

Figure 20: SD/NS-SEC_A_So symbol

Interfaces:

Table 13: SD/NS-SEC_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK	SD_AI_CK
NS_CI_QL	SD_AI_QL
NS_CI_SSF	SD_AI_CS
NS_CI_CS	SD/NS-SEC_A_So_MI_CkMode
SD/NS-SEC_A_So_MI_CkOperation	SD/NS-SEC_A_So_MI_cLTI
SD/NS-SEC_A_So_MI_ QLMode	

Processes:

This function generates a SEC type system clock as defined in EN 300 462-2-1 [9] and specified in EN 300 462-5-1 [11]. The function shall operate in QL-enabled or QL-disabled mode as selected by MI_QLMode.

The function shall support three types of operation:

- forced free running operation working in the free run mode;

- forced holdover operation, working in the Holdover mode (HO);

- normal operation, working in the locked or HO depending on the input signals.

These 3 types of operation are activated by user management input (CkOperation) while modes, defined in EN 300 462-1-1 [8], are automatically activated by the status of input signals. Figure 21 shows the relationship between types of operation and modes.
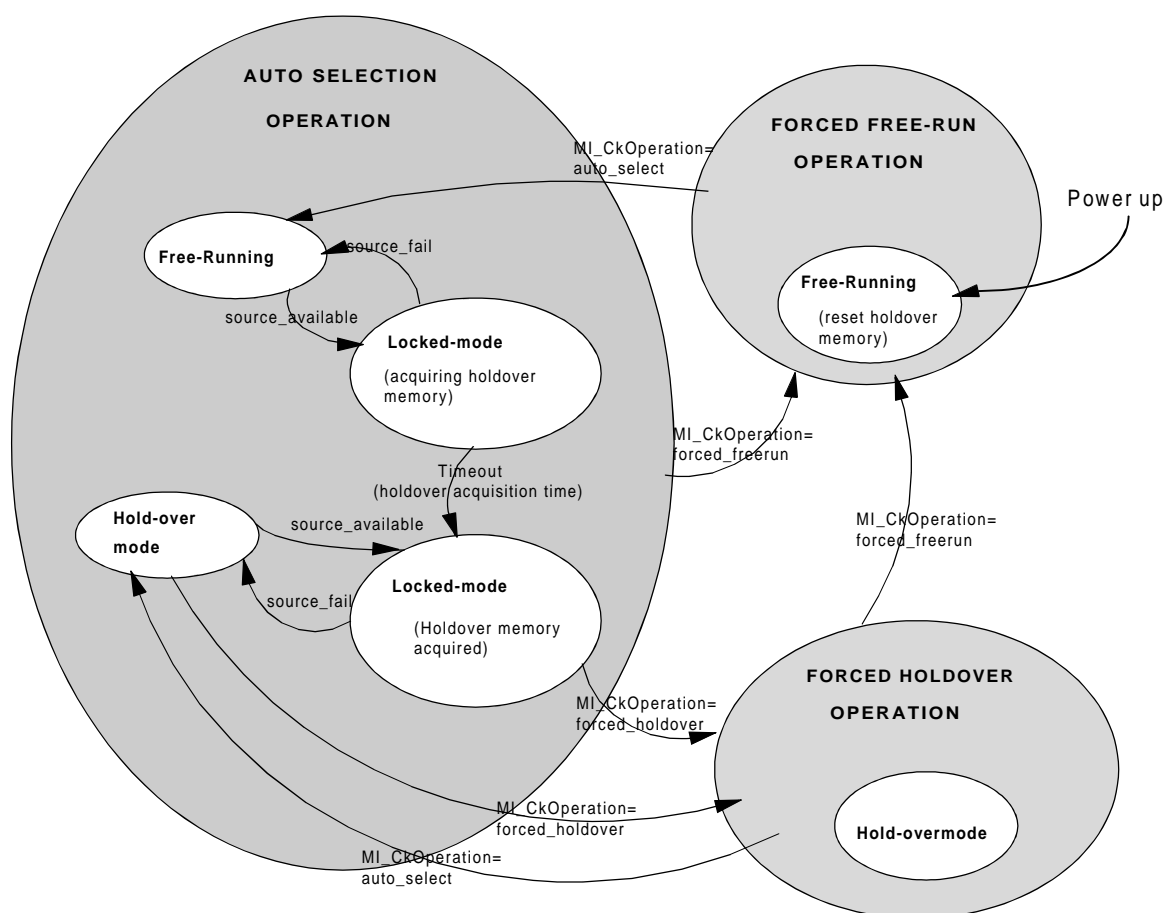
Figure 21: Operational types

Bandwidth, transients, pull in and pull out ranges, noise, input and output jitter for Locked Mode (LO) operation, holdover accuracy and output phase deviation for HO operation, frequency accuracy, transients, noise and output jitter for freerun mode operation shall be as specified in EN 300 462-5-1 [11].

Forced Free-running operation:

This type of operation is activated by a management command, the equipment is in free run mode.

- Clock generation:

    The outgoing clock (AI_CK) is not defined by an incoming reference or stored incoming reference data in the holdover memory. The hold-over memory is reset to a default value.

- QL processing (in QL-enabled mode):

    The outgoing QL of the free running mode is QL-SEC.

- CS processing:

    The outgoing CS of the free running mode is None.

Forced holdover operation:

This type of operation is activated by a management command, the equipment is in HO.

- Clock generation:

    The outgoing clock (AI_CK) is defined by stored reference data in the holdover memory.

- QL processing (in QL-enabled mode):

    The outgoing QL of the HO is QL-SEC.

- CS processing:

    The outgoing CS of the HO is None.

Auto selection operation:

This type of operation is activated by a management command.

- Clock generation:

    The auto selection operation works according two modes, locked and holdover:

    - LO:

        In the LO the outgoing clock (AI_CK) is locked to the incoming reference clock (CI_CK) and the holdover memory is constantly updated with this reference clock.

        As shown on figure 21, some time is required before the holdover memory is acquired.

    - HO:

        The HO conforms to the HO defined above. The holdover memory is no longer updated by the incoming reference clock.

    The selection between the two modes is done automatically depending on the quality of the incoming reference signal and the selected QL Mode.

- QL-enabled mode:

    The LO is selected if the incoming reference is not in the SF state and the QL of the incoming reference is better or equal to QL-SEC.

    The HO is selected without delay when the incoming reference goes into the SF state or the QL of the incoming signal is lower than QL-SEC.

    The HO is left when both the SF state and the QL of the incoming signal is equal or better than QL-SEC.

    - QL-disabled mode:

        The LO is selected if the incoming reference is not in the SF state.

        The HO is selected when the incoming reference goes into the SF state.

        The actual mode is reported to the management (MI_CkMode).

    - QL processing (in QL-enabled mode):

        If the function is in the LO the outgoing QL follows the incoming QL.

        In case of a change of the selected synchronization source (which is detected by a change of the incoming CS), the outgoing QL shall be set to the new incoming QL after the settling time t_s, to allow the internal oscillator to adjust to a possible frequency change.

        If the incoming QL changes without a change of the selected synchronization source (no change of the CI_CS), the outgoing QL shall follow without settling time.

If the function is in the HO, the outgoing QL shall be set to QL-SEC as soon as the incoming CS value is "None" or if the incoming QL is too low (NS_CI_QL<"QL-SEC").

After leaving the HO, the outgoing QL shall be set to the new incoming QL after the settling time t_s.

The settling time t_s shall be in the range of 180 ms to 300 ms.

- CS processing:

Normally the outgoing CS shall follow the incoming CS immediately.

If the function is in the HO due to a too low QL value of the selected source (NS_CI_QL<"QL-SEC"), the outgoing CS shall be set to "None".

Defects:

The function shall detect a Loss of Timing Inputs (dLTI) if a unconnected signal is present at its CP (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "None" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS≠"None" for at least Y seconds. The values of X and Y are for further study.

Consequent actions: None.

Defect correlation:

   cLTI   ←   dLTI

Performance monitoring: None.

5.3.2 SD layer to NS layer SEC quality adaptation sink function (SD/NS-SEC_A_Sk)

Symbol:
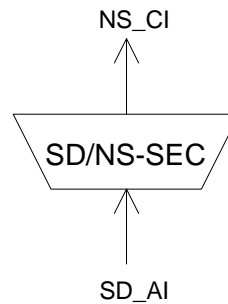
NS_CI

SD/NS-SEC

SD_AI

Figure 22: SD/NS-SEC_A_Sk symbol

Interfaces:

Table 14: SD/NS-SEC_A_Sk input and output signals

Input(s)	Output(s)
SD_AI_CK	NS_CI_CK
SD_AI_QL	NS_CI_QL
SD_AI_TSF	NS_CI_SSF
SD_AI_CS	NS_CI_CS

Processes:

This function connects input with output only. Currently no processes are defined within this function.

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF

Defect Correlation: None.

Performance monitoring: None.

5.3.3 SD layer to NS layer SSU quality adaptation source function (SD/NS-SSU-A_So)

This function is for further study.

5.3.4 SD layer to NS layer SSU quality adaptation sink function (SD/NS-SSU_A_Sk)

This function is for further study.

5.3.5 SD layer to NS layer PRC quality adaptation source function (SD/NS-PRC-A_So)

This function is for further study.

5.3.6 SD layer to NS layer adaptation source function (SD/NS_A_So)

Symbol:
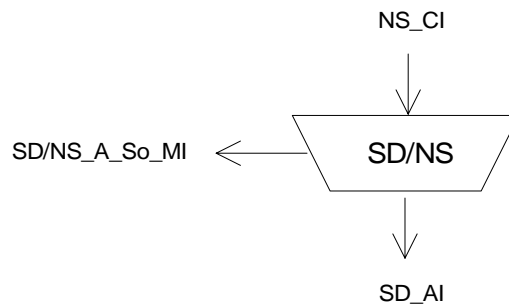
Figure 23: SD/NS_A_So symbol

Interfaces:

Table 15: SD/NS_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK	SD_AI_CK
NS_CI_QL	SD_AI_QL
NS_CI_SSF	SD_AI_CS
NS_CI_CS	SD_AI_TSF
	SD/NS_A_So_MI_cLTI

Processes:

This function produces the station output clock process.

Wander limitation: The wander at the output of this function shall be within the Maximum Time Interval Error (MTIE) mask specified in subclause 6.1 figure 2 of EN 300 462-5-1 [11].

> NOTE: There might be a need for an AIS generator, this is for further study.

Defects:

The function shall detect a Loss of Timing Inputs (dLTI) if a unconnected signal is present at its CP (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "None" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS≠"None" for at least Y seconds. The values of X and Y are for further study.

Consequent actions:

> aTSF   ←   CI_SSF

Defect Correlation:

> cLTI   ←   dLTI

Performance monitoring: None.

6 NS layer atomic functions

Within this layer the same connection function is used for one or two independent selection processes which may have independent inputs:

- a single selection of an input reference for the NE SD;

- a single or no selection of an input reference for the station clock output.

The use of several independent selection processes for this station clock output is for further study.

These two processes shall work in the same QL mode.
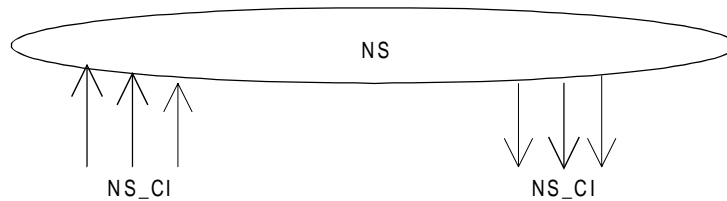
Figure 24: NS layer atomic functions

NS Layer CP.

The CI at this point is a CK with associated server SF, QL and CSid.

6.1 NS_connection functions (NS_C)

Symbol:
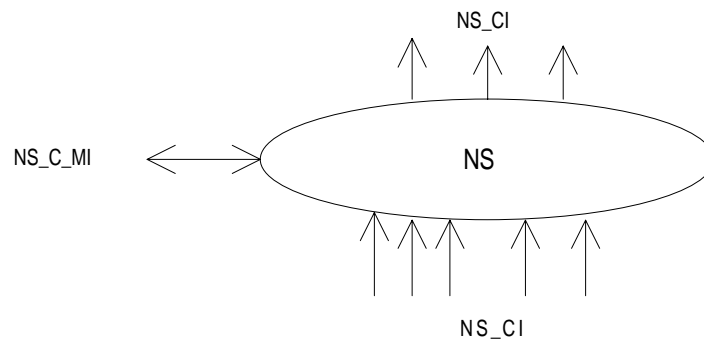
Figure 25: NS_C symbol

Interfaces:

Table 16: NS_C input and output signals

Input(s)	Output(s)
per input: NS_CI_CK NS_CI_SSF NS_CI QL NS_CI_CS per function: NS_C_MI_Qlmode per selector: NS_C_MI_WTR NS_C_MI_EXTCMD per input of a selector: NS_C_MI_priority NS_C_MI_CLR_WTR NS_C_MI_Set_lockout NS_C_MI_Clr_Lockout	per output: NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS per selector: NS_C_MI_Selected Input NS_C_MI_Reject_Request per input of a selector: NS_C_MI_State

Processes:

This function performs one or more independent selection processes. Each selection process selects a synchronization source out of the nominated set of synchronization source inputs determined by the selection algorithm.

The function can operate in QL enabled or disabled mode as defined by MI_QLmode.

NOTE 1: The number of input signals to the connection process and the amount of connection processes in the function are not specified in the present document. That is a property of individual NEs. Examples are presented in annex C.

Automatic reference selection process:

The function shall perform the automatic reference selection process as defined in subclause 4.6 and annex A.

EXTCMDs:

The function shall support the use of EXTCMDs as defined in subclause 4.11.

Priority:

The function shall support the use of synchronization source priorities as defined in subclause 4.10.

Holdoff time:

The function shall support a holdoff timer per input of a selection process (nominated source) as defined in subclause 4.8.

WTR time:

The function shall support a WTR timer per input of a selection process (nominated source) as defined in subclause 4.9.

Via MI_CLR_WTR the WTR timer can be cleared before the WTR time is expired.

Signal fail extension:

For each input to a selection process the SF information to the Selector is a combination (OR function) of the incoming SF information (CI_SSF) and the SF information delayed by the WTR and holdoff process. Detailed information is provided in annex A, figure A.1.

SF[m] = CI_SF[m] or WTR/HO[CI_SF[m]]

Status report:

The state of each input to a selection process (available, failed, WTR) shall be reported via MI_State.

The actual selected source of a selection process shall be reported via MI_SelectedInput.

Unconnected NS signal generator:

The function shall generate an unconnected NS signal. The unconnected NS signal has a undefined clock, a QL of QL-UNC, a CS value of "None" and SF true.

NOTE 2: This signal is a logical signal defined for the purpose of this formal specification; it is not observable as such at any of the NEs interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected NS signal to the output.

Defect Correlations: None.

Performance monitoring: For further study.

# 7	TL to SD layer atomic function

## 7.1	STM-1 multiplex section adaptation functions

### 7.1.1	STM-1 multiplex section to sd adaptation source (MS1/SD_A_So)

Symbol:

Figure 26: MS1/SD_A_So symbol

Interfaces:

Table 17: MS1/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS1_TI_CK MS1_TI_FS MS1_RI_CS MS1/SD_A_So_MI_SSMdis MS1/SD_A_So_MI_QLmode	MS1_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [1].

The SSM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). Table 18 presents the relation between the existing set of QLs and the output SSM.

Table 18: Quality level set coding into SSM

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

> if (MI_QLmode== dis)
>
> then   S1[5-8] = 1111
>
> else   if (RI_CS == CI_CS) or (SSMdis == true)
>
> then   S1[5-8] = 1111
>
> else   S1[5-8] = SSM[CI_QL]
>
> fi
>
> fi

Defect Correlations: None.

Performance monitoring: None.

7.1.2   STM-1 multiplex section to SD adaptation sink (MS1/SD_A_Sk)

Symbol:

SD_CI

MS1/SD_A_Sk_MI ⟶ ⟶│ MS1/SD │⟶ ⟶ MS1_RI
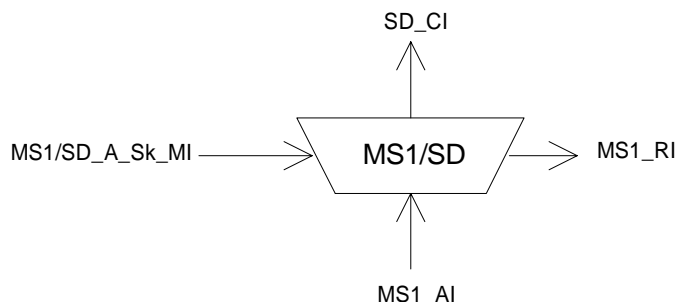
MS1_AI

Figure 27: MS1/SD_A_Sk symbol

Interfaces:

Table 19: MS1/SD_A_Sk input and output signals

Input(s)	Output(s)
MS1_AI_D	SD_CI_CK
MS1_AI_CK	SD_CI_SSF
MS1_AI_FS	SD_CI_CS
MS1_AI_TSF	SD_CI_QL
MS1/SD_A_Sk_MI_SSMsupp	MS1_RI_CS
MS1/SD_A_Sk_MI_CSid	
MS1/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [1]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

    if (MI_QLmode == disabled) or (MI_SSMsupp == false)

    then   CI_QL = QL-NSUPP

    else   CI_QL = QL[SSM]

    fi

Defect Correlations: None.

Performance monitoring: None.

7.2   STM-4 multiplex section adaptation functions

7.2.1   STM-4 multiplex section to SD adaptation source (MS4/SD_A_So)

Symbol:
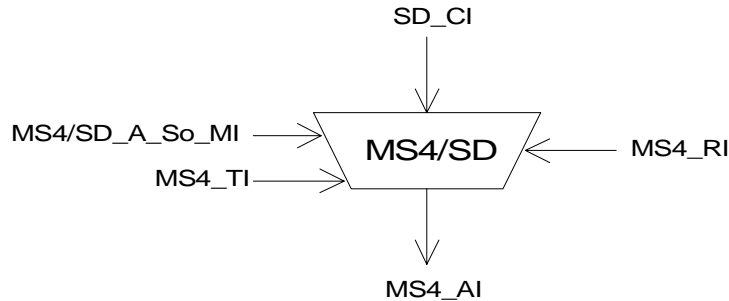
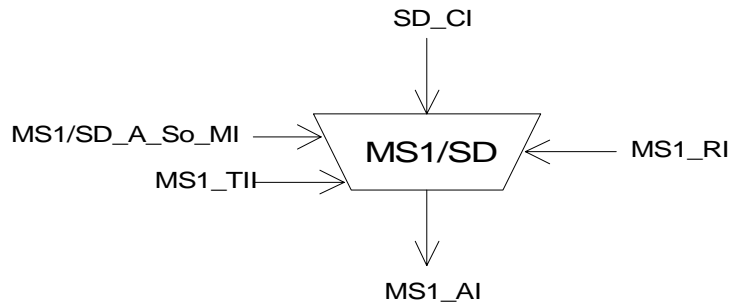**Figure 28: MS4/SD_A_So symbol**

Interfaces:

Table 20: MS4/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS4_TI_CK MS4_TI_FS MS4_RI_CS MS4/SD_A_So_MI_SSMdis MS4/SD_A_So_MI_QLmode	MS4_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [1].

The SSM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM.

Table 21: Quality level set coding into SSM

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

>   if (MI_QLmode== dis)

>   then   S1[5-8] = 1111

>   else   if (RI_CS == CI_CS) or (SSMdis == true)

>   then   S1[5-8] = 1111

>   else   S1[5-8] = SSM[CI_QL]

>   fi

>   fi

Defect Correlations: None.

Performance monitoring: None.

## 7.2.2   STM-4 multiplex section to SD adaptation sink (MS4/SD_A_Sk)

Symbol:

SD_CI

MS4/SD_A_Sk_MI ——→ MS4/SD ⤳ MS4_RI
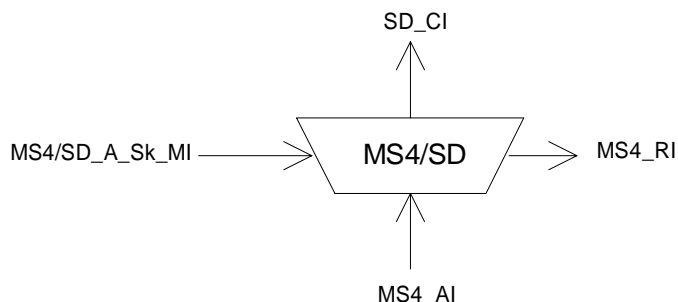
MS4_AI

Figure 29: MS4/SD_A_Sk symbol

Interfaces:

Table 22: MS4/SD_A_Sk input and output signals

Input(s)	Output(s)
MS4_AI_D	SD_CI_CK
MS4_AI_CK	SD_CI_SSF
MS4_AI_FS	SD_CI_CS
MS4_AI_TSF	SD_CI_QL
MS4/SD_A_Sk_MI_SSMsupp	MS4_RI_CS
MS4/SD_A_Sk_MI_CSid	
MS4/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [1]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF

      if (MI_QLmode == disabled) or (MI_SSMsupp == false)

      then   CI_QL = QL-NSUPP

      else   CI_QL = QL[SSM]

      fi

Defect Correlations: None.

Performance monitoring: None.

7.3   STM-16 multiplex section adaptation functions

## 7.3.1   STM-16 multiplex section to SD adaptation source (MS16/SD_A_So)

Symbol:
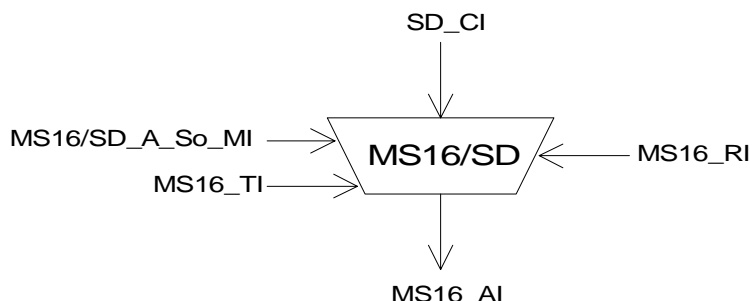
Figure 30: MS16/SD_A_So symbol

Interfaces:

Table 23: MS16/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS MS16_TI_CK MS16_TI_FS MS16_RI_CS MS16/SD_A_So_MI_SSMdis MS16/SD_A_So_MI_QLmode	MS16_AI_D

Processes:

This function converts the CI_QL into the 4 bit SSM code (bits 5 to 8 of byte S1), as defined in ETS 300 147 [1].

The SSM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM.

Table 24: Quality level set coding into SSM

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4 bit SSM code.

Defects: None.

Consequent actions:

    if (MI_QLmode== dis)

    then   S1[5-8] = 1111

    else   if (RI_CS == CI_CS) or (SSMdis == true)

    then   S1[5-8] = 1111

     else   S1[5-8] = SSM[CI_QL]

     fi

    fi

Defect correlations: None.

Performance monitoring: None.

## 7.3.2   STM-16 multiplex section to SD adaptation sink (MS16/SD_A_Sk)

Symbol:

SD_CI

MS16/SD_A_Sk_MI ———→ MS16/SD ⟩—→ MS16_RI
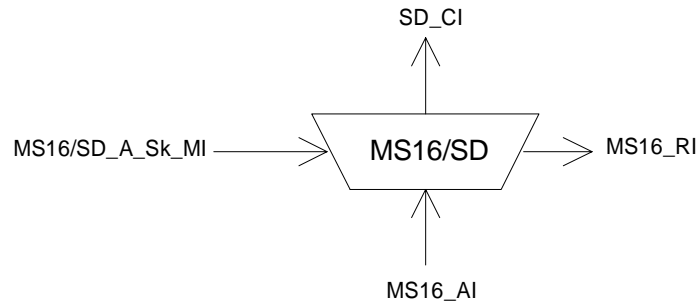
MS16_AI

Figure 31: MS16/SD_A_Sk symbol

Interfaces:

Table 25: MS16/SD_A_Sk input and output signals

Input(s)	Output(s)
MS16_AI_D	SD_CI_CK
MS16_AI_CK	SD_CI_SSF
MS16_AI_FS	SD_CI_CS
MS16_AI_TSF	SD_CI_QL
MS16/SD_A_Sk_MI_SSMsupp	MS16_RI_CS
MS16/SD_A_Sk_MI_CSid	
MS16/SD_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via bits 5 to 8 of byte S1 as defined in ETS 300 147 [1]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

S1[5-8]: In QL-enabled mode and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM bit in the S1 byte should not interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF

      if (MI_QLmode == disabled) or (MI_SSMsupp == false)

      then   CI_QL = QL-NSUPP

      else   CI_QL = QL[SSM]

      fi

Defect correlations: None.

Performance monitoring: None.

7.4   P31s adaptation functions

7.4.1   P31s to SD adaptation source (P31s/SD_A_So)

Symbol:

SD_CI

P31s/SD_A_So_MI →   P31s/SD   ← P31s_RI
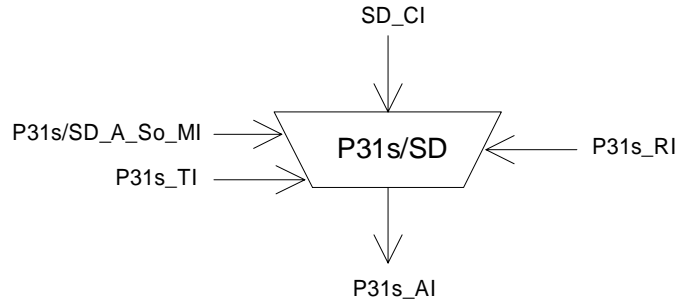
P31s_TI →

P31s_AI

Figure 32: P31s/SD_A_So symbol

Interfaces:

Table 26: P31s/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	P31s_AI_D
SD_CI_CS	
P31s_TI_CK	
P31s_TI_FS	
P31s_TI_MFS	
P31s_RI_CS	
P31s/SD_A_So_MI_TMmode	
P31s/SD_A_So_MI_SSMdis	
P31s/SD_A_So_MI_QLmode	

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code (multiframed bit 8 of byte MA), or into the 1 bit TM code, as defined in subclause 4.3.4 of ETS 300 337 [4]. This is controlled by MI_TMmode.

TMmode: For the case TMmode is disabled the function shall generate the SSM code. For the case TMmode is enabled the function shall generate the TM code.

MA[6-7]: If TMmode is disabled, the value of the multiframe indicator bits shall be set as specified by
ETS 300 337 [5], 500 μs TU multiframe sequence, and aligned with P31s_TI_MFS. Such multiframe indicator is available for SSM processing. If TMmode is enabled, the multiframe indicator is not required for this mode of operation.

					Multiframe indicator		
1	2	3	4	5	6	7	8

Figure 33: Multiframe indicator bits in byte MA

The SSM or TM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM and TM codes.

   NOTE: There may be another parallel adaptation function, e.g. P31s/TUG_A_So that also generates multiframe
            sequence. The equipment should take care that the multiframe sequences generated are the same from all
            adaptation function involved.

MA[8], MA[8][1-4]: For the case of TMmode is disabled, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall transport the 4 bit SSM code. For the case of TMmode is enabled, bit 8 of byte MA shall transport the 1 bit TM code.

Table 27: Quality level set coding into SSM and TM

Quality Level (CI_QL)	SSM coding [MSB..LSB]	TM coding
QL-PRC	0010	0
QL-SSUT	0100	1
QL-SSUL	1000	1
QL-SEC	1011	1

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern, while the transmitted TM code shall be forced to the "1" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM [TM] shall be forced to the "1111" ["1"] pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM/TM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM [TM] to the "1111" ["1"] pattern.

Defects: None.

Consequent actions:

    if (MI_TMmode == dis)

    then   if (MI_QLmode == dis)

    then MA[8][1-4] = 1111

    else if (RI_CS == CI_CS) or (SSMdis == true)

        then   MA[8][1-4] = 1111

        else MA[8][1-4] = SSM[CI_QL]

      fi

    fi

    else   if (MI_QLmode == dis)

    then MA[8] = 1

    else if (RI_CS == CI_CS) or (SSMdis == true)

        then   MA[8] = 1

        else MA[8] = TM[CI_QL]

      fi

    fi

    fi

Defect correlations: None.

Performance monitoring: None.

7.4.2   P31s to SD adaptation sink (P31s/SD_A_Sk)
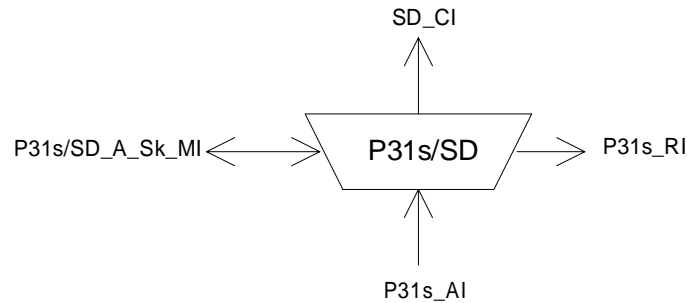
Symbol:

Figure 34: P31s/SD_A_Sk symbol

Interfaces:

Table 28: P31s/SD_A_Sk input and output signals

Input(s)	Output(s)
P31s_AI_D	SD_CI_CK
P31s_AI_CK	SD_CI_SSF
P31s_AI_FS	SD_CI_CS
P31s_AI_TSF	SD_CI_QL
P31s/SD_A_So_MI_TMmode	P31s_RI_CS
P31s/SD_A_So_MI_QLmode	P31s/SD_A_Sk_MI_cLOM
P31s/SD_A_Sk_MI_SSMsupp	
P31s/SD_A_Sk_MI_CSid	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via the multiframed bit 8 of byte MA, or the 1 bit TM, transmitted via bit 8 of byte MA as defined in ETS 300 337 [4]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

TMmode: For the case TMmode is disabled the function shall interpret bit 8 of byte MA as the SSM code. For the case TMmode is enabled the function shall interpret bit 8 of byte MA as the TM code.

MA[6-7]: In QL-enabled mode and if TMmode is disabled and if SSMsupp is true, the function shall recover the 500 μs (multi)frame start phase performing multiframe alignment on bits 6 and 7 of byte MA. Out-Of-Multiframe (OOM) shall be assumed once when an error is detected in the MA bit 6 and 7 sequence. Multiframe alignment shall be assumed to be recovered, and the In-Multiframe (IM) state shall be entered, when in four consecutive P31s frames an error free MA sequence is found.

MA[8][1-4]: In QL-enabled mode and if TMmode is disabled and SSMsupp is true, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall be recovered and accepted if the same code is present in three consecutive 4 bit multiframes. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

MA[8]: In QL-enabled mode and if TMmode is enabled and SSMsupp is true, bit 8 of byte MA shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[TM] as specified in table 5 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM/TM support: For the case MI_SSMsupp is false, the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects:

If the multiframe alignment process is in the OOM state and the MA[6-7] multiframe is not recovered within X ms, a dLOM defect shall be declared. Once in a dLOM state, this state shall be exited when the multiframe is recovered (multiframe alignment process enter the IM state). X shall be a value in the range 1 ms to 5 (ms). X is not configurable. dLOM shall be cleared when QLmode is disabled or SSMsupp is false or TMmode is enabled.

Consequent actions:

aSSF ← dLOM or AI_TSF

      if (MI_QLmode == disabled) or (MI_SSMsupp == false)

      then   CI_QL = QL-NSUPP

      else   if (MI_TMmode == disabled)

        then CI_QL = QL[SSM]

        else CI_QL = QL[TM]

        fi

      fi

Defect correlations:

    cLOM   ←   dMFP and (not AI_TSF)

    NOTE: There may be another parallel adaptation function, e.g. P31s/TUG_A_sk that generates also cLOM. The EMF should take care that fLOM is reported only once.

Performance monitoring: None.

7.5   P4s adaptation functions

7.5.1   P4s to SD adaptation source (P4s/SD_A_So)

Symbol:
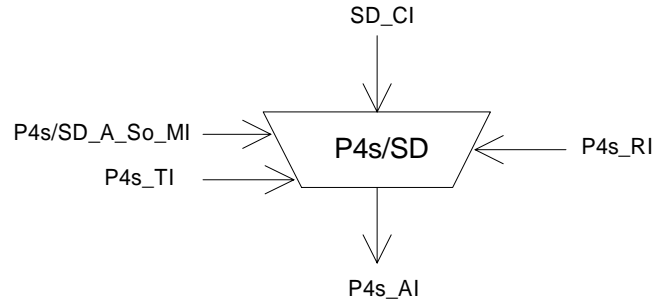
Figure 35: P4s/SD _A_So symbol

Interfaces:

Table 29: P4s/SD _A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS P4s_TI_CK P4s_TI_FS P4s_TI_MFS P4s_RI_CS P4s/SD_A_So_MI_TMmode P4s/SD_A_So_MI_SSMdis P4s/SD_A_So_MI_QLmode	P4s_AI_D

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code (multiframed bit 8 of byte MA), or into the 1 bit TM code, as defined in subclause 4.3.4 of ETS 300 337 [4]. This is controlled by MI_TMmode.

TMmode: For the case TMmode is disabled the function shall generate the SSM code. For the case TMmode is enabled the function shall generate the TM code.

MA[6-7]: If TMmode is disabled, the value of the multiframe indicator bits shall be set as specified by ETS 300 337 [5], 500 µs TU multiframe sequence, and aligned with P4s_TI_MFS. Such multiframe indicator is available for SSM processing. If TMmode is enabled, the multiframe indicator is not required for this mode of operation.

| 1 | 2 | 3 | 4 | 5 | Multiframe indicator | | 8 |
| | | | | | 6 | 7 | |
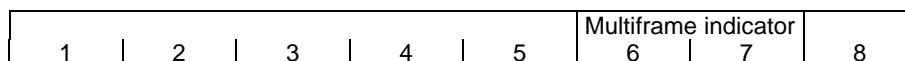
Figure 36: Multiframe indicator bits in byte MA

The SSM or TM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM and TM codes.

NOTE: There may be another parallel adaptation function, e.g. P31s/TUG_A_So that also generates multiframe sequence. The equipment should take care that the multiframe sequences generated are the same from all adaptation function involved.

MA[8], MA[8][1-4]: For the case of TMmode is disabled, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall transport the 4 bit SSM code. For the case of TMmode is enabled, bit 8 of byte MA shall transport the 1 bit TM code.

Table 30: Quality level set coding into SSM and TM

Quality Level (CI_QL)	SSM coding [MSB..LSB]	TM coding
QL-PRC	0010	0
QL-SSUT	0100	1
QL-SSUL	1000	1
QL-SEC	1011	1

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern, while the transmitted TM code shall be forced to the "1" pattern.

Timing loop prevention: If RI_CS equals CI_CS the transmitted SSM [TM] shall be forced to the "1111" ["1"] pattern to prevent a timing loop condition to occur. See subclause 4.13.

SSM/TM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see subclause 4.5.2). For the case MI_SSMdis is true, the function shall force the SSM [TM] to the "1111" ["1"] pattern.

Defects: None.

Consequent actions:

    if (MI_TMmode == dis)

    then   if (MI_QLmode == dis)

    then MA[8][1-4] = 1111

    else if (RI_CS == CI_CS) or (SSMdis == true)

       then   MA[8][1-4] = 1111

       else MA[8][1-4] = SSM[CI_QL]

     fi

    fi

   else   if (MI_QLmode == dis)

    then MA[8] = 1

    else if (RI_CS == CI_CS) or (SSMdis == true)

       then   MA[8] = 1

       else MA[8] = TM[CI_QL]

       fi

    fi

    fi

Defect correlations: None.

Performance monitoring: None.
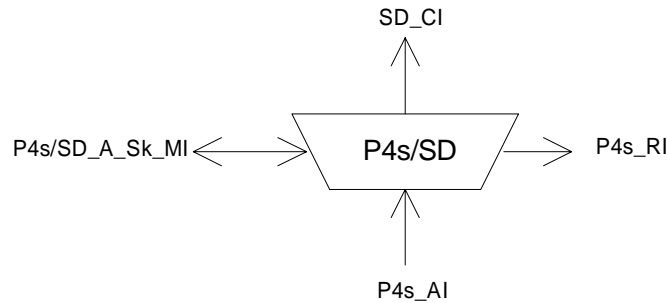
7.5.2   P4s to SD adaptation sink (P4s/SD_A_Sk)

Symbol:

SD_CI

P4s/SD_A_Sk_MI ⟷   P4s/SD   ⟶ P4s_RI

P4s_AI

Figure 37: P4s/SD_A_Sk symbol

Interfaces:

Table 31: P4s/SD_A_Sk input and output signals

Input(s)	Output(s)
P4s_AI_D	SD_CI_CK
P4s_AI_CK	SD_CI_SSF
P4s_AI_FS	SD_CI_CS
P4s_AI_TSF	SD_CI_QL
P4s/SD_A_So_MI_TMmode	P4s_RI_CS
P4s/SD_A_So_MI_QLmode	P4s/SD_A_Sk_MI_cLOM
P4s/SD_A_Sk_MI_SSMsupp	
P4s/SD_A_Sk_MI_Csid	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via the multiframed bit 8 of byte MA, or the 1 bit TM, transmitted via bit 8 of byte MA as defined in ETS 300 337 [4]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

TMmode: For the case TMmode is disabled the function shall interpret bit 8 of byte MA as the SSM code. For the case TMmode is enabled the function shall interpret bit 8 of byte MA as the TM code.

MA[6-7]: In QL-enabled mode and if TMmode is disabled and if SSMsupp is true, the function shall recover the 500 μs (multi)frame start phase performing multiframe alignment on bits 6 and 7 of byte MA. Out-of-multiframe (OOM) shall be assumed once when an error is detected in the MA bit 6 and 7 sequence. Multiframe alignment shall be assumed to be recovered, and the in-multiframe (IM) state shall be entered, when in four consecutive P4s frames an error free MA sequence is found.

MA[8][1-4]: In QL-enabled mode and if TMmode is disabled and SSMsupp is true, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall be recovered and accepted if the same code is present in three consecutive 4 bit multiframes. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

MA[8]: In QL-enabled mode and if TMmode is enabled and SSMsupp is true, bit 8 of byte MA shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[TM] as specified in table 5 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM/TM support: For the case MI_SSMsupp is false, the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in subclause 4.13.

Defects:

If the multiframe alignment process is in the OOM state and the MA[6-7] multiframe is not recovered within X ms, a dLOM defect shall be declared. Once in a dLOM state, this state shall be exited when the multiframe is recovered (multiframe alignment process enter the IM state). X shall be a value in the range 1 to 5 (ms). X is not configurable. dLOM shall be cleared when QLmode is disabled or SSMsupp is false or TMmode is enabled.

Consequent actions:

    aSSF   ←   dLOM or AI_TSF

        if (MI_QLmode == disabled) or (MI_SSMsupp == false)

        then   CI_QL = QL-NSUPP

        else   if (MI_TMmode == disabled)

          then CI_QL = QL[SSM]

          else CI_QL = QL[TM]

          fi

        fi

Defect correlations:

    cLOM   ←   dLOM and (not AI_TSF)

    NOTE: There may be another parallel function, e.g. P4s/TUG_A_sk function that generates also cLOM. The EMF should take care that fLOM is reported only once.

Performance monitoring: None.

7.6   P12s layer adaptation functions

7.6.1   P12s layer adaptation source functions

Two types of P12s/SD_A_So functions are defined:

- type 1 for a 2 Mbit/s station clock output supporting SSM: P12s/SD-sc-1_A_So;

- type 2 for a 2 Mbit/s station clock output not supporting SSM: P12s/SD-sc-2_A_So.

Other types are for further study.

7.6.1.1   Type 1 P12s to SD adaptation source for station clock output supporting SSM (P12s/SD-sc-1_A_So)

Symbol:
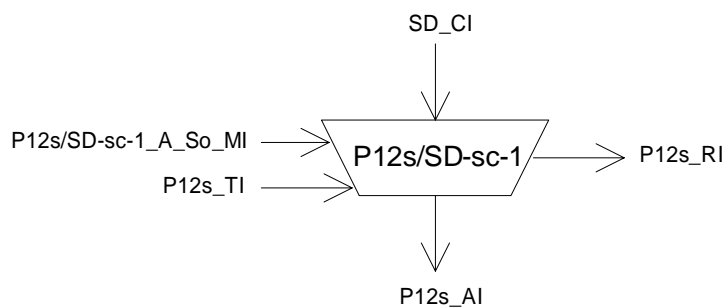
Figure 38: P12s/SD-sc-1_A_So symbol

Interfaces:

Table 32: P12s/SD-sc-1_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	P12s_AI_D
SD_CI_CS	P12s_AI_CK
SD_CI_SSF	P12s_AI_FS
P12s_TI_CK	P12s_AI_MFS
P12s_TI_FS	P12s_AI_AISinsert
P12s_TI_MFS	P12s_RI_CS
P12s/SD-sc-1_A_So_MI_SelSaSSM	P12s_RI_QL
P12s/SD-sc-1_A_So_MI_QLmode	
P12s/SD-sc-1_A_So_MI_SSMsupp	
P12s/SD-sc-1_A_So_MI_QLminimum	

Processes:

This function converts the CI_QL and CI_SSF information into the 4 bit SSM code transmitted in one of the five S_a bits, as defined in ITU-T Recommendation G.704 [13], and an AISinsert control signal.

The SSM message that shall be generated and inserted depends on the applied QL indication that is input to the adaptation source function (CI_QL). The following table presents the relation between the existing set of QLs and the output SSM codes.

Table 33: Quality level set coding into SSM

Quality Level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSUT	0100
QL-SSUL	1000
QL-SEC	1011
QL-UNC	1111

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the transmitted SSM code shall be forced to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available.

Sax: The 4 bit SSM code shall be inserted in one of the Sa bits (S_{ax}, x = 4 to 8) as selected via MI_SelSaSSM. The four bit SSM code shall be transported in alignment with the CRC-4 submultiframe.

Interworking: For interworking with old equipment not supporting SSM processing AIS insertion can be used instead of SSM insertion to pass synchronization quality information via the interface. For the case MI_SSMsuppis true, the function shall force the SSM to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the CSid received via CI_CS into RI_CS and the clock QL received via CI_QL into RI_QL to support timing loop prevention as described under consequent actions (see subclause 4.13).

Defects: None.

Consequent actions:

    if (MI_QLmode== dis)

    then S_{ax}[1-4] = 1111

      RI_QL = QL-NSUPP

      if (CI_SSF == true)

      then AI_AISinsert = true

        RI_CS = none

      else AI_AISinsert = false

        RI_CS = CI_CS

      fi

    else   if (MI_SSMsupp==true)

      then S_{ax}[1-4] = 1111

        RI_QL=QL-NSUPP

        if(CI_SSF == true) or (CI_QL<MI_QLminimum)

        then   AI_AISinsert = true

          RI_CS = none

        else   AI_AISinsert = false

          RI_CS = CI_CS

        fi

    else   AI_AISinsert = false

      if (CI_SSF == true)

      then S_{ax}[1-4] = 1111

        RI_CS = none

        RI_QL = QL-DNU

      else S_{ax}[1-4] = SSM[CI_QL]

        RI_CS = CI_CS

        RI_QL = CI_QL

      fi

     fi

    fi

Defect correlations: None.

Performance monitoring: None.

7.6.1.2 Type 2 P12s to SD adaptation source for station clock output port not supporting SSM (P12s/SD-sc-2_A_So)

Symbol:
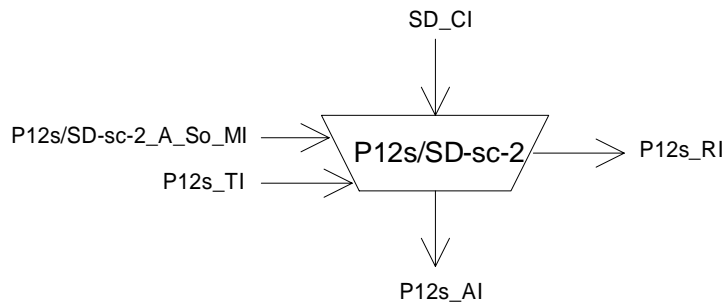
Figure 39: P12s/SD-sc-2_A_So symbol

Interfaces:

Table 34: P12s/SD-sc-2_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	P12s_AI_CK
SD_CI_CS	P12s_AI_FS
SD_CI_SSF	P12s_AI_MFS
P12s_TI_CK	P12s_AI_AISinsert
P12s_TI_FS	P12s_RI_CS
P12s_TI_MFS	P12s_RI_QL
P12s/SD-sc-2_A_So_MI_QLminimum	
P12s/SD-sc-2_A_So_MI_QLmode	

Processes:

This function converts the CI_QL and CI_SSF information into an AISinsert control signal.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) AI_AISinsert shall be activated if CI_SSF is true. For the case of QL-enabled mode, AI_AISinsert shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the CSid received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see also subclause 4.13). RI_QL shall be fixed to QL-NSUPP.

Defects: None.

Consequent actions:

     RI_QL = QL-NSUPP

     if (MI_QLmode == dis)

     then   if (CI_SSF == true)

       then AI_AISinsert = true

         RI_CS = none

         else   AI_AISinsert = false

         RI_CS = CI_CS

       fi

     else   if (CI_SSF == true) or (CI_QL < MI_QLminimum)

       then AI_AISinsert = true

         RI_CS = none

       else AI_AISinsert = false

         RI_CS = CI_CS

       fi

     fi

Defect correlations: None.

Performance monitoring: None.

7.6.2   P12s layer adaptation sink functions

Two types of P12s/SD_A_Sk functions are defined:

- type 1 for a 2 Mbit/s traffic input port: P12s/SD-tf_A_Sk;

- type 2 for a 2 Mbit/s station clock input port: P12s/SD-sc_A_Sk.

7.6.2.1   Type 1 P12s to SD adaptation sink for traffic input port (P12s/SD-tf_A_Sk)
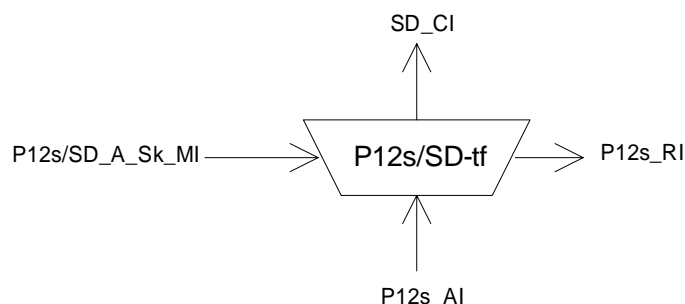
Symbol:

Figure 40: P12s/SD-tf_A_Sk symbol

Interfaces:

Table 35: P12s/SD-tf_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D	SD_CI_CK
P12s_AI_CK	SD_CI_SSF
P12s_AI_FS	SD_CI_CS
P12s_AI_TSF	SD_CI_QL
P12s_AI_MFS	P12s_RI_CS (for further study)
P12s_AI_MFP	
P12s/SD-tf_A_Sk_MI_SSMsupp	
P12s/SD-tf_A_Sk_MI_SelSaSSM	
P12s/SD-tf_A_Sk_MI_QLmode	
P12s/SD-tf_A_Sk_MI_CSid	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via one of the S_a bits as defined in
ITU-T Recommendation G.704 [13]. It supplies the timing signal, recovered by the physical section layer, to the SD
layer.

Sax[1-4]: In QL-enabled mode and if SSMsupp is true, bits Sax[1] to Sax[4] (x = MI_SelSaSSM is a value in the
set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted
code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be
ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced
to the QL-NSUPP.

Clock Source identifier: The function shall insert the CSid received via MI_CSid into CI_CS to support timing loop
prevention as described in subclause 4.13. RI_CS generation is for further study.

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF or (AI_ MFP==false and Qlmode==enabled and SSMsupp==true)

     if (MI_QLmode == disabled) or (MI_SSMsupp == false)

     then   CI_QL = QL-NSUPP

     else   CI_QL = QL[SSM]

     fi

Defect correlations: None.

Performance monitoring: None.

7.6.2.2   Type 2 P12s to SD adaptation sink for station clock input port (P12s/SD-sc_A_Sk)
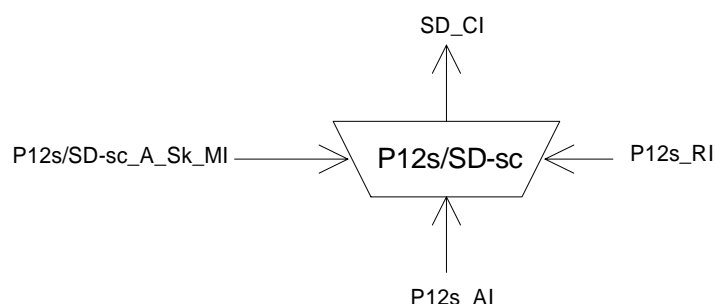
Symbol:

Figure 41: P12s/SD-sc _A_Sk symbol

Interfaces:

Table 36: P12s/SD-sc_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D	SD_CI_CK
P12s_AI_CK	SD_CI_SSF
P12s_AI_FS	SD_CI_CS
P12s_AI_TSF	SD_CI_QL
P12s_AI_MFS	
P12s_AI_MFP	
P12s_RI_CS	
P12s_RI_QL	
P12s/SD-tf_A_Sk_MI_SSMsupp	
P12s/SD-tf_A_Sk_MI_SelSaSSM	
P12s/SD-tf_A_Sk_MI_CSid	
P12s/SD-sc_A_Sk_MI_QLmode	

Processes:

This functions extracts and accepts the 4 bit SSM, transmitted via one of the S_a bits as defined in ITU-T Recommendation G.704 [13]. It supplies the timing signal, recovered by the physical section layer, to the SD layer.

Sax: In QL-enabled mode and if SSMsupp is true, bits Sax[1] to Sax[4] (x = MI_SelSaSSM is a value in the set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in table 4 and output via CI_QL.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: For the case MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall process the CSid received via RI_CS to support timing loop prevention (see subclause 4.13). The function shall determine the value of the CI_CS output signal as follows:

```
if (RI_CS == none)

then    CI_CS = MI_CSid

else    if (SSMsupp == true) and (MI_QLMode==enabled)

   then if (RI_QL == CI_QL) or (RI_QL == QL-NSUPP)

     then    CI_CS = RI_CS

     else    CI_CS = MI_CSid

      fi

   else  CI_CS = RI_CS

    fi

   fi
```

Defects: None.

Consequent actions:

aSSF   ←   AI_TSF or (AI_MFP==false and Qlmode==enabled and SSMsupp==true)

```
if (MI_QLmode == disabled) or (MI_SSMsupp == false)

then    CI_QL = QL-NSUPP

else    CI_QL = QL[SSM]

fi
```

Defect correlations: None.

Performance monitoring: None.

ETSI

7.7 T12 layer adaptation functions

7.7.1 T12 to SD adaptation source (T12/SD_A_So)

Symbol:
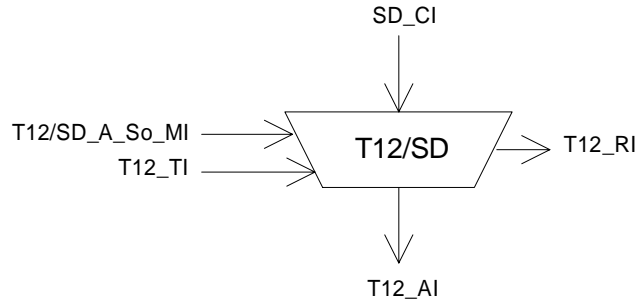
Figure 42: T12/SD_A_So symbol

Interfaces:

Table 37: T12/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL	T12_AI_CK
SD_CI_CS	T12_AI_SQLCH
SD_CI_SSF	T12_RI_CS
SD_CI_CK	T12_RI_QL
T12/SD_A_So_MI_QLminimum	
T12/SD_A_So_MI_QLmode	

Processes:

This function converts the CI_QL and CI_SSF information into an SQLCH control signal.

QLmode: For the case the function operates in QL-disabled mode (MI_QLmode = dis) AI_SQLCH shall be activated if CI_SSF is true. For the case of QL-enabled mode, AI_SQLCH shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock Source identifier & quality level: The function shall insert the CSid received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see also subclause 4.13). RI_QL shall be fixed to QL-NSUPP.

Defects: None.

Consequent actions:

     RI_QL = QL-NSUPP

     if (MI_QLmode == dis)

     then   if (CI_SSF == true)

       then   AI_SQLCH = true

           RI_CS = none

       else   AI_SQLCH = false

           RI_CS = CI_CS

       fi

     else   if (CI_SSF == true) or (CI_QL < MI_QLminimum)

       then AI_SQLCH = true

           RI_CS = none

       else AI_SQLCH = false

           RI_CS = CI_CS

       fi

     fi

Defect correlations: None.

Performance monitoring: None.

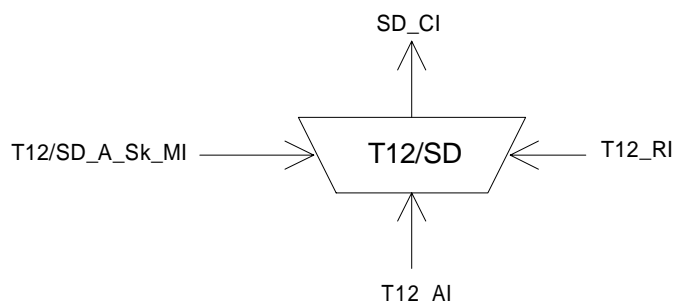## 7.7.2   T12 to SD adaptation sink (T12/SD_A_Sk)

Symbol:

Figure 43: T12/SD_A_Sk symbol

Interfaces:

Table 38: T12/SD_A_Sk input and output signals

Input(s)	Output(s)
T12_AI_CK	SD_CI_CK
T12_AI_TSF	SD_CI_SSF
T12_RI_CS	SD_CI_CS
T12_RI_QL	SD_CI_QL
T12/SD_A_Sk_MI_Csid	

Processes:

This function adapts the 2 048 kHz TI from an external reference to an equipment specific timing CI. This function regenerates the received CK and supplies the recovered timing signal to the SD layer.

Regeneration: The function shall output a valid CK when any combination of the following signal conditions exist at the input:

-    An input electrical amplitude level with any value in the range specified by ETS 300 166 [2];

-    Jitter modulation applied to the input signal with any value defined in EN 300 462-5-1 [11];

-    The input signal frequency has any value in the range 2 048 kHz ± 50 ppm.

   NOTE: The frequency and jitter/wander tolerance is further constrained by the requirements of the client (SD) layer. For example in the MS SDH layer, the frequency offset should not exceed 4,6 ppm.

SSM support: CI_QL shall be forced to the QL-NSUPP.

Clock Source identifier: The function shall process the CSid received via RI_CS to support timing loop prevention (see subclause 4.13). The function shall determine the value of the CI_CS output signal as follows:

   if (RI_CS == none)

   then   CI_CS = MI_CSid

   else   CI_CS = RI_CS

   fi

Defects: None.

Consequent actions:

   aSSF   ←   AI_TSF

Defect correlations: None.

Performance monitoring: None.

8 Equipment clock to TLs clock adaptation functions

8.1 STM-N layer

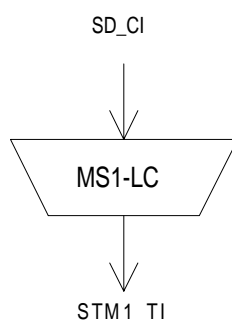### 8.1.1 STM-1 Layer Clock (LC) adaptation source (MS1-LC_A_So)

Symbol:

SD_CI

MS1-LC

STM1_TI

Figure 44: MS1-LC_A_So symbol

Interfaces:

Table 39: MS1-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS_TI_CK MS1_TI_FS

Processes:

This function performs the STM-1 clock and Frame Start (FS) signal generation locked to the NE CK SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM1_TI_CK for the STM-1 signal. The STM1_TI_CK frequency shall be 155 520 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-1 output interface shall be as specified in EN 300 462-5-1 [11] for optical interfaces and EN 300 417-2-1 [7] for electrical interface.

Frame Start signal generation: The function shall generate the FS reference signal STM1_TI_FS for the STM-1 signal. The STM1_TI_FS signal shall be active once per 19 440 clock cycle.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.1.2   STM-4 LC adaptation source (MS4-LC_A_So)

Symbol:

```
                        SD_CI
                          |
                          v
                   /----------------\
                   \   MS4-LC        /
                    \--------------/
                          |
                          v
                       STM4_TI
```

Figure 45: MS4-LC_A_So symbol

Interfaces:

Table 40: MS4-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS4_TI_CK MS4_TI_FS

Processes:

This function performs the STM-4 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM1_TI_CK for the STM-4 signal. The STM4_TI_CK frequency shall be 622 080 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-4 output interface shall be as specified in EN 300 462-5-1 [11].

Frame Start signal generation: The function shall generate the FS reference signal STM4_TI_FS for the STM-4 signal. The STM4_TI_FS signal shall be active once per 77 760 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.
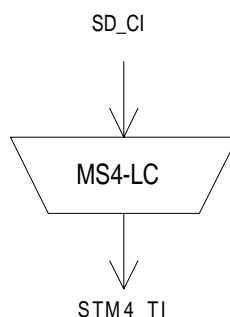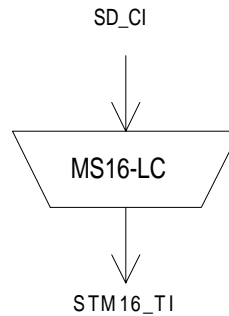
8.1.3   STM-16 LC adaptation source (MS16-LC_A_So)

Symbol:

SD_CI

MS16-LC

STM16_TI

Figure 46: MS16-LC_A_So symbol

Interfaces:

Table 41: MS16-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	MS16_TI_CK
	MS16_TI_FS

Processes:

This function performs the STM-16 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STM16_TI_CK for the STM-16 signal. The STM16_TI_CK frequency shall be 2 488 320 kHz locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-16 output interface shall be as specified in EN 300 462-5-1 [11].

Frame Start signal generation: The function shall generate the FS reference signal STM16_TI_FS for the STM-16 signal. The STM16_TI_FS signal shall be active once per 311 040 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.2   VC layers

8.2.1   VC-4 LC adaptation source (S4-LC_A_So)

Symbol:

Figure 47: S4-LC A_So symbol

Interfaces:

Table 42: S4-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S4_TI_CK
	S4_TI_FS
	S4_TI_MFS

Processes:

This function performs the VC-4 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S4_TI_CK for the VC-4 signal. The S4_TI_CK frequency shall be 150 336 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study

Frame Start signal generation: The function shall generate the FS reference signal S4_TI_FS for the VC-4 signal. The S4_TI_FS signal shall be active once per 18 792 clock cycle and the multiframe reference shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

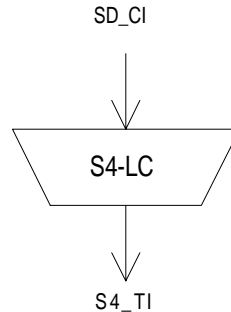## 8.2.2   VC-3 LC adaptation source (S3-LC_A_So)

Symbol:
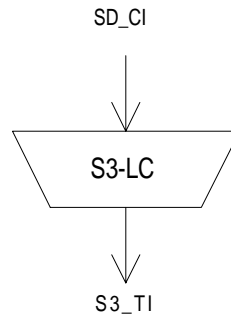
SD_CI

S3-LC

S3_TI

Figure 48: S3-LC_A_So symbol

Interfaces:

Table 43: S3-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S3_TI_CK
	S3_TI_FS
	S3_TI_MFS

Processes:

This function performs the VC-3 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S3_TI_CK for the VC-3 signal. The S3_TI_CK frequency shall be 48 960 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study

Frame Start signal generation: The function shall generate the FS reference signal S3_TI_FS for the VC-3 signal. The S3_TI_FS signal shall be active once per 6 120 clock cycle and the S3_TI_MFS once every four frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

**Performance monitoring:**   None.

8.2.3   VC-2 LC adaptation source (S2-LC_A_So)

Symbol:

```
            SD_CI
              │
              ▼
        ╱──────────╲
        ╲  S2-LC   ╱
         ╲────────╱
              │
              ▼
           S2_TI
```

Figure 49: S2-LC_A_So symbol

Interfaces:

Table 44: S2-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S2_TI_CK S2_TI_FS

Processes:

This function performs the VC-2 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S2_TI_CK for the VC-2 signal. The S2_TI_CK frequency shall be 6 848 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the FS reference signal S2_TI_FS for the VC-2 signal. The S2_TI_FS signal shall be active once per 856 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.
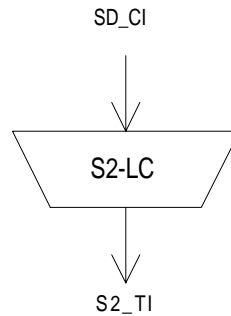
8.2.4   VC-12 LC adaptation source (S12-LC_A_So)

Symbol:
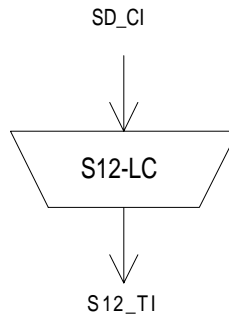
SD_CI

S12-LC

S12_TI

Figure 50: S12-LC_A_So symbol

Interfaces:

Table 45: S12-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S12_TI_CK S12_TI_FS

Processes:

This function performs the VC-12 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S12_TI_CK for the VC-12 signal. The S12_TI_CK frequency shall be 2 240 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the FS reference signal S12_TI_FS for the VC-12 signal. The S12_TI_FS signal shall be active once per 280 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.
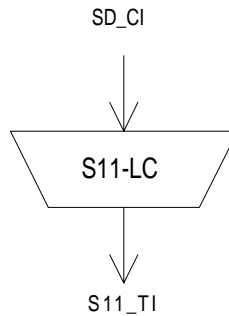
8.2.5   VC-11 LC adaptation source (S11-LC_A_So)

Symbol:

```
                           SD_CI
                             |
                             v
                    ┌─────────────────┐
                     \    S11-LC     /
                      └─────────────┘
                             |
                             v
                          S11_TI
```

Figure 51: S3-LC_A_So symbol

Interfaces:

Table 46: S3-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	S11_TI_CK
	S11_TI_FS

Processes:

This function performs the VC-11 clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal S11_TI_CK for the VC-11 signal. The S11_TI_CK frequency shall be 1 664 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the FS reference signal S11_TI_FS for the VC-11 signal. The S11_TI_FS signal shall be active once per 208 clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.
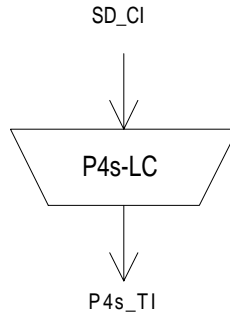
8.3   Pxx layers

8.3.1   P4s LC adaptation source (P4s-LC_A_So)

Symbol:

SD_CI

P4s-LC

P4s_TI

Figure 52: P4s-LC_A_So symbol

Interfaces:

Table 47: P4s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P4s_TI_CK
	P4s_TI_FS
	P4s_TI_MFS

Processes:

This function performs the P4s clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P4s_TI_CK for the P4s signal. The P4s_TI_CK frequency shall be 139 264 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the FS reference signal P4s_TI_FS for the P4s signal. The P4s_TI_FS signal shall be active once per 17 408 clock cycles. P4s_TI_MFS shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

8.3.2   P31s LC adaptation source (P31s-LC_A_So)
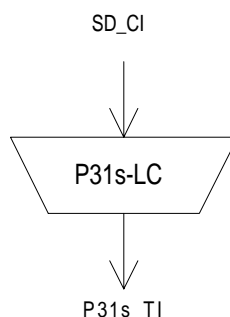
Symbol:

```
                        SD_CI
                          │
                          ▼

                  ╲ P31s-LC ╱

                          │
                          ▼

                       P31s_TI
```

Figure 53: P31s-LC_A_So symbol

Interfaces:

Table 48: P31s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P31s_TI_CK P31s_TI_FS P31s_TI_MFS

Processes:

This function performs the P31s clock and FS signal generation locked to the NE CK SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P31s_TI_CK for the P31s signal. The P31s_TI_CK frequency shall be 34 368 kHz locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame Start signal generation: The function shall generate the FS reference signal P31s_TI_FS for the P31s signal. The P31s_TI_FS signal shall be active once per 4 296 clock cycles and P31s_TI_MFS once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

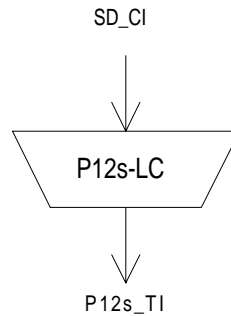**Performance monitoring:**   None.

8.3.3   P12s LC adaptation source (P12s-LC_A_So)

Symbol:

SD_CI

P12s-LC

P12s_TI

Figure 54: P12s-LC_A_So symbol

Interfaces:

Table 49: P12s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P12s_TI_CK
	P12s_TI_FS
	P12s_TI_MFS

Processes:

This function performs the P12s clock and FS signal generation locked to the CK SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P12s_TI_CK for the P12s signal. The P12s_TI_CK frequency shall be 2 048 kHz locked to the input signal SD_CI_CK.

   NOTE: If a SD_CI_SSF is present at the input of the function, it is also present at the input of P12s/SD and an AIS is generated by P12_TT.

Jitter limiter: The function shall process the signal such that in the absence input jitter at the synchronization interface, the intrinsic jitter at the E12 output interface is compatible with EN 300 462-5-1 [11].

Frame Start signal generation: The function shall generate the FS reference signal P12s_TI_FS for the P12s signal. The P12s_TI_FS signal shall be active once per 256 clock cycles and P12s_TI_MFS once every 16 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.
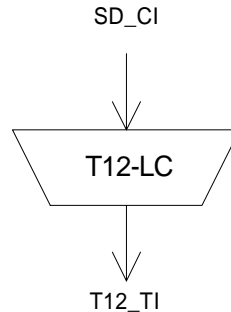
8.4   T12 layer

8.4.1   T12 LC adaptation source (T12-LC_A_So)

Symbol:

SD_CI

T12-LC

T12_TI

Figure 55: T12-LC_A_So symbol

Interfaces:

Table 50: T12-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	T12_TI_CK

Processes:

This function performs the T12 CK generation locked to the CK SD_CI_CK, to time the adaptation source functions T12/SD_A_So.

Clock generation: The function shall generate the clock reference signal T12_TI_CK for the 2 048 kHz signal. The T12_TI_CK frequency shall be 2 048 kHz locked to the input signal SD_CI_CK.

   NOTE: If a SD_CI_SSF is present at the input of the function, it is also present at the input of T12s/SD and a squelch action is activated.

Jitter limiter: The function shall process the signal such that in the absence of input jitter at the synchronization interface, the intrinsic jitter at the 2 048 kHz output interface is compatible with EN 300 462-5-1 [11].

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

Annex A (normative):
Synchronization selection process

This annex specifies the detailed operation of the automatic synchronization reference selection process located in the NS_C function. Refer to clause 4 for an introduction to this process.

A selection process needs the quality level (NS_CI_QL) and SF (NS_CI_SSF) information from each input (i.e. each SD_TT_Sk and SD/NS_A_Sk combination; the pair is henceforth called a "timing source") after it has passed through a holdoff/wait-to-restore process (HO/WtR).

Via the management interface it receives the priority (which includes disabling) of each timing source and its lock-out status. Switch requests (clear, manual, forced) and requests to change the mode of operation between QL-enabled and QL-disabled are also coming in through the management interface.

The output of the selection control process is the actually selected input ("select q") and its QL. The actually selected input is reported towards the management interface. In addition, rejection messages are sent towards the management interface. Figure A.1 shows the interfaces between the selection control process and its environment.
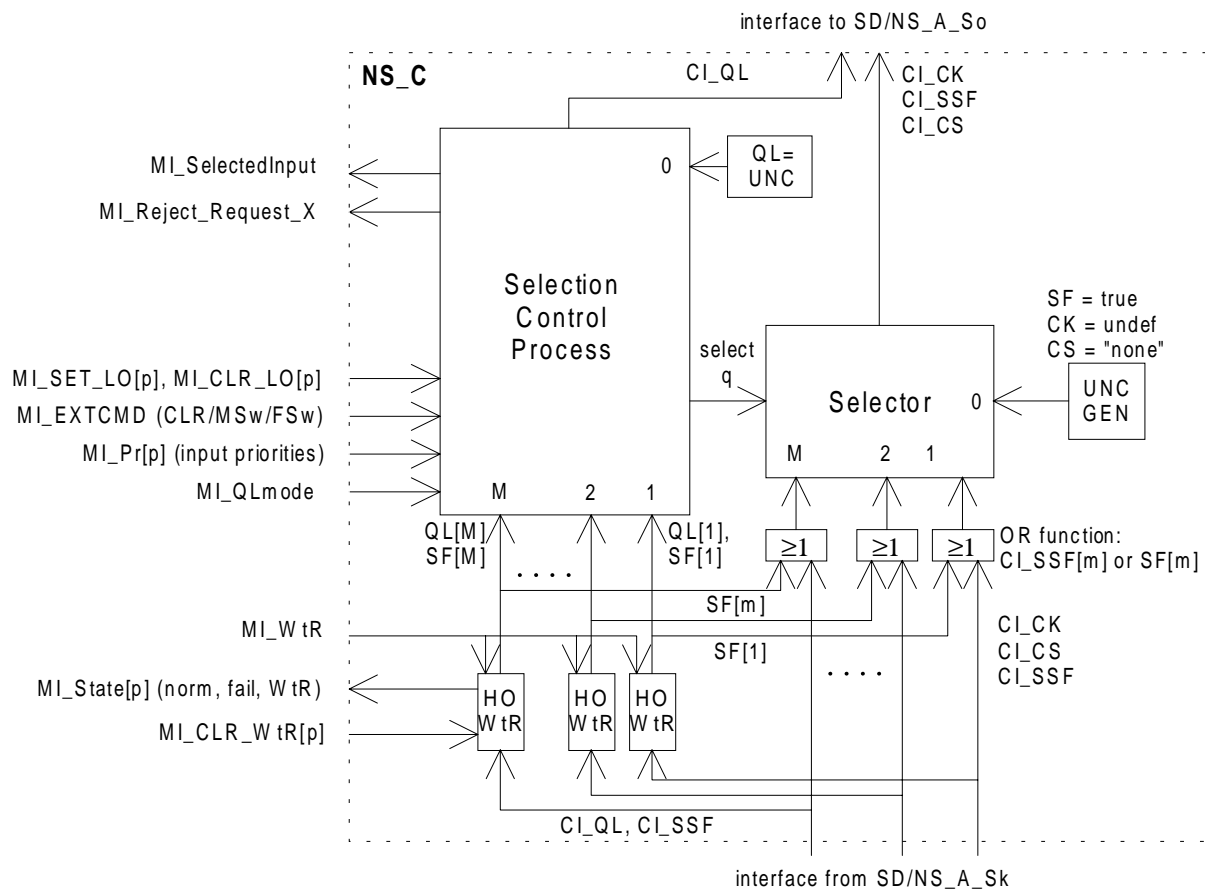

Figure A.1: Environment of selection control process

The selector supports M inputs (1 to M) and one output. In addition, the selector has a $M+1^{th}$ input, the null (0) input connected to an "unconnect" signal generator process.

      Unconnect signal - A signal with CI_CK is undefined, CI_SSF is true and CI_CS is "none".

In the SDL diagrams that describe the selection process there are six states which correspond to the two modes of operation (QL-mode enabled (1) and QL-mode disabled (2)) and within each of these modes three "maintenance" states: no request active (A), MSw active (B) and FSw active (C). For each of these six states the reaction to all possible input variations are given.

In the SDL diagrams "report q" is a MI_selected input information and QL_out equals CI_CL, as defined in figure A.1.

Table A.1: Notational conventions and parameters used in the SDL diagrams

| Parameter	Abbreviation	Values (high to low)/Explanation
Quality Level [input]	QL[p]	PRC, SSU-T, SSU-L, SEC, DNU, INV, FAILED, undef(ined)
Quality Level [0]	QL[0]	UNConnected
Priority [input]	Pr[p]	1, 2, ..., K, dis(abled)
Priority [0]	Pr[0]	undef(ined)
Signal Fail [input]	SF[p]	false, true
Signal Fail [0]	SF[0]	true
Lock Out status [input]	LO[p]	on, off
Lock Out status [0]	LO[0]	off
input	p	1, 2, ..., M
selected input	q	0,1, 2, ..., M
Number of timing sources	M	
Number of different priorities	K	K = M
	:=	assignment symbol
	==	equality test symbol
	<=	less or equal test symbol
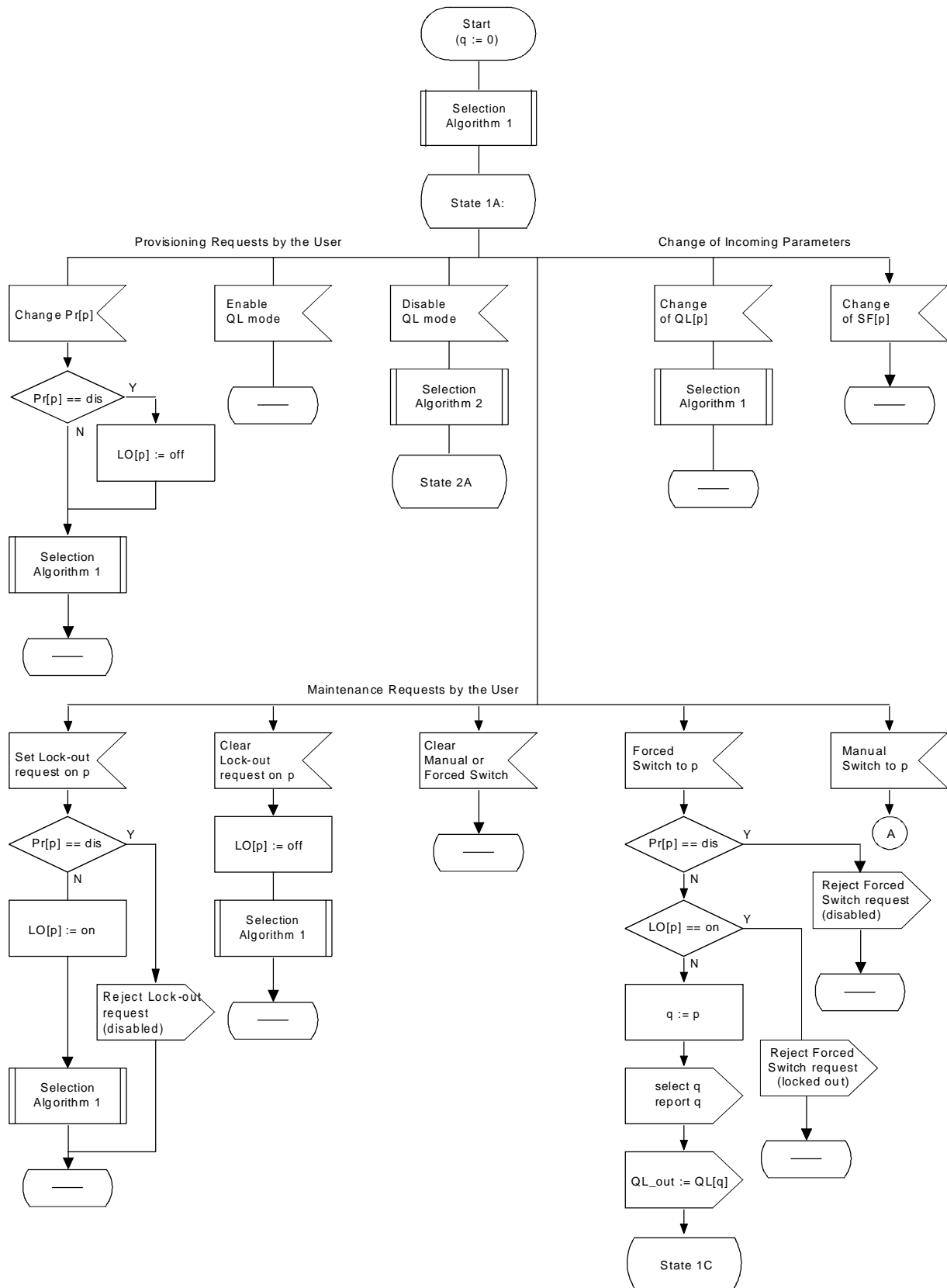
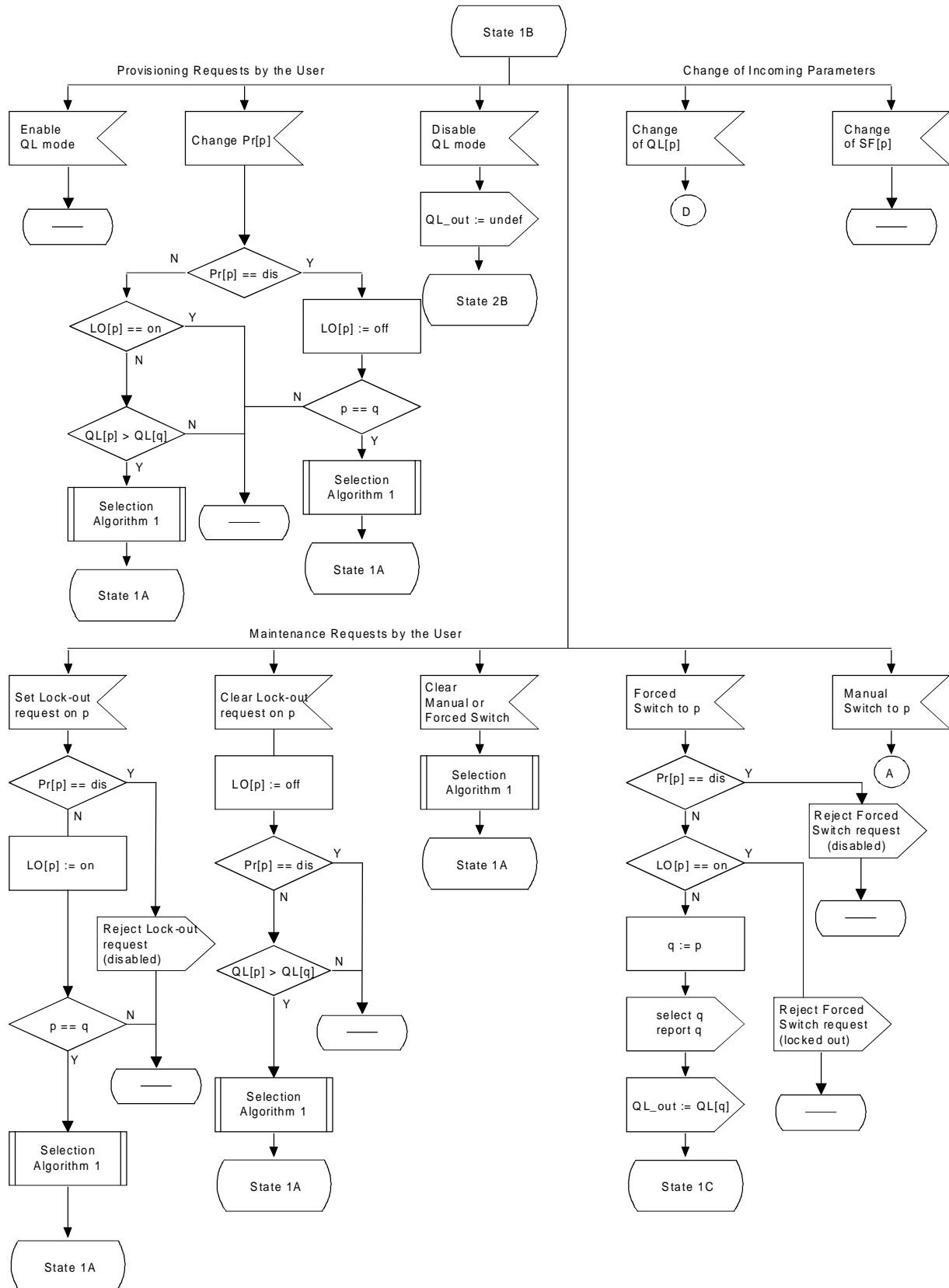**Figure A.2: QL enabled mode, no active switch request (state 1A)**

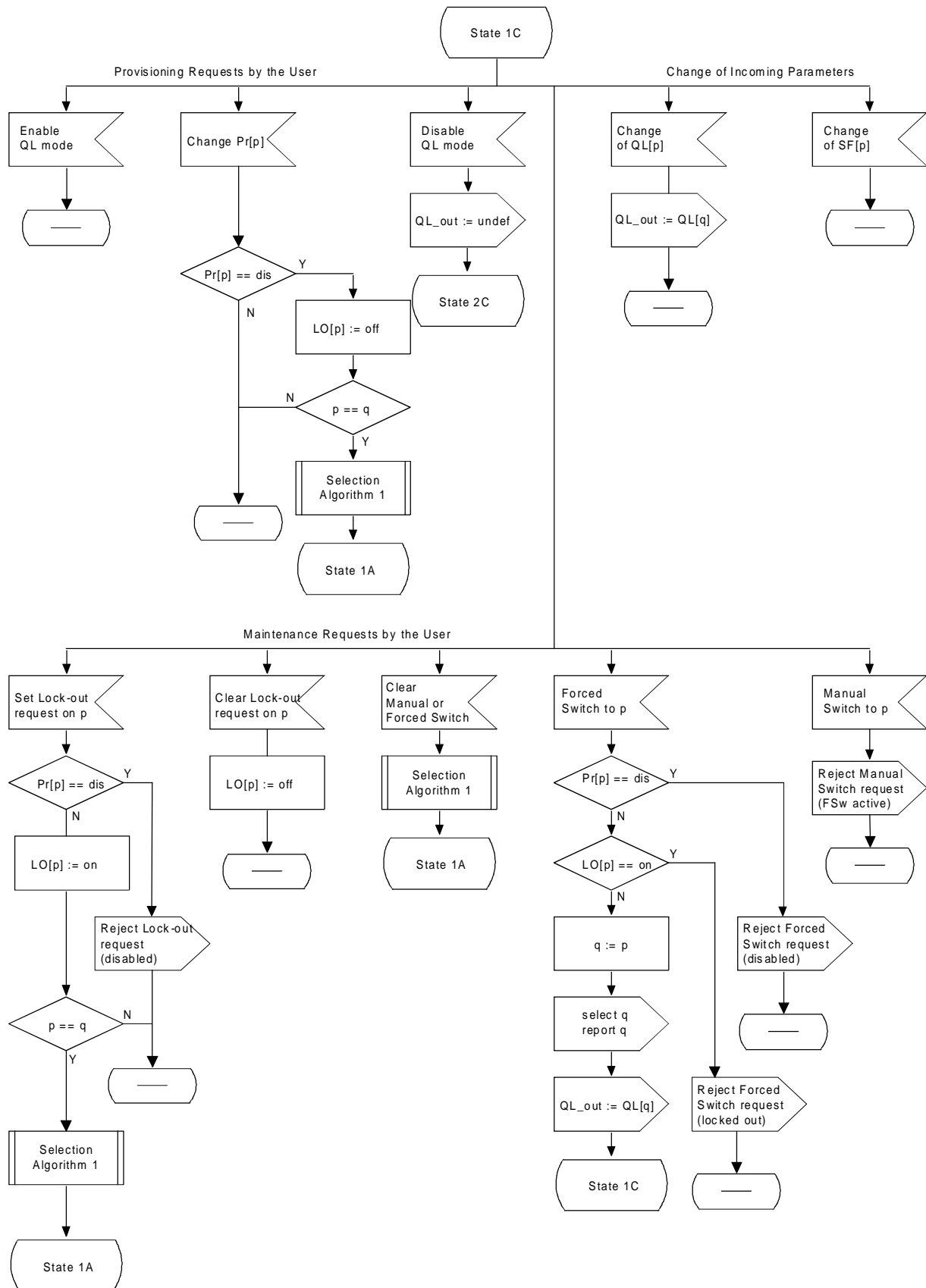**Figure A.3: QL enabled mode, active MSw request (state 1B)**
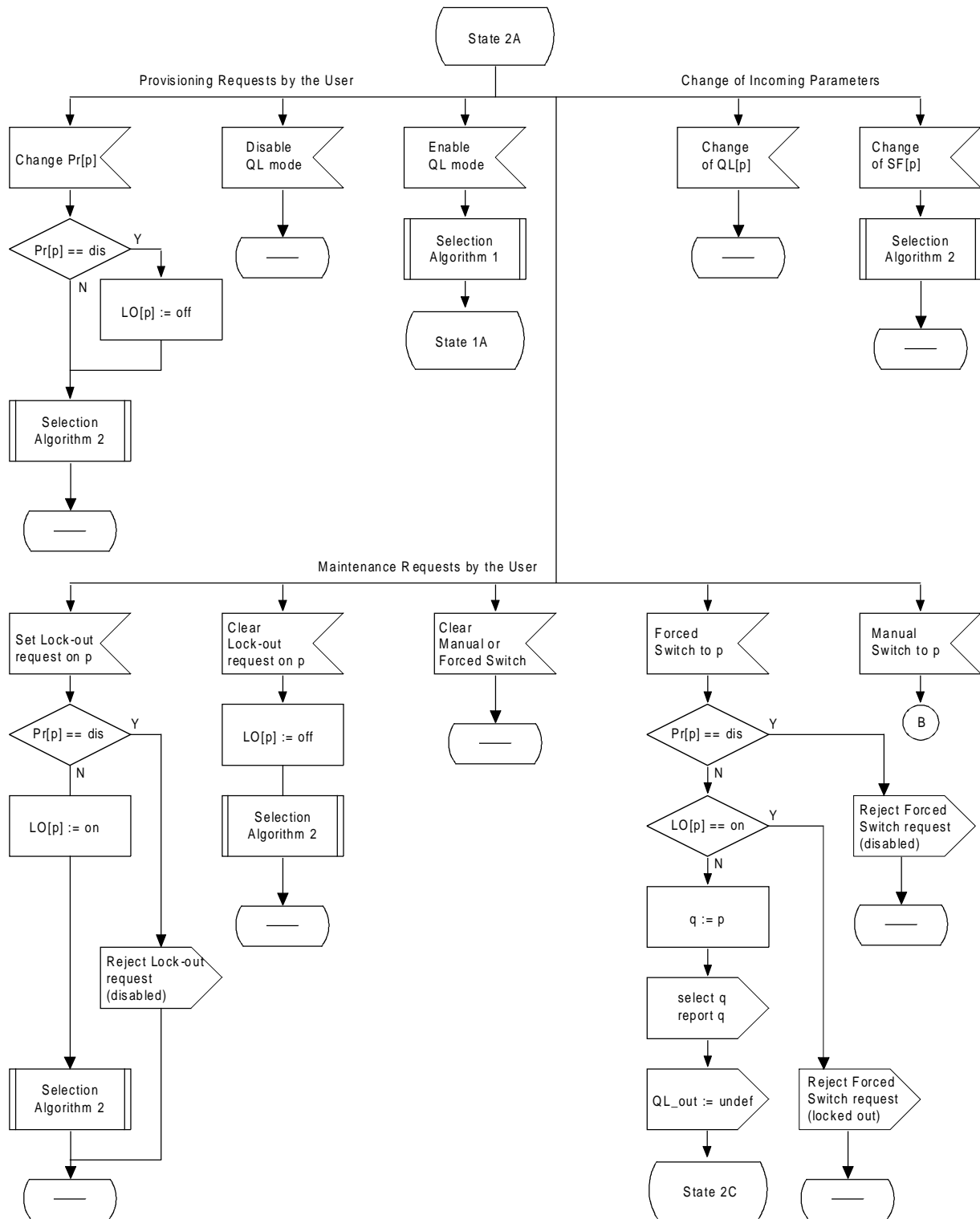
Figure A.4: QL mode enabled, active FSw (state 1C)

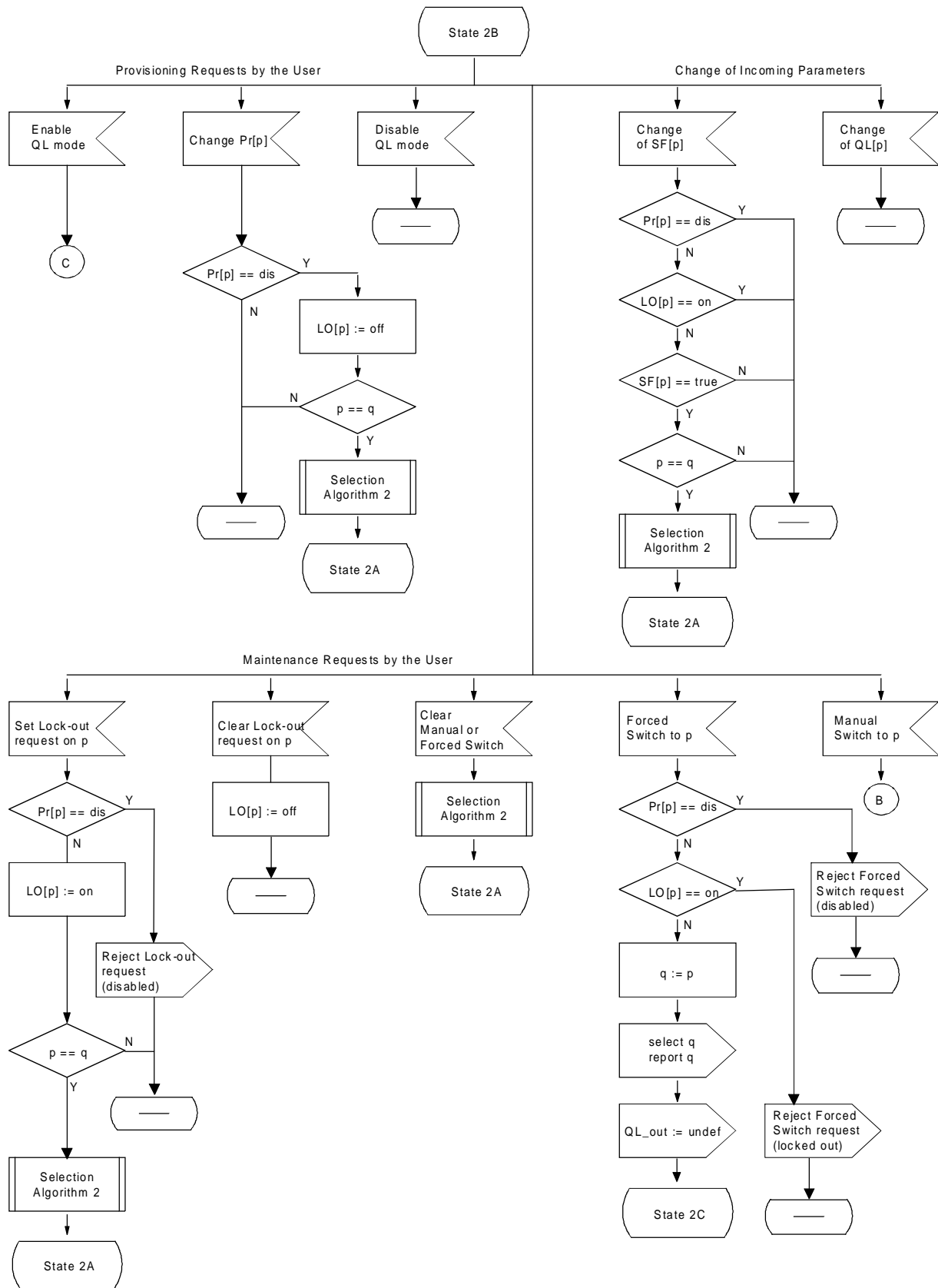**Figure A.5: QL mode disabled, no external switch request active (state 2A)**

Figure A.6: QL mode disabled, active MSw request (state 2B)

State 2C

Provisioning Requests by the User

Change of Incoming Parameters

Enable QL mode

QL_out := QL[q]

State 1C

Change Pr[p]

Pr[p] == dis — Y

N

LO[p] := off

p == q — N

Y

Selection Algorithm 2

State 2A

Disable QL mode

Change of QL[p]

Change of SF[p]

Maintenance Requests by the User

Set Lock-out request on p

Pr[p] == dis — Y

N

LO[p] := on

Reject Lock-out request (disabled)

p == q — N

Y

Selection Algorithm 2

State 2A

Clear Lock-out request on p

LO[p] := off

Clear Manual or Forced Switch

Selection Algorithm 2

State 2A

Forced Switch to p

Pr[p] == dis — Y

N

LO[p] == on — Y

N

q := p

select q report q

QL_out := undef

State 2C

Reject Forced Switch request (disabled)

Reject Forced Switch request (locked out)

Manual Switch to p
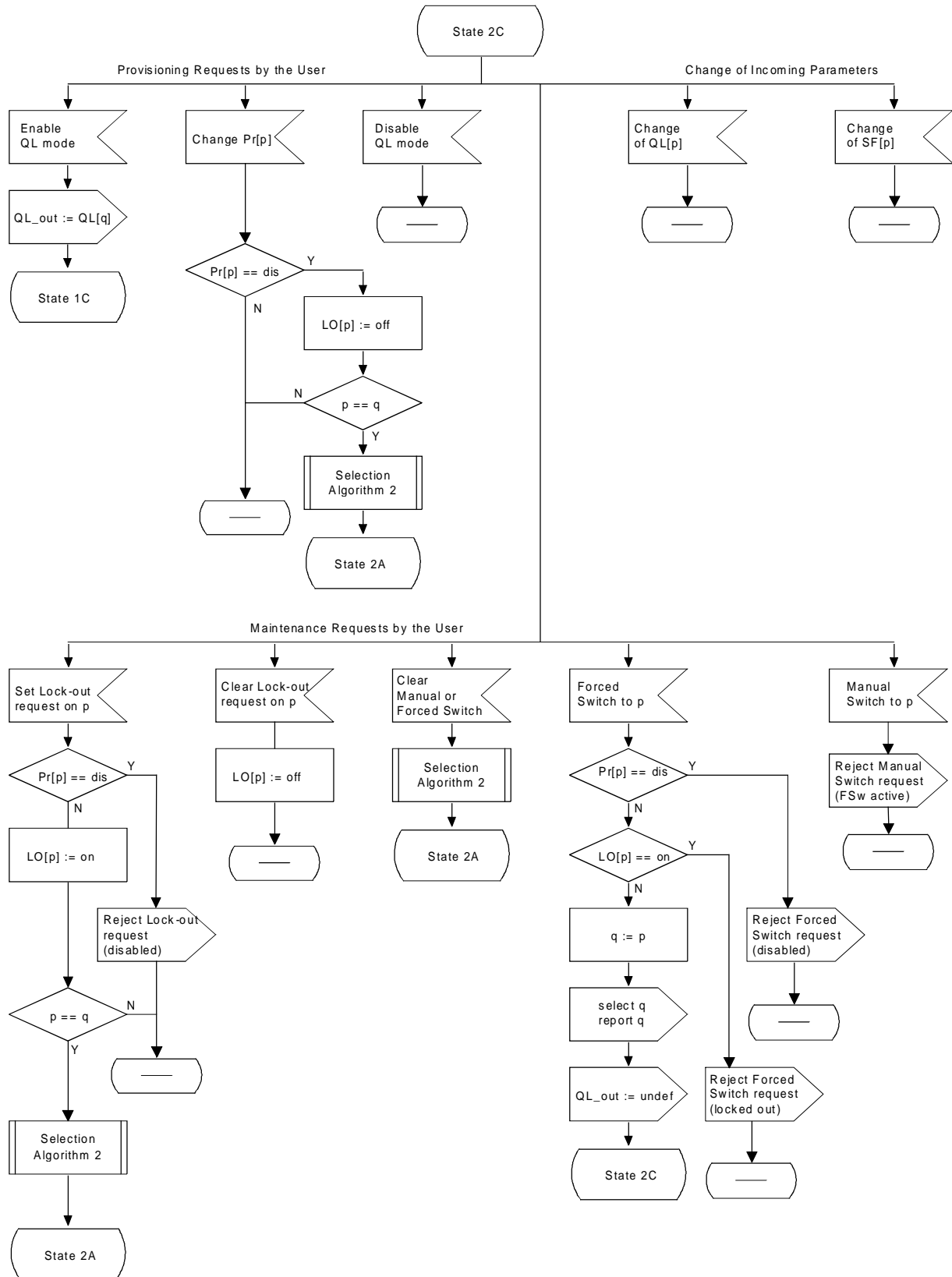
Reject Manual Switch request (FSw active)

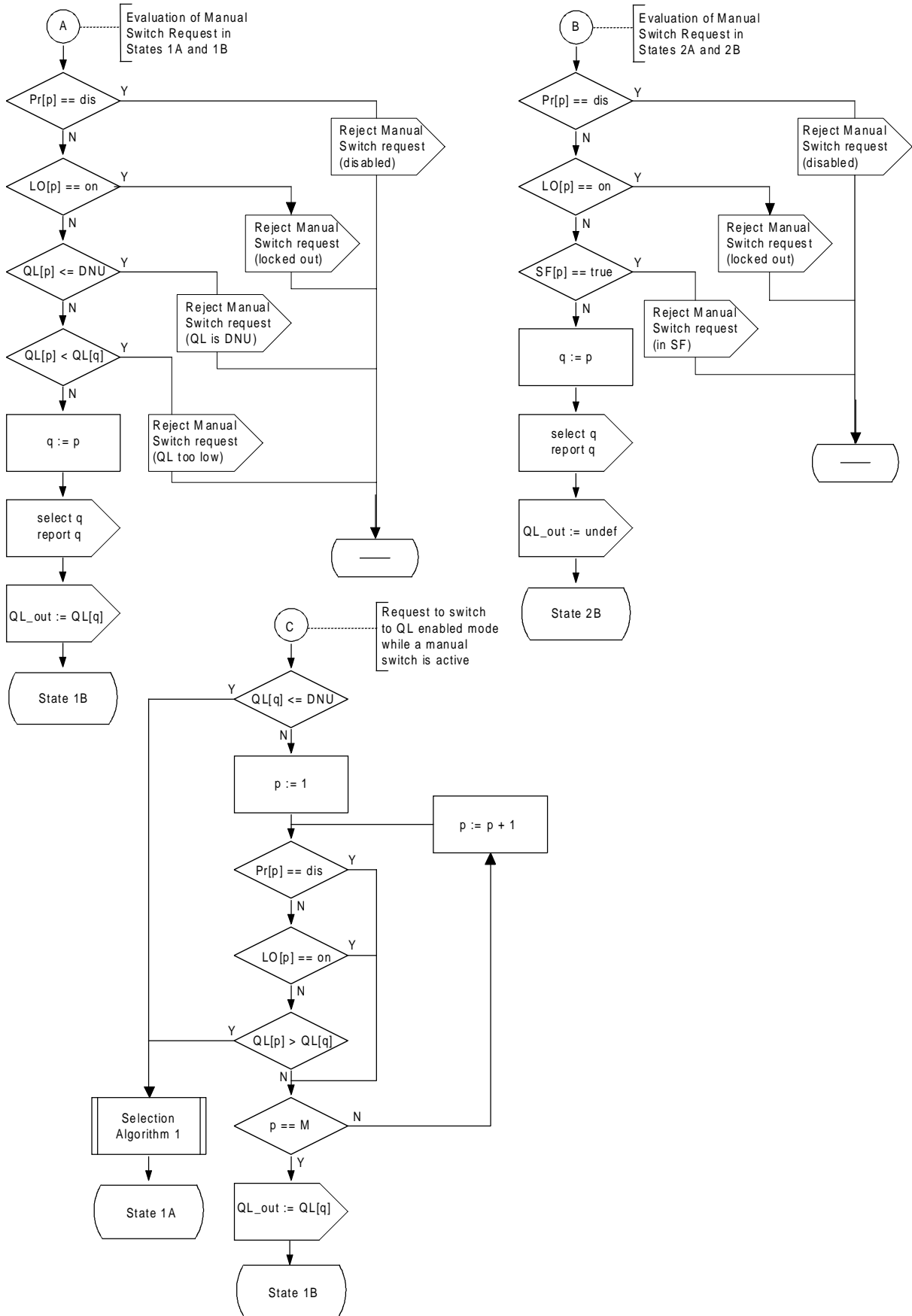**Figure A.7: QL mode disabled, active FSw request (state 2C)**
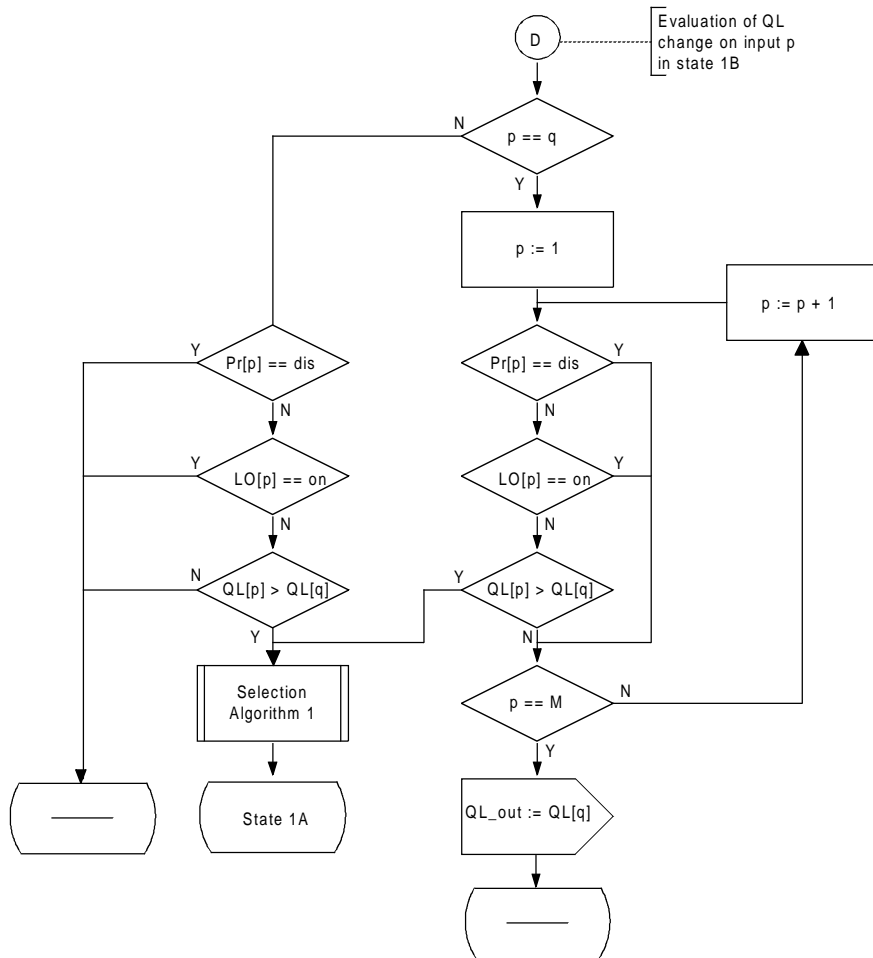
Figure A.8: Continuations of previous states

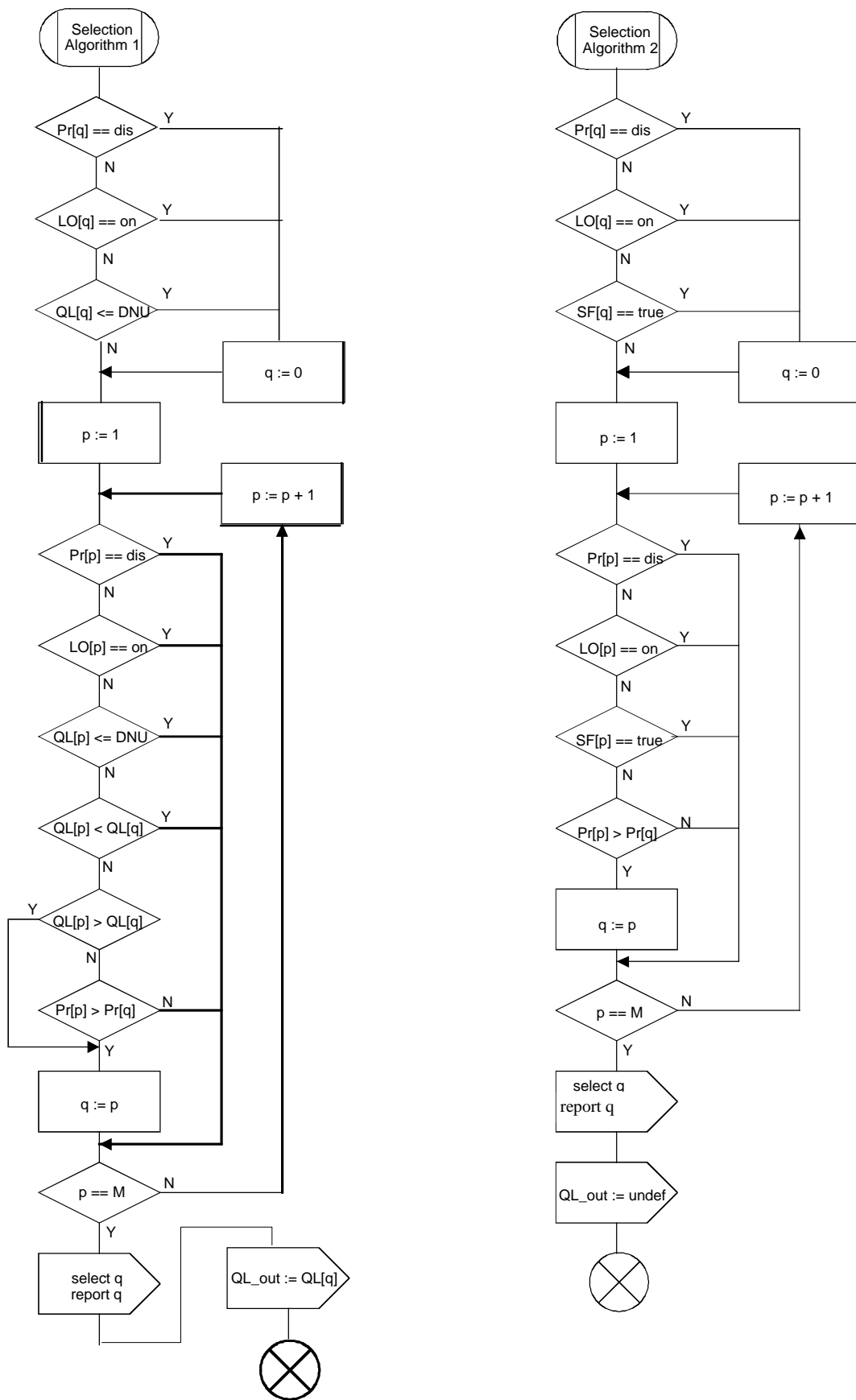**Figure A.9: Continuations of previous states**

Figure A.10: Synchronization selection algorithms for QL mode enabled (1) and QL mode disabled (2)

Annex B (informative):
TL models for synchronization information

This annex shows the interfaces (sink and source) - between NNI and SD_CP - that are able to transport synchronization information using the atomic functions described in different parts of EN 300 417.
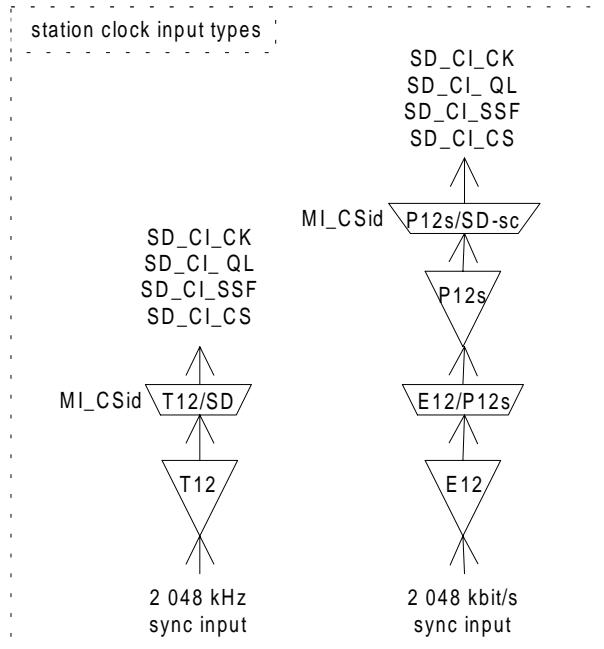

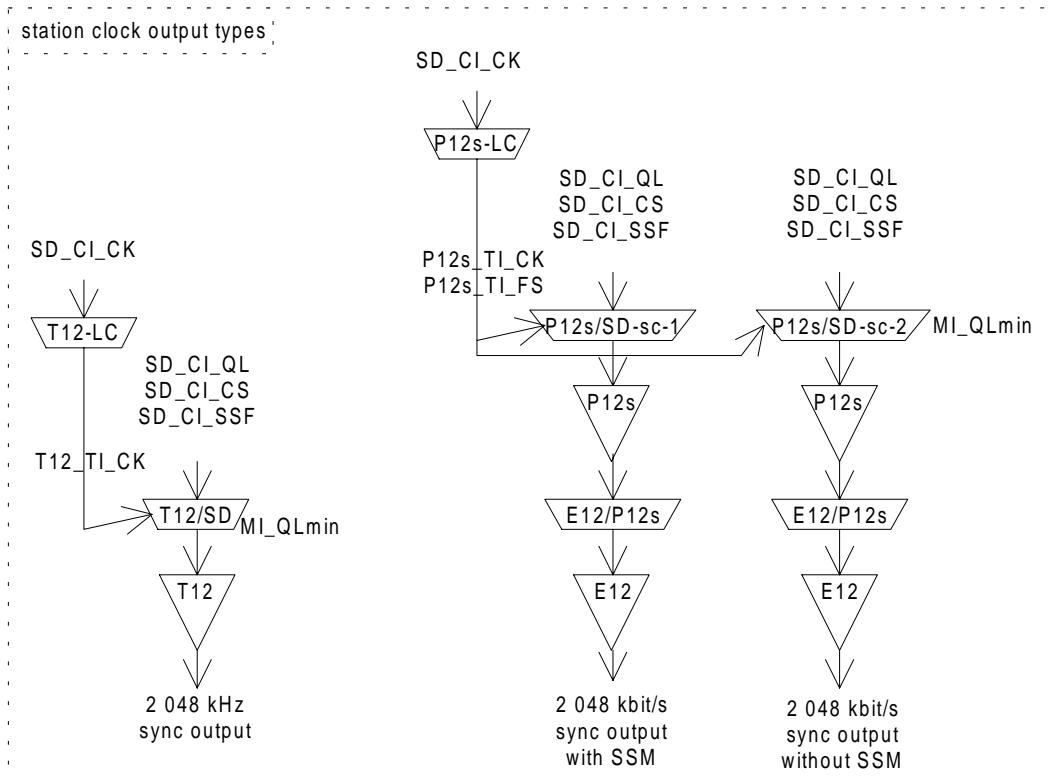**Figure B.1: Synchronization transport port models: station clock inputs**

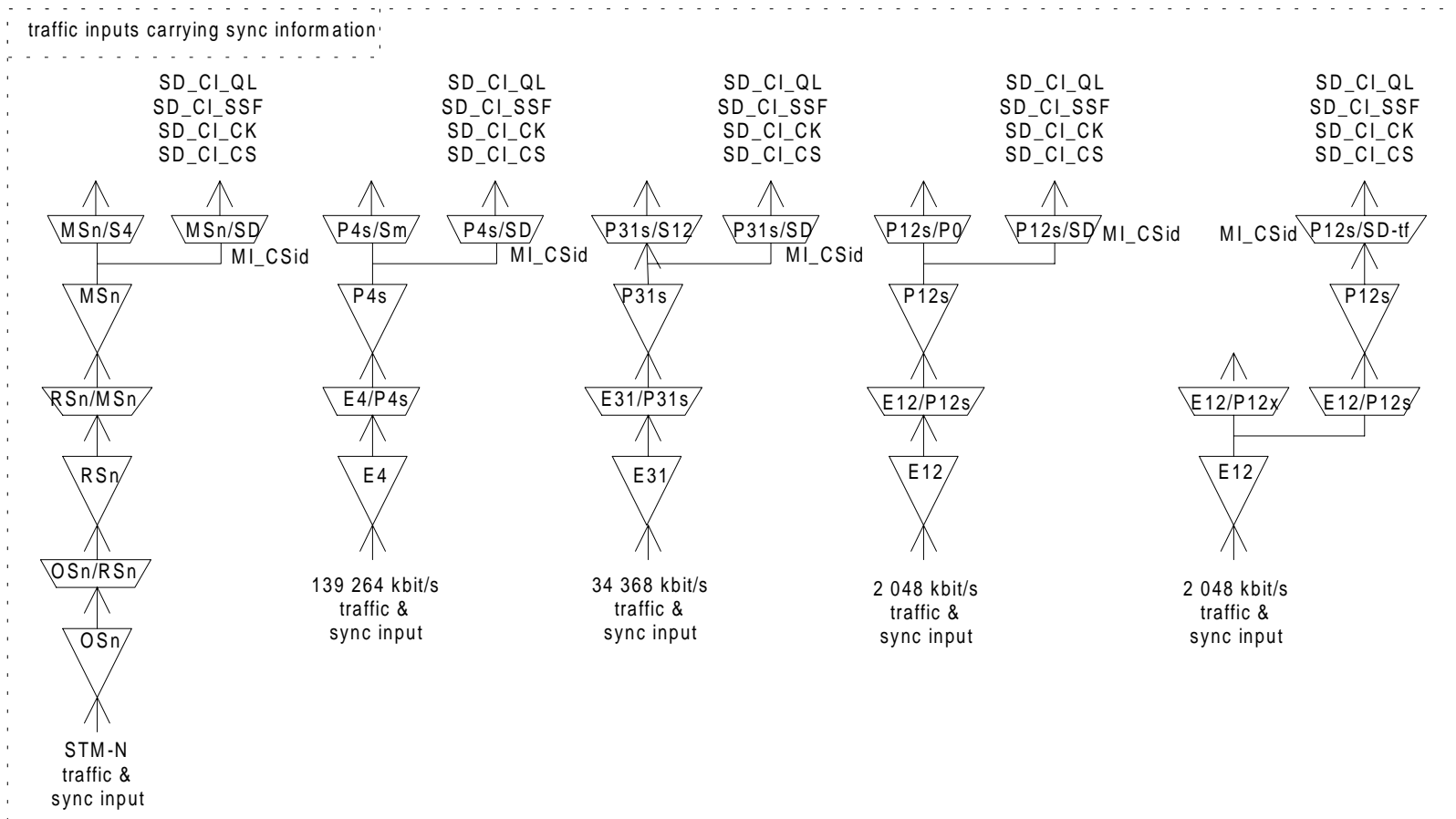**Figure B.2: Synchronization transport port models: station clock outputs**

traffic inputs carrying sync information

SD_CI_QL	SD_CI_QL	SD_CI_QL	SD_CI_QL	SD_CI_QL
SD_CI_SSF	SD_CI_SSF	SD_CI_SSF	SD_CI_SSF	SD_CI_SSF
SD_CI_CK	SD_CI_CK	SD_CI_CK	SD_CI_CK	SD_CI_CK
SD_CI_CS	SD_CI_CS	SD_CI_CS	SD_CI_CS	SD_CI_CS

MSn/S4   MSn/SD   MI_CSid   P4s/Sm   P4s/SD   MI_CSid   P31s/S12   P31s/SD   MI_CSid   P12s/P0   P12s/SD MI_CSid   MI_CSid P12s/SD-tf

MSn   P4s   P31s   P12s   P12s

RSn/MSn   E4/P4s   E31/P31s   E12/P12s   E12/P12x   E12/P12s

RSn   E4   E31   E12   E12

OSn/RSn

OSn

STM-N
traffic &
sync input

139 264 kbit/s
traffic &
sync input

34 368 kbit/s
traffic &
sync input

2 048 kbit/s
traffic &
sync input

2 048 kbit/s
traffic &
sync input

Figure B.3: Synchronization transport port models: traffic (line and tributary) inputs
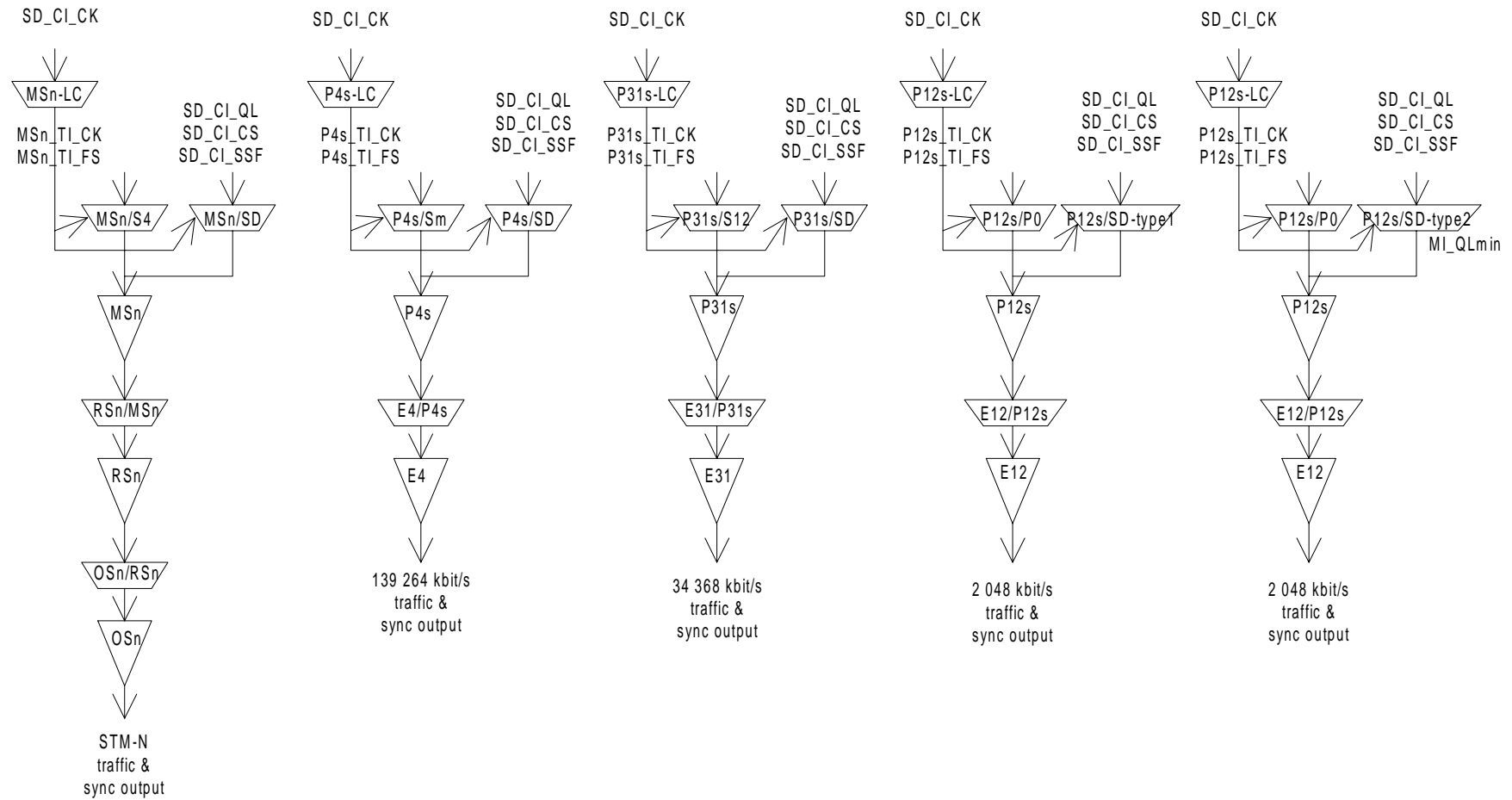
traffic outputs carrying sync information

SD_CI_CK

MSn-LC

MSn_TI_CK
MSn_TI_FS

SD_CI_QL
SD_CI_CS
SD_CI_SSF

MSn/S4   MSn/SD

MSn

RSn/MSn

RSn

OSn/RSn

OSn

STM-N
traffic &
sync output

SD_CI_CK

P4s-LC

P4s_TI_CK
P4s_TI_FS

SD_CI_QL
SD_CI_CS
SD_CI_SSF

P4s/Sm   P4s/SD

P4s

E4/P4s

E4

139 264 kbit/s
traffic &
sync output

SD_CI_CK

P31s-LC

P31s_TI_CK
P31s_TI_FS

SD_CI_QL
SD_CI_CS
SD_CI_SSF

P31s/S12   P31s/SD

P31s

E31/P31s

E31

34 368 kbit/s
traffic &
sync output

SD_CI_CK

P12s-LC

P12s_TI_CK
P12s_TI_FS

SD_CI_QL
SD_CI_CS
SD_CI_SSF

P12s/P0   P12s/SD-type1

P12s

E12/P12s

E12

2 048 kbit/s
traffic &
sync output

SD_CI_CK

P12s-LC

P12s_TI_CK
P12s_TI_FS

SD_CI_QL
SD_CI_CS
SD_CI_SSF

P12s/P0   P12s/SD-type2

MI_QLmin

P12s

E12/P12s

E12

2 048 kbit/s
traffic &
sync output

Figure B.4: Synchronization transport port models: traffic (line and tributary) outputs

Annex C (informative):
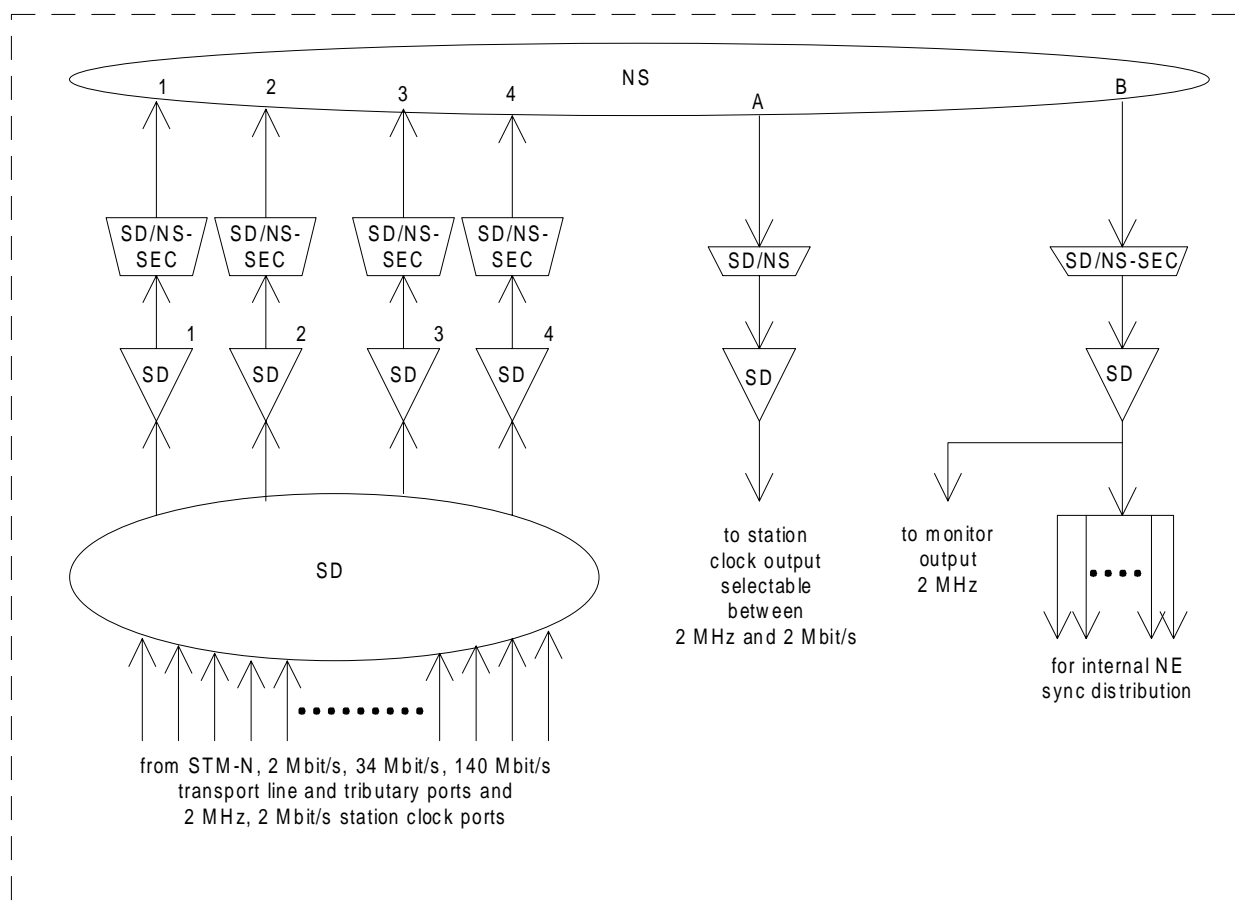# Examples of synchronization functionality in the NE

Figure C.1: Example 1 of a Network Element's SD layer functional model

Figure C.1 presents an example of the SD layer functionality within a NE providing SEC quality timing. The NE in the example offers four timing ports that can be connected to the transport ports carrying synchronization information, selected from the set of line and tributary transport ports and/or station clock ports within the NE.

Output B of NS_C function may use all four input signals to select the best synchronization reference input signal. Output A should exclude input signals derived from station clock ports. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

   NOTE 1:   The correct provisioning is a responsibility of the user of the equipment.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criterion it is used as reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the NE. In addition, it is output also via station clock output dedicated for monitoring the internal CK.

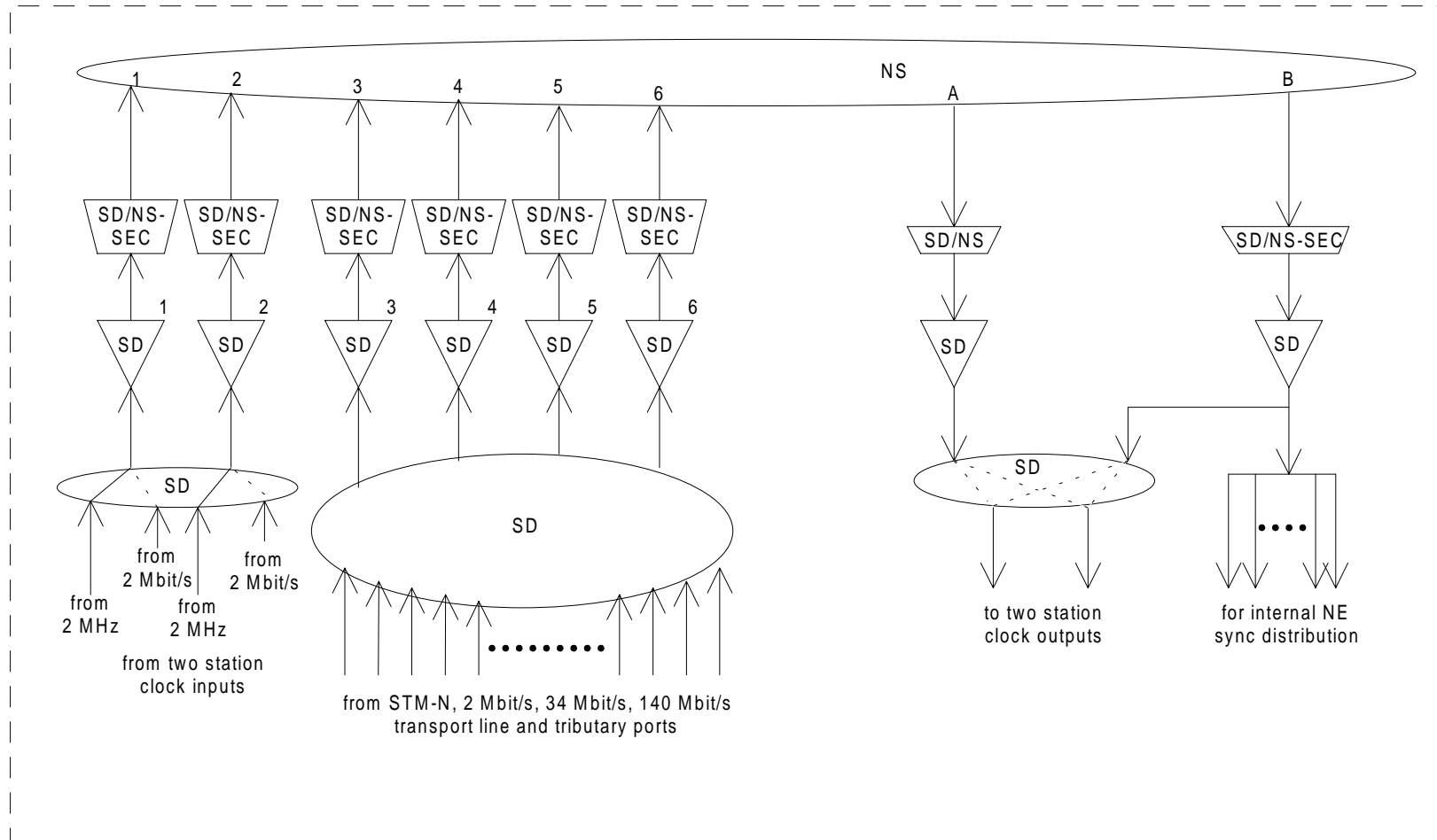The signal at output A of NS_C is connected to the station clock output.

Figure C.2: Example 2 of a Network Element's SD layer functional model

Figure C.2 presents a second example of the SD layer functionality within a NE providing SEC quality timing. The NE in the example offers two station clock timing ports each of them being either of the type 2 MHz or 2 Mbit/s. These station clock based synchronization reference input signals can be connected both to a timing port (SD_TT_Sk #1, #2).

The NE offers furthermore four timing ports that can be connected to a number of transport ports carrying synchronization information, selected from the set of line and tributary transport ports within the NE. Signals from timing ports within the range #3 to #6 that are not connected to a transport port will be disconnected in the NS_C function.

Output B of NS_C function may use all six input signals to select the best synchronization reference input signal. Output A should exclude input signals #1 and #2. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criterion it is used as reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the NE. As an option it can be output also via one or both station clock outputs. The latter to support monitoring of the internal CK, or to provide a synchronization signal to e.g. a small synchronous NE that is the last in the chain.

The signal at output A of NS_C is connected to the station clock output selector (SD_C). Depending on the application in the network, station clock outputs #1 and #2 can operate as a protection pair both sourced by the same input of SD_C, or as two independent outputs sourced by the same or different input signals (as appropriate for the application).

NOTE 2:   Figure C.2 presents two instances of SD_C functions (the first connected to SD_TT_Sk functions #1 and #2 and the second connected to SD_TT_Sk functions #3 to #6) to reflect explicitly the supported connectivity in the NE. The station clock input signals can be connect to timing ports 1, and 2 and not to timing ports 3 to 6. Similarly, the line and tributary input signals can be connected to timing ports 3 to 6, and not to timing ports 1 and 2.

Annex D (informative):
Delay time allocation

D.1   Delay and processing times for the synchronization selection process

The following delay and processing times are defined for a SEC using the QL enabled mode for the reference selection process. They are based on a ring configuration with 20 NEs. Delay and processing times for other applications (e.g. SSU) are for further study.

Three delay time values are defined for the synchronization selection process of the SEC. These are the non-switching message delay T_{NSM}, the switching message delay T_{SM} and the holdover message delay T_{HM}. These times are measurable at the interfaces of the NE.

These delay times are caused by internal delay and processing times of the SD atomic functions. The hold off time t_h and processing time t_p are part of the reference selection process of the NS_C function. The settling time t_s is part of the SD/NS-SEC_A_So function. For a detailed description see clause 5.
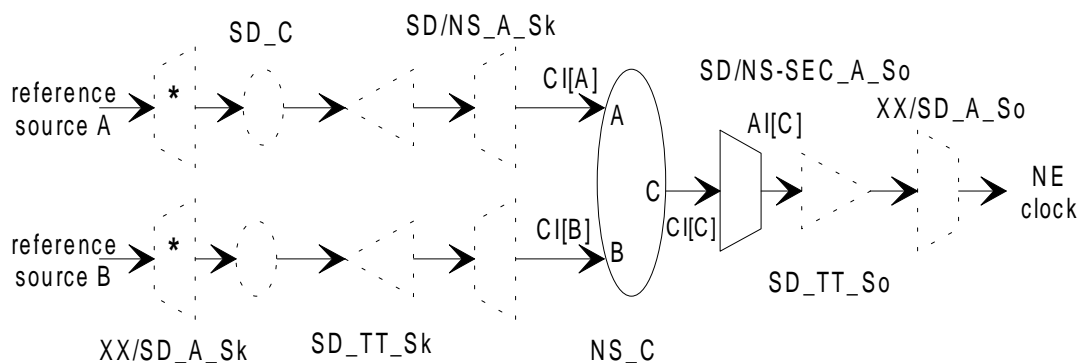

Figure D.1: Example configuration for clock selection

The timing diagrams in the following description are based on a configuration with two clock reference sources as shown in figure D.1.

The dotted functions in the figure do not contribute to delay and processing times. The persistence check for SSM acceptance in the XX/SD_A_Sk functions is also not considered in the following as it is small compared to the overall time.

D.2   Non switching message delay T_{NSM}

This delay applies when the QL of the selected reference signal changes and the sync source is maintained. T_{NSM} defines the maximum time between the change of the input QL and the change of the output QL.
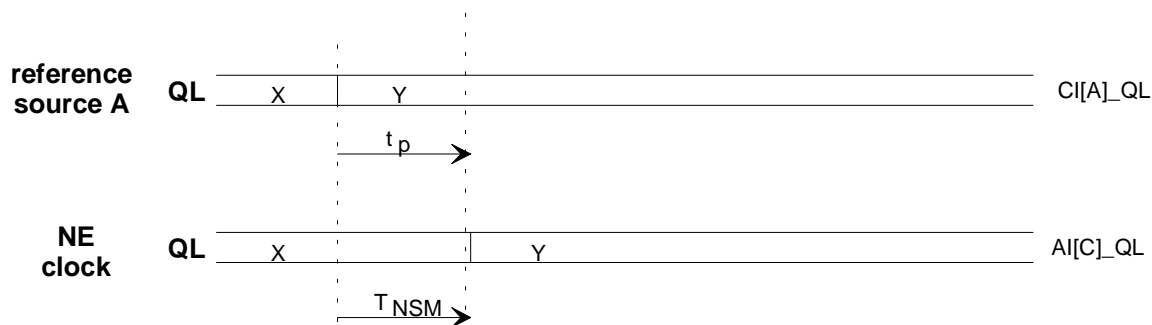

Figure D.2: T_{NSM}

T_{NSM} is due to the processing time t_p of the reference selection process in the NS_C function.

A maximum value of 200 ms is defined for T_{NSM}.

$T_{NSM} = t_p = 0$ ms to 200 ms.

D.3   Switching message delay T_{SM}

This delay applies if a switch over to another reference source is performed with a different QL value. T_{SM} defines the time between the triggering of the new selection (e.g. change of the QL of a reference, EXTCMD, etc.) and the change of the QL at the output.
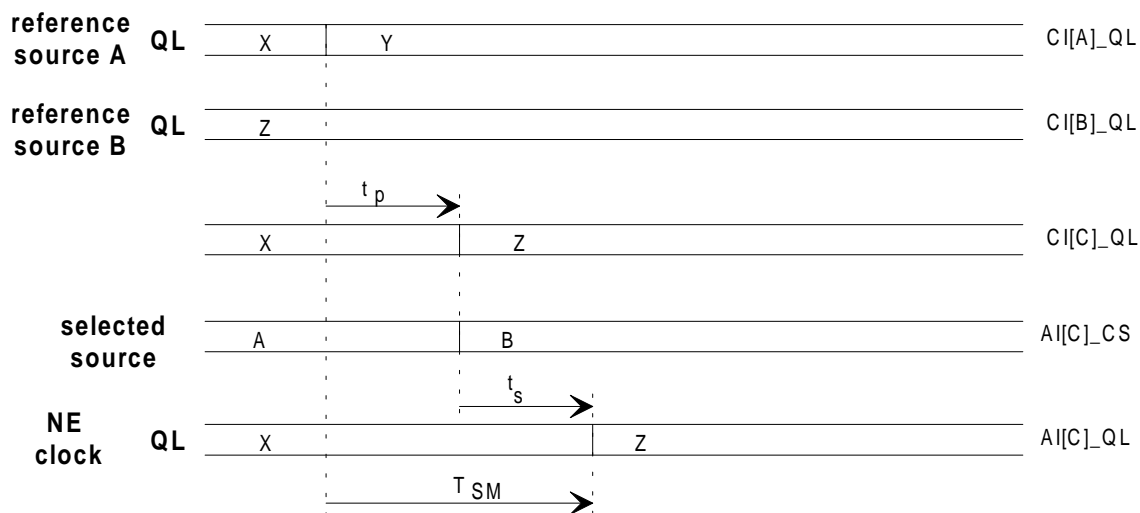

Figure D.3: T_{SM}

T_{SM} is due to the processing time t_p of the selection process in the NS_C function and the settling time t_s of the oscillator in the SD/NS-SEC_A_So function.

A range of 180 ms to 500 ms is defined for T_{SM}.

$T_{SM} = (t_p + t_s) = 180$ ms to 500 ms.

D.4 Holdover message delay T$_{HM}$

This delay applies when the SEC should enter a HO due to a failure condition of the selected sync source and the unavailability of any other synchronization source. When this event occurs the SEC goes immediately into HO. The outgoing QL changes to QL_SEC after the time T$_{HM}$.
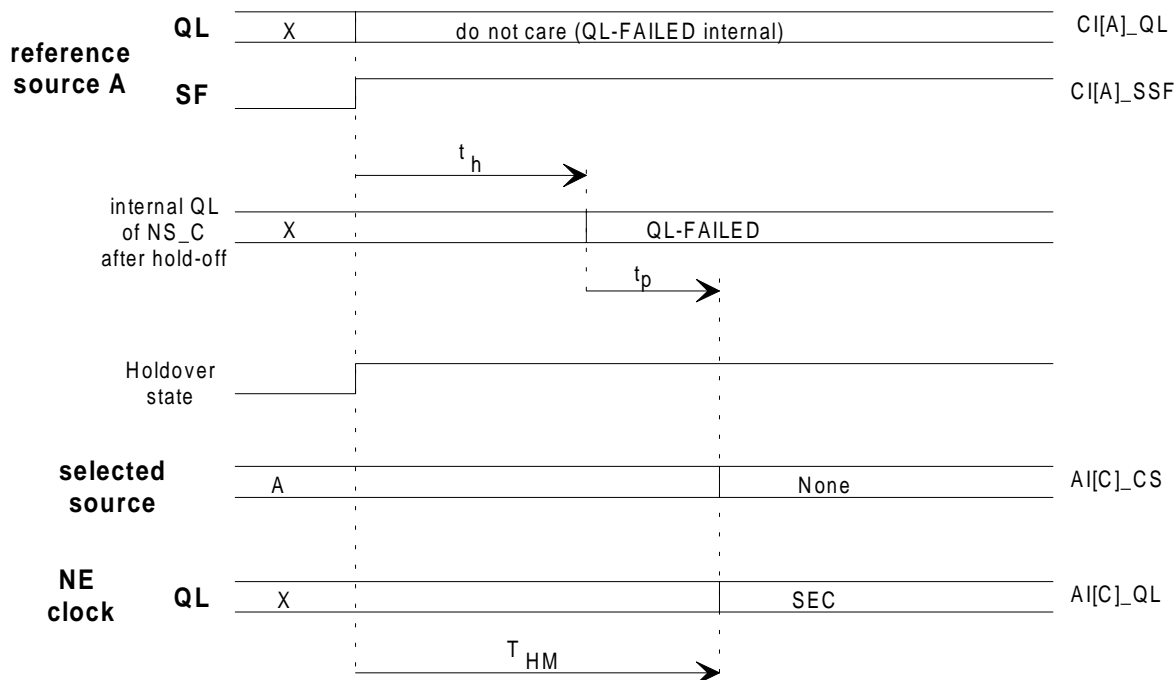

Figure D.4: T$_{HM}$

NOTE: The internal QL of NS_C after hold-off characterizes a signal located between the WTR bloc and the selection control process box defined in figure A.1

T$_{HM}$ is due to the QL-FAILED (SSF) hold off time t$_h$ and the processing time t$_p$ of the selection process in the NS_C function.

A range of 300 ms to 2 000 ms is defined for T$_{HM}$.

$T_{HM} = t_h + t_p = 300$ ms to 2 000 ms.

D.5   Wait to restore time T_{WTR}

The WTR time applies when a synchronization source signal recovers from a failure condition. This signal comes only available for the selection process after SF is cleared at least for the time T_{WTR}.
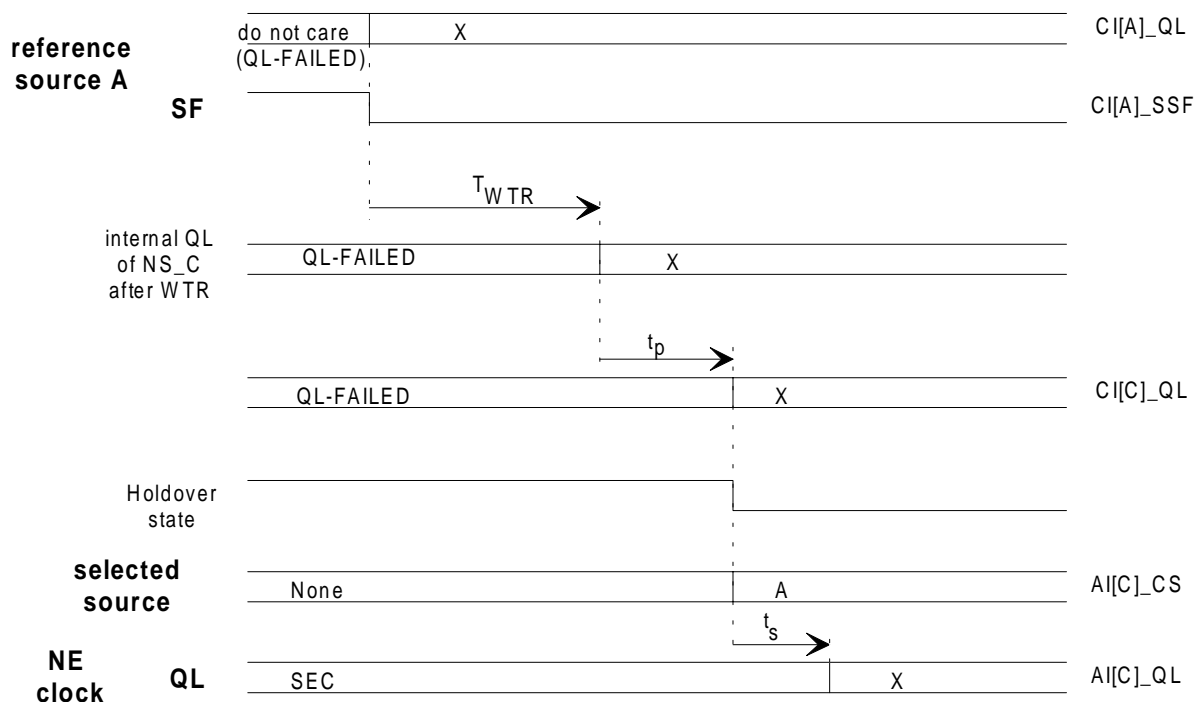

Figure D.5: T_{WTR}

NOTE: The internal QL of NS_C after WTR characterizes a signal located between the WTR block and the selection control process box defined in figure A.1.

T_{WTR} is implemented in the NS_C function. The definition of WTR is in clause 4.

Annex E (informative):
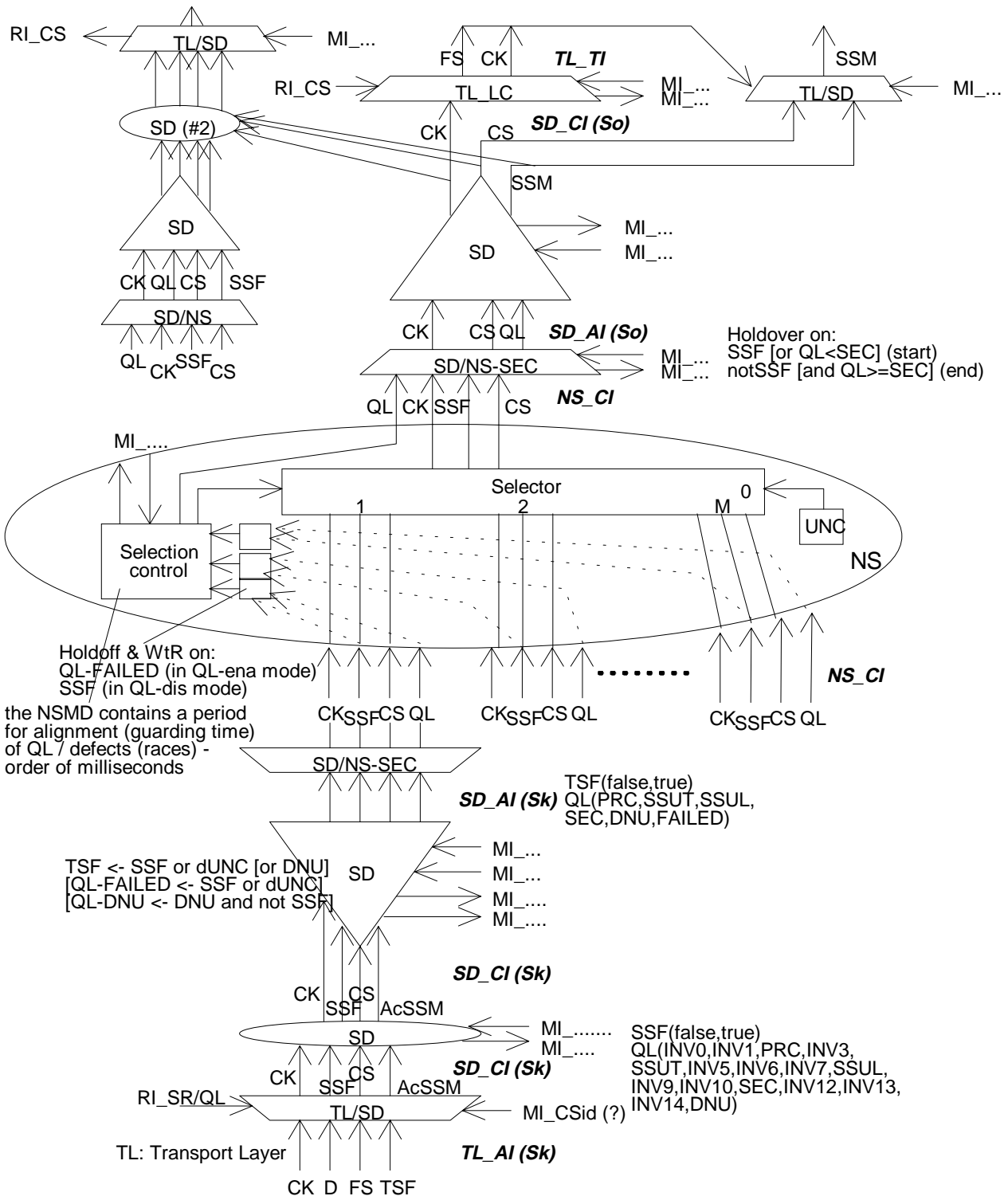# Overview of inputs/outputs to the atomic functions

Figure E.1: Interconnection of atomic functions

Bibliography

- EN 300 417-3-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 3-1: Synchronous Transport Module-N (STM-N) regenerator and multiplex section layer functions".

- EN 300 417-4-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 4-1: Synchronous Digital Hierarchy (SDH) path layer functions".

- EN 300 417-5-1: "Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 5-1: Plesiochronous Digital Hierarchy (PDH) path layer functions".

History

Document history		
Edition 1	August 1998	Publication as ETS 300 417-6-1
V1.1.2	November 1998	Publication (Converted to EN 300 417-6-1)